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NCP4306

Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies

The NCP4306 is high performance driver tailored to control a synchronous rectification MOSFET in switch mode power supplies. Thanks to its high performance drivers and versatility, it can be used in various topologies such as DCM or CCM flyback, quasi resonant flyback, forward and half bridge resonant LLC.

The combination of externally or fixed adjustable minimum off-time and on-time blanking periods helps to fight the ringing induced by the PCB layout and other parasitic elements. A reliable and noise less operation of the SR system is insured due to the Self Synchronization feature. The NCP4306 also utilizes Kelvin connection of the driver to the MOSFET to achieve high efficiency operation at full load and utilizes a light load detection architecture to achieve high efficiency at light load.

The precise turn−off threshold, extremely low turn−off delay time and high sink current capability of the driver allow the maximum synchronous rectification MOSFET conduction time and enables maximum SMPS efficiency. The high accuracy driver and 5 V gate clamp enables the use of GaN MOSFETs.

Features

- Self−Contained Control of Synchronous Rectifier in CCM, DCM and QR for Flyback or LLC Applications
- Precise True Secondary Zero Current Detection
- Typically 15 ns Turn off Delay from Current Sense Input to Driver
- Rugged Current Sense Pin (up to 200 V)
- Ultrafast Turn−off Trigger Interface / Disable Input (10.5 ns)
- Adjustable or Fixed Minimum ON−Time
- Adjustable or Fixed Minimum OFF-Time with Ringing Detection
- Improved Robust Self Synchronization Capability
- 7 A / 2 A Peak Current Sink / Source Drive Capability
- Operating Voltage Range up to V_{CC} = 35 V
- Automatic Light−load Disable Mode
- GaN Transistor Driving Capability
- Low Startup and Disable Current Consumption
- Maximum Operation Frequency up to 1 MHz
- TSOP6 and SOIC-8 Packages
- This is a Pb−Free Device

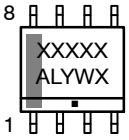
ON Semiconductor®

www.onsemi.com

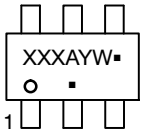
SOIC−8 NB
CASE 751−07

TSOP−6
CASE 318G−02

MARKING DIAGRAMS



SOIC−8 NB
IC (Pb−Free)



TSOP−6
IC (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Typical Applications

- Notebook Adapters
- High Power Density AC / DC Power Supplies (Cell Phone Chargers)
- LCD TVs
- All SMPS with High Efficiency Requirements

ORDERING INFORMATION TABLE

Table 1. AVAILABLE DEVICES

Device	Package	Package Marking	Packing	Shipping †
NCP4306AAAZZZADR2G	SOIC8	6AAAZZZA	SOIC−8 (Pb−Free)	2500 / Tape and Reel
NCP4306AADZZZADR2G		6AADZZZA		
NCP4306AAHZZZADR2G		6AAHZZZA		
NCP4306DADZZDASNT1G	TSOP6	6AC	TSOP−6 (Pb−Free)	3000 / Tape and Reel
NCP4306DAHZZAASNT1G		6AD		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011 / D.

See the ON Semiconductor Device Nomenclature document (TND310 / D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

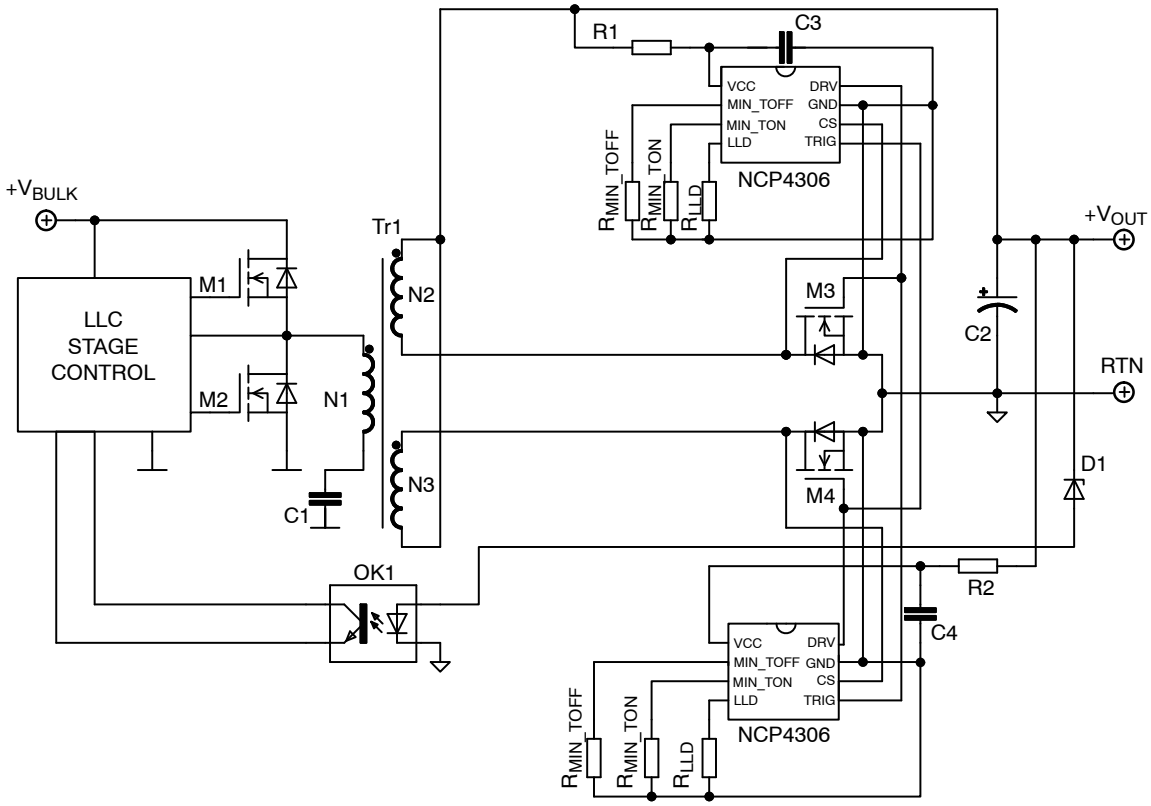


Figure 1. Typical Application Example – LLC Converter with optional LLD and Trigger Utilization

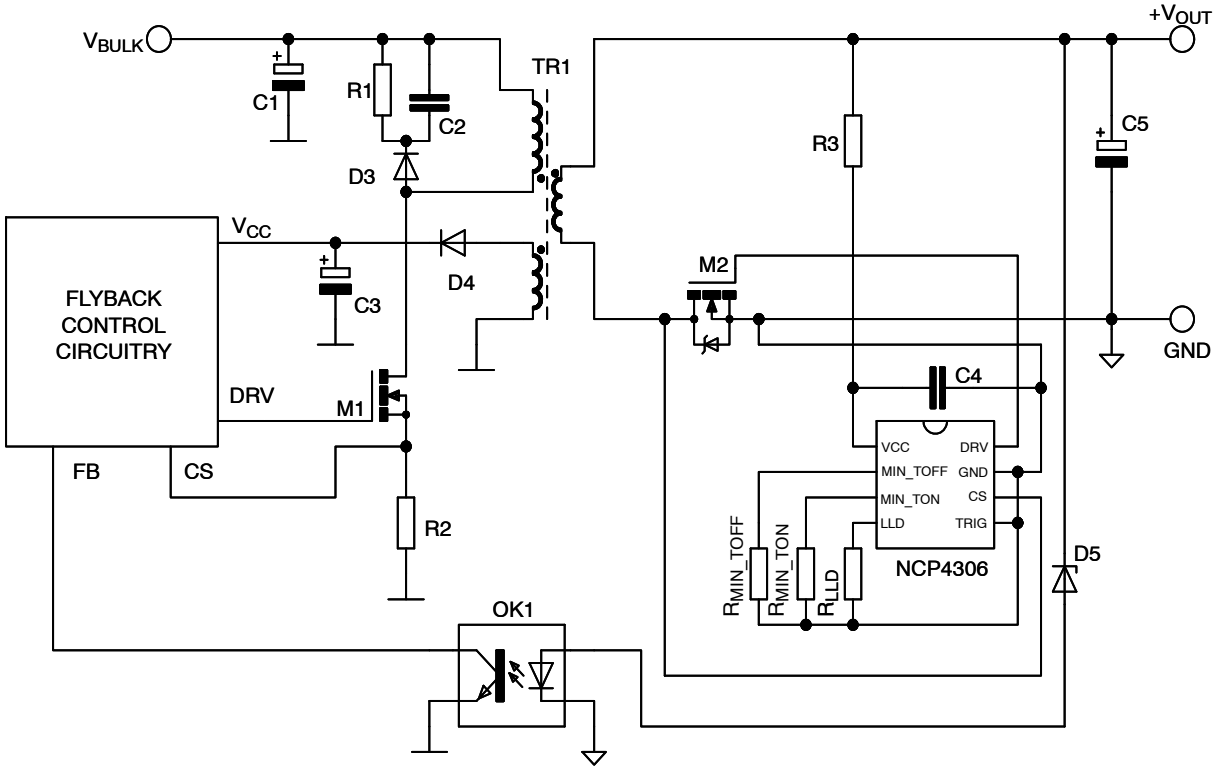


Figure 2. Typical Application Example – DCM, CCM or QR Flyback Converter with optional LLD and disabled TRIG

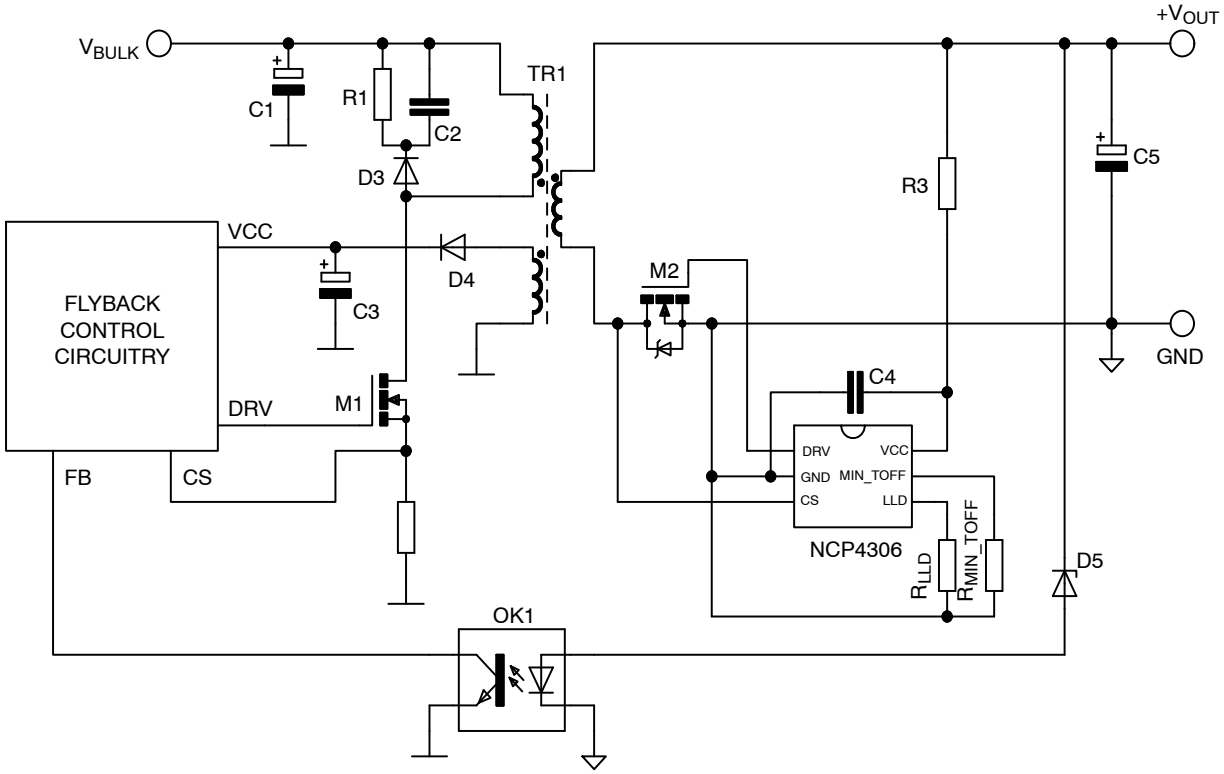


Figure 3. Typical Application Example – DCM, CCM or QR Flyback Converter with NCP4306 in TSOP6 (v Cxxxxxx)

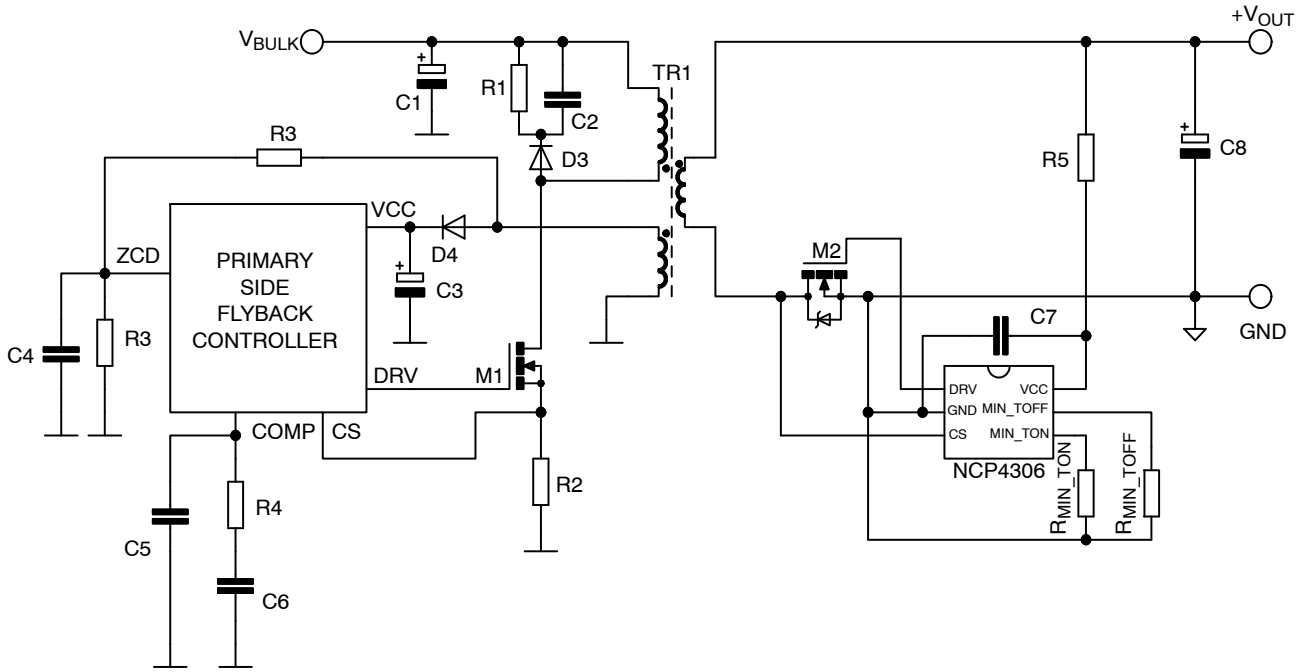


Figure 4. Typical Application Example – Primary Side Flyback Converter and NCP4306 in TSOP6

PIN FUNCTION DESCRIPTION

Table 2. PIN FUNCTION DESCRIPTION

TSOP6 Bxxxxxx	TSOP6 Cxxxxxx	TSOP6 Dxxxxxx	TSOP6 Exxxxxx	TSOP6 Fxxxxxx	TSOP6 Gxxxxxx	SOIC8 Axxxxxx	Pin Name	Description
6	6	6	6	6	6	1	VCC	Supply voltage pin
–	5	5	5	–		2	MIN_TOFF	Adjust the minimum off time period by connecting resistor to ground
5	–	4	–	5	–	3	MIN_TON	Adjust the minimum on time period by connecting resistor to ground
4	4	–	–	–	4	4	LLD	This input modulates the driver clamp level and / or turns the driver off during light load conditions
–	–	–	4	4	5	5	TRIG / DIS	Ultrafast turn−off input that can be used to turn off the SR MOSFET in CCM applications in order to improve efficiency. Activates disable mode if pulled−up for more than 100 μs
3	3	3	3	3	3	6	CS	Current sense pin detects if the current flows through the SR MOSFET and / or its body diode
2	2	2	2	2	2	7	GND	Ground connection for the SR MOSFET driver and V_{CC} decoupling capacitor. Ground connection for minimum t_{ON} and t_{OFF} adjust resistors, LLD and trigger inputs GND pin should be wired directly to the SR MOSFET source terminal / soldering point using Kelvin connection
1	1	1	1	1	1	8	DRV	Driver output for the SR MOSFET

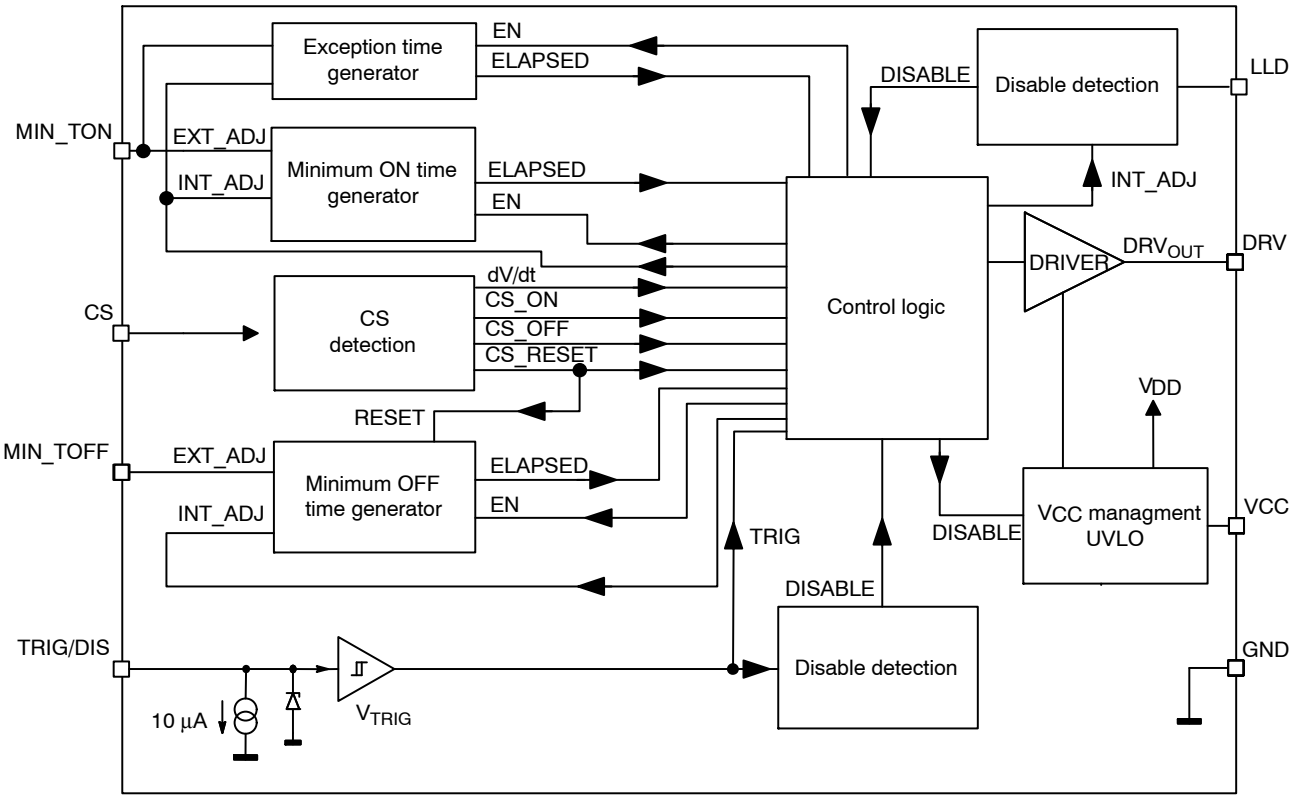


Figure 5. Internal Circuit Architecture – NCP4306

ABSOLUTE MAXIMUM RATINGS

Table 3. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 37.0	V
TRIG / DIS, MIN_TON, MIN_TOFF, LLD Input Voltage (Note 3)	$V_{TRIG\ /\ DIS}$, V_{MIN_TON}, V_{MIN_TOFF}, V_{LLD}	−0.3 to V_{CC}	V
Driver Output Voltage	V_{DRV}	−0.3 to 17.0	V
Current Sense Input Voltage	V_{CS}	−4 to 200	V
Current Sense Dynamic Input Voltage (t_{PW} = 200 ns)	V_{CS_DYN}	−10 to 200	V
MIN_TON, MIN_TOFF, LLD, TRIG Input Current	I_{MIN_TON}, I_{MIN_TOFF}, I_{LLD}, I_{TRIG}	−10 to 10	mA
DRV Pin Current (t_{PW} = 10 μs)	I_{DRV_DYN}	−3 to 12	A
VCC Pin Current (t_{PW} = 10 μs)	I_{VCC_DYN}	3	A
Junction to Air Thermal Resistance, 1 oz 1 in2 Copper Area, SOIC8	$R_{\theta J-A\_SOIC8}$	200	°C / W
Junction to Air Thermal Resistance, 1 oz 1 in2 Copper Area TSOP6	$R_{\theta J-A\_TSOP6}$	250	°C / W
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature	T_{STG}	−60 to 150	°C
ESD Capability, Human Body Model (except pin CS) (Note 1)	ESD_{HBM}	2000	V
ESD Capability, Human Body Model Pin CS	ESD_{HBM}	600	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	200	V
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	Class C1	-

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Except pin CS: Human Body Model 2000 V per JEDEC Standard JESD22−A114E.
   All pins: Machine Model Method 200 V per JEDEC Standard JESD22−A115−A
   Charged Machine Model per JEDEC Standard JESD22−C101F
2. This device meets latchup tests defined by JEDEC Standard JESD78D.
3. If voltage higher than 22 V is connected to pin, pin input current increases. Internal ESD clamp contains 24 V Zener diode with 3 kΩ in series. It is recommended to add serial resistance in case of higher input voltage to limit input pin current.

Table 4. RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min	Max	Unit
Maximum Operating Voltage	V_{CC}		35	V
Operating Junction Temperature	T_J	−40	125	°C

ELECTRICAL CHARACTERISTICS

Table 5. ELECTRICAL CHARACTERISTICS

−40 °C ≤ T_J ≤ 125 °C; V_{CC} = 12 V; C_{DRV} = 0 nF; R_{MIN_TON} = R_{MIN_TOFF} = 10 kΩ or internally set values; V_{LLD} = 3.0 V or LLD internally disabled; $V_{TRIG\ /\ DIS}$ = 0 V; V_{CS} = 4 V, unless otherwise noted. Typical values are at T_J = +25 °C

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
SUPPLY SECTION							
VCC UVLO	V_{CC} rising		V_{CCON}	3.7	4.0	4.2	V
	V_{CC} falling		V_{CCOFF}	3.2	3.5	3.7	
VCC UVLO Hysteresis			V_{CCHYS}		0.5		V
Start−up Delay	V_{CC} rising from 0 to V_{CCON} + 1 V @ tr = 10 µs		t_{START_DEL}		50	80	µs
Current Consumption, t_{MIN_TON} = t_{MIN_TOFF} = 1 µs, t_{LLD} = 130 µs	C_{DRV} = 0 nF, f_{CS} = 100 kHz	xAxxxxx	I_{CC}		1.8	2.5	mA
		xBxxxxx			1.7	2.4	
	C_{DRV} = 1 nF, f_{CS} = 100 kHz	xAxxxxx			2.8	4.0	
		xBxxxxx			2.1	3.4	
	C_{DRV} = 10 nF, f_{CS} = 100 kHz	xAxxxxx			12	15	
		xBxxxxx			6.7	9.0	
Current Consumption			I_{CC}		1.4	2.2	mA
Current Consumption below UVLO	V_{CC} = V_{CCOFF} − 0.1 V		I_{CC_UVLO}		35	60	µA
Current Consumption in Disable Mode	t > t_{LLD} , V_{LLD} = 0.55 V		I_{CC_DIS}		60	100	µA
	$V_{TRIG\ /\ DIS}$ = 5 V; V_{LLD} = 0.55 V				60	100	
	t > t_{LLD}, LLD set internally				37	80	
	$V_{TRIG\ /\ DIS}$ = 5 V, LLD set internally				37	80	
DRIVER OUTPUT							
Output Voltage Rise−Time	C_{DRV} = 10 nF, 10 % to 90 % V_{DRVMAX}, V_{CS} = 4 to −1 V		t_r		60	100	ns
Output Voltage Fall−Time	C_{DRV} = 10 nF, 90 % to 10 % V_{DRVMAX}, V_{CS} = −1 to 4 V		t_f		25	45	ns
Driver Source Resistance			R_{DRV_SOURCE}		2		Ω
Driver Sink Resistance			R_{DRV_SINK}		0.5		Ω
Output Peak Source Current			I_{DRV_SOURCE}		2		A
Output Peak Sink Current			I_{DRV_SINK}		7		A
Maximum Driver Pulse Length			$t_{DRV\_ON\_MAX}$		4		ms
Maximum Driver Output Voltage	V_{CC} = 35 V, C_{DRV} > 1 nF, (ver. xAxxxxx)		V_{DRVMAX}	9	10	11	V
	V_{CC} = 35 V, C_{DRV} > 1 nF, (ver. xBxxxxx)			4.5	5.0	5.5	
Minimum Driver Output Voltage	V_{CC} = V_{CCOFF} + 200 mV, (ver. xAxxxxxx)		V_{DRVMIN}	3.4	3.7	3.9	V
	V_{CC} = V_{CCOFF} + 200 mV, (ver. xBxxxxxx)			3.4	3.7	3.9	
CS INPUT							
Total Propagation Delay From CS to DRV Output On	V_{CS} goes down from 4 to −1 V, t_{f_CS} <= 5 ns		t_{PD_ON}		30	60	ns
Total Propagation Delay From CS to DRV Output Off	V_{CS} goes up from −1 to 4 V, t_{r_CS} <= 5 ns		t_{PD_OFF}		13	23	ns
Turn On CS Threshold Voltage			$V_{TH\_CS\_ON}$	−120	−75	−40	mV
Turn Off CS Threshold Voltage	Guaranteed by Design		$V_{TH\_CS\_OFF}$	−1		0	mV
Turn Off Timer Reset Threshold Voltage			$V_{TH\_CS\_RESET}$	0.4	0.5	0.6	V
CS Leakage Current	V_{CS} = 200 V		$I_{CS\_LEAKAGE}$			500	nA
dV / dt Detector High Threshold			$V_{CS\_DVDT\_H}$		3.0		V

Table 5. ELECTRICAL CHARACTERISTICS (continued)

−40 °C ≤ T_J ≤ 125 °C; V_{CC} = 12 V; C_{DRV} = 0 nF; R_{MIN_TON} = R_{MIN_TOFF} = 10 kΩ or internally set values; V_{LLD} = 3.0 V or LLD internally disabled; $V_{TRIG\ /\ DIS}$ = 0 V; V_{CS} = 4 V, unless otherwise noted. Typical values are at T_J = +25 °C

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
CS INPUT							
dV / dt Detector Low Threshold			$V_{CS\_DVDT\_L}$		0.5		V
dV / dt Detector Threshold	(Note 4)	ver. xxDxxxx	$t_{dV\ /\ dt}$	13	25	37	ns
TRIGGER DISABLE INPUT							
Minimum Trigger Pulse Duration	$V_{TRIG\ /\ DIS}$ = 5 V; Shorter pulses may not be proceeded		$t_{TRIG\_PW\_MIN}$			10	ns
Trigger Threshold Voltage			V_{TRIG_TH}	1.6	2.0	2.2	V
Trigger to DRV Propagation Delay	$V_{TRIG\ /\ DIS}$ goes from 0 to 5 V, $t_{r\_TRIG\ /\ DIS}$ <= 5 ns		t_{PD_TRIG}		10.0	16.5	ns
Trigger Blank Time After DRV Turn−on Event	V_{CS} drops below $V_{TH\_CS\_ON}$		t_{TRIG_BLANK}	30	55	80	ns
Delay to Disable Mode	$V_{TRIG\ /\ DIS}$ goes from 0 to 5 V		t_{DIS_TIM}	75	100	125	µs
Disable Recovery Timer	$V_{TRIG\ /\ DIS}$ goes down from 5 to 0 V; t_{MIN_TOFF} = 130 ns		t_{DIS_REC}		1.5	3.0	µs
Minimum Pulse Duration to Disable Mode End	$V_{TRIG\ /\ DIS}$ = 0 V; Shorter pulses may not be proceeded		t_{DIS_END}			200	ns
Pull Down Current	$V_{TRIG\ /\ DIS}$ = 5 V		$I_{TRIG\ /\ DIS}$	7	11	15	µA
Maximum Transition Time	$V_{TRIG\ /\ DIS}$ goes from 1 to 3 V or from 3 to 1 V		t_{TRIG_TRAN}			10	µs
MINIMUM T_{ON} AND T_{OFF} ADJUST							
Minimum t_{ON} time	R_{MIN_TON} = 0 Ω (ver. xxxZxxx)		t_{ON_MIN}		55		ns
Minimum t_{OFF} time	R_{MIN_TOFF} = 0 Ω (ver. xxxxZxx)		t_{OFF_MIN}		70		ns
Minimum t_{ON} time	R_{MIN_TON} = 10 kΩ (ver. xxxZxxx)		t_{ON_MIN}	0.90	1.00	1.10	µs
Minimum t_{OFF} time	R_{MIN_TOFF} = 10 kΩ (ver. xxxxZxx)		t_{OFF_MIN}	0.90	1.00	1.10	µs
Minimum t_{ON} time	R_{MIN_TON} = 50 kΩ (ver. xxxZxxx)		t_{ON_MIN}	4.50	5.00	5.50	µs
Minimum t_{OFF} time	R_{MIN_TOFF} = 50 kΩ (ver. xxxxZxx)		t_{OFF_MIN}	4.40	4.90	5.40	µs
Internal minimum t_{ON} time	t_{ON_MIN} = 130 ns, (ver. xxxAxxx)		t_{ON_MIN}	−20%	t_{ON_MIN}	+20%	ns
	t_{ON_MIN} = 220, 310, 400 ns (ver. xxx[B−D]xxx)		t_{ON_MIN}	−15%	t_{ON_MIN}	+15%	ns
	t_{ON_MIN} = 500, 600, 800, 1000, 1200, 1400, 1700, 2000 ns (ver. xxx[E−L]xxx)		t_{ON_MIN}	−10%	t_{ON_MIN}	+10%	ns
Internal minimum t_{OFF} time	t_{OFF_MIN} = 0.9, 1.0, 1.1, 1.2, 1.4, 1.6, 1.8, 2.0, 2.2, 2.4, 2.6, 2.9, 3.2, 3.5, 3.9 µs (ver. xxxx[A−O]xx)		t_{OFF_MIN}	−10%	t_{OFF_MIN}	+10%	µs
LLD ADJUST							
LLD Pull Up Current	(ver. xxxxxZx)		I_{LLD}	−21	−20	−19	µA
LLD Time Selection	IC disabled		V_{LLD}			0.3	V
	t_{LLD} = 68 µs			0.40	0.51	0.63	
	t_{LLD} = 130 µs			0.75	0.89	1.03	
	t_{LLD} = 280 µs			1.15	1.32	1.50	
	t_{LLD} = 540 µs			1.68	1.82	1.97	
	t_{LLD} = 1075 µs			2.20	2.50	2.70	
	LLD function disabled			3.10			
LLD Main Time	V_{LLD} = 0.51 V or ver. xxxxxAx		t_{LLD}	53	68	83	µs
	V_{LLD} = 0.89 V or ver. xxxxxBx			100	130	160	
	V_{LLD} = 1.32 V or ver. xxxxxCx			220	280	340	
	V_{LLD} = 1.82 V or ver. xxxxxDx			420	540	660	
	V_{LLD} = 2.45 V or ver. xxxxxEx			840	1075	1310	

Table 5. ELECTRICAL CHARACTERISTICS (continued)
$-40\ ^{\circ}C \le T_J \le 125\ ^{\circ}C$; V_{CC} = 12 V; C_{DRV} = 0 nF; $R_{MIN\_TON} = R_{MIN\_TOFF}$ = 10 kΩ or internally set values; V_{LLD} = 3.0 V or LLD internally disabled; $V_{TRIG\ /\ DIS}$ = 0 V; V_{CS} = 4 V, unless otherwise noted. Typical values are at $T_J = +25\ ^{\circ}C$

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LLD ADJUST						
LLD Reduced Time	Disable mode activated	t_{LLD_RED}		$0.5 \times t_{LLD}$		μs
LLD Blanking Time		t_{LLD_BLK}		$0.25 \times t_{LLD}$		μs
Disable Recovery Time	t_{MIN_TOFF} = 130 ns	$t_{LLD\_DIS\_REC}$		1.5	3.0	μs
EXCEPTION TIMER						
Exception Time	(ver. xxHxxxx)	t_{EXC}		$4 \times t_{MIN\_TON}$		μs
Exception Timer Ratio Accuracy		$Ratio_{EXC}$	−15		+15	%

4. Test signal:

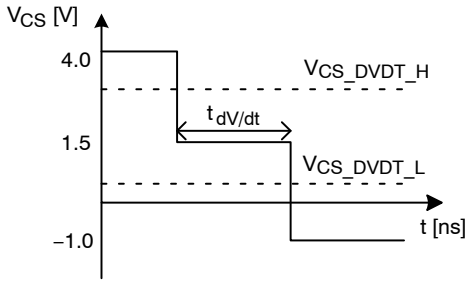


Figure 6. Test Signal

TYPICAL CHARACTERISTICS

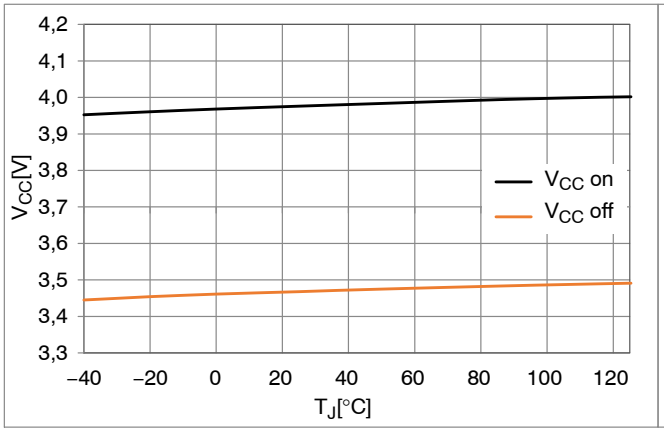


Figure 7. V_{CCON} and V_{CCOFF} Levels

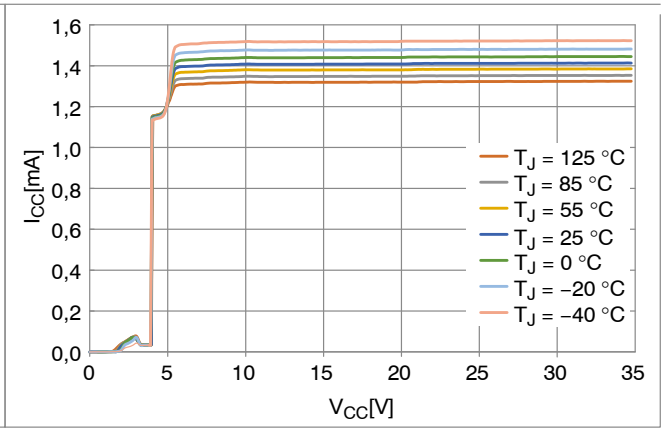


Figure 8. Current Consumption V_{CS} = 4 V

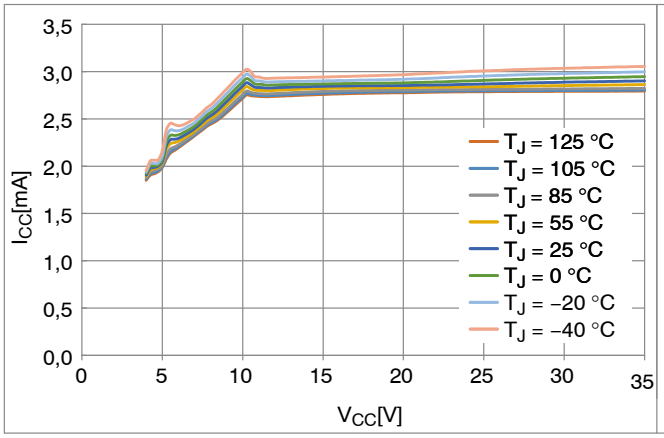


Figure 9. Current Consumption, f_{CS} = 100 kHz, C_{DRV} = 1 nF, Ver. xAxxxxx

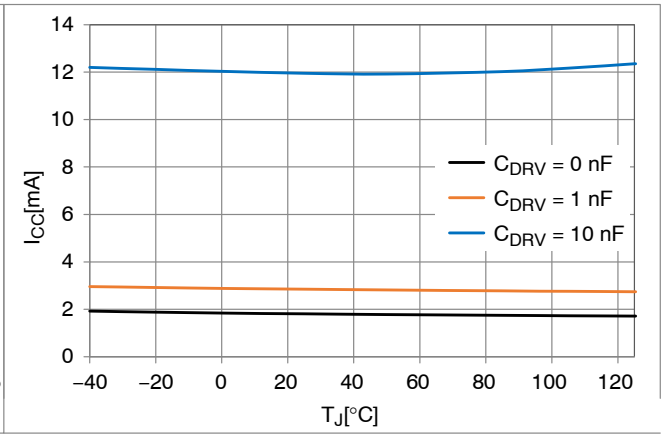


Figure 10. Current Consumption, f_{CS} = 100 kHz, Ver. xAxxxxx

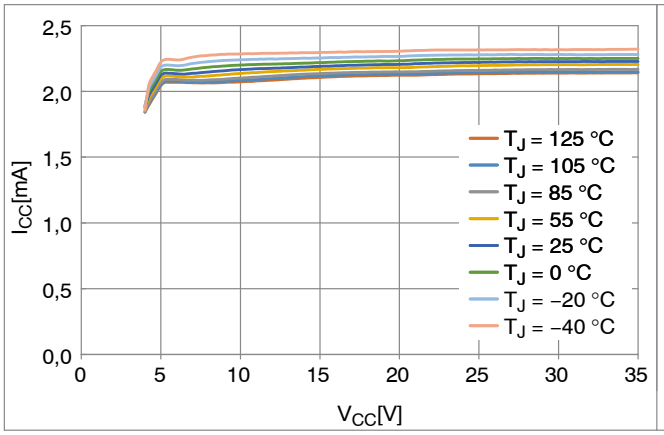


Figure 12. Current Consumption, f_{CS} = 100 kHz, C_{DRV} = 1 nF, Ver. xBxxxx

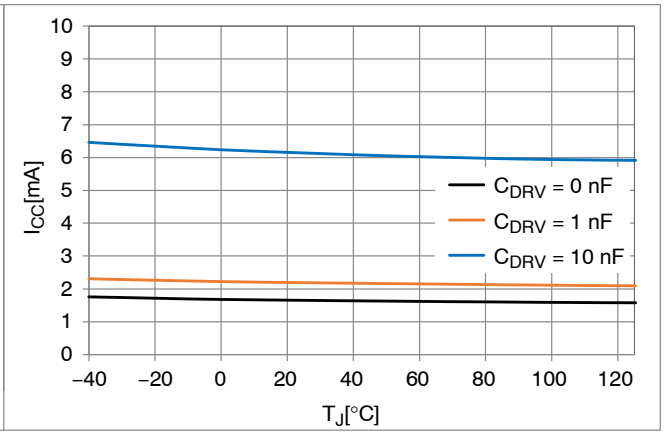


Figure 11. Current Consumption, f_{CS} = 100 kHz, Ver. xBxxxxx

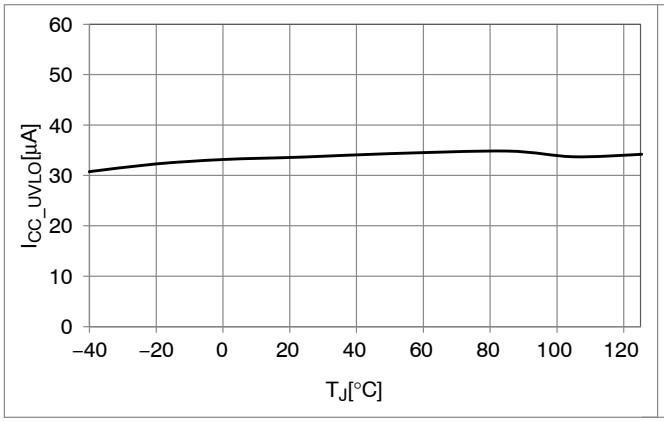


Figure 13. Current Consumption below UVLO, $V_{CC} = V_{CCOFF} - 0.1$ V

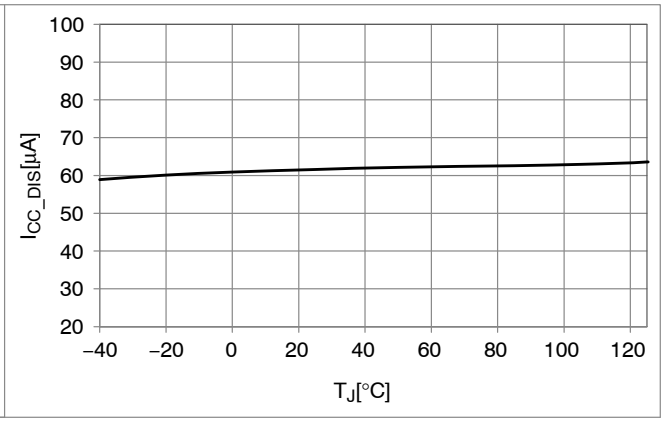


Figure 14. Current Consumption in Disable Mode $V_{CS} = 4$ V, $t > t_{LLD}$

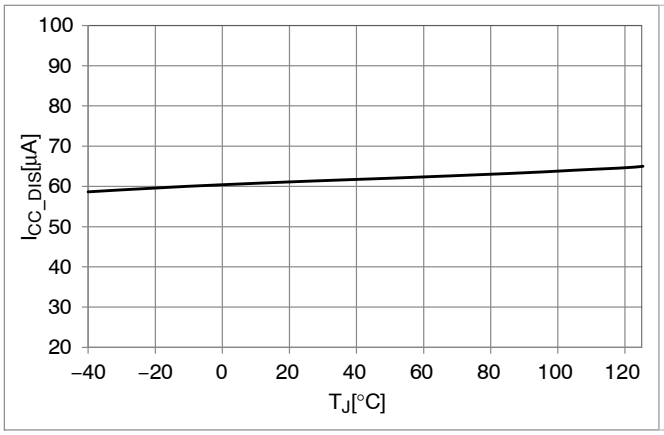


Figure 15. Current Consumption in Disable Mode, $V_{TRIG/DIS} = 5$ V

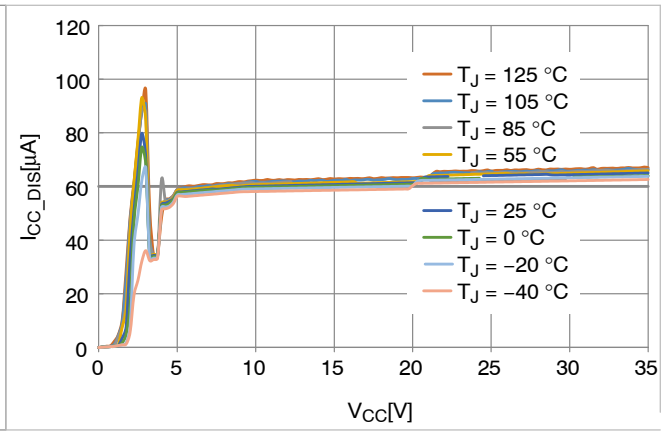


Figure 16. Current Consumption in Disable Mode, $V_{CS} = 4$ V, $t > t_{LLD}$

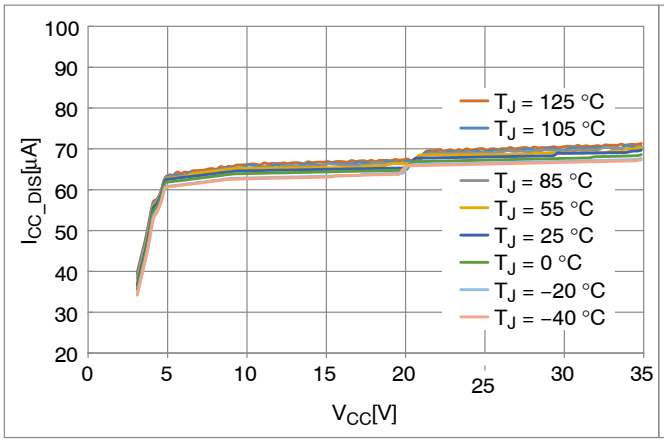


Figure 17. Current Consumption in Disable Mode, $V_{TRIG/DIS} = 5$ V

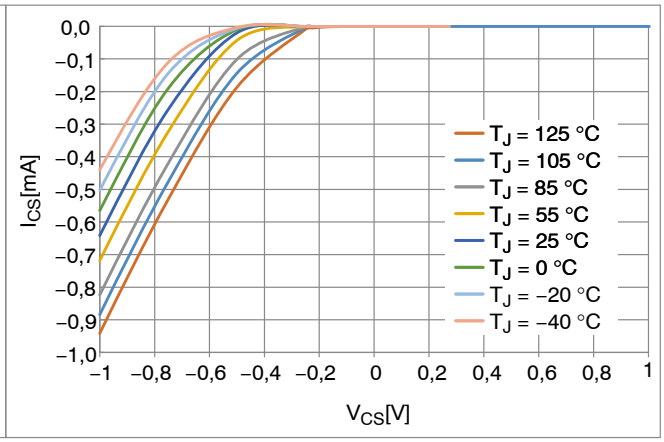


Figure 18. CS Input Current

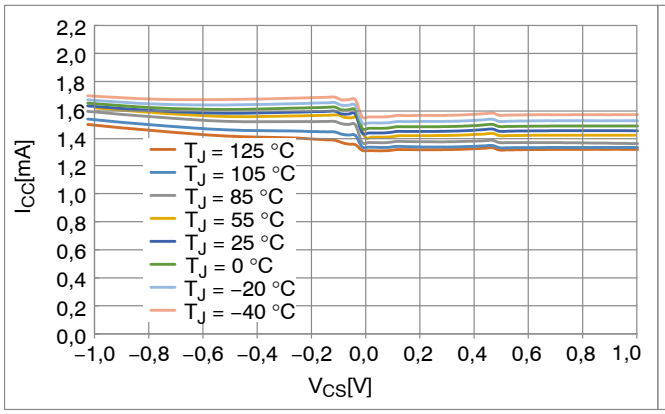


Figure 19. Supply Current vs. CS Voltage

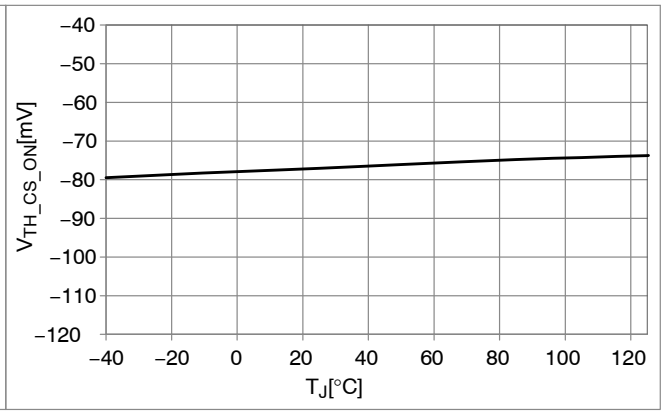


Figure 20. CS Turn−on Threshold

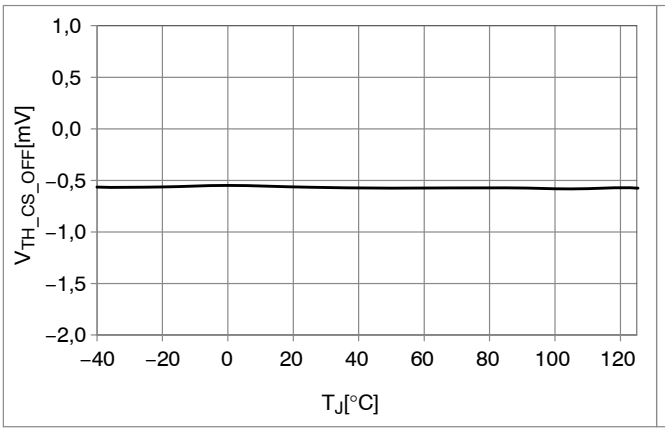


Figure 21. CS turn−off Threshold

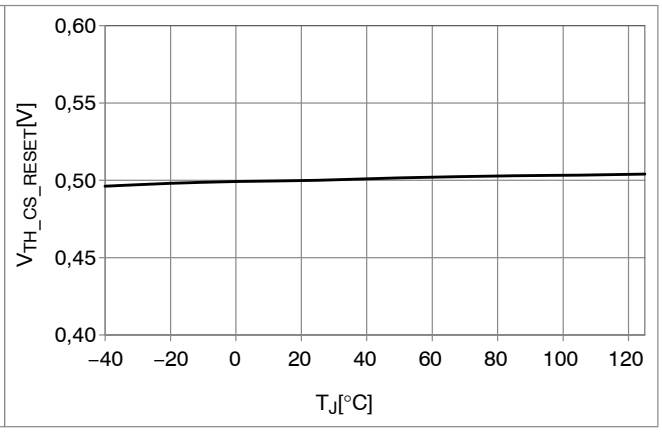


Figure 22. CS Reset Threshold

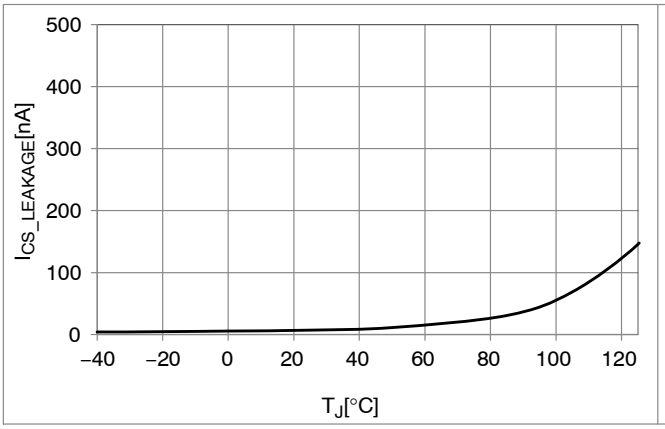


Figure 23. CS Input Leakage V_{CS} = 200 V

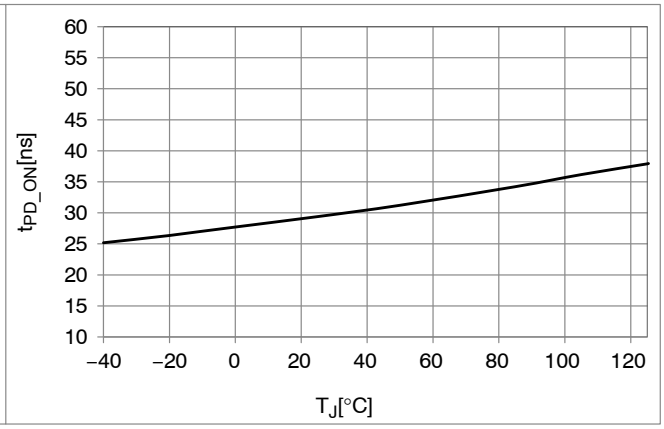


Figure 24. Propagation Delay from CS to DRV Output On

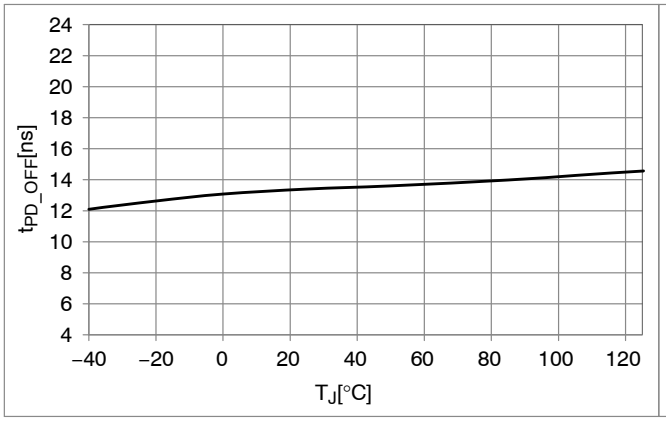


Figure 25. Propagation Delay from CS to DRV Output Off

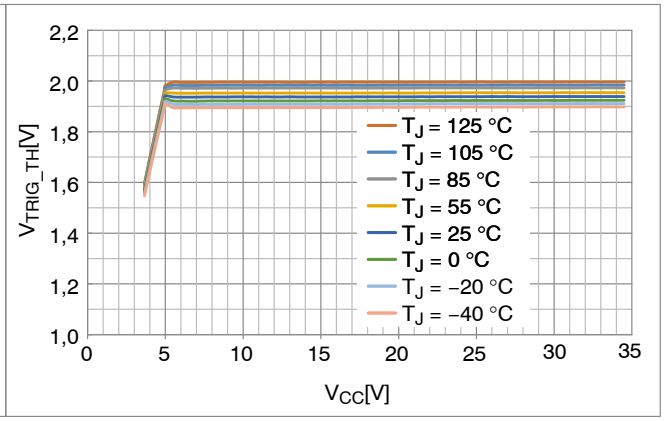


Figure 26. Trigger Pin Threshold

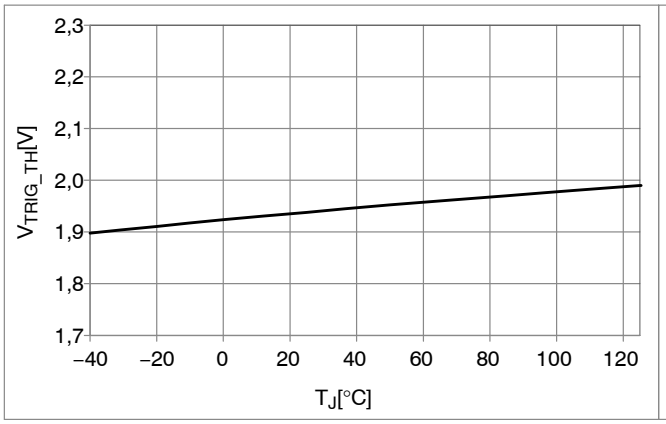


Figure 27. Trigger Pin Threshold

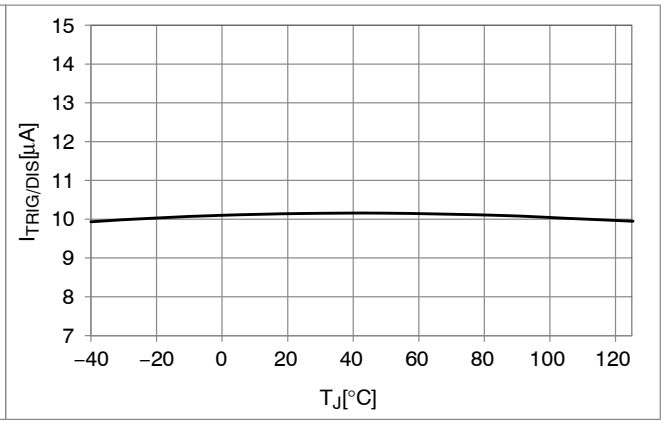


Figure 28. Trigger Pin Pull Down Current

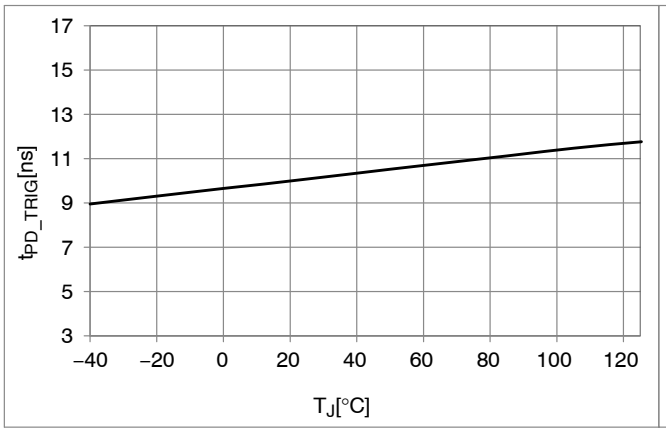


Figure 29. Propagation Delay from TRIG to DRV Output Off

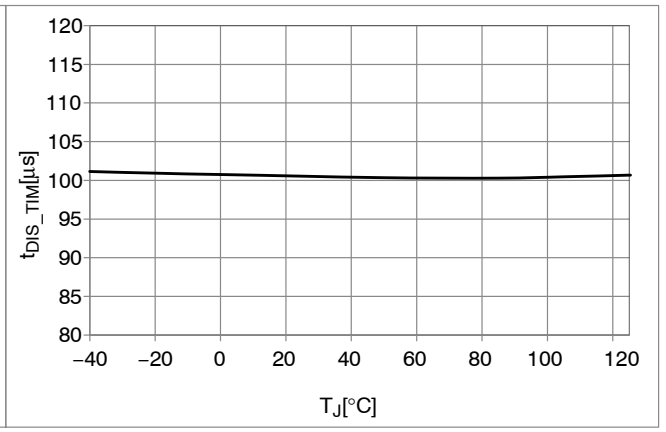


Figure 30. Delay to Disable Mode, $V_{TRIG/DIS}$ = 5 V

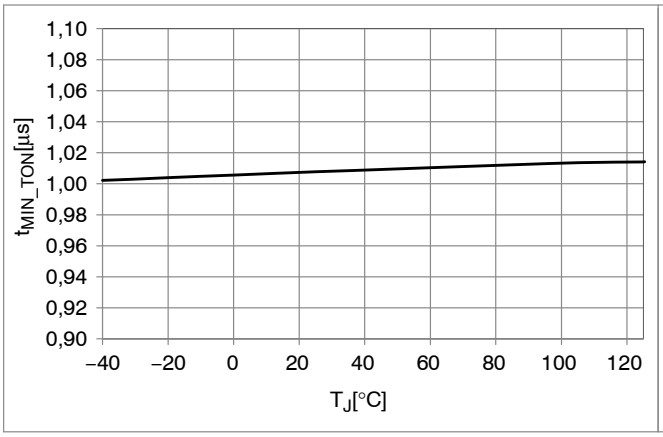


Figure 31. Minimum on Time R_{MIN_TON} = 10 kΩ

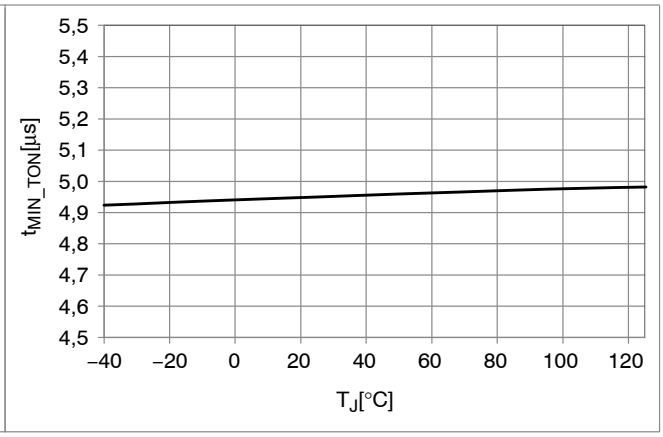


Figure 32. Minimum on Time R_{MIN_TON} = 50 kΩ

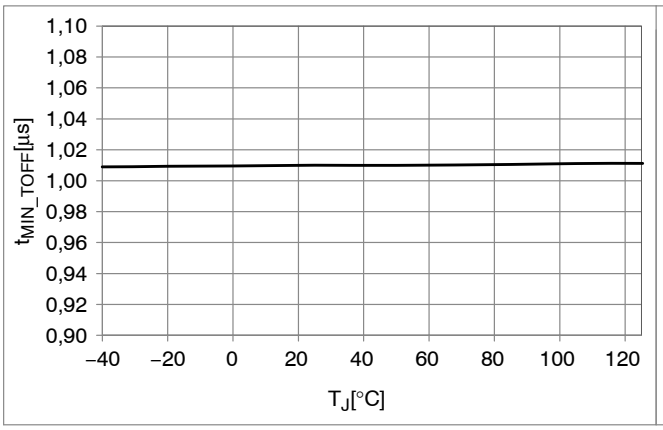


Figure 33. Minimum on Time R_{MIN_TOFF} = 10 kΩ

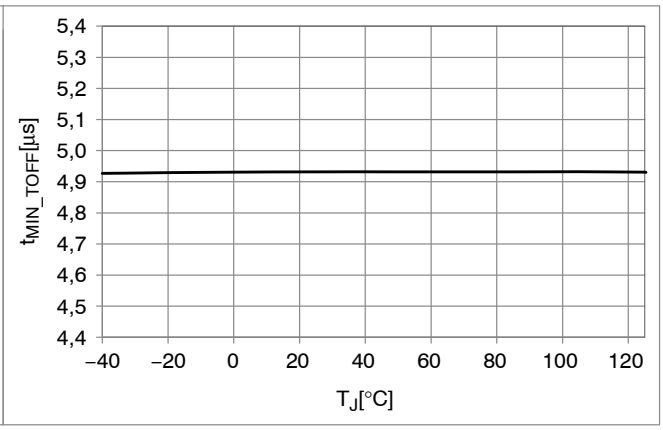


Figure 34. Minimum on Time R_{MIN_TOFF} = 50 kΩ

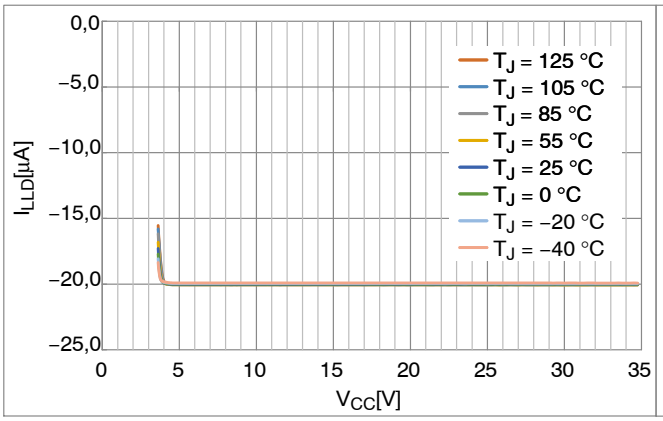


Figure 35. LLD Current, V_{LLD} = 3.0 V

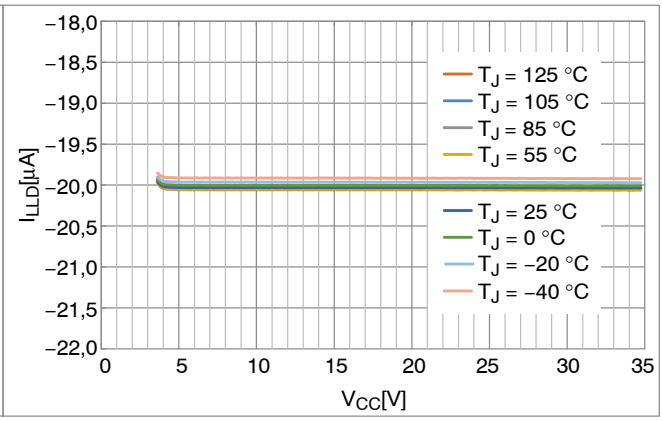


Figure 36. LLD current, V_{LLD} = 2.5 V

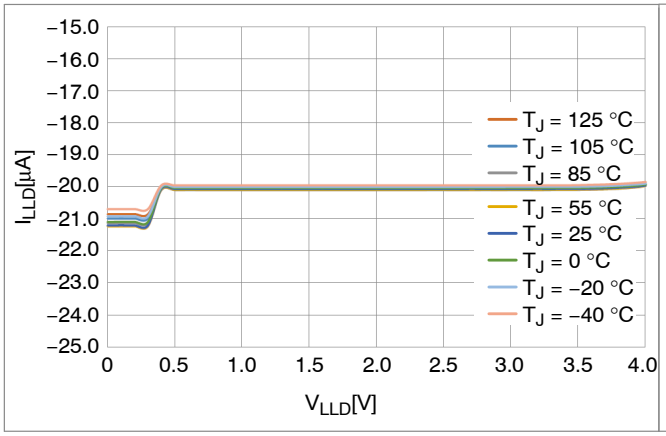


Figure 37. LLD Current

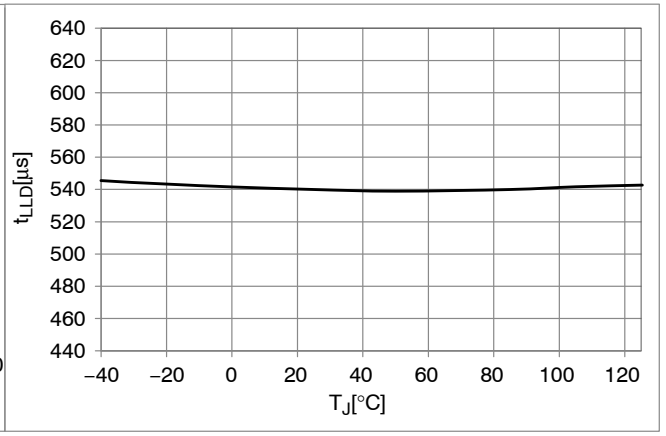


Figure 38. LLD Time, V_{LLD} = 1.82 V (or Internal Option)

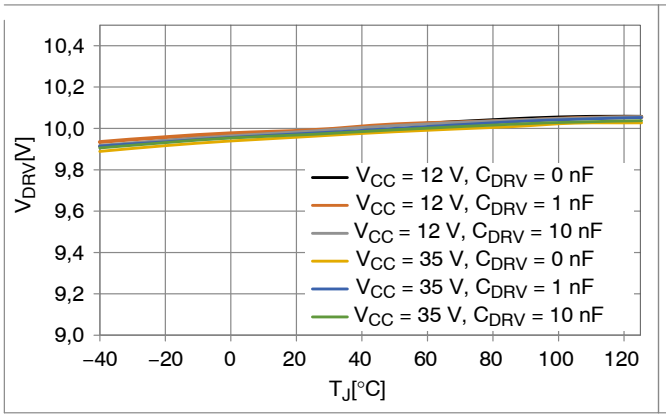


Figure 39. Driver Output Voltage, Ver. xAxxxxx

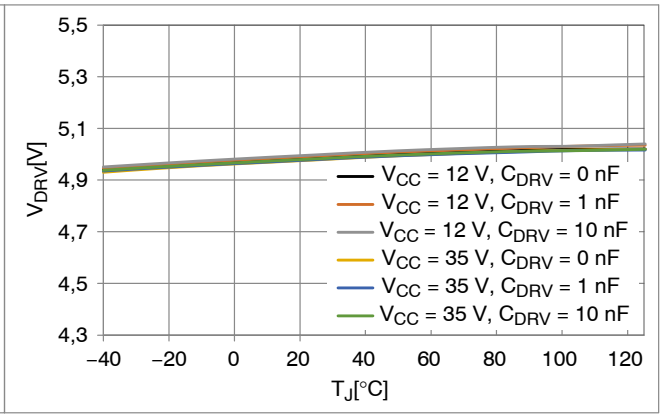


Figure 40. Driver Output Voltage, Ver. xBxxxxx

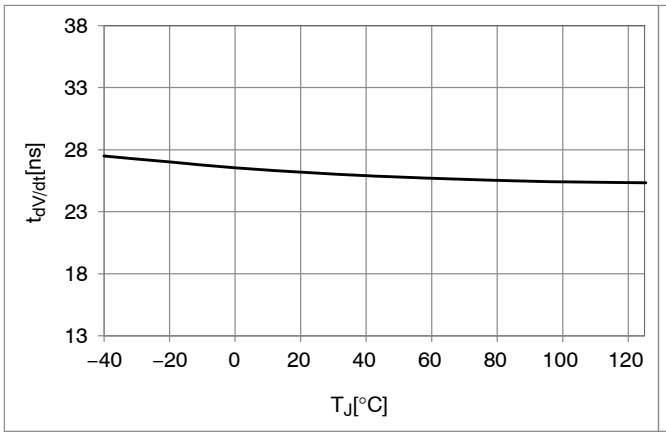


Figure 41. dV/dt Detector Time Threshold, Ver. xxDxxxx

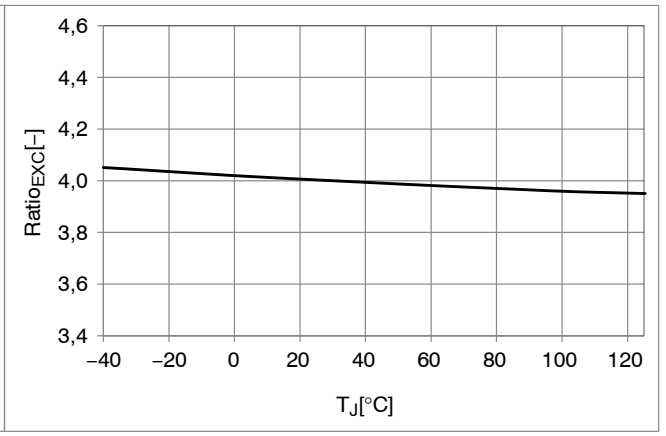


Figure 42. Exception Timer Ratio to t_{MIN_TON}, Ver. xxHxxxx

GENERAL DESCRIPTION

The NCP4306 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high−speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP4306 has enough versatility to keep the synchronous rectification system efficient under any operating mode.

The NCP4306 works from an available voltage with range from 4.0 / 3.5 V to 35 V (typical). The wide V_{CC} range allows direct connection to the SMPS output voltage of most adapters such as notebooks, cell phone chargers and LCD TV adapters.

Precise turn−off threshold of the current sense comparator together with an accurate offset current source allows the user to adjust for any required turn−off current threshold of the SR MOSFET switch using a single resistor. Compared to other SR controllers that provide turn−off thresholds in the range of −10 mV to −5 mV, the NCP4306 offers a turn−off threshold of 0 mV. When using a low R_{DS_ON} SR (1 mΩ) MOSFET our competition, with a −10 mV turn off, will turn off with 10 A still flowing through the SR FET, while our 0 mV turn off turns off the FET at 0 A; significantly reducing the turn−off current threshold and improving efficiency. Many of the competitor parts maintain a drain source voltage across the MOSFET causing the SR MOSFET to operate in the linear region to reduce turn−off time. Thanks to the 6 A sink current of the NCP4306 significantly reduces turn off time allowing for a minimal drain source voltage to be utilized and efficiency maximized.

To overcome false triggering issues after turn−on and turn−off events, the NCP4306 provides adjustable minimum on−time and off−time blanking periods. Blanking times can be set internally during production or adjusted independently of IC VCC using external resistors connected to GND (internal or external option depends on IC variant). If needed, externally set blanking periods can be modulated using additional components.

An extremely fast turn−off comparator, implemented on the current sense pin, allows for NCP4306 implementation in CCM applications without any additional components or external triggering.

An ultrafast trigger input offers the possibility to further increase efficiency of synchronous rectification systems operated in CCM mode (for example, CCM flyback or forward). The time delay from trigger input to driver turn off event is t_{PD_TRIG}. Additionally, the trigger input can be used to disable the IC and activate a low consumption standby mode. This feature can be used to decrease standby consumption of an SMPS. If the trigger input is not wanted than the trigger pin can be tied to GND.

An output driver features capability to keep SR transistor turned−off even when there is no supply voltage for the NCP4306. SR transistor drain voltage goes up and down during SMPS operation and this is transferred through drain gate capacitance to gate and may open transistor. The NCP4306 keeps DRV pin pulled low even without any supply voltage and thanks to this the risk of turned−on SR transistor before enough V_{CC} is applied to the NCP4306 is eliminated.

Finally, the NCP4306 features a Light Load Detection function that can be set internally or externally at LLD pin by resistor connected to ground. This function detects light load or no load conditions and during them between conduction phases it decreases current consumption. This helps to improve SMPS efficiency. If LLD function is not needed pin can be left open.

SUPPLY SECTION

Supply voltage should be connected to VCC pin. Minimum voltage for proper operation is 4.0 / 3.5 V typically and maximum level is 35 V. Decoupling capacitor between VCC and GND pin is needed for proper operation and its recommended value is 1 μF. If IC is supplied from SMPS output voltage, few ohm resistor is recommended between SMPS output voltage and VCC pin. Resistor task is to divide decoupling cap from output to avoid closing HF currents through NCP4306 decoupling cap, because these currents may causes drops at GND connection that affects SR transistor sensing and incorrect SR transistor turn−off.

SR transistor is usually used in low side configuration (placed in return path), but it may be also used in high side configuration (placed in positive line). It is not possible to use SMPS V_{OUT} for SR supply in high side configuration so it is needed to provide supply differently. One possibility is to use auxiliary winding as shown in Figure 43. Voltage from auxiliary winding is rectified, filtered and use as supply voltage.

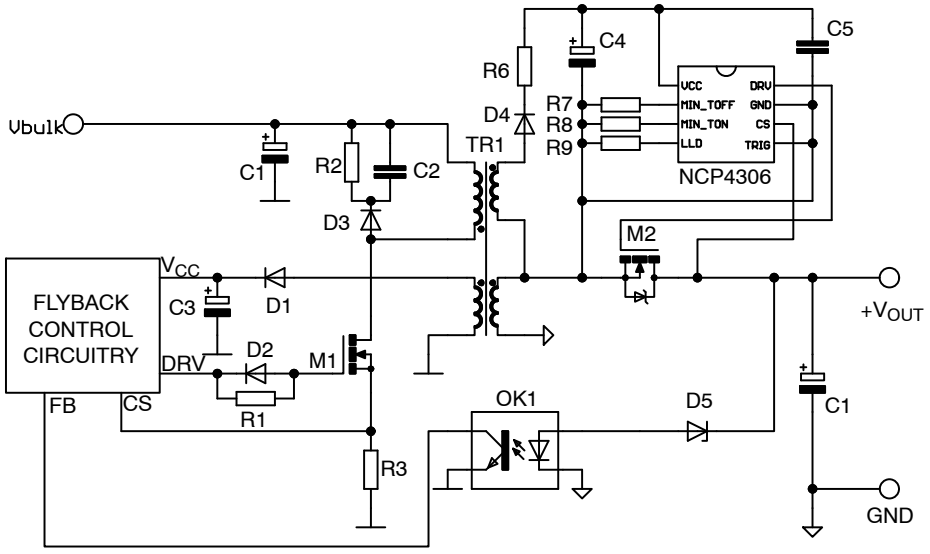


Figure 43. High Side Configuration Supplied from Auxiliary Winding

If auxiliary winding is not acceptable, transformer forward voltage can be used as supply source (Figure 44). Forward voltage is regulated by simple voltage regulator to fit NCP4306 VCC restriction. Penalty for this solution is slightly lower efficiency.

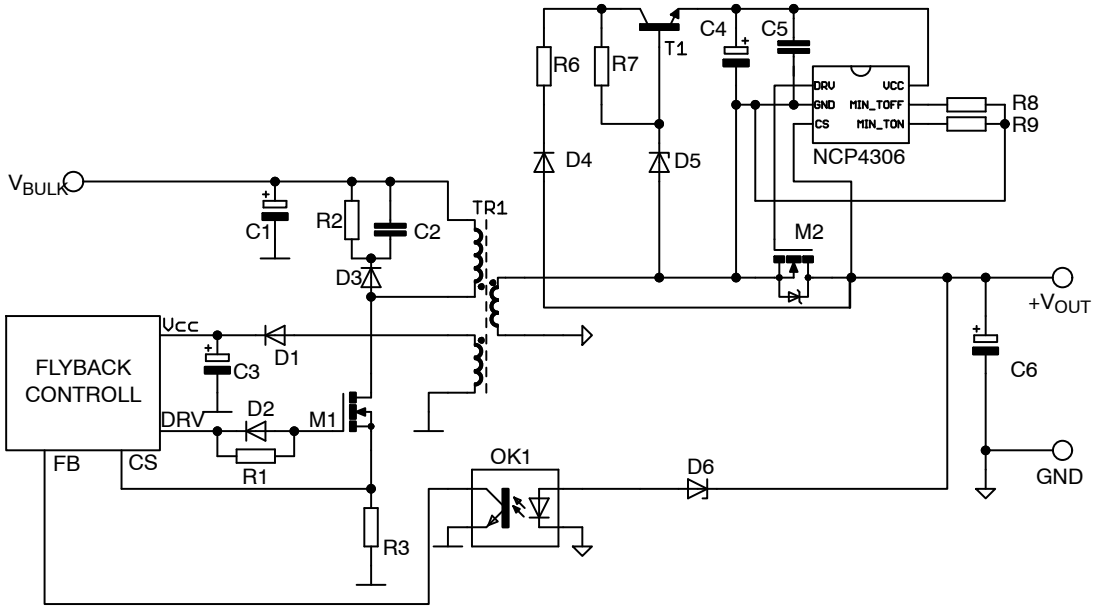


Figure 44. High Side Configuration Supplied from Transformer Forward Voltage

Auxiliary winding or forward voltage can be used as supply source also for low side configuration if V_{OUT} is not high enough (Figure 45). Do not focus just on SR controller UVLO, but also on SR transistor characteristics. Some transistors may be not turned−on enough even at 5 V so in these case SR controller supply voltage should be increased.

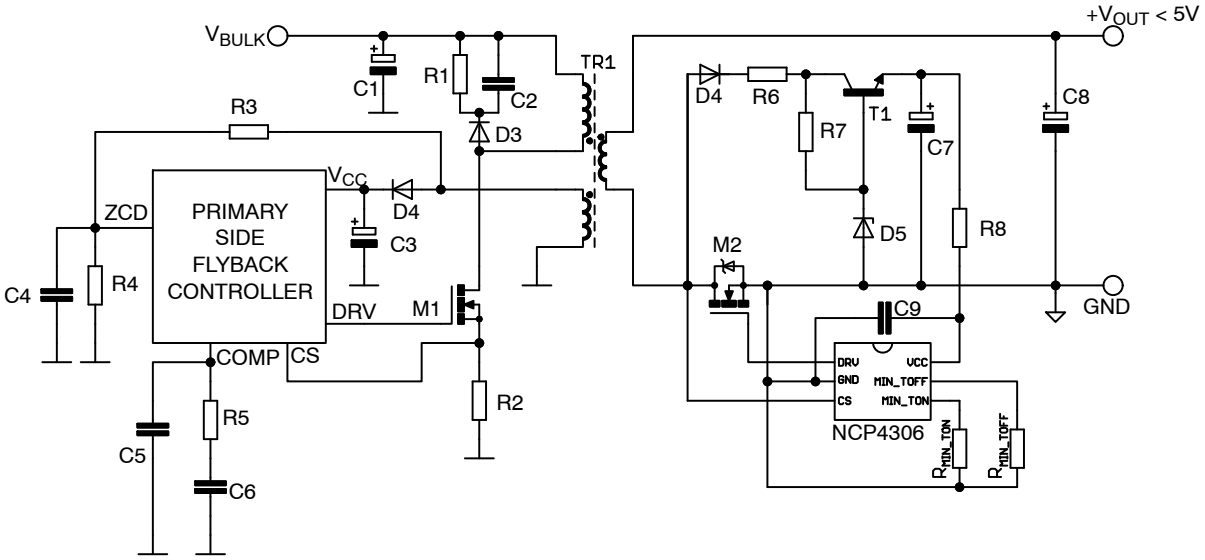


Figure 45. Low Side Configuration Supplied from Transformer Forward Voltage for Low V_{OUT} SMPS

Current Sense Input

Figure 46 shows the internal connection of the CS circuitry on the current sense input. When the voltage on the secondary winding of the SMPS reverses, the body diode of M1 starts to conduct current and the voltage of M1's drain drops approximately to −1 V. Once the voltage on the CS pin is lower than $V_{TH\_CS\_ON}$ threshold, M1 is turned−on. Because of parasitic impedances, significant ringing can occur in the application. To overcome false sudden turn−off due to mentioned ringing, the minimum conduction time of the SR MOSFET is activated. Minimum conduction time can be adjusted using the R_{MIN_TON} resistor or can be chosen from internal fixed values.

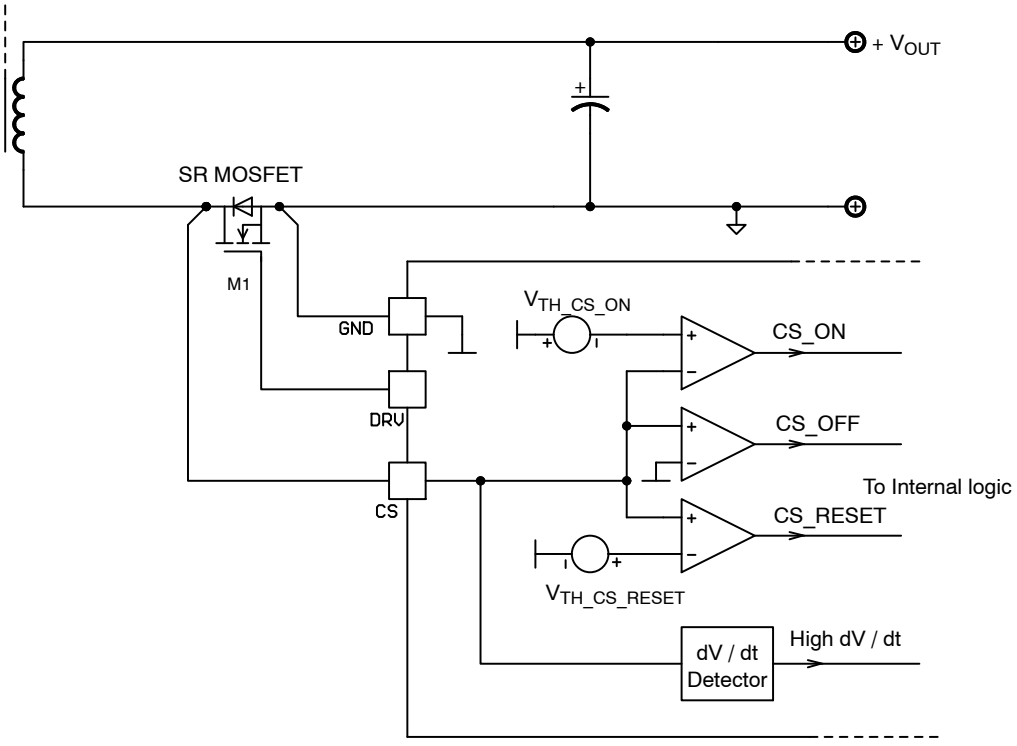


Figure 46. Current Sensing Circuitry Functionality

The SR MOSFET is turned−off as soon as the voltage on the CS pin is higher than $V_{TH\_CS\_OFF}$ (typically −0.5 mV). For the same ringing reason, a minimum off−time timer is asserted once the V_{CS} goes above $V_{TH\_CS\_RESET}$. The minimum off−time can be externally adjusted using R_{MIN_TOFF} resistor or can be chosen from internally fixed values (depends on version). The minimum off−time generator can be re−triggered by MIN_TOFF reset comparator if some spurious ringing occurs on the CS input after SR MOSFET turn−off event. This feature significantly simplifies SR system implementation in flyback converters.

In an LLC converter the SR MOSFET M1 channel conducts while secondary side current is decreasing (refer to Figure 47). Therefore the turn−off current depends on MOSFET R_{DSON}. The −0.5 mV threshold provides an optimum switching period usage while keeping enough time margin for the gate turn−off. To ensure proper switching, the min_t_{OFF} timer is reset, when the V_{DS} of the MOSFET rings and falls down past the $V_{TH\_CS\_RESET}$. The minimum off−time needs to expire before another drive pulse can be initiated. Minimum off−time timer is started again when V_{DS} rises above $V_{TH\_CS\_RESET}$.

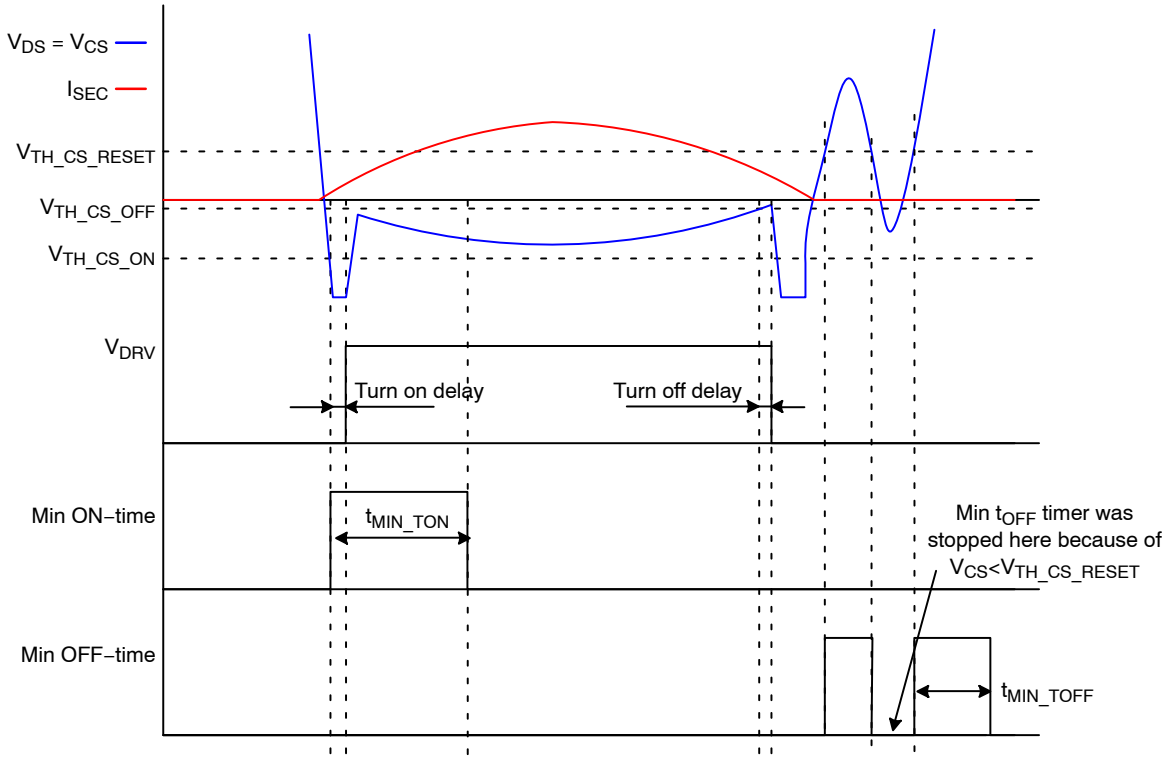


Figure 47. CS Input Comparators Thresholds and Blanking Periods Timing in LLC

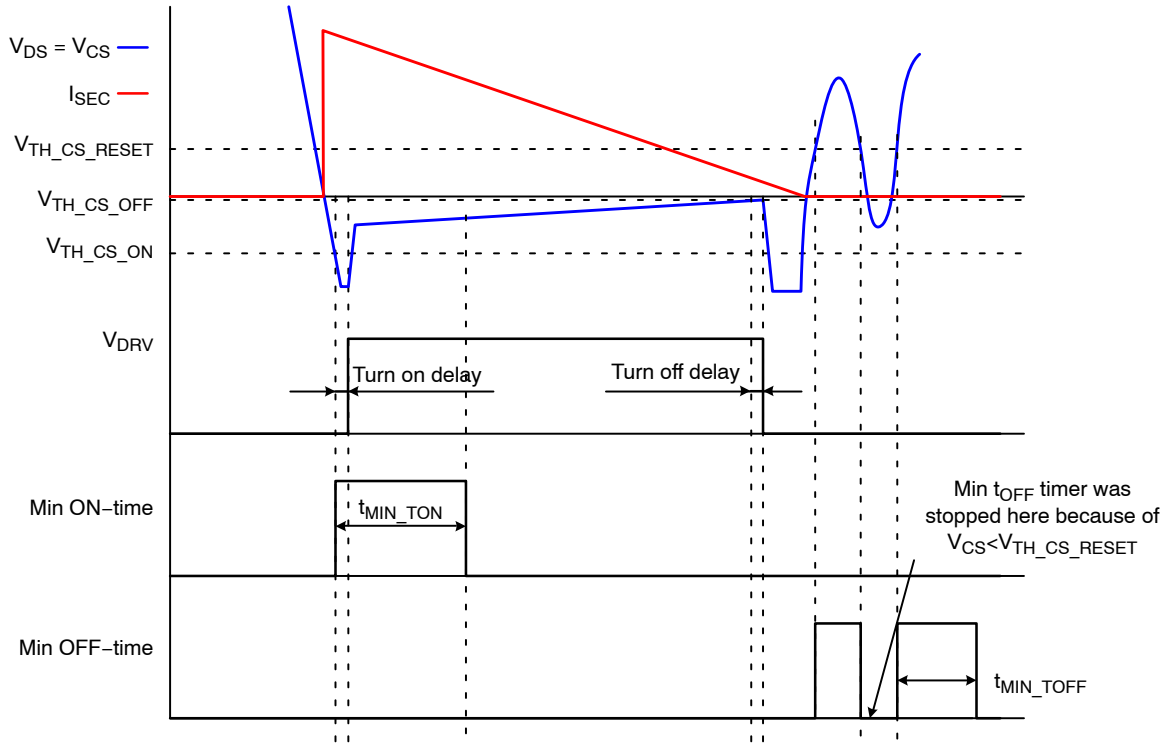


Figure 48. CS Input Comparators Thresholds and Blanking Periods Timing in Flyback

SR Transistor Selection

An SMPS designer should consider all important SR MOSFET parameters for its optimum selection in given application and not stick only to the lowest $R_{DS(ON)}$ requirement. The lower $R_{DS(ON)}$ device is selected the more significant role the lead parasitic inductances play in turn−of threshold sensing i.e. the more premature turn−off will happen (refer to section below for parasitic inductance impact to V_{DS} sensing). The lower $R_{DS(ON)}$ switch also usually features higher input capacitance that increases driving losses. The higher output capacitance and higher reverse recovery charge of body diode then results in higher drain−to source voltage peaks in CCM applications. Thus the higher $R_{DS(ON)}$ MOSFET can usually provide better or at least same efficiency result when compare to a switch which was selected with minimum available $R_{DS(ON)}$ resistance requirement only.

Sensing V_{DS} drop across the SR transistor, which is ideally product of transistor's $R_{DS(ON)}$ and secondary side current, is affected by voltage drop at parasitic inductance of package (bonding, leads, …) and PCB layout−(refer to Figure 49). The current that flows through the SR MOSFET experiences a high $\Delta i(t) / \Delta t$ that induces an error voltage on the SR MOSFET bonds and leads due to their parasitic inductance. This error voltage is proportional to the derivative of the SR MOSFET current; and shifts the CS input voltage to zero when significant current still flows through the MOSFET channel. As a result, the SR MOSFET is turned−off prematurely and the efficiency of the SMPS is not optimized – refer to Figure 50 for a better understanding.

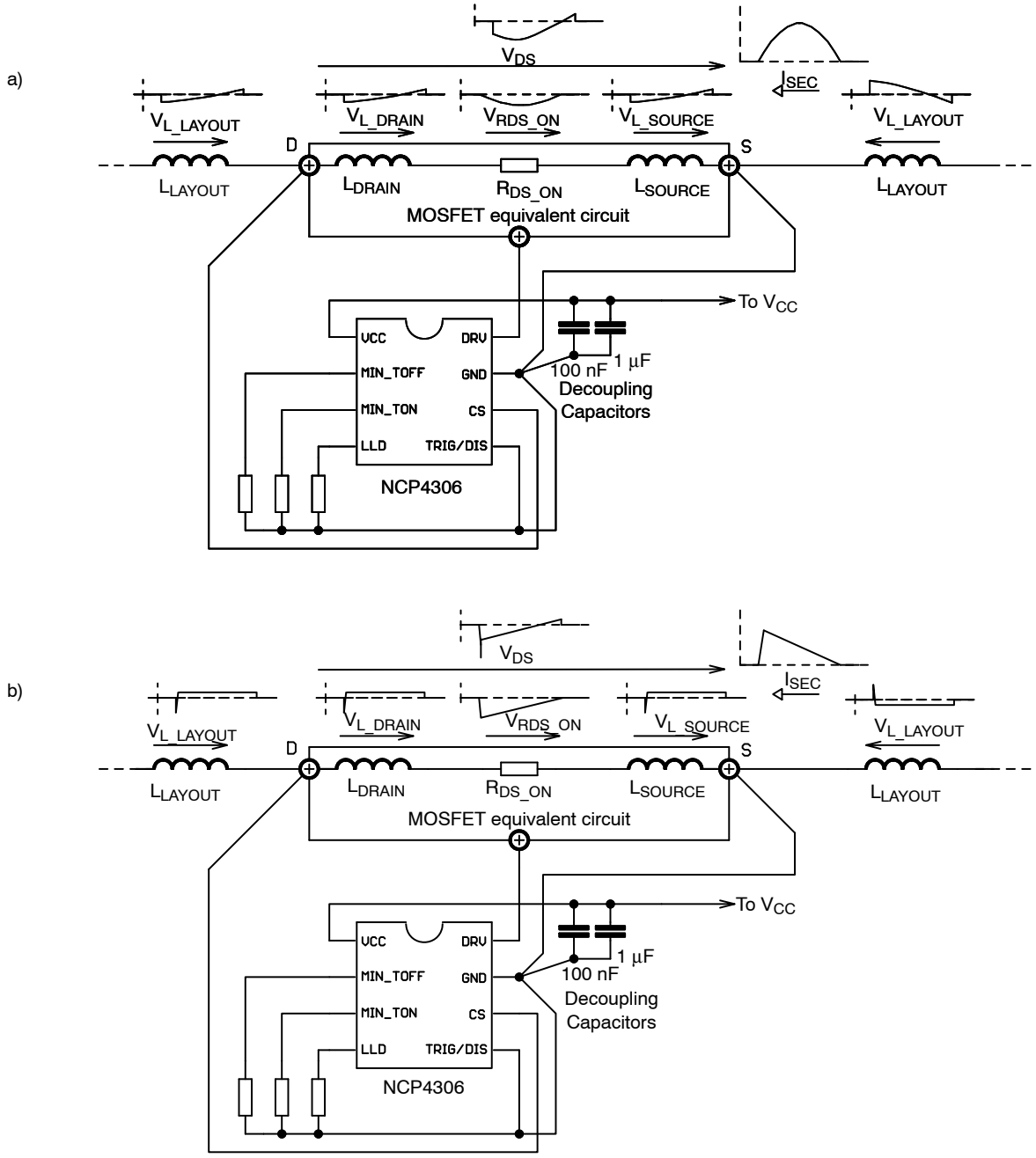


Figure 49. SR System Connection Including MOSFET and Layout Parasitic Inductances in a) LLC and b) Flyback Application

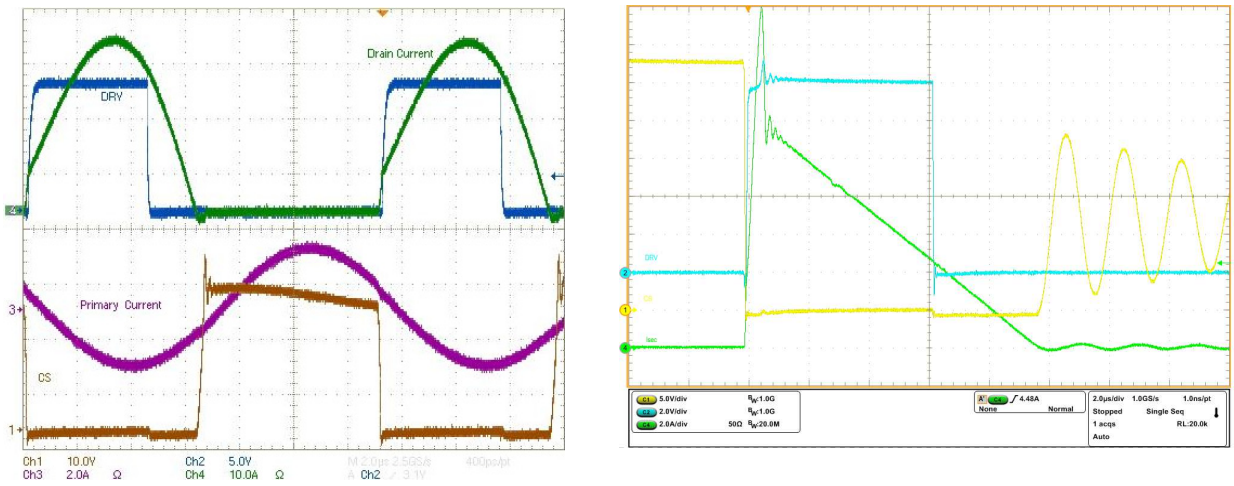


Figure 50. Waveforms from SR System Implemented in a) LLC and b) Flyback Application and Using MOSFET in TO220 Package With Long Leads – SR MOSFET channel Conduction Time is Reduced

Note that the efficiency impact caused by the error voltage due to the parasitic inductance increases with lower MOSFETs R_{DS_ON} and / or higher operating frequency.

It is thus beneficial to minimize SR MOSFET package leads length in order to maximize application efficiency. The optimum solution for applications with high secondary current Δi / Δt and high operating frequency is to use lead−less SR MOSFET i.e. SR MOSFET in SMT package. The parasitic inductance of a SMT package is negligible causing insignificant CS turn−off threshold shift and thus minimum impact to efficiency (refer to Figure 51).

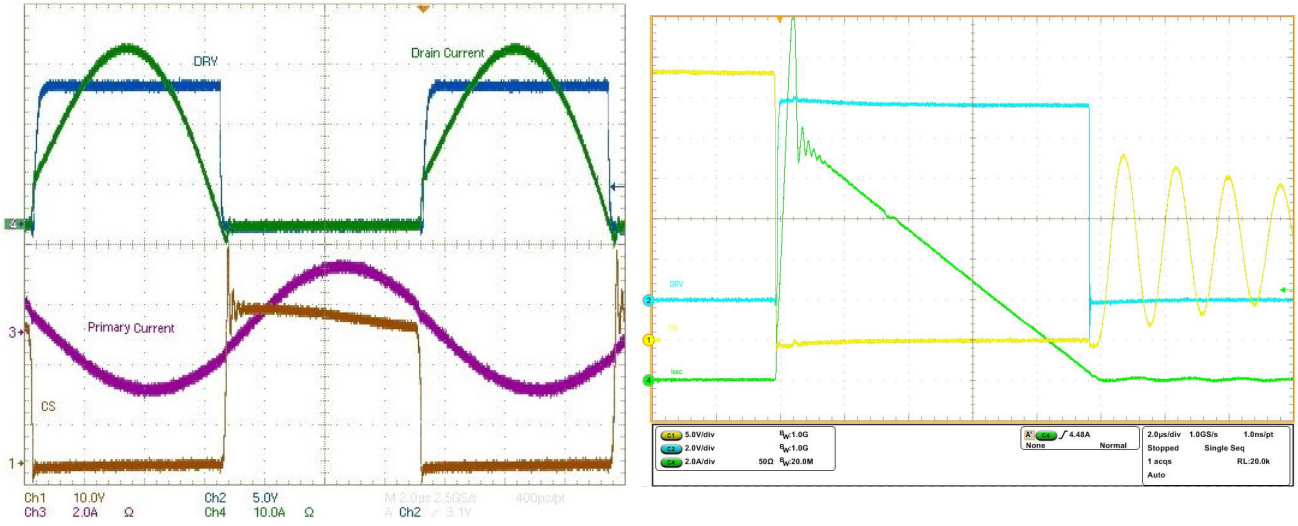


Figure 51. Waveforms from SR System Implemented in a) LLC b) Flyback Application and Using MOSFET in SMT Package with Minimized Parasitic Inductance – SR MOSFET Channel Conduction Time is Optimized

It can be deduced from the above paragraphs on the induced error voltage and parameter tables that turn−off threshold precision is quite critical. If we consider a SR MOSFET with R_{DS_ON} of 1 mΩ, the 1 mV error voltage on the CS pin results in a 1 A turn−off current threshold difference; thus the PCB layout is very critical when implementing the SR system. Note that the CS turn−off comparator is referred to the GND pin. Any parasitic impedance (resistive or inductive – even on the magnitude of mΩ and nH values) can cause a high error voltage that is then evaluated by the CS comparator. Ideally the CS turn−off comparator should detect voltage that is caused by secondary current directly on the SR MOSFET channel resistance. In reality there will be small parasitic impedance on the CS path due to the bonding wires, leads and soldering. To assure the best efficiency results, a Kelvin connection of the SR controller to the power circuitry should be implemented. The GND pin should be connected to the SR MOSFET source soldering point and current sense pin should be connected to the SR MOSFET drain soldering point – refer to Figure 49. Using a Kelvin connection will avoid any impact of PCB layout parasitic elements on the SR controller functionality; SR MOSFET parasitic elements will still play a role in attaining an error voltage. Figure 52 and Figure 53 show examples of SR system layouts using MOSFETs in D2PAK and SO8FL packages.

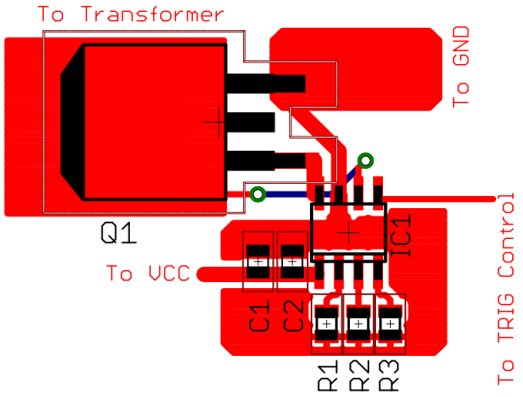


Figure 52. Recommended Layout When Using SR MOSFET in D2PAK Package

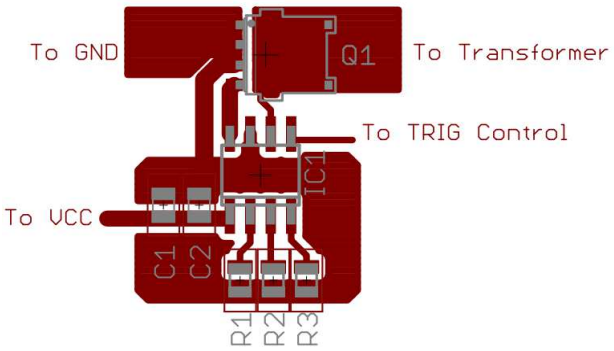


Figure 53. Recommended Layout When Using SR MOSFET in SMT Package SO8 FL

Trigger / Disable input

The NCP4306 features an ultrafast trigger input that exhibits a maximum of t_{PD_TRIG} delay from its activation to the start of SR MOSFET turn−off of process. This input can be used in applications operated in deep Continues Conduction Mode (CCM) to further increase efficiency and / or to activate disable mode of the SR driver in which the consumption of the NCP4306 is reduced to maximum of I_{CC_DIS}.

NCP4306 is capable to turn−off the SR MOSFET reliably in CCM applications just based on CS pin information only, without using the trigger input. However, natural delay of the ZCD comparator and DRV turn−off delay increase overlap between primary and secondary MOSFETs switching (also known as cross conduction). If one wants to achieve absolutely maximum efficiency with deep CCM applications, then the trigger signal coming from the primary side should be applied to the trigger pin. It is good to set trigger pulse in way there is just short overlap between primary and secondary switches. Short overlap is usually advantageous than leaving end of conduction phase on body diode. Reason is body diode has usually longer recovery time and resulting overlap time (simultaneously conduction primary and secondary side switches) is longer. There are several possibilities for transferring the trigger signal from the primary to the secondary side – refer to Figure 68 and Figure 69.

The trigger signal is blanked for t_{TRIG_BLANK} after the DRV turn−on process has begun. The blanking technique is used to increase trigger input noise immunity against the parasitic ringing that is present during the turn on process due to the SMPS layout. The trigger input is supersedes the CS input except trigger blanking period. TRIG / DIS signal turns the SR MOSFET off or prohibits its turn−on when the TRIG / DIS pin is pulled above V_{TRIG_TH}.

The SR controller enters disable mode when the trigger pin is pulled−up for more than t_{DIS_TIM}. In disable mode the IC consumption is significantly reduced. To recover from disable mode and enter normal operation, the TRIG / DIS pin has to be pulled low at least for t_{DIS_END}.

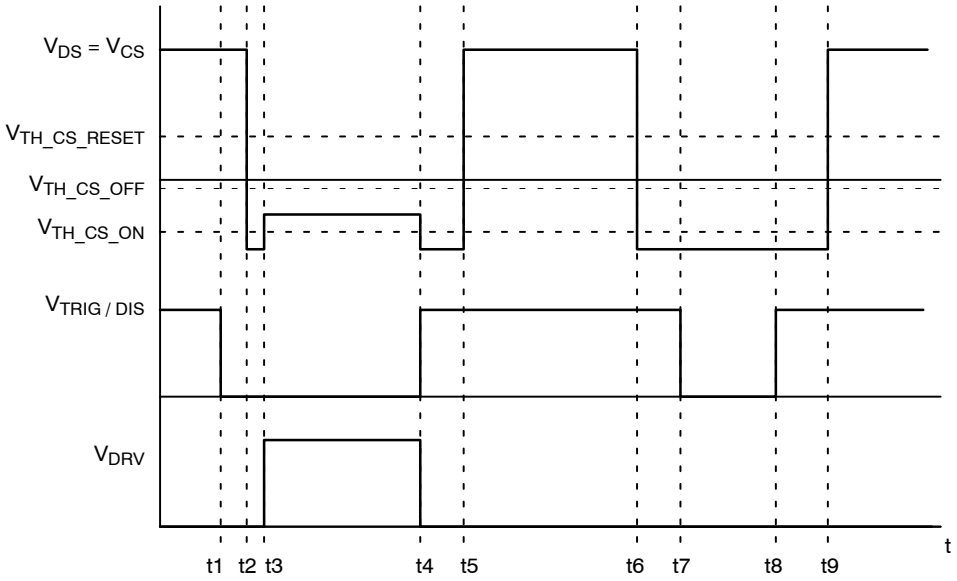


Figure 54. Trigger Input Functionality Waveforms Using the Trigger to Turn−off and Block the DRV Signal

Figure 54 shows basic TRIG / DIS input functionality. At t1 the TRIG / DIS pin is pulled low to enter into normal operation. At t2 the CS pin is dropped below the $V_{TH\_CS\_ON}$, signaling to the NCP4306 to start to turn the SR MOSFET on. At t3 the NCP4306 begins to drive the MOSFET. At t4, the SR MOSFET is conducting and the TRIG / DIS pin is pulled high. This high signal on the TRIG / DIS pin almost immediately turns off the drive to the SR MOSFET, turning off the MOSFET. The DRV is not turned−on in other case (t6) because the trigger pin is high in the time when CS pin signal crosses turn−on threshold. This figure clearly shows that the DRV can be asserted only on falling edge of the CS pin signal in case the trigger input is at low level (t2).

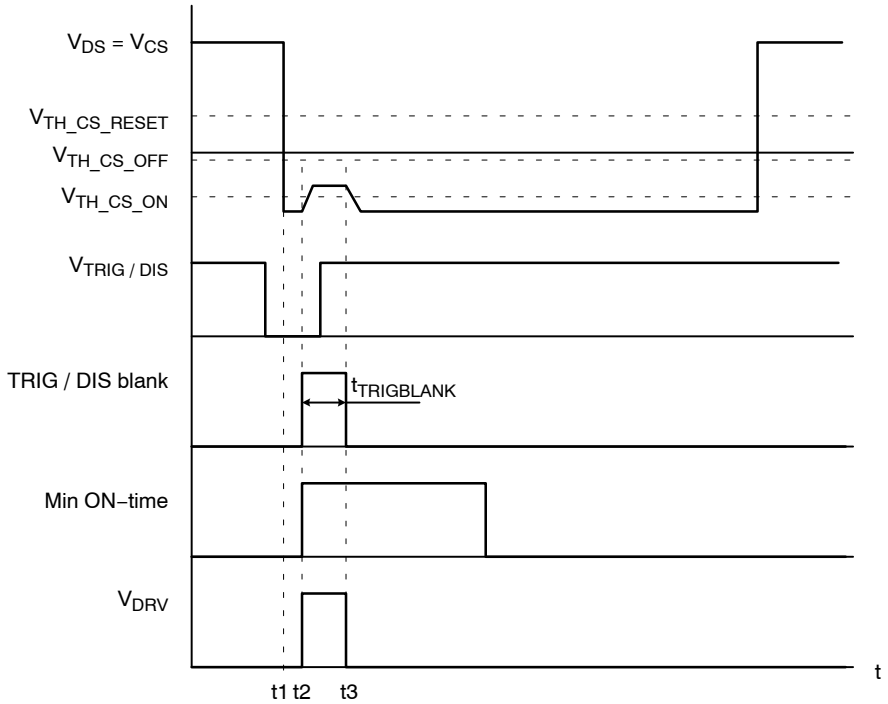


Figure 55. Trigger Input Functionality Waveforms – Trigger Blanking

In Figure 55 above, at time t1 the CS pin falls below the $V_{TH\_CS\_ON}$ while the Trigger is low setting in motion the DRV signal that appears at t2. At time t2 the DRV signal and Trigger blanking clock begin. TRIG / DIS signal goes high shortly after time t2. Due to the Trigger blanking clock (t_{TRIG_BLANK}) the Trigger's high signal does not affect the DRV signal until the t_{TRIG_BLANK} timer has expired. At time t3 the TRIG / DIS signal is reevaluated and the DRV

signal is turned off. The TRIG / DIS input is blanked for t_{TRIG_BLANK} after DRV set signal to avoid undesirable behavior during SR MOSFET turn−on event. The blanking time in combination with high threshold voltage (V_{TRIG_TH}) prevent triggering on ringing and spikes that are present on the TRIG / DIS input pin during the SR MOSFET turn−on process. Controller's response to the narrow pulse on the TRIG / DIS pin is depicted in Figure 55 – this short trigger pulse enables to turn the DRV on for t_{TRIG_BLANK}. Note that this case is valid only if device not entered disable mode before.

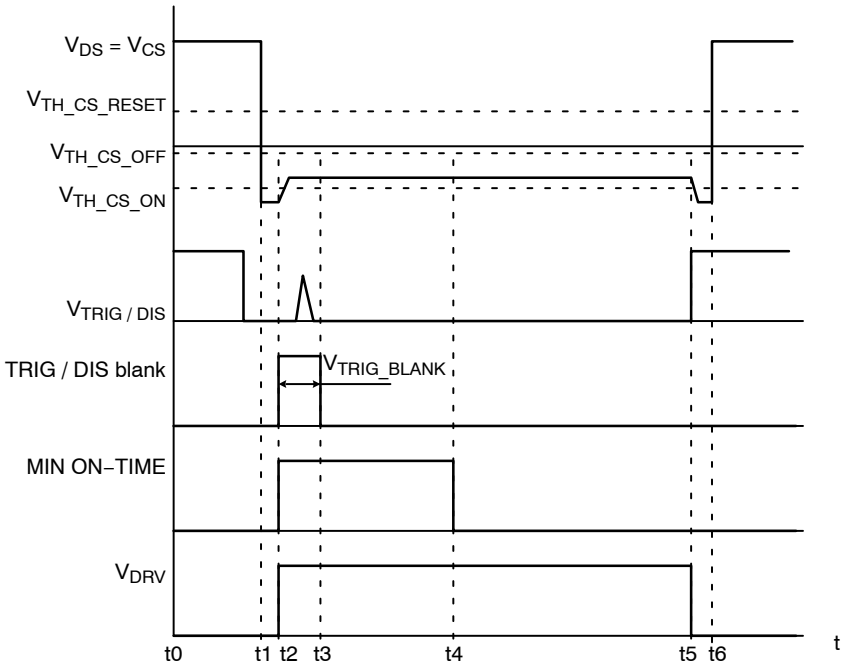


Figure 56. Trigger Input Functionality Waveforms – Trigger Blanking Acts Like a Filter

Figure 56 above shows almost the same situation as in Figure 55 with one main exception; the TRIG / DIS signal was not high after trigger blanking timer expired so the DRV signal remains high. The advantage of the trigger blanking time during DRV turn−on is evident from Figure 56 since it acts like a filter on the TRIG / DIS pin. Rising edge of the DRV signal may cause spikes on the trigger input. If it wasn't for the TRIG / DIS blanking these spikes, in combination with ultra−fast performance of the trigger logic, could turn the SR MOSFET off in an inappropriate time.

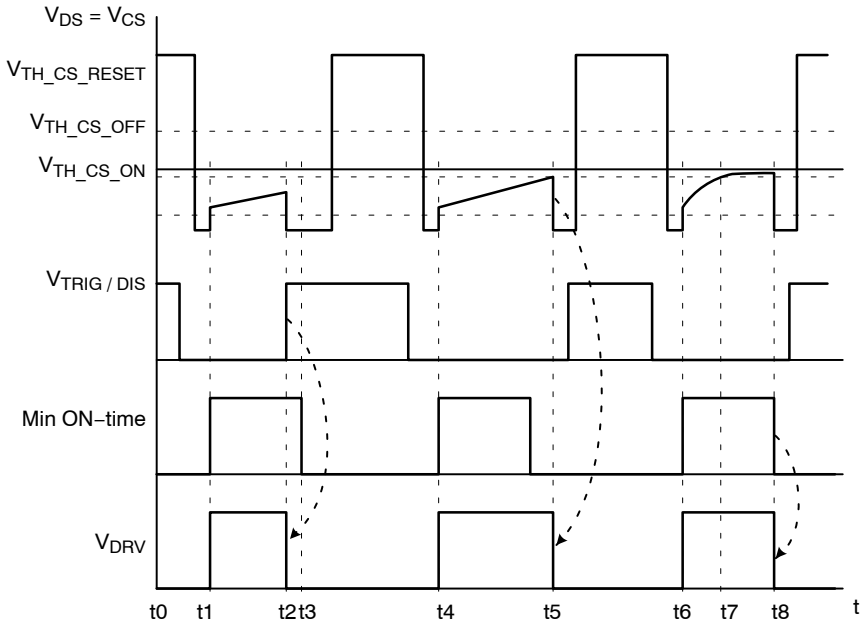


Figure 57. Trigger Input Functionality Waveforms – Trigger over Ride, CS Turn Off and Min On−time