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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# NCP43080

## Synchronous Rectifier Controller

The NCP43080 is a synchronous rectifier controller for switch mode power supplies. The controller enables high efficiency designs for flyback and quasi resonant flyback topologies.

Externally adjustable minimum off-time and on-time blanking periods provides flexibility to drive various MOSFET package types and PCB layout. A reliable and noise less operation of the SR system is insured due to the Self Synchronization feature. The NCP43080 also utilizes Kelvin connection of the driver to the MOSFET to achieve high efficiency operation at full load and utilizes a light load detection architecture to achieve high efficiency at light load.

The precise turn-off threshold, extremely low turn-off delay time and high sink current capability of the driver allow the maximum synchronous rectification MOSFET conduction time. The high accuracy driver and 5 V gate clamp make it ideally suited for directly driving GaN devices.

### Features

- Self-Contained Control of Synchronous Rectifier in CCM, DCM and QR for Flyback, Forward or LLC Applications
- Precise True Secondary Zero Current Detection
- Rugged Current Sense Pin (up to 150 V)
- Adjustable Minimum ON-Time
- Adjustable Minimum OFF-Time with Ringing Detection
- Adjustable Maximum ON-Time for CCM Controlling of Primary QR Controller
- Improved Robust Self Synchronization Capability
- 8 A / 4 A Peak Current Sink / Source Drive Capability
- Operating Voltage Range up to  $V_{CC} = 35\text{ V}$
- Automatic Light-load & Disable Mode
- Adaptive Gate Drive Clamp
- GaN Transistor Driving Capability (options A and C)
- Low Startup and Disable Current Consumption
- Maximum Operation Frequency up to 1 MHz
- SOIC-8 and DFN-8 (4x4) and WDFN8 (2x2) Packages
- These are Pb-Free Devices

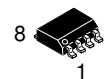
### Typical Applications

- Notebook Adapters
- High Power Density AC/DC Power Supplies (Cell Phone Chargers)
- LCD TVs
- All SMPS with High Efficiency Requirements

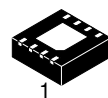


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SOIC-8  
D SUFFIX  
CASE 751

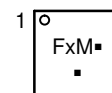
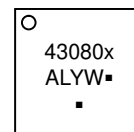
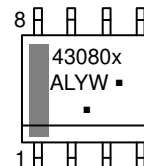


DFN8  
MN SUFFIX  
CASE 488AF



WDFN8  
MT SUFFIX  
CASE 511AT

### MARKING DIAGRAMS



43080x = Specific Device Code  
x = A, B, C, D or Q  
Fx = Specific Device Code  
x = A or D  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 33 of this data sheet.

# NCP43080

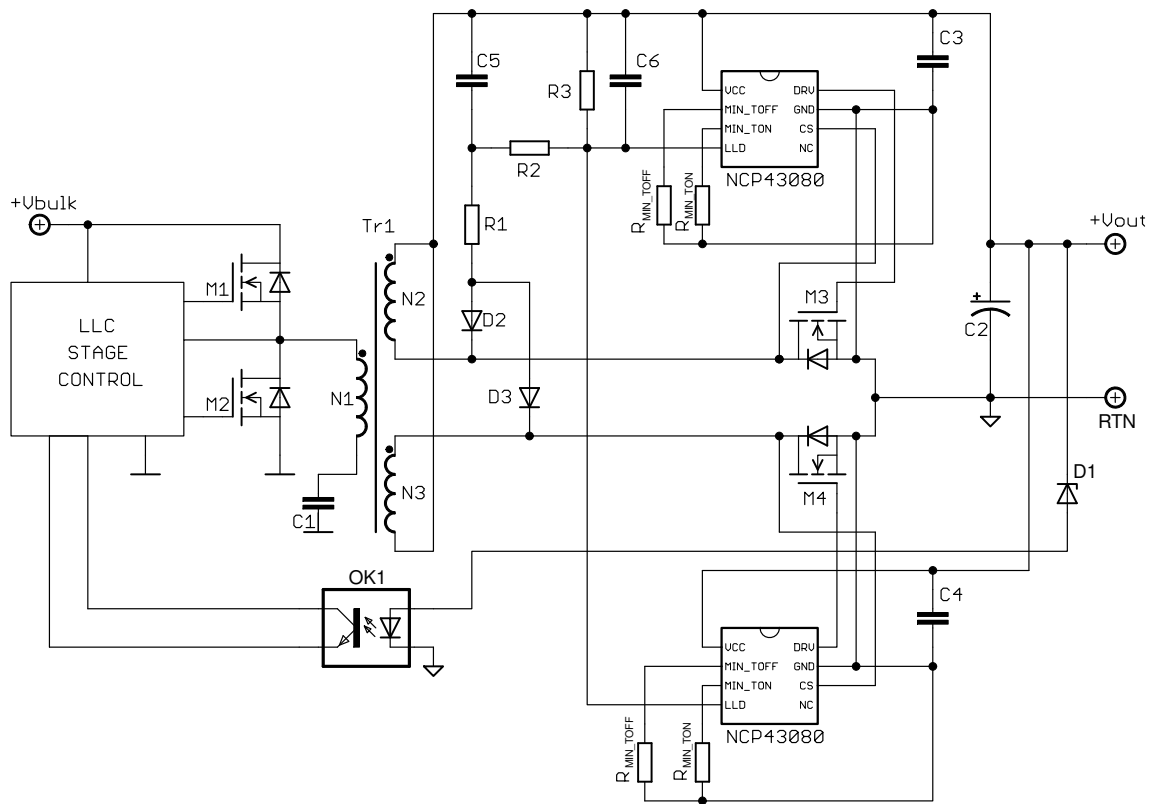


Figure 1. Typical Application Example – LLC Converter with Optional LLD

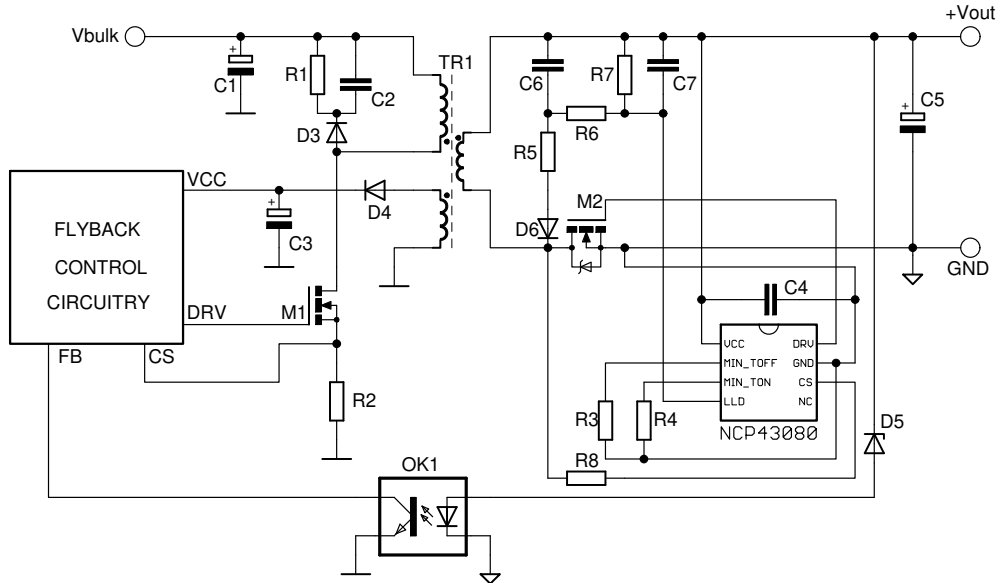
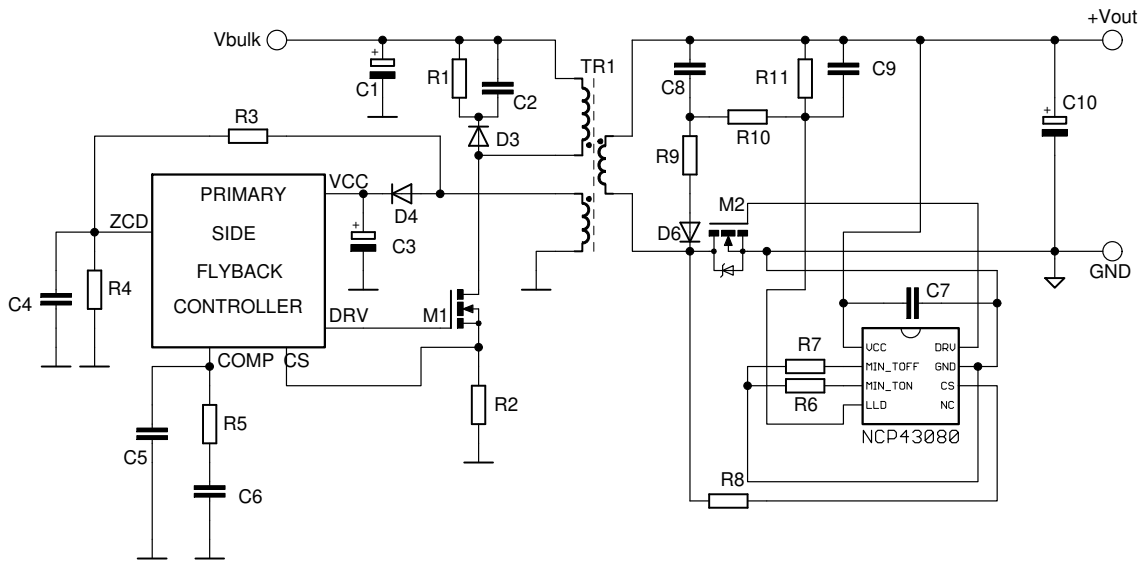
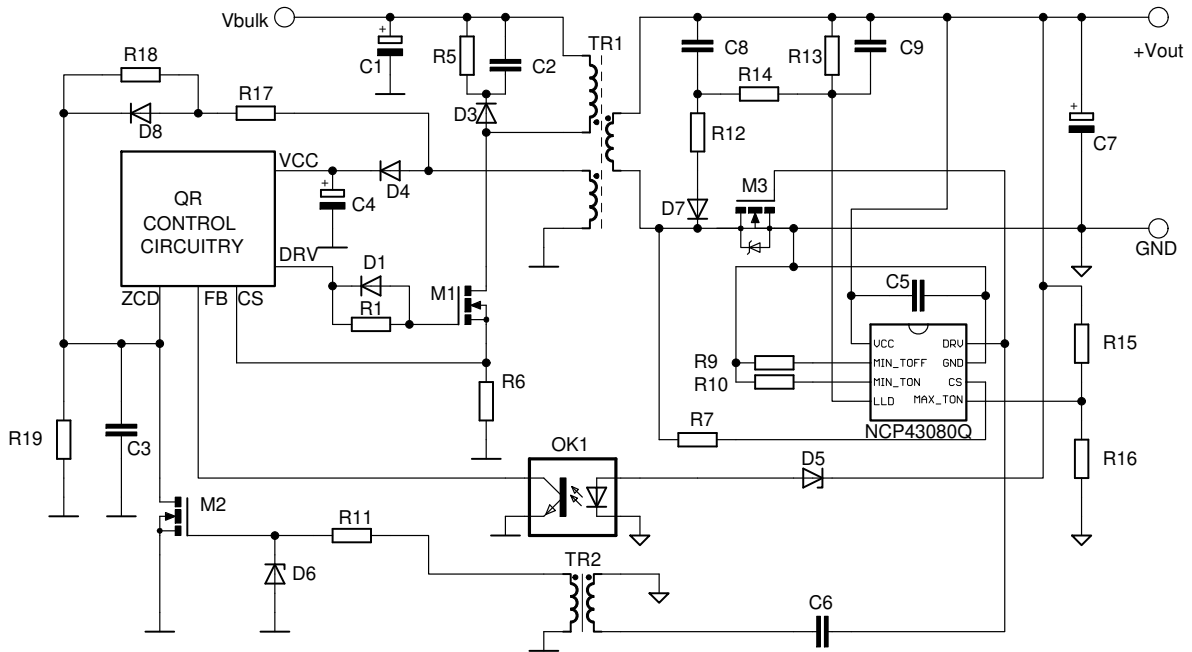


Figure 2. Typical Application Example – DCM, CCM or QR Flyback Converter with optional LLD

# NCP43080



**Figure 3. Typical Application Example – Primary Side Flyback Converter with optional LLD**



**Figure 4. Typical Application Example – QR Converter – Capability to Force Primary into CCM Under Heavy Loads utilizing MAX-TON**

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## PIN FUNCTION DESCRIPTION

ver. A, B, C, D	ver. Q	Pin Name	Description
1	1	VCC	Supply voltage pin
2	2	MIN_TOFF	Adjust the minimum off time period by connecting resistor to ground.
3	3	MIN_TON	Adjust the minimum on time period by connecting resistor to ground.
4	4	LLD	This input modulates the driver clamp level and/or turns the driver off during light load conditions.
5	–	NC	Leave this pin opened or tie it to ground.
6	6	CS	Current sense pin detects if the current flows through the SR MOSFET and/or its body diode. Basic turn-off detection threshold is 0 mV. A resistor in series with this pin can decrease the turn off threshold if needed.
7	7	GND	Ground connection for the SR MOSFET driver, V <sub>CC</sub> decoupling capacitor and for minimum on and off time adjust resistors and LLD input. GND pin should be wired directly to the SR MOSFET source terminal/soldering point using Kelvin connection. DFN8 exposed flag should be connected to GND
8	8	DRV	Driver output for the SR MOSFET
–	5	MAX_TON	Adjust the maximum on time period by connecting resistor to ground.

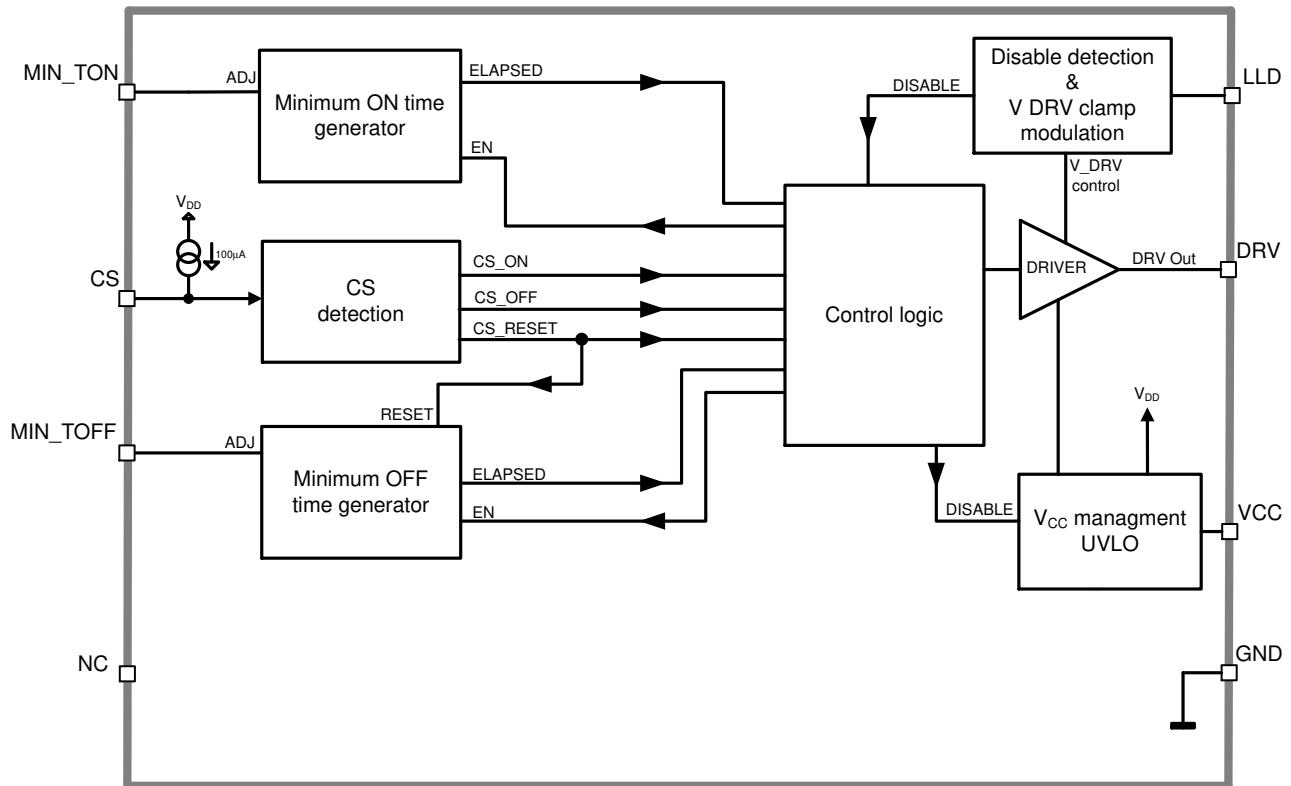


Figure 5. Internal Circuit Architecture – NCP43080A, B, C, D

# NCP43080

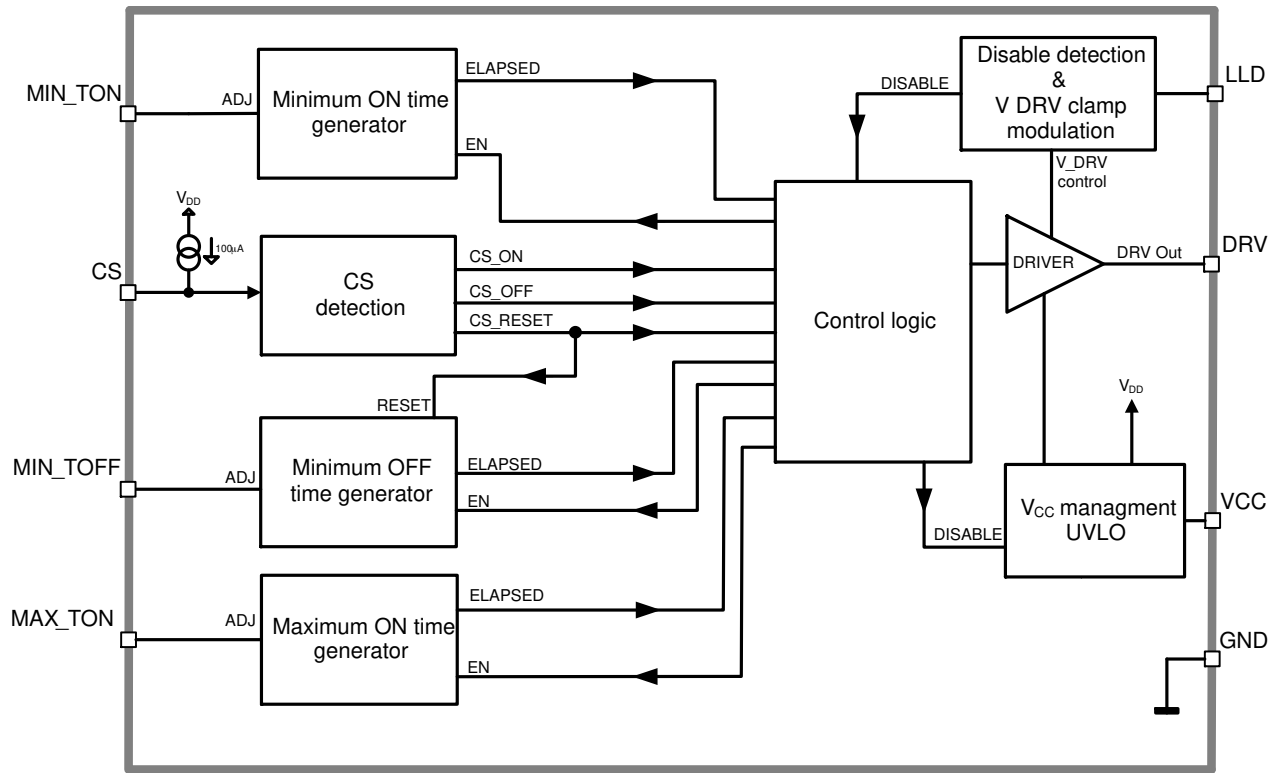


Figure 6. Internal Circuit Architecture – NCP43080Q (CCM QR) with MAX\_TON

# NCP43080

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	-0.3 to 37.0	V
MIN_TON, MIN_TOFF, MAX_TON, LLD Input Voltage	$V_{MIN\_TON}$ , $V_{MIN\_TOFF}$ , $V_{MAX\_TON}$ , $V_{LLD}$	-0.3 to $V_{CC}$	V
Driver Output Voltage	$V_{DRV}$	-0.3 to 17.0	V
Current Sense Input Voltage	$V_{CS}$	-4 to 150	V
Current Sense Dynamic Input Voltage ( $t_{PW} = 200$ ns)	$V_{CS\_DYN}$	-10 to 150	V
MIN_TON, MIN_TOFF, MAX_TON, LLD Input Current	$I_{MIN\_TON}$ , $I_{MIN\_TOFF}$ , $I_{MAX\_TON}$ , $I_{LLD}$	-10 to 10	mA
Junction to Air Thermal Resistance, 1 oz 1 in <sup>2</sup> Copper Area, SOIC8	$R_{\theta J-A\_SOIC8}$	160	°C/W
Junction to Air Thermal Resistance, 1 oz 1 in <sup>2</sup> Copper Area, DFN8	$R_{\theta J-A\_DFN8}$	80	°C/W
Junction to Air Thermal Resistance, 1 oz 1 in <sup>2</sup> Copper Area, WDFN8	$R_{\theta J-A\_WDFN8}$	160	°C/W
Maximum Junction Temperature	$T_{JMAX}$	150	°C
Storage Temperature	$T_{STG}$	-60 to 150	°C
ESD Capability, Human Body Model, Except Pin 6, per JESD22-A114E	$ESD_{HBM}$	2000	V
ESD Capability, Human Body Model, Pin 6, per JESD22-A114E	$ESD_{HBM}$	1000	V
ESD Capability, Machine Model, per JESD22-A115-A	$ESD_{MM}$	200	V
ESD Capability, Charged Device Model, Except Pin 6, per JESD22-C101F	$ESD_{CDM}$	750	V
ESD Capability, Charged Device Model, Pin 6, per JESD22-C101F	$ESD_{CDM}$	250	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device meets latch-up tests defined by JEDEC Standard JESD78D Class I.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Maximum Operating Input Voltage	$V_{CC}$		35	V
Operating Junction Temperature	$T_J$	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS

-40°C ≤  $T_J$  ≤ 125°C;  $V_{CC} = 12$  V;  $C_{DRV} = 0$  nF;  $R_{MIN\_TON} = R_{MIN\_TOFF} = 10$  kΩ;  $V_{LLD} = 0$  V;  $V_{CS} = -1$  to +4 V;  $f_{CS} = 100$  kHz,  $DC_{CS} = 50\%$ , unless otherwise noted. Typical values are at  $T_J = +25$ °C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
<b>SUPPLY SECTION</b>						
VCC UVLO (ver. B & C)	$V_{CC}$ rising	$V_{CCON}$	8.3	8.8	9.3	V
	$V_{CC}$ falling	$V_{CCOFF}$	7.3	7.8	8.3	
VCC UVLO Hysteresis (ver. B & C)		$V_{CCHYS}$		1.0		V
VCC UVLO (ver. A, D & Q)	$V_{CC}$ rising	$V_{CCON}$	4.20	4.45	4.80	V
	$V_{CC}$ falling	$V_{CCOFF}$	3.70	3.95	4.20	
VCC UVLO Hysteresis (ver. A, D & Q)		$V_{CCHYS}$		0.5		V
Start-up Delay	$V_{CC}$ rising from 0 to $V_{CCON} + 1$ V @ $tr = 10$ μs	$t_{START\_DEL}$		75	125	μs

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## ELECTRICAL CHARACTERISTICS

-40°C ≤ T<sub>J</sub> ≤ 125°C; V<sub>CC</sub> = 12 V; C<sub>DRV</sub> = 0 nF; R<sub>MIN\_TON</sub> = R<sub>MIN\_TOFF</sub> = 10 kΩ; V<sub>LLD</sub> = 0 V; V<sub>CS</sub> = -1 to +4 V; f<sub>CS</sub> = 100 kHz, DC<sub>CS</sub> = 50%, unless otherwise noted. Typical values are at T<sub>J</sub> = +25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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### SUPPLY SECTION

Current Consumption, R <sub>MIN_TON</sub> = R <sub>MIN_TOFF</sub> = 0 kΩ	C <sub>DRV</sub> = 0 nF, f <sub>SW</sub> = 500 kHz	A, C	I <sub>CC</sub>	3.0	4.0	5.6	mA
		B, D, Q		3.5	4.5	6.0	
	C <sub>DRV</sub> = 1 nF, f <sub>SW</sub> = 500 kHz	A, C		4.5	6.0	7.5	
		B, D, Q		7.7	9.0	10.7	
	C <sub>DRV</sub> = 10 nF, f <sub>SW</sub> = 500 kHz	A, C		20	25	30	
		B, D, Q		40	50	60	
Current Consumption	No switching, V <sub>CS</sub> = 0 V, R <sub>MIN_TON</sub> = R <sub>MIN_TOFF</sub> = 0 kΩ	I <sub>CC</sub>	1.0	2.0	2.5	mA	
Current Consumption below UVLO	No switching, V <sub>CC</sub> = V <sub>CCOFF</sub> - 0.1 V, V <sub>CS</sub> = 0 V	I <sub>CC_UVLO</sub>		75	125	μA	
Current Consumption in Disable Mode	V <sub>LLD</sub> = V <sub>CC</sub> - 0.1 V, V <sub>CS</sub> = 0 V	I <sub>CC_DIS</sub>	30	55	75	μA	

### DRIVER OUTPUT

Output Voltage Rise-Time	C <sub>DRV</sub> = 10 nF, 10% to 90% V <sub>DRVMAX</sub>	t <sub>r</sub>		40	55	ns
Output Voltage Fall-Time	C <sub>DRV</sub> = 10 nF, 90% to 10% V <sub>DRVMAX</sub>	t <sub>f</sub>		20	35	ns
Driver Source Resistance		R <sub>DRV_SOURCE</sub>		1.2		Ω
Driver Sink Resistance		R <sub>DRV_SINK</sub>		0.5		Ω
Output Peak Source Current		I <sub>DRV_SOURCE</sub>		4		A
Output Peak Sink Current		I <sub>DRV_SINK</sub>		8		A
Maximum Driver Output Voltage	V <sub>CC</sub> = 35 V, C <sub>DRV</sub> > 1 nF, V <sub>LLD</sub> = 0 V, (ver. B, D and Q)	V <sub>DRVMAX</sub>	9.0	9.5	10.5	V
	V <sub>CC</sub> = 35 V, C <sub>DRV</sub> > 1 nF, V <sub>LLD</sub> = 0 V, (ver. A, C)		4.3	4.7	5.5	
Minimum Driver Output Voltage	V <sub>CC</sub> = V <sub>CCOFF</sub> + 200 mV, V <sub>LLD</sub> = 0 V, (ver. B)	V <sub>DRVMIN</sub>	7.2	7.8	8.5	V
	V <sub>CC</sub> = V <sub>CCOFF</sub> + 200 mV, V <sub>LLD</sub> = 0 V, (ver. C)		4.2	4.7	5.3	
	V <sub>CC</sub> = V <sub>CCOFF</sub> + 200 mV, V <sub>LLD</sub> = 0 V		3.6	4.0	4.4	
Minimum Driver Output Voltage	V <sub>LLD</sub> = V <sub>CC</sub> - V <sub>LLDREC</sub> V	V <sub>DRVLLDMIN</sub>	0.0	0.4	1.2	V

### CS INPUT

Total Propagation Delay From CS to DRV Output On	V <sub>CS</sub> goes down from 4 to -1 V, t <sub>r_CS</sub> = 5 ns	t <sub>PD_ON</sub>		35	60	ns
Total Propagation Delay From CS to DRV Output Off	V <sub>CS</sub> goes up from -1 to 4 V, t <sub>r_CS</sub> = 5 ns	t <sub>PD_OFF</sub>		12	23	ns
CS Bias Current	V <sub>CS</sub> = -20 mV	I <sub>CS</sub>	-105	-100	-95	μA
Turn On CS Threshold Voltage		V <sub>TH_CS_ON</sub>	-120	-75	-40	mV
Turn Off CS Threshold Voltage	Guaranteed by Design	V <sub>TH_CS_OFF</sub>	-1		0	mV
Turn Off Timer Reset Threshold Voltage		V <sub>TH_CS_RESET</sub>	0.4	0.5	0.6	V
CS Leakage Current	V <sub>CS</sub> = 150 V	I <sub>CS_LEAKAGE</sub>			0.4	μA

### MINIMUM t<sub>ON</sub> and t<sub>OFF</sub> ADJUST

Minimum t <sub>ON</sub> time	R <sub>MIN_TON</sub> = 0 Ω	t <sub>ON_MIN</sub>	25	56	75	ns
Minimum t <sub>OFF</sub> time	R <sub>MIN_TOFF</sub> = 0 Ω	t <sub>OFF_MIN</sub>	160	245	290	ns
Minimum t <sub>ON</sub> time	R <sub>MIN_TON</sub> = 10 kΩ	t <sub>ON_MIN</sub>	0.92	1.00	1.08	μs
Minimum t <sub>OFF</sub> time	R <sub>MIN_TOFF</sub> = 10 kΩ	t <sub>OFF_MIN</sub>	0.92	1.00	1.08	μs
Minimum t <sub>ON</sub> time	R <sub>MIN_TON</sub> = 50 kΩ	t <sub>ON_MIN</sub>	4.62	5.00	5.38	μs
Minimum t <sub>OFF</sub> time	R <sub>MIN_TOFF</sub> = 50 kΩ	t <sub>OFF_MIN</sub>	4.62	5.00	5.38	μs



# NCP43080

## ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ;  $V_{CC} = 12\text{ V}$ ;  $C_{DRV} = 0\text{ nF}$ ;  $R_{MIN\_TON} = R_{MIN\_TOFF} = 10\text{ k}\Omega$ ;  $V_{LLD} = 0\text{ V}$ ;  $V_{CS} = -1\text{ to }+4\text{ V}$ ;  $f_{CS} = 100\text{ kHz}$ ,  $DC_{CS} = 50\%$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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### MAXIMUM $t_{ON}$ ADJUST

Maximum $t_{ON}$ Time	$V_{MAX\_TON} = 3\text{ V}$	$t_{ON\_MAX}$	4.3	4.8	5.3	$\mu\text{s}$
Maximum $t_{ON}$ Time	$V_{MAX\_TON} = 0.3\text{ V}$	$t_{ON\_MAX}$	41	48	55	$\mu\text{s}$
Maximum $t_{ON}$ Output Current	$V_{MAX\_TON} = 0.3\text{ V}$ , $V_{CS} = 0\text{ V}$	$I_{MAX\_TON}$	-105	-100	-95	$\mu\text{A}$

### LLD INPUT

Disable Threshold	$V_{LLD\_DIS} = V_{CC} - V_{LLD}$	$V_{LLD\_DIS}$	0.8	0.9	1.0	V
Recovery Threshold	$V_{LLD\_REC} = V_{CC} - V_{LLD}$	$V_{LLD\_REC}$	0.9	1.0	1.1	V
Disable Hysteresis		$V_{LLD\_DISH}$		0.1		V
Disable Time Hysteresis	Disable to Normal, Normal to Disable	$t_{LLD\_DISH}$		45		$\mu\text{s}$
Disable Recovery Time		$t_{LLD\_DIS\_REC}$	6.0	12.5	16.0	$\mu\text{s}$
Low Pass Filter Frequency		$f_{LPLL}$	6	10	13	kHz
Driver Voltage Clamp Threshold	$V_{DRV} = V_{DRVMAX}$ , $V_{LLDMAX} = V_{CC} - V_{LLD}$	$V_{LLDMAX}$		2.0		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL CHARACTERISTICS

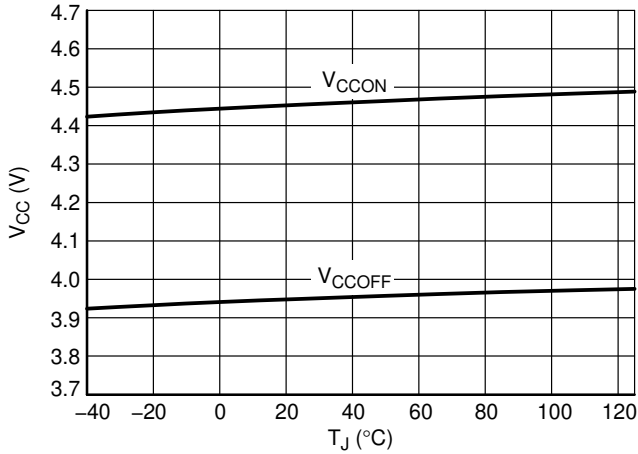


Figure 7.  $V_{CCON}$  and  $V_{CCOFF}$  Levels, ver. A, D, Q

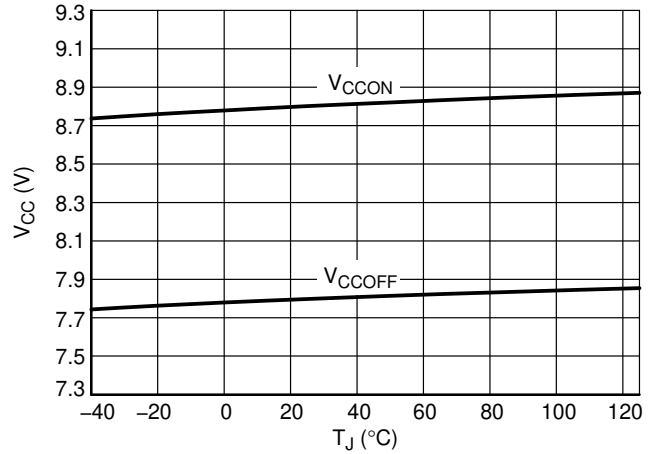


Figure 8.  $V_{CCON}$  and  $V_{CCOFF}$  Levels, ver. B, C

TYPICAL CHARACTERISTICS

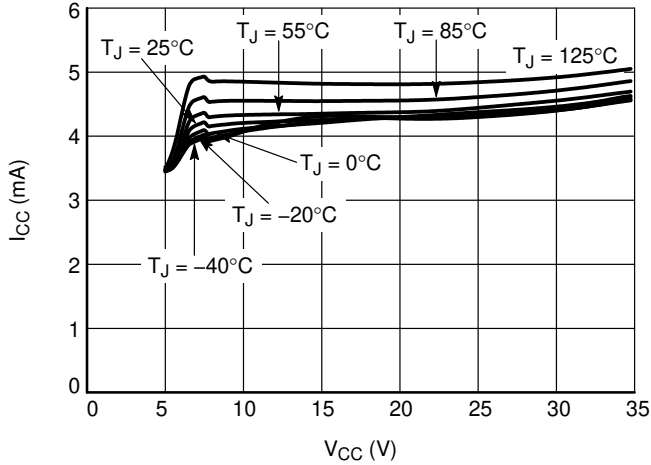


Figure 9. Current Consumption,  $C_{DRV} = 0 \text{ nF}$ ,  $f_{CS} = 500 \text{ kHz}$ , ver. D

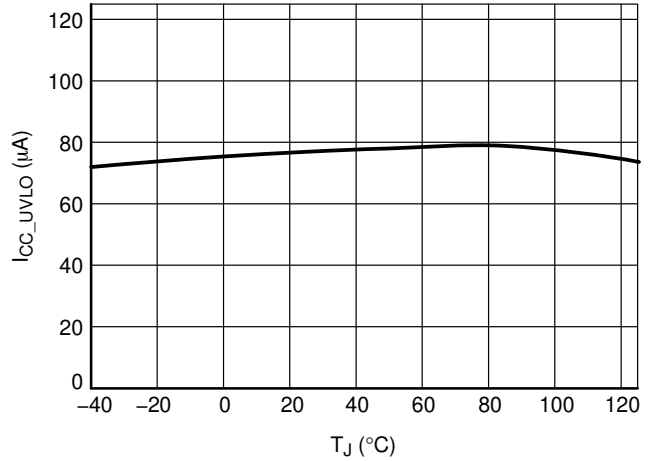


Figure 10. Current Consumption,  $V_{CC} = V_{CCOFF} - 0.1 \text{ V}$ ,  $V_{CS} = 0 \text{ V}$ , ver. D

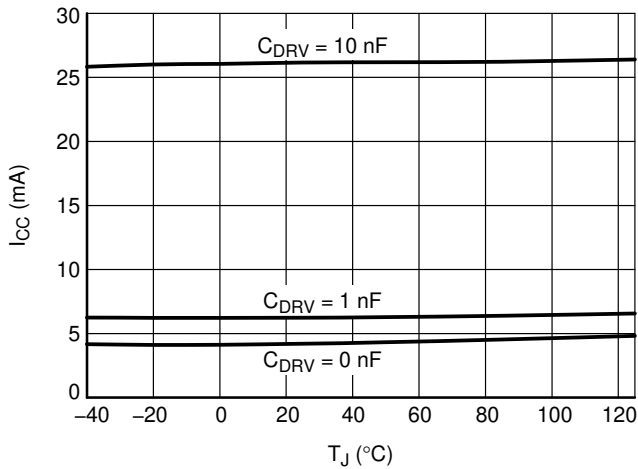


Figure 11. Current Consumption,  $V_{CC} = 12 \text{ V}$ ,  $V_{CS} = -1 \text{ to } 4 \text{ V}$ ,  $f_{CS} = 500 \text{ kHz}$ , ver. A

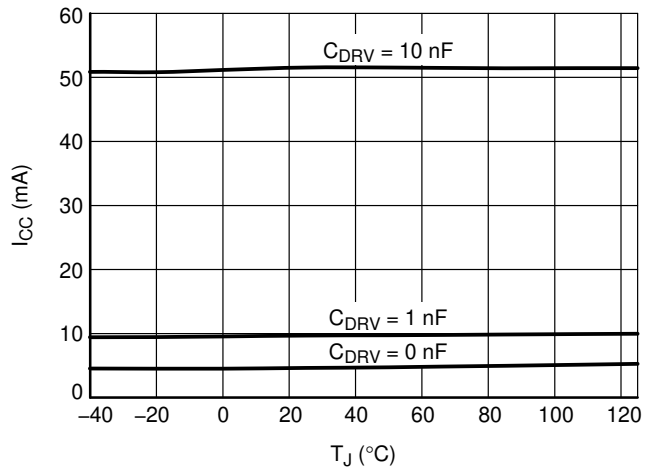


Figure 12. Current Consumption,  $V_{CC} = 12 \text{ V}$ ,  $V_{CS} = -1 \text{ to } 4 \text{ V}$ ,  $f_{CS} = 500 \text{ kHz}$ , ver. D

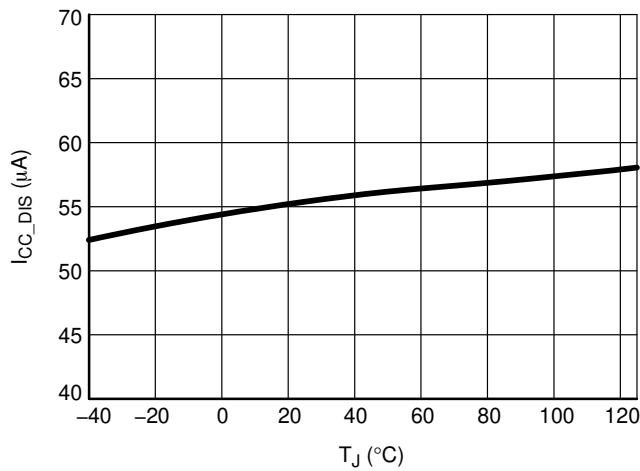


Figure 13. Current Consumption in Disable,  $V_{CC} = 12 \text{ V}$ ,  $V_{CS} = 0 \text{ V}$ ,  $V_{LLD} = V_{CC} - 0.1 \text{ V}$

TYPICAL CHARACTERISTICS

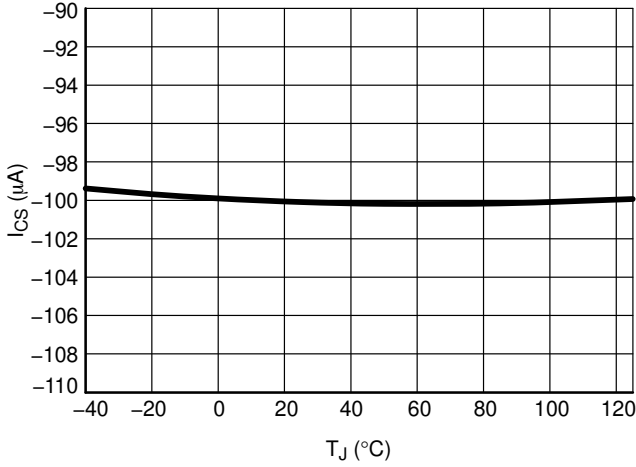


Figure 14. CS Current,  $V_{CS} = -20\text{ mV}$

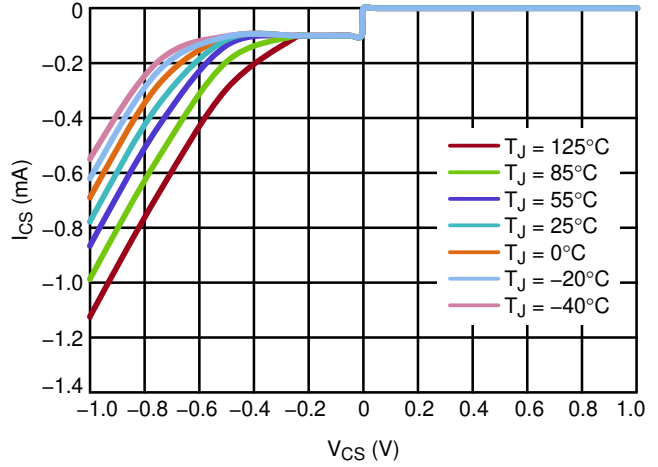


Figure 15. CS Current,  $V_{CC} = 12\text{ V}$

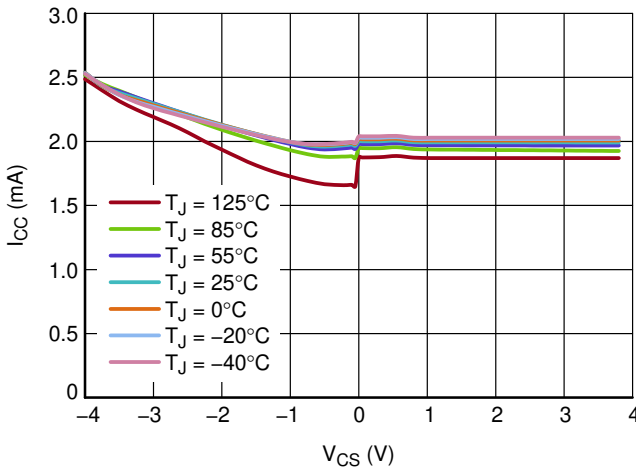


Figure 16. Supply Current vs. CS Voltage,  $V_{CC} = 12\text{ V}$

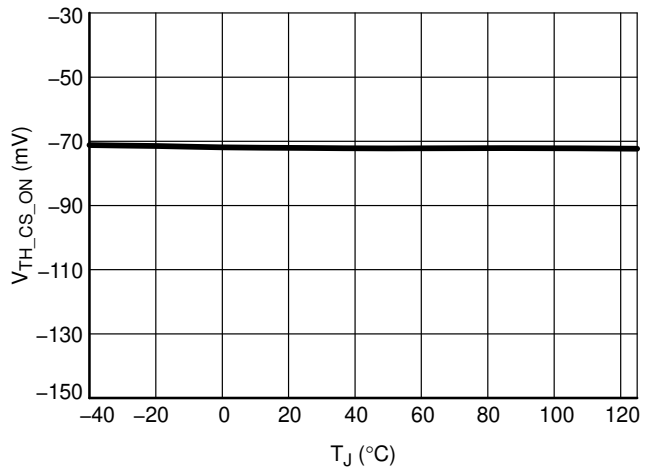


Figure 17. CS Turn-on Threshold

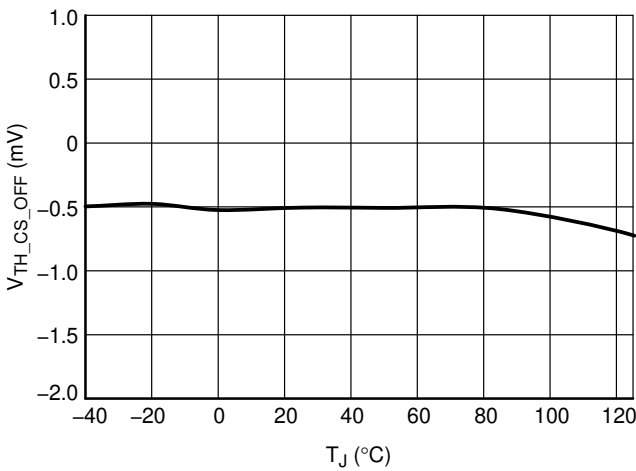


Figure 18. CS Turn-off Threshold

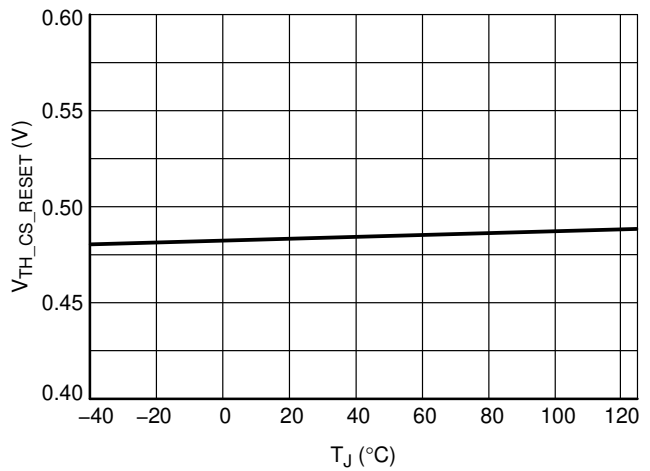


Figure 19. CS Reset Threshold

TYPICAL CHARACTERISTICS

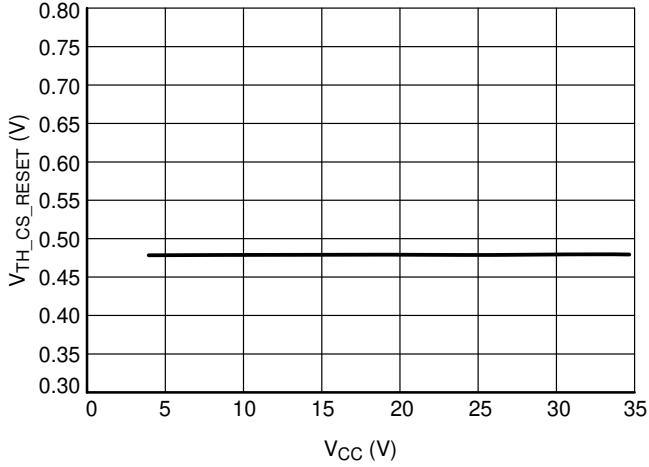


Figure 20. CS Reset Threshold

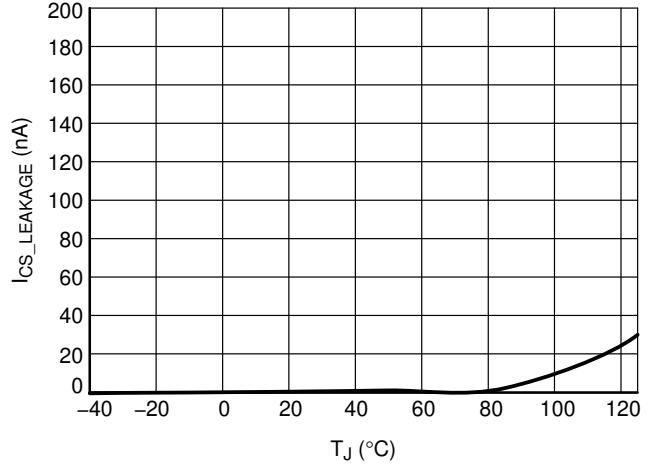


Figure 21. CS Leakage, V<sub>CS</sub> = 150 V

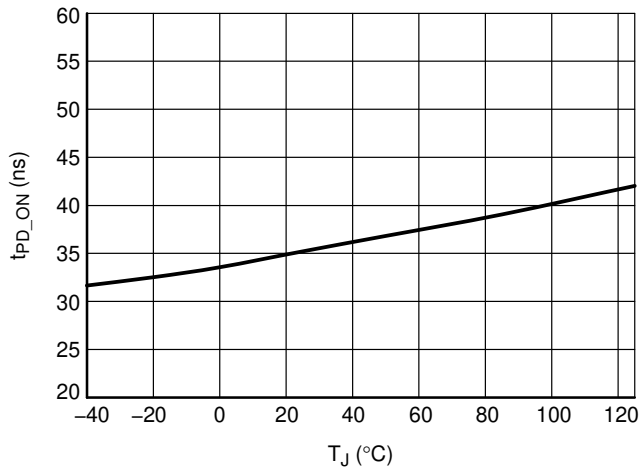


Figure 22. Propagation Delay from CS to DRV Output On

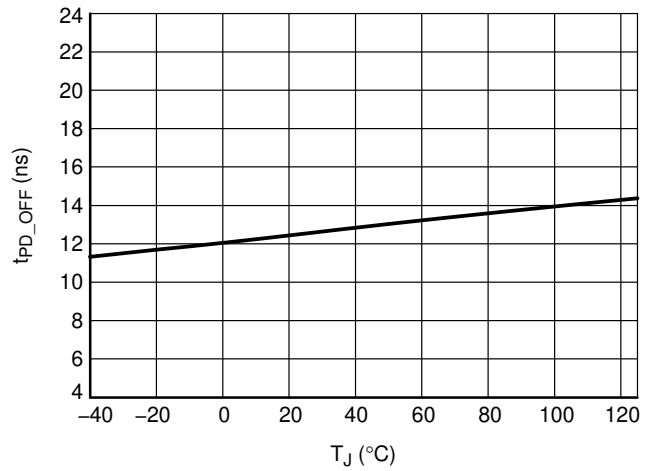


Figure 23. Propagation Delay from CS to DRV Output Off

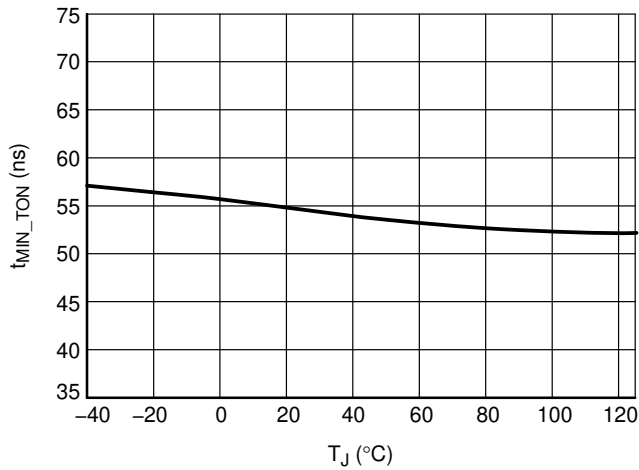


Figure 24. Minimum On-time R<sub>MIN\_TON</sub> = 0 Ω

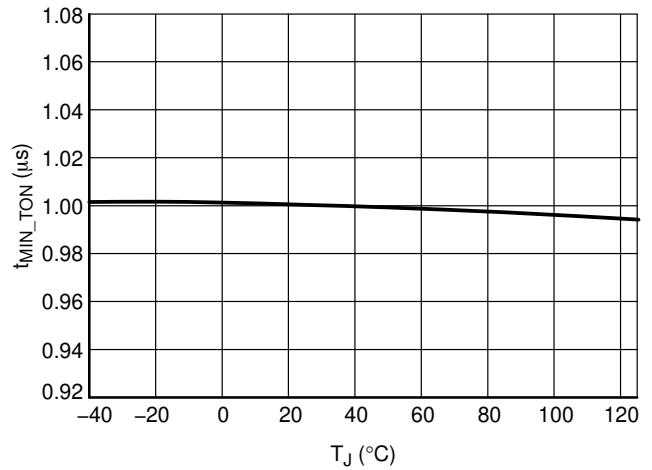


Figure 25. Minimum On-time R<sub>MIN\_TON</sub> = 10 kΩ

TYPICAL CHARACTERISTICS

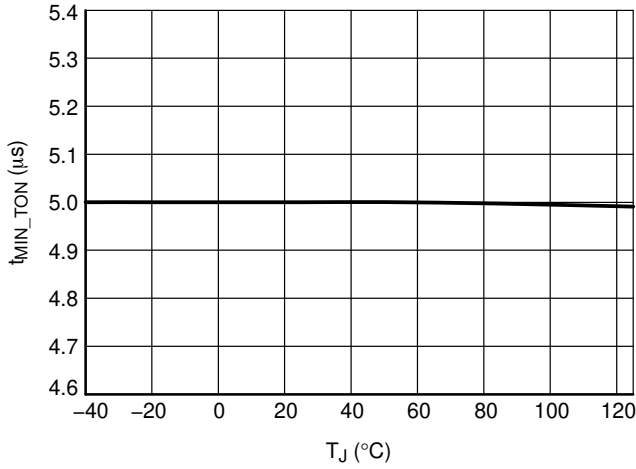


Figure 26. Minimum On-time R<sub>MIN\_TON</sub> = 50 kΩ

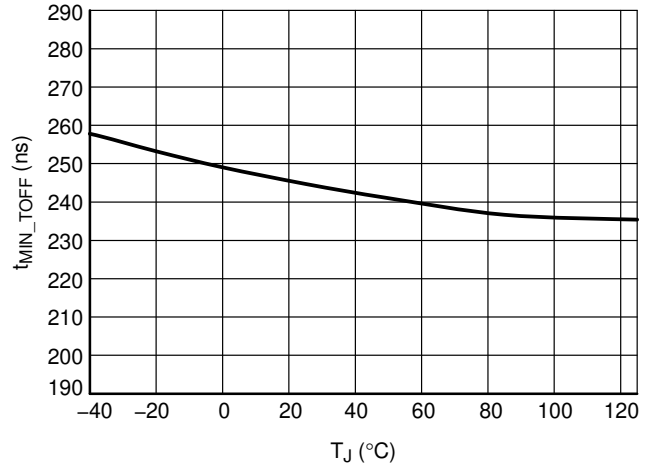


Figure 27. Minimum Off-time R<sub>MIN\_TOFF</sub> = 0 Ω

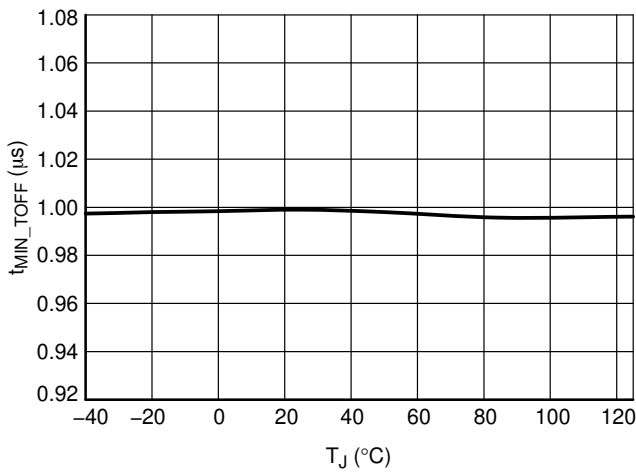


Figure 28. Minimum Off-time R<sub>MIN\_TOFF</sub> = 10 kΩ

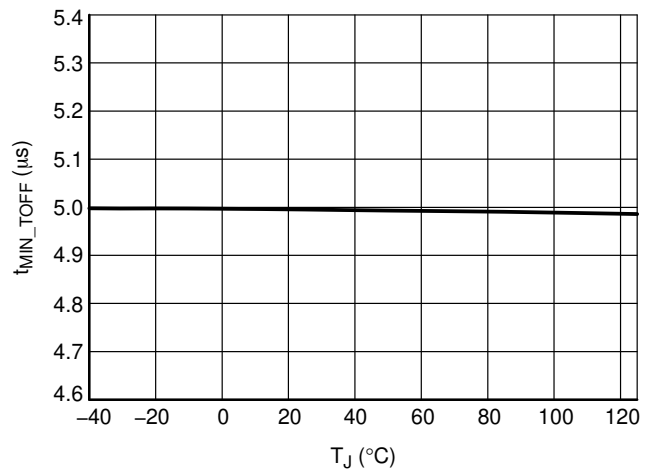


Figure 29. Minimum Off-time R<sub>MIN\_TOFF</sub> = 50 kΩ

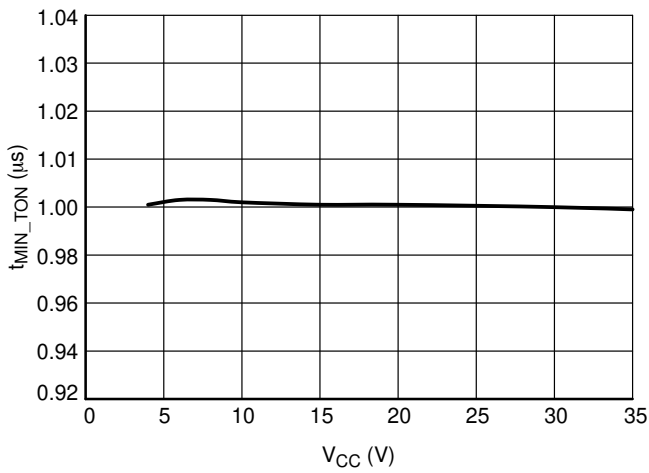


Figure 30. Minimum On-time R<sub>MIN\_TON</sub> = 10 kΩ

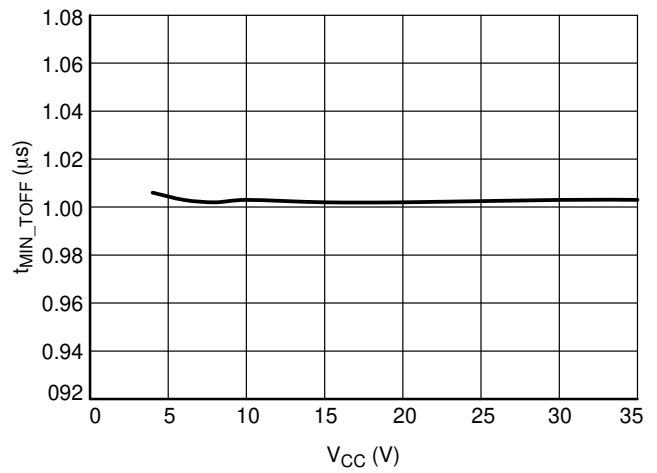


Figure 31. Minimum Off-time R<sub>MIN\_TOFF</sub> = 10 kΩ

TYPICAL CHARACTERISTICS

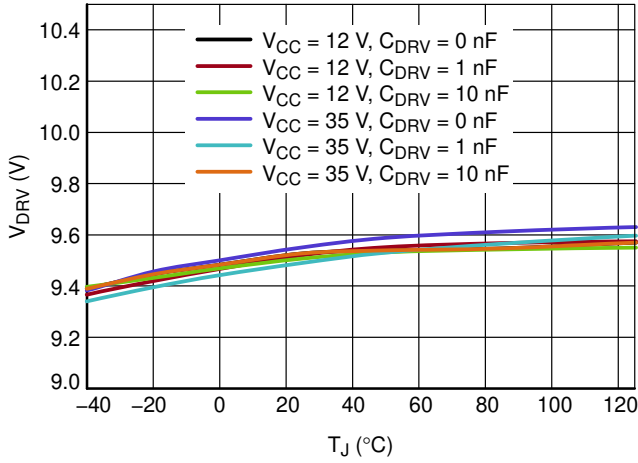


Figure 32. Driver and Output Voltage, ver. B, D and Q

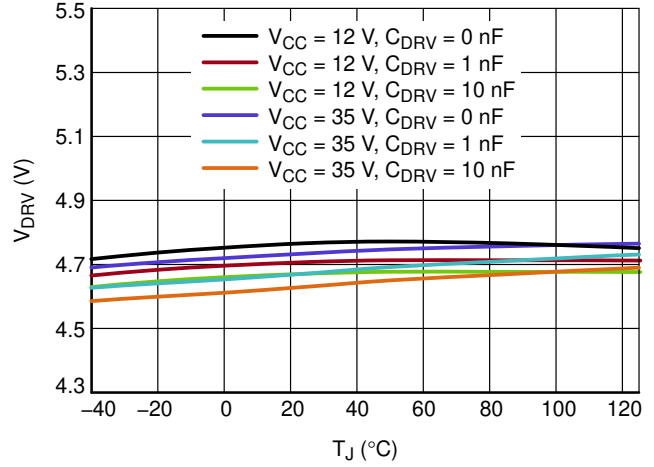


Figure 33. Driver Output Voltage, ver. A and C

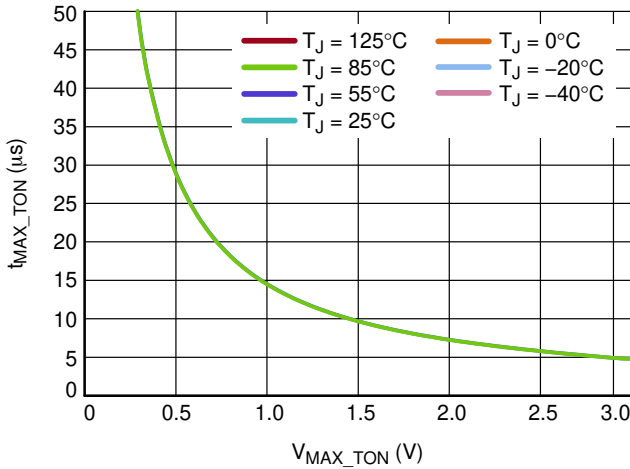


Figure 34. Maximum On-time, ver. Q

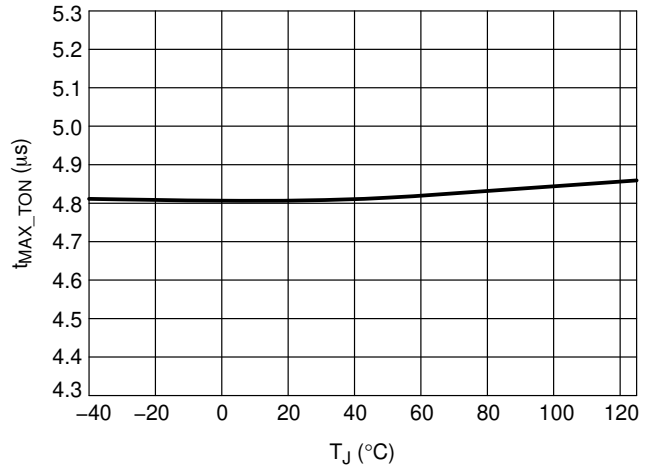


Figure 35. Maximum On-time,  $V_{MAX\_TON} = 3\text{ V}$ , ver. Q

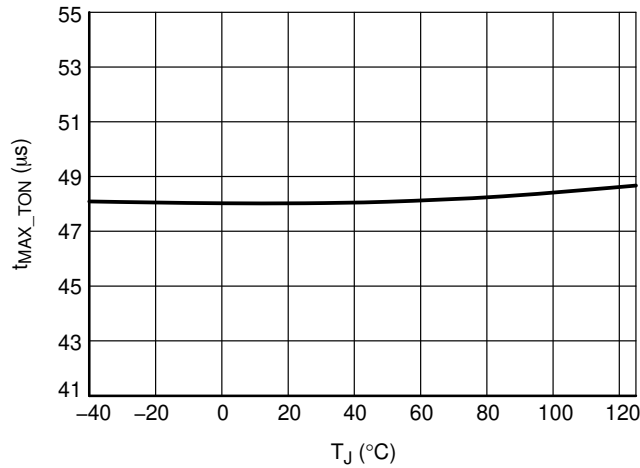


Figure 36. Maximum On-time,  $V_{MAX\_TON} = 0.3\text{ V}$ , ver. Q

## APPLICATION INFORMATION

### General description

The NCP43080 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high-speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP43080 has enough versatility to keep the synchronous rectification system efficient under any operating mode.

The NCP43080 works from an available voltage with range from 4 V (A, D & Q options) or 8 V (B & C options) to 35 V (typical). The wide  $V_{CC}$  range allows direct connection to the SMPS output voltage of most adapters such as notebooks, cell phone chargers and LCD TV adapters.

Precise turn-off threshold of the current sense comparator together with an accurate offset current source allows the user to adjust for any required turn-off current threshold of the SR MOSFET switch using a single resistor. Compared to other SR controllers that provide turn-off thresholds in the range of  $-10$  mV to  $-5$  mV, the NCP43080 offers a turn-off threshold of 0 mV. When using a low  $R_{DS(on)}$  SR (1 m $\Omega$ ) MOSFET our competition, with a  $-10$  mV turn off, will turn off with 10 A still flowing through the SR FET, while our 0 mV turn off turns off the FET at 0 A; significantly reducing the turn-off current threshold and improving efficiency. Many of the competitor parts maintain a drain source voltage across the MOSFET causing the SR MOSFET to operate in the linear region to reduce turn-off time. Thanks to the 8 A sink current of the NCP43080 significantly reduces turn off time allowing for a minimal drain source voltage to be utilized and efficiency maximized.

To overcome false triggering issues after turn-on and turn-off events, the NCP43080 provides adjustable minimum on-time and off-time blanking periods. Blanking times can be adjusted independently of IC  $V_{CC}$  using external resistors connected to GND. If needed, blanking periods can be modulated using additional components.

An extremely fast turn-off comparator, implemented on the current sense pin, allows for NCP43080 implementation in CCM applications without any additional components or external triggering.

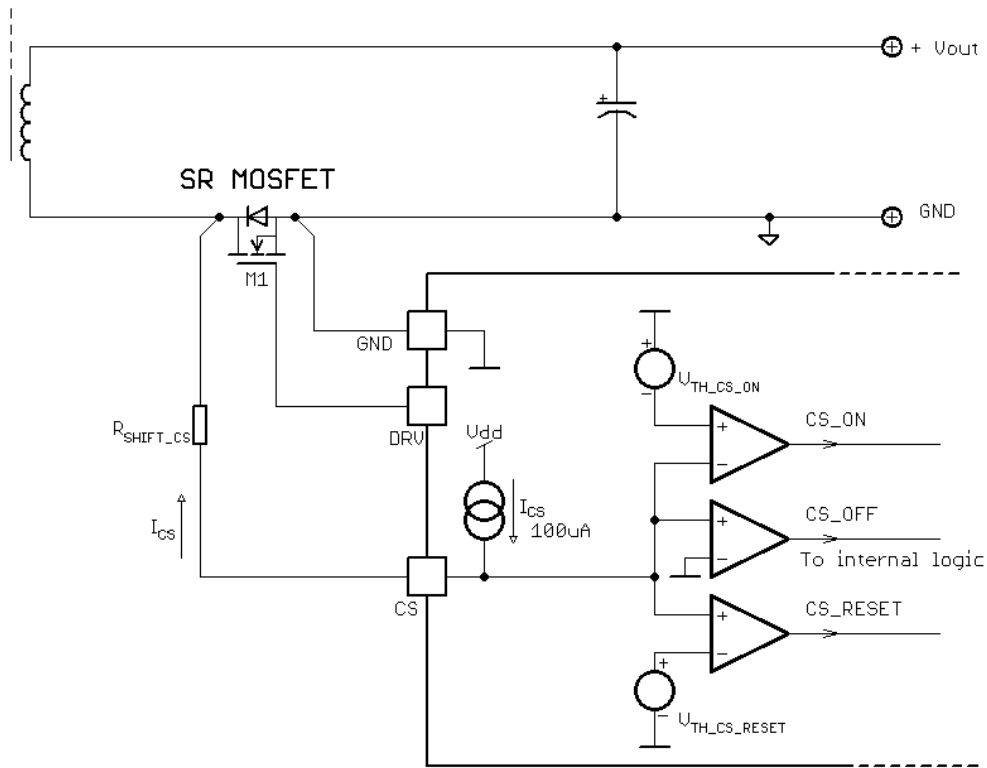
An output driver features capability to keep SR transistor closed even when there is no supply voltage for NCP43080. SR transistor drain voltage goes up and down during SMPS operation and this is transferred through drain gate capacitance to gate and may turn on transistor. NCP43080 uses this pulsing voltage at SR transistor gate (DRV pin) and uses it internally to provide enough supply to activate internal driver sink transistor. DRV voltage is pulled low (not to zero) thanks to this feature and eliminate the risk of turned on SR transistor before enough  $V_{CC}$  is applied to NCP43080.

Some IC versions include a MAX\_TON circuit that helps a quasi resonant (QR) controller to work in CCM mode when a heavy load is present like in the example of a printer's motor starting up.

Finally, the NCP43080 features a special pin (LLD) that can be used to reduce gate driver voltage clamp according to application load conditions. This feature helps to reduce issues with transition from disabled driver to full driver output voltage and back. Disable state can be also activated through this pin to decrease power consumption in no load conditions. If the LLD feature is not wanted then the LLD pin can be tied to GND.

### Current Sense Input

Figure 37 shows the internal connection of the CS circuitry on the current sense input. When the voltage on the secondary winding of the SMPS reverses, the body diode of M1 starts to conduct current and the voltage of M1's drain drops approximately to  $-1$  V. The CS pin sources current of 100  $\mu$ A that creates a voltage drop on the  $R_{SHIFT\_CS}$  resistor (resistor is optional, we recommend shorting this resistor). Once the voltage on the CS pin is lower than  $V_{TH\_CS\_ON}$  threshold, M1 is turned-on. Because of parasitic impedances, significant ringing can occur in the application. To overcome false sudden turn-off due to mentioned ringing, the minimum conduction time of the SR MOSFET is activated. Minimum conduction time can be adjusted using the  $R_{MIN\_TON}$  resistor.



**Figure 37. Current Sensing Circuitry Functionality**

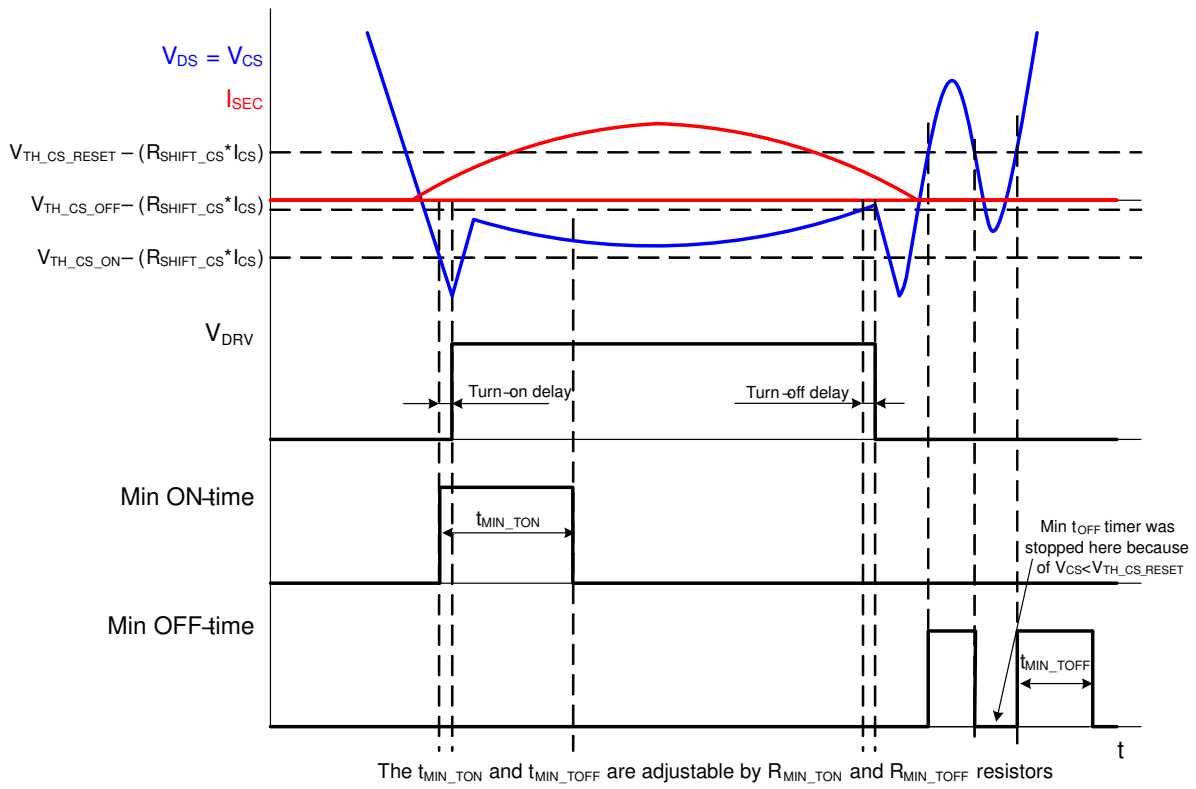
The SR MOSFET is turned-off as soon as the voltage on the CS pin is higher than  $V_{TH\_CS\_OFF}$  (typically  $-0.5\text{ mV}$  minus any voltage dropped on the optional  $R_{SHIFT\_CS}$ ). For the same ringing reason, a minimum off-time timer is asserted once the  $V_{CS}$  goes above  $V_{TH\_CS\_RESET}$ . The minimum off-time can be externally adjusted using  $R_{MIN\_TOFF}$  resistor. The minimum off-time generator can be re-triggered by  $MIN\_TOFF$  reset comparator if some spurious ringing occurs on the CS input after SR MOSFET turn-off event. This feature significantly simplifies SR system implementation in flyback converters.

In an LLC converter the SR MOSFET M1 channel conducts while secondary side current is decreasing (refer to

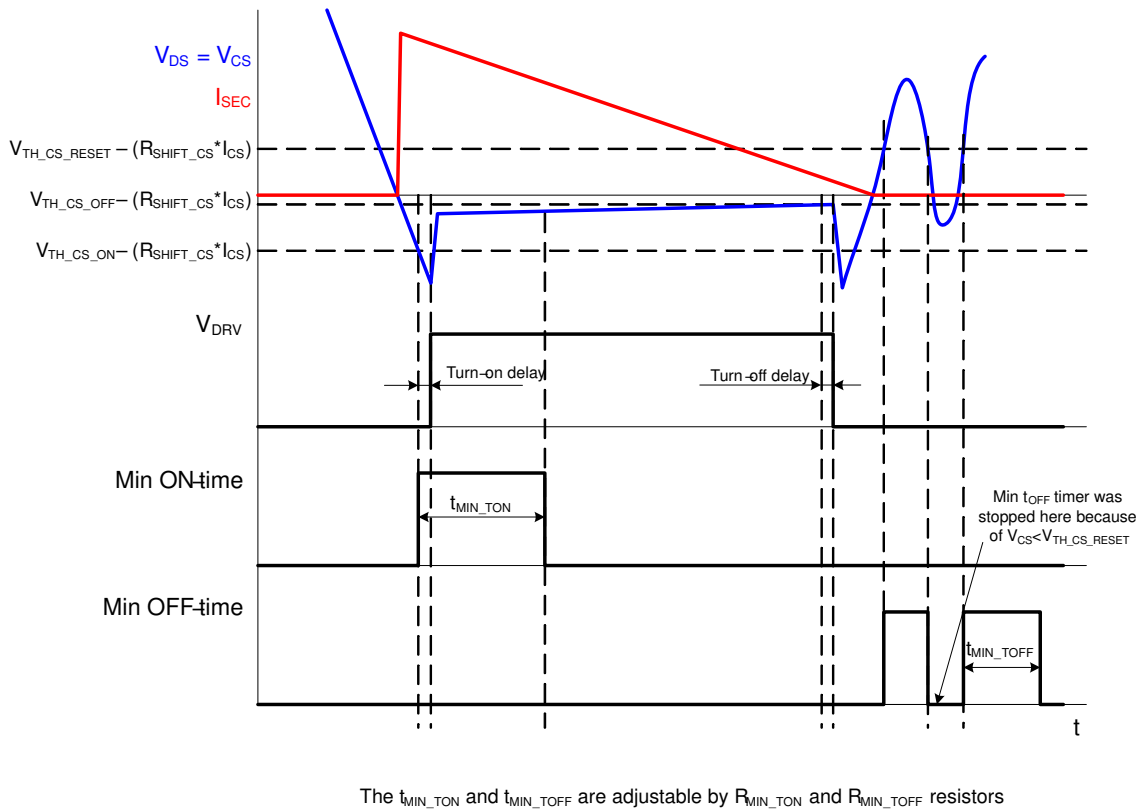
Figure 38). Therefore the turn-off current depends on MOSFET  $R_{DSON}$ . The  $-0.5\text{ mV}$  threshold provides an optimum switching period usage while keeping enough time margin for the gate turn-off. The  $R_{SHIFT\_CS}$  resistor provides the designer with the possibility to modify (increase) the actual turn-on and turn-off secondary current thresholds. To ensure proper switching, the  $min\_toff$  timer is reset, when the  $V_{DS}$  of the MOSFET rings and falls down past the  $V_{TH\_CS\_RESET}$ . The minimum off-time needs to expire before another drive pulse can be initiated. Minimum off-time timer is started again when  $V_{DS}$  rises above  $V_{TH\_CS\_RESET}$ .



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**Figure 38. CS Input Comparators Thresholds and Blanking Periods Timing in LLC**



**Figure 39. CS Input Comparators Thresholds and Blanking Periods Timing in Flyback**

## NCP43080

If no  $R_{SHIFT\_CS}$  resistor is used, the turn-on, turn-off and  $V_{TH\_CS\_RESET}$  thresholds are fully given by the CS input specification (please refer to electrical characteristics table). The CS pin offset current causes a voltage drop that is equal to:

$$V_{RSHIFT\_CS} = R_{SHIFT\_CS} * I_{CS} \quad (\text{eq. 1})$$

Final turn-on and turn off thresholds can be then calculated as:

$$V_{CS\_TURN\_ON} = V_{TH\_CS\_ON} - (R_{SHIFT\_CS} * I_{CS}) \quad (\text{eq. 2})$$

$$V_{CS\_TURN\_OFF} = V_{TH\_CS\_OFF} - (R_{SHIFT\_CS} * I_{CS}) \quad (\text{eq. 3})$$

$$V_{CS\_RESET} = V_{TH\_CS\_RESET} - (R_{SHIFT\_CS} * I_{CS}) \quad (\text{eq. 4})$$

Note that  $R_{SHIFT\_CS}$  impact on turn-on and  $V_{TH\_CS\_RESET}$  thresholds is less critical than its effect on the turn-off threshold.

It should be noted that when using a SR MOSFET in a through hole package the parasitic inductance of the MOSFET package leads (refer to Figure 40) causes a turn-off current threshold increase. The current that flows through the SR MOSFET experiences a high  $\Delta i(t)/\Delta t$  that induces an error voltage on the SR MOSFET leads due to their parasitic inductance. This error voltage is proportional to the derivative of the SR MOSFET current; and shifts the CS input voltage to zero when significant current still flows through the MOSFET channel. As a result, the SR MOSFET is turned-off prematurely and the efficiency of the SMPS is not optimized – refer to Figure 41 for a better understanding.

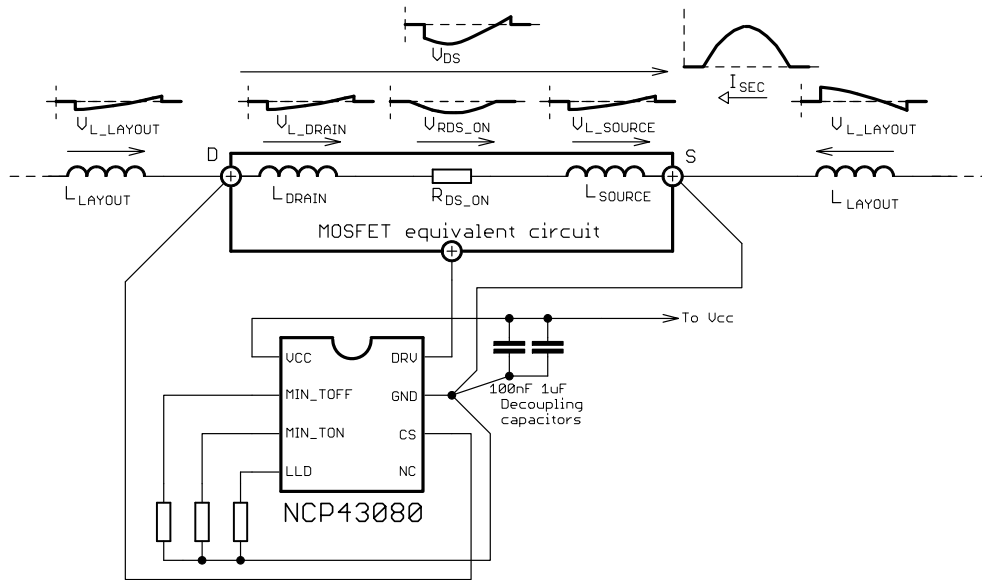
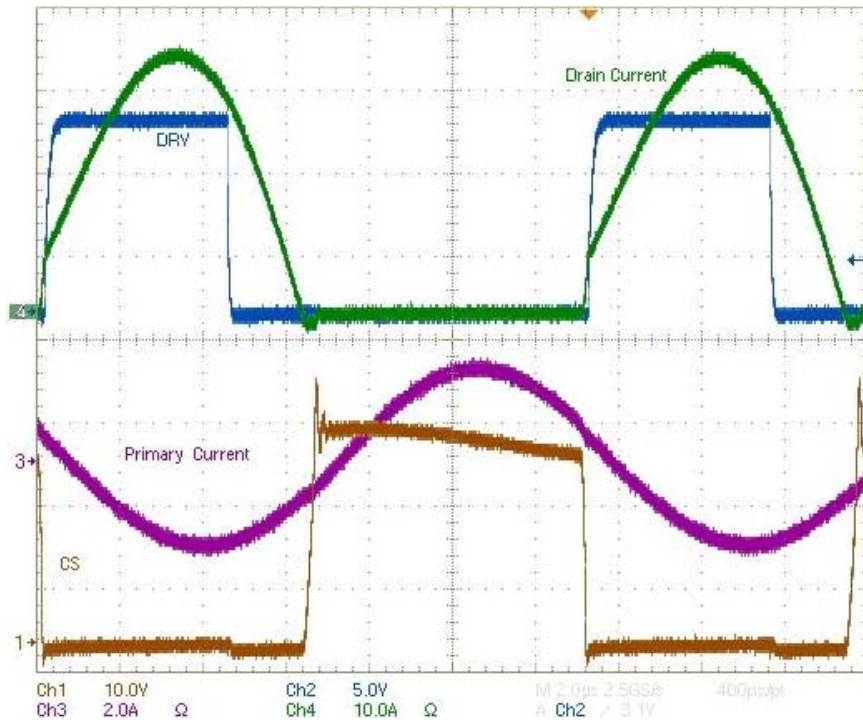


Figure 40. SR System Connection Including MOSFET and Layout Parasitic Inductances in LLC Application

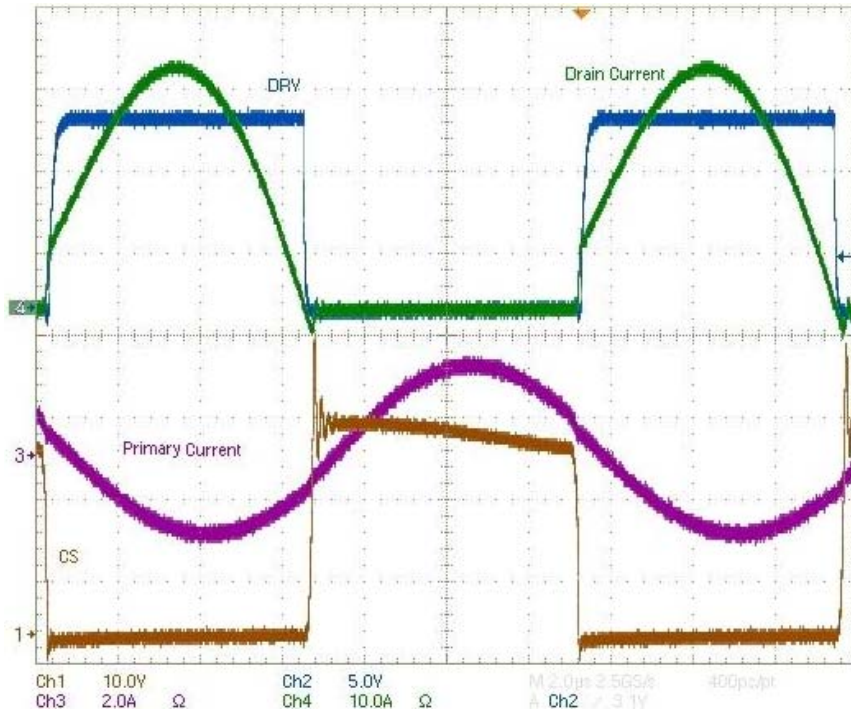


**Figure 41. Waveforms From SR System Implemented in LLC Application and Using MOSFET in TO220 Package With Long Leads – SR MOSFET channel Conduction Time is Reduced**

Note that the efficiency impact caused by the error voltage due to the parasitic inductance increases with lower MOSFETs  $R_{DS(on)}$  and/or higher operating frequency.

It is thus beneficial to minimize SR MOSFET package leads length in order to maximize application efficiency. The optimum solution for applications with high secondary

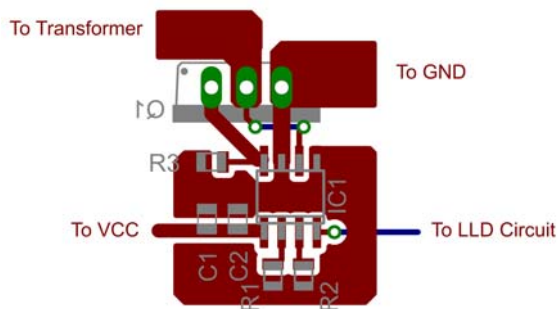
current  $\Delta i/\Delta t$  and high operating frequency is to use lead-less SR MOSFET i.e. SR MOSFET in SMT package. The parasitic inductance of a SMT package is negligible causing insignificant CS turn-off threshold shift and thus minimum impact to efficiency (refer to Figure 42).



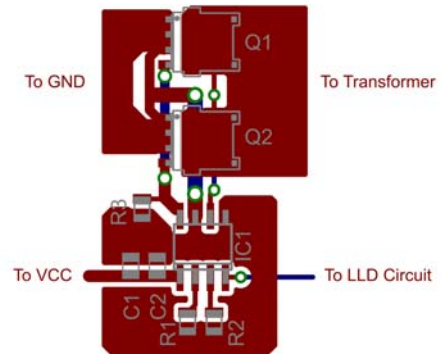
**Figure 42. Waveforms from SR System Implemented in LLC Application and Using MOSFET in SMT Package with Minimized Parasitic Inductance – SR MOSFET Channel Conduction Time is Optimized**

It can be deduced from the above paragraphs on the induced error voltage and parameter tables that turn-off threshold precision is quite critical. If we consider a SR MOSFET with  $R_{DS(on)}$  of 1 mΩ, the 1 mV error voltage on the CS pin results in a 1 A turn-off current threshold difference; thus the PCB layout is very critical when implementing the SR system. Note that the CS turn-off comparator is referred to the GND pin. Any parasitic impedance (resistive or inductive – even on the magnitude of mΩ and nH values) can cause a high error voltage that is then evaluated by the CS comparator. Ideally the CS turn-off comparator should detect voltage that is caused by secondary current directly on the SR MOSFET channel resistance. In reality there will be small parasitic impedance on the CS path due to the bonding wires, leads and soldering. To assure the best efficiency results, a Kelvin connection of

the SR controller to the power circuitry should be implemented. The GND pin should be connected to the SR MOSFET source soldering point and current sense pin should be connected to the SR MOSFET drain soldering point – refer to Figure 40. Using a Kelvin connection will avoid any impact of PCB layout parasitic elements on the SR controller functionality; SR MOSFET parasitic elements will still play a role in attaining an error voltage. Figure 44 and Figure 43 show examples of SR system layouts using MOSFETs in TO220 and SMT packages. It is evident that the MOSFET leads should be as short as possible to minimize parasitic inductances when using packages with leads (like TO220). Figure 43 shows how to layout design with two SR MOSFETs in parallel. It has to be noted that it is not easy task and designer has to paid lot of attention to do symmetric Kelvin connection.



**Figure 44. Recommended Layout When Using SR MOSFET in TO220 Package**



**Figure 43. Recommended Layout When Using SR MOSFET in SMT Package (2x SO8 FL)**

# NCP43080

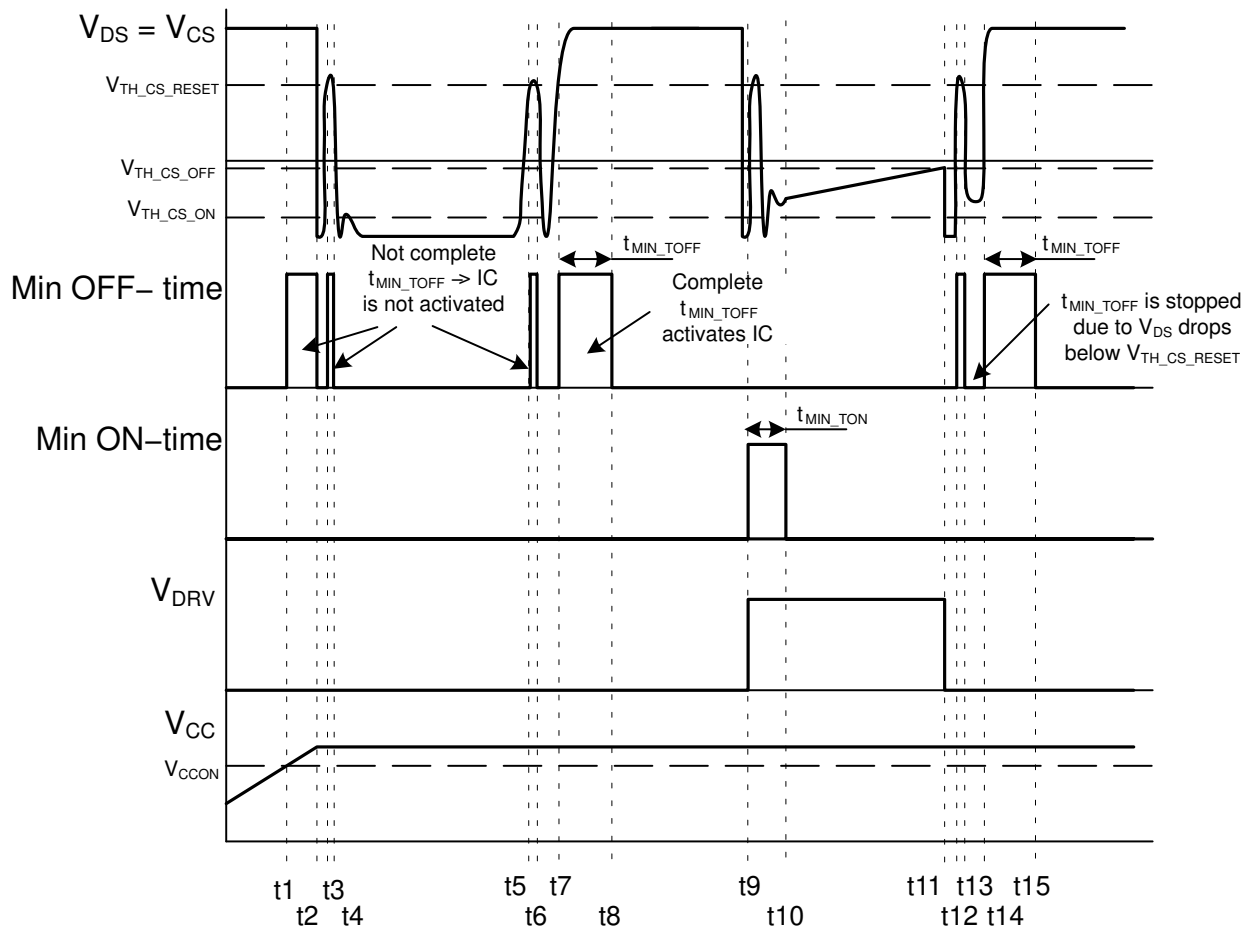


Figure 45. NCP43080 Operation after Start-Up Event

### Self Synchronization

Self synchronization feature during start-up can be seen at Figure 45. Figure 45 shows how the minimum off-time timer is reset when CS voltage is oscillating through  $V_{TH\_CS\_RESET}$  level. The NCP43080 starts operation at time  $t_1$  (time  $t_1$  can be seen as a wake-up event from the disable mode through LLD pin). Internal logic waits for one complete minimum off-time period to expire before the NCP43080 can activate the driver after a start-up or wake-up event. The minimum off-time timer starts to run at time  $t_1$ , because  $V_{CS}$  is higher than  $V_{TH\_CS\_RESET}$ . The timer is then reset, before its set minimum off-time period expires, at time  $t_2$  thanks to CS voltage lower than  $V_{TH\_CS\_RESET}$  threshold. The aforementioned reset situation can be seen again at time  $t_3$ ,  $t_4$ ,  $t_5$  and  $t_6$ . A

complete minimum off-time period elapses between times  $t_7$  and  $t_8$  allowing the IC to activate a driver output after time  $t_8$ .

### Minimum $t_{ON}$ and $t_{OFF}$ Adjustment

The NCP43080 offers an adjustable minimum on-time and off-time blanking periods that ease the implementation of a synchronous rectification system in any SMPS topology. These timers avoid false triggering on the CS input after the MOSFET is turned on or off.

The adjustment of minimum  $t_{ON}$  and  $t_{OFF}$  periods are done based on an internal timing capacitance and external resistors connected to the GND pin – refer to Figure 46 for a better understanding.

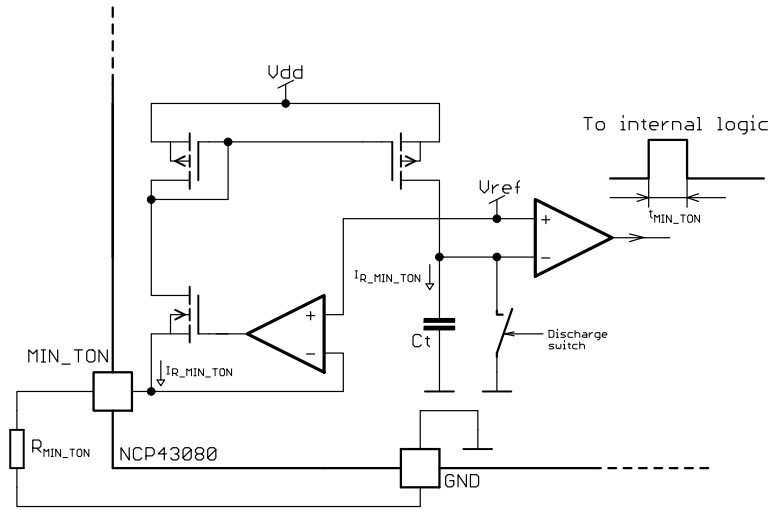


Figure 46. Internal Connection of the MIN\_TON Generator (the MIN\_TOFF Works in the Same Way)

Current through the MIN\_TON adjust resistor can be calculated as:

$$I_{R\_MIN\_TON} = \frac{V_{ref}}{R_{Ton\_min}} \quad (\text{eq. 5})$$

If the internal current mirror creates the same current through  $R_{MIN\_TON}$  as used the internal timing capacitor ( $C_t$ ) charging, then the minimum on-time duration can be calculated using this equation.

$$t_{MIN\_TON} = C_t \frac{V_{ref}}{I_{R\_MIN\_TON}} = C_t \frac{V_{ref}}{\frac{V_{ref}}{R_{MIN\_TON}}} = C_t \cdot R_{MIN\_TON} \quad (\text{eq. 6})$$

The internal capacitor size would be too large if  $I_{R\_MIN\_TON}$  was used. The internal current mirror uses a proportional current, given by the internal current mirror ratio. One can then calculate the MIN\_TON and MIN\_TOFF blanking periods using below equations:

$$t_{MIN\_TON} = 1.00 \cdot 10^{-4} \cdot R_{MIN\_TON} [\mu\text{s}] \quad (\text{eq. 7})$$

$$t_{MIN\_TOFF} = 1.00 \cdot 10^{-4} \cdot R_{MIN\_TOFF} [\mu\text{s}] \quad (\text{eq. 8})$$

Note that the internal timing comparator delay affects the accuracy of Equations 7 and 8 when MIN\_TON/MIN\_TOFF times are selected near to their minimum possible values. Please refer to Figures 47 and 48 for measured minimum on and off time charts.

# NCP43080

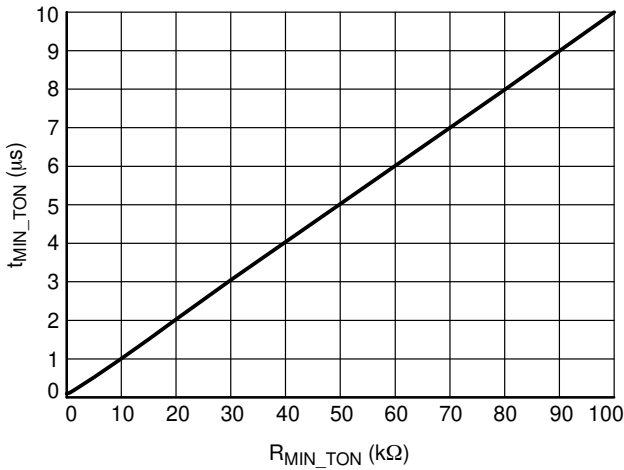


Figure 47. MIN\_TON Adjust Characteristics

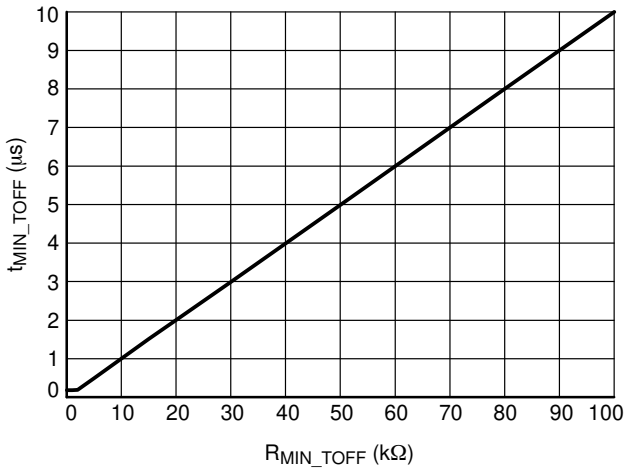


Figure 48. MIN\_TOFF Adjust Characteristics

The absolute minimum  $t_{ON}$  duration is internally clamped to 55 ns and minimum  $t_{OFF}$  duration to 245 ns in order to prevent any potential issues with the MIN\_TON and/or MIN\_TOFF pins being shorted to GND.

The NCP43080 features dedicated anti-ringing protection system that is implemented with a MIN\_TOFF blank generator. The minimum off-time one-shot generator is restarted in the case when the CS pin voltage crosses  $V_{TH\_CS\_RESET}$  threshold and MIN\_TOFF period is active. The total off-time blanking period is prolonged due to the ringing in the application (refer to Figure 38).

Some applications may require adaptive minimum on and off time blanking periods. With NCP43080 it is possible to modulate blanking periods by using an external NPN transistor – refer to Figure 49. The modulation signal can be derived based on the load current, feedback regulator voltage or other application parameter.

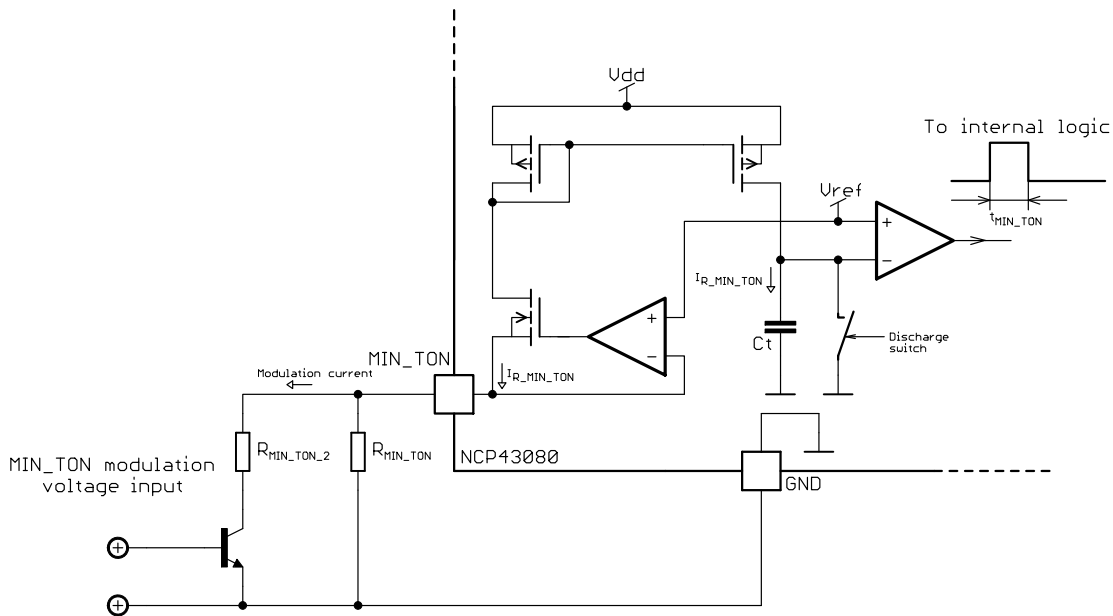


Figure 49. Possible Connection for MIN\_TON and MIN\_TOFF Modulation

## Maximum $t_{ON}$ adjustment

The NCP43080Q offers an adjustable maximum on-time (like the  $min\_t_{ON}$  and  $min\_t_{OFF}$  settings shown above) that can be very useful for QR controllers at high loads. Under high load conditions the QR controller can operate in CCM thanks to this feature. The NCP43080Q version has the ability to turn-off the DRV signal to the SR MOSFET before the secondary side current reaches zero. The DRV signal from the NCP43080Q can be fed to the primary side through a pulse transformer (see Figure 4 for detail) to a transistor on the primary side to emulate a ZCD event before an actual ZCD event occurs. This feature helps to keep the minimum switching frequency up so that there is better energy transfer through the transformer (a smaller transformer core can be used). Also another advantage is that the IC controls the SR MOSFET and turns off from secondary side before the primary side is turned on in CCM to ensure no cross conduction. By controlling the SR MOSFET's turn off before the primary side turn off, producing a zero cross conduction operation, this will improve efficiency.

The Internal connection of the MAX\_TON feature is shown in Figure 50. Figure 50 shows a method that allows for a modification of the maximum on-time according to output voltage. At a lower  $V_{OUT}$ , caused by hard overload or at startup, the maximum on-time should be longer than at nominal voltage. Resistor  $R_A$  can be used to modulate maximum on-time according to  $V_{OUT}$  or any other parameter.

The operational waveforms at heavy load in QR type SMPS are shown in Figure 51. After  $t_{MAX\_TON}$  time is exceeded, the synchronous switch is turned off and the secondary current is conducted by the diode. Information about turned off SR MOSFET is transferred by the DRV pin through a small pulse transformer to the primary side where it acts on the ZCD detection circuit to allow the primary switch to be turned on. Secondary side current disappears before the primary switch is turned on without a possibility of cross current condition.

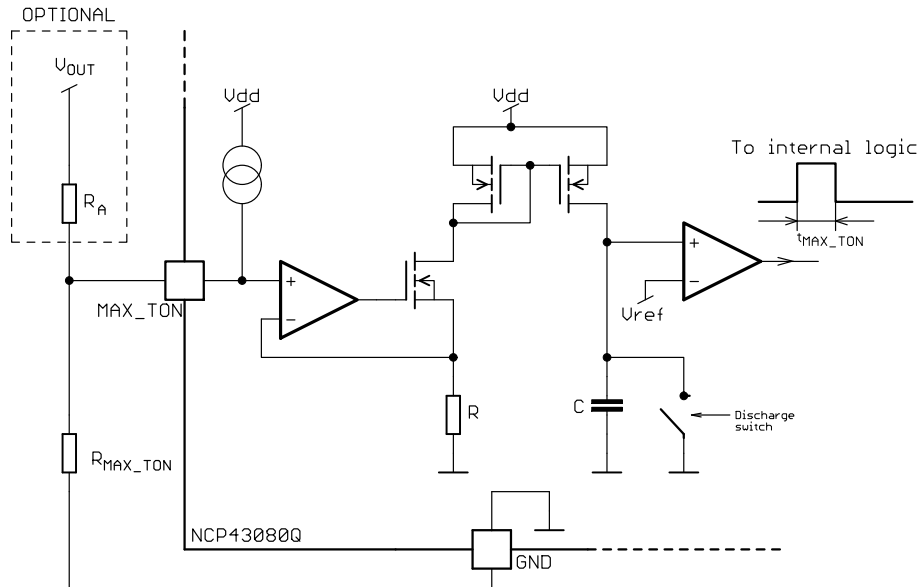


Figure 50. Internal Connection of the MAX\_TON Generator, NCP43080Q



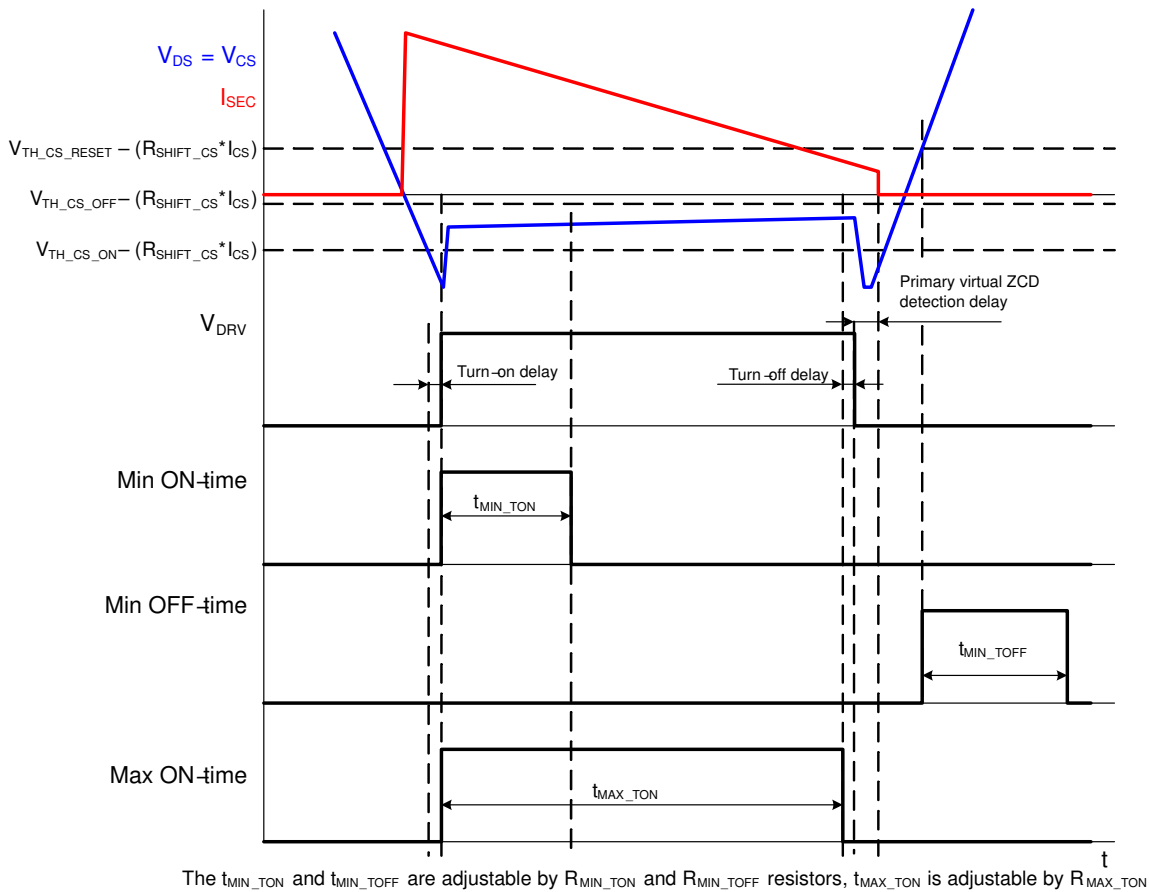


Figure 51. Function of MAX\_TON Generator in Heavy Load Condition

**Adaptive Gate Driver Clamp and automatic Light Load Turn-off**

As synchronous rectification system significantly improves efficiency in most of SMPS applications during medium or full load conditions. However, as the load reduces into light or no-load conditions the SR MOSFET driving losses and SR controller consumption become more critical. The NCP43080 offers two key features that help to optimize application efficiency under light load and no load conditions:

1<sup>st</sup> – The driver clamp voltage is modulated and follows the output load condition. When the output load decreases the driver clamp voltage decreases as well. Under heavy load conditions the SR MOSFET’s gate needs to be driven very hard to optimize the performance and reduce conduction losses. During light load conditions it is not as critical to drive the SR MOSFET’s channel into such a low  $R_{DS(on)}$  state. This adaptive gate clamp technique helps to optimize efficiency during light load conditions especially in LLC applications where the SR MOSFETs with high input capacitance are used.

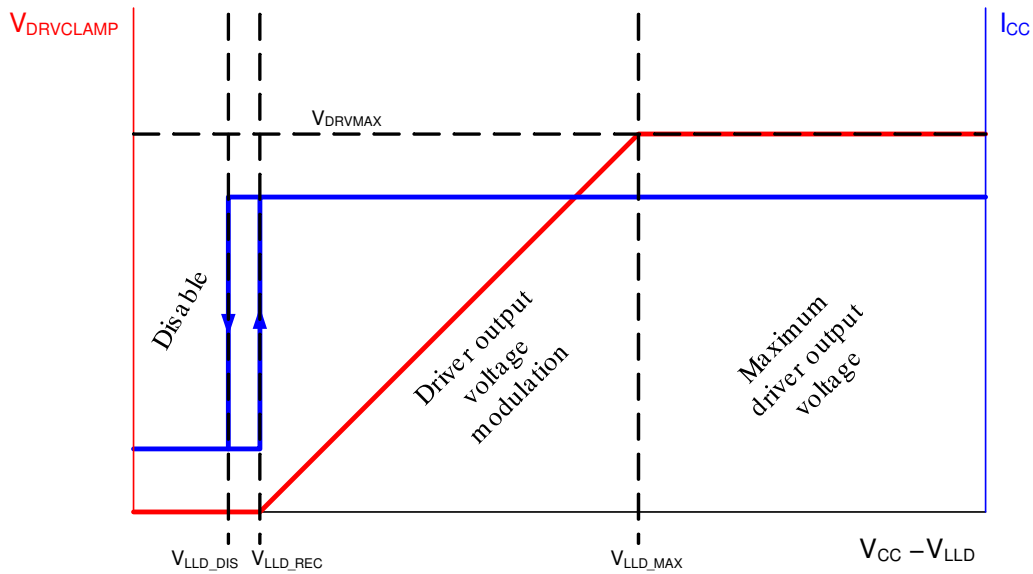
Driver voltage modulation improves the system behavior when SR controller state is changed in and out of normal or disable modes. Soft transient between drop at body diode

and drop at MOSFET’s  $R_{DS(on)}$  only improves stability during load transients.

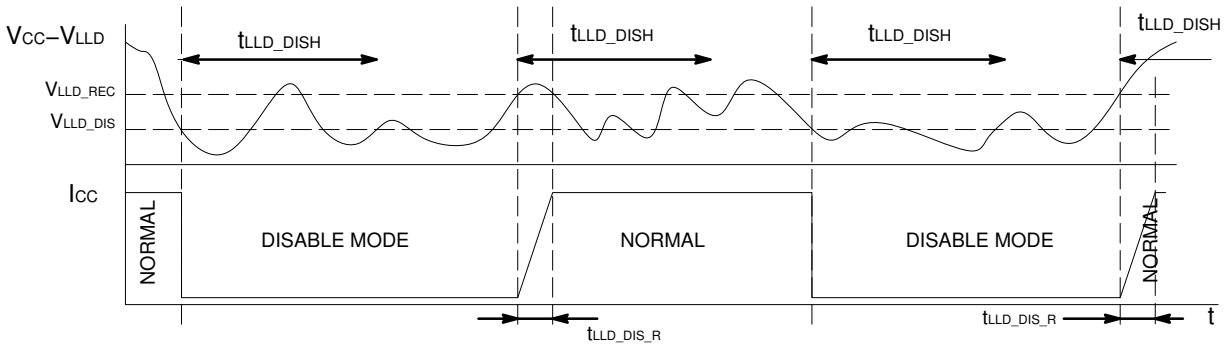
2<sup>nd</sup> – In extremely low load conditions or no load conditions the NCP43080 fully disables driver output and reduces the internal power consumption when output load drops below the level where skip-mode takes place.

Both features are controlled by voltage at LLD pin. The LLD pin voltage characteristic is shown in Figure 52. Driver voltage clamp is a linear function of the voltage difference between the  $V_{CC}$  and LLD pins from  $V_{LLD\_REC}$  point up to  $V_{LLD\_MAX}$ . A disable mode is available, where the IC current consumption is dramatically reduced, when the difference of  $V_{CC} - V_{LLD}$  voltage drops below  $V_{LLD\_DIS}$ . When the voltage difference between the  $V_{CC} - V_{LLD}$  pins increase above  $V_{LLC\_REC}$  the disable mode ends and the IC regains normal operation. It should be noted that there are also some time delays to enter and exit from the disable mode. Time waveforms are shown at Figure 53. There is a time,  $t_{LLD\_DISH}$ , that the logic ignores changes from disable mode to normal or reversely. There is also some time  $t_{LLD\_DIS\_R}$  that is needed after an exit from the disable mode to assure proper internal block biasing before SR controller starts work normally.

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**Figure 52. LLD Voltage to Driver Clamp and Current Consumption Characteristic (DRV Unloaded)**



**Figure 53. LLD Pin Disable Behavior in Time Domain**

The two main SMPS applications that are using synchronous rectification systems today are flyback and LLC topologies. Different light load detection techniques are used in NCP43080 controller to reflect differences in operation of both mentioned applications.

Detail of the light load detection implementation technique used in NCP43080 in flyback topologies is displayed at Figure 54. Using a simple and cost effective peak detector implemented with a diode D1, resistors R1

through R3 and capacitors C2 and C3, the load level can be sensed. Output voltage of this detector on the LLD pin is referenced to controller VCC with an internal differential amplifier in NCP43080. The output of the differential amplifier is then used in two places. First the output is used in the driver block for gate drive clamp voltage adjustment. Next, the output signal is evaluated by a no-load detection comparator that activates IC disable mode in case the load is disconnected from the application output.