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65 W Off-Line Adapter Featuring Very Low No-Load Power Consumption Evaluation Board User's Manual



ON Semiconductor®

http://onsemi.com

EVAL BOARD USER'S MANUAL

Overview

When designing an offline Ac-Dc power adapter, one key consideration is the power consumption in standby mode. Standby power consumption, also sometimes referred to as vampire power or phantom load, is the power consumed by electronic devices when they are switched off, but still plugged into the wall. It is estimated that standby power accounts for nearly 10% of the energy usage in the average American home. One common contributor to vampire power in the home is notebook adapters. These adapters spend a lot of time left underneath desks with the notebook computer disconnected or powered off. The following design note features the latest techniques for minimizing the standby power consumption of a 65 W notebook adapter.

When focusing on the no load power consumption of an adapter design, the key losses need to be identified. Switching losses and circuit biasing must be minimized or eliminated completely. The latest technique for minimizing losses during no load is to turn off the Ac-Dc controller and allow the output voltage to drop. Because the adapter is not supplying power, a drop in output voltage is viewed as acceptable. The following design utilizes the NCP1246 flyback controller and the NCP4354A secondary side controller to realize this technique. Both controllers have built-in features focused on minimizing no load input power consumption. Primary side flyback controller NCP1246 is a fixed frequency current mode controller featuring dynamic self supply. It also supports OFF mode and integrated active X2 capacitor discharge feature, which significantly reduces input power at very light load and no load conditions. NCP1246 includes frequency fold-back and skip mode to provide high efficiency in light load. Secondary side controller NCP4354A provides output voltage and current regulation (CCCV operation of whole SMPS), very light load condition detection, OFF mode control and indication LED driver. The NCP4354A is specially design for use in tandem with the NCP1246, detecting no load conditions and triggering OFF mode via the NCP1246 FB pin.

Key Features

- Constant Voltage Constant Current Regulation (CCCV)
- Very Low Input Power at Light and No Load
- High Efficiency Across the Entire Load Range
- Overpower Protection
- Universal Mains Operation

Circuit Description

The primary side uses a flyback topology, providing the advantage of a cost effective power stage design. The power stage operates in both CCM (continuous conduction mode) and DCM (discontinuous conduction mode), allowing it to accept a wide universal input voltage range. The CCM operation provides desired full load performance with good efficiency and low ripple of primary current. The DCM operation then permits an increase of efficiency under the light load conditions, by decreasing the switching losses. The device switches at 65 kHz which represents a good trade-off between switching losses and magnetic core size.

The adapter primary side consists of several important sections. The first is an input EMI filter to reduce the conducted EMI to the ac line at the input of the adapter. The EMI filter is formed by common-mode inductors L3 and capacitors C1, C2, C3 and C11 with differential mode inductor L2. The varistor R7 is used to protect the adapter against the line overvoltage peaks. When the power supply is disconnected from the AC mains, X capacitors C2, C13 and Y capacitors C3 and C4 are discharged through HV pin via the following path: rectifying diodes D101, D103, surge protection T network R100, R101 and C100. This feature replaces commonly used discharging resistors and saves approximately 25 mW of input power consumption at 230 Vac. The next block is the rectifier with bulk capacitor. The main power stage of the flyback converter utilizes the low R_{DSon} MOSFET SPP11N60C3 along with a custom designed transformer TR1 KA5038-BL from Coilcraft. The detailed design procedure of a flyback adapter can be found in the application note AND8461/D at ON Semiconductor website: http://www.onsemi.com.

Secondary rectification is done by a low forward voltage drop Schottky diode NTST30100SG from ON Semiconductor. A simple RC snubber across the secondary rectifier damps the high frequency ringing caused by the unclamped leakage inductance of the secondary side of the transformer and the rectification diode capacitance. Secondary controller NCP4354A provides the output voltage and output current regulation. Output voltage is set by voltage divider R112, R117, R118 and R127, output current is sensed at sense resistor R111. Regulation output is coupled to the NCP1246 primary side controller via the optocoupler. The NCP4354 secondary controller also detects very light load condition via D105, R114, C106, R115 and R116 by OFFDET pin. When light load condition is detected, the primary controller is switched into OFF mode by ON/OFF current sink to DRIVE pin via optocoupler. The built in LED driver indicates primary side operation (when SMPS is not in OFF mode). The LED driver switches with 1 kHz frequency and 12% duty cycle in order to optimize LED efficiency.

Parameter	Symbol	Value	Units
Input Voltage	V _{IN}	85 – 265	V _{AC}
Input Frequency	f _{IN}	30 - 80	Hz
Output Voltage	V _{OUT}	19	V
Nominal Output Current	IOUTNOM	3.4	А
Output Current Limit	IOUTLIM	3.9	A
Efficiency I _{OUT} > 3% I _{OUTMAX}	η	> 84	%
Efficiency I _{OUT} > 25% I _{OUTMAX}	η	> 90	%
No-Load Power Consumption V_{IN} = 115 V/ 60 Hz	P _{IN}	11	mW
No-Load Power Consumption V_{IN} = 230 V/ 50 Hz	P _{IN}	21	mW
Output Voltage Ripple I _{OUT} = 3.5 A	V _{OUT_PK-PK}	50	mV
Load Regulation I _{OUT} = 50 mA - 3.5 A	LOAD _{REG}	31.7	mV/A
Maximal Load Resistance to Stay in On-Mode	R _{OUTON}	4.4	kΩ
Minimal Load Resistance to Activate Off-Mode	R _{OUTOFF}	5.5	kΩ
Board Dimension		156 x 51 x 27	mm

Table 1.

Evaluation Board Schematic

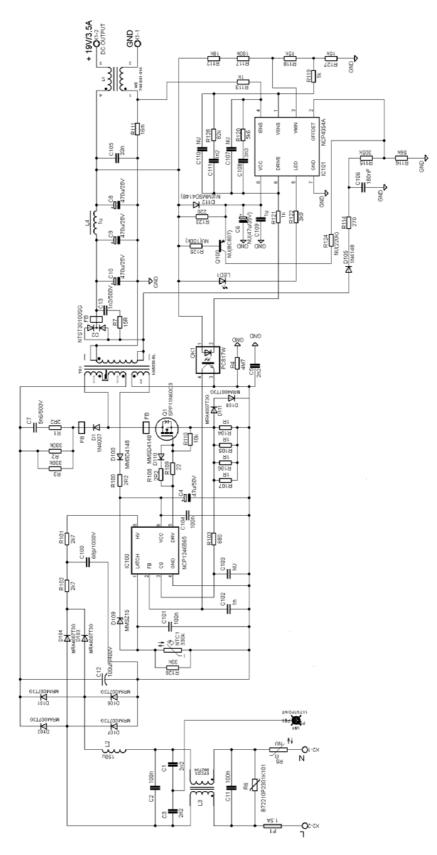


Figure 1. Evaluation Board Schematic

No Load Input Power Consumption

Input power consumption was measured by Yokogawa WT210 power meter. Input power was integrated for 20 minutes and averaged from 4 measurements.

Table 2.

Input Voltage [V; Hz]	Input Power [mW]	
85 V; 60 Hz	9	
115 V; 60 Hz	11	
230 V; 50 Hz	21	
265 V; 50 Hz	25	

Load Regulation

The main impact on load regulation is the serial resistance of the output common mode inductor and the voltage drop on the output current sensing resistor (65.5 mV @ 3.9 A). Output voltage is sensed in front of them by resistor divider.

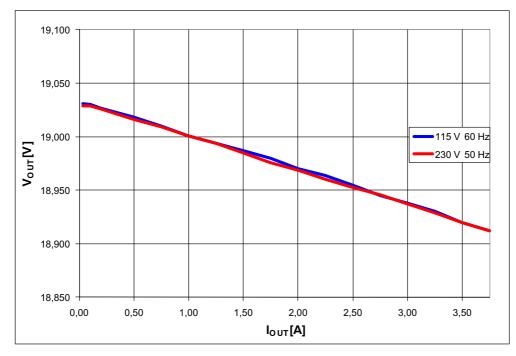


Figure 2. Load Regulation is 31.7 mV/A

Load Characteristic

The following load characteristic shows how current limitation works. When output current reaches 3.9 A, output

voltage starts to be limited to keep current at a level given by sensing resistor R111 and voltage threshold of 62.5 mV at current OTA sensing pin ISNS.

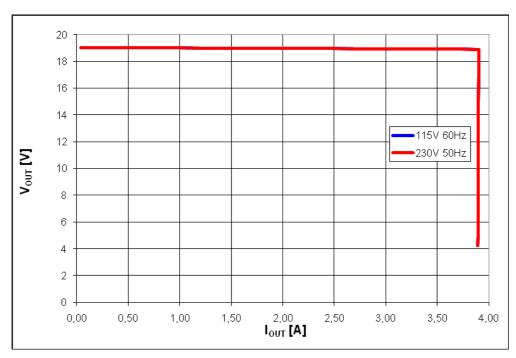


Figure 3. Load Regulation is 31.7 mV/A

Efficiency

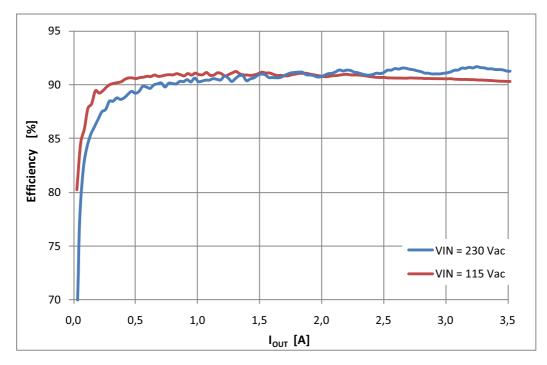


Figure 4. Converter Efficiency for Low and High Line

Output Voltage Ripple

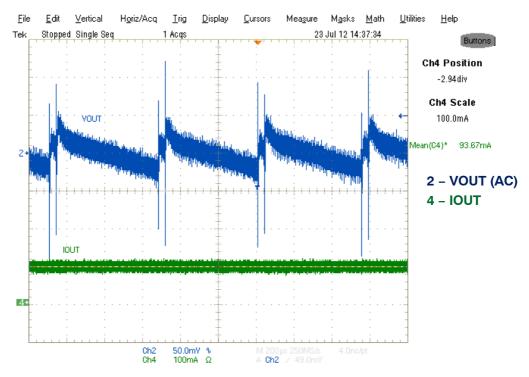


Figure 5. V_{IN} = 230 V_{AC}, I_{OUT} = 100 mA, Primary Controller is in Skip Mode, Δ V_{OUTPK-PK} = 90 mV

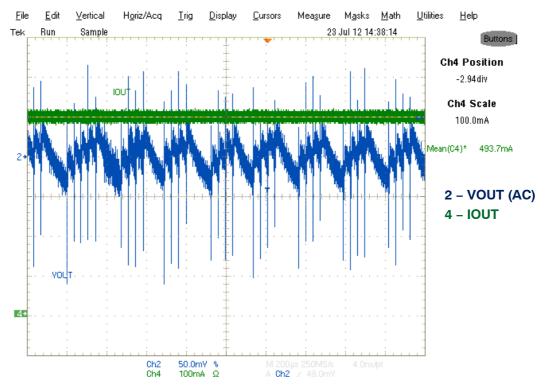


Figure 6. V_{IN} = 230 V_{AC}, I_{OUT} = 500 mA, Δ V_{OUTPK-PK} = 90 mV

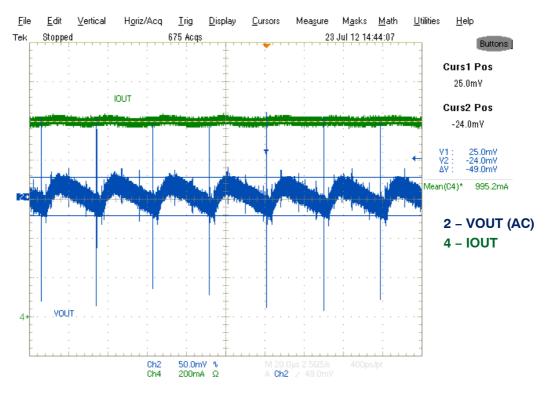


Figure 7. V_{IN} = 230 V_{AC}, I_{OUT} = 1.0 A, Δ V_{OUTPK-PK} = 50 mV

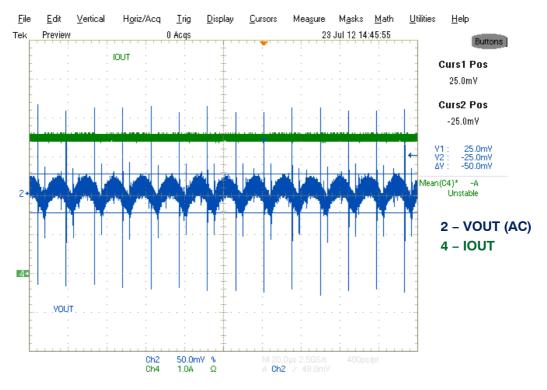


Figure 8. V_{IN} = 230 V_{AC}, I_{OUT} = 3.5 A, Δ V_{OUTPK-PK} = 50 mV

OFF Mode

Off-mode is activated, when output current is below set level. In this design, the off-mode threshold is set to approximately 3.5 mA. This condition is detected by OFFDET comparator through additional rectifier (D105) with bulk capacitor (C106) and voltage divider (R115 and R116). C106 charging current is limited by R114 to avoid full recharge of C106 by short and sporadic pulses in deep skip mode. When very light load is detected, ONOFF current starts to be sunk by the DRIVE pin. The internal pull up current source is connected to VSNS pin and increases its voltage (Figure 10 A). Thanks to this current, voltage OTA starts to sink limited current to help ONOFF current pull the primary FB voltage below the off mode detection level (Figure 11 B). When the primary side detects off mode, FB pull up current is decreased to save energy. After that the FB pull down current through optocoupler can be lower. The secondary side stops sinking additional current by voltage OTA after VSNS voltage drops below VREF to save output capacitor energy (Figure 12 C). Off mode is interrupted when VOUT falls below the VMIN threshold that is detected by VMIN comparator (Figure 9 D). ONOFF current then disappears and primary side FB voltage increases. When primary FB voltage is within operation range, the primary controller starts to operate. The output capacitor is then recharged to nominal output voltage.

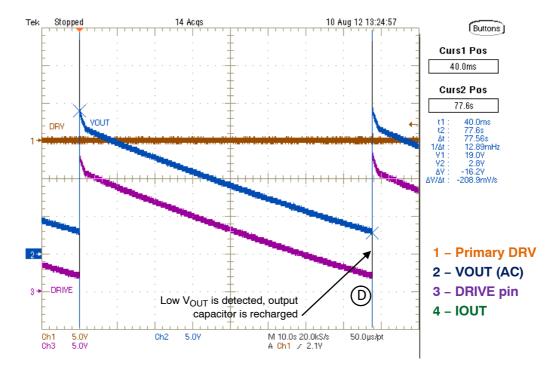


Figure 9. V_{IN} = 230 V_{AC} , I_{OUT} = 0 A, Off-mode Period $t_{OFFMODE}$ = 77.5 s, V_{OUTMIN} = 2.8 V

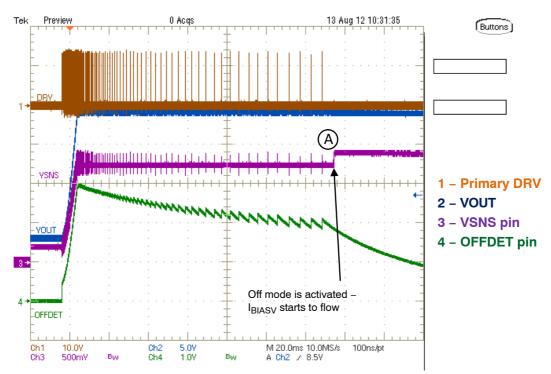


Figure 10. V_{IN} = 230 V_{AC} , I_{OUT} = 0 A, Output Capacitor Recharge when V_{OUT} drops below V_{MIN} Level in Off-mode

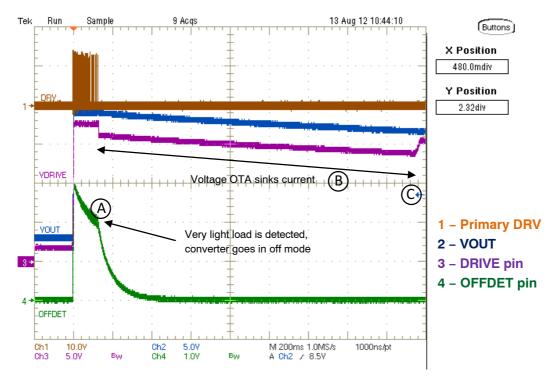


Figure 11. V_{IN} = 230 V_{AC}, I_{OUT} = 0 A, ON–mode to OFF–mode Transition.

The voltage drop on the DRIVE pin indicates the higher voltage OTA sink current (1.5 mA) at time 200 ms after OFF-mode trigger. During this time, the VSNS pin is connected to a 10 mA pull up current source, which increases the voltage at VSNS pin. The OTA stops sinking current 1700 ms after trigger, because VSNS voltage drops below VREF. There is only ONOFF current sunk through OPTO after $V_{SNS} < V_{REF}$.

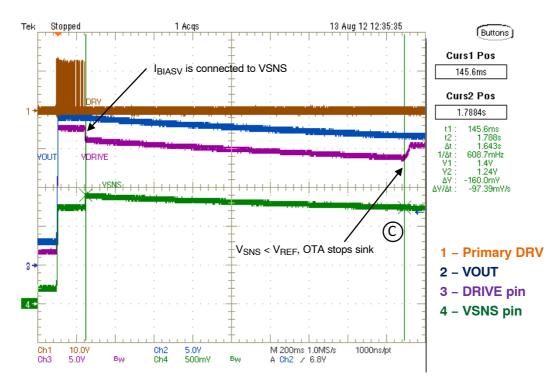


Figure 12. V_{IN} = 230 V_{AC} , I_{OUT} = 0 A, Same Condition as is shown in Figure 11, but VOFFDET is replaced by VSNS. This waveform shows the time when internal current source (I_{BIASV}) is connected to VSNS. This allows voltage OTA to sink less current until VSNS voltage is higher than V_{REF} .

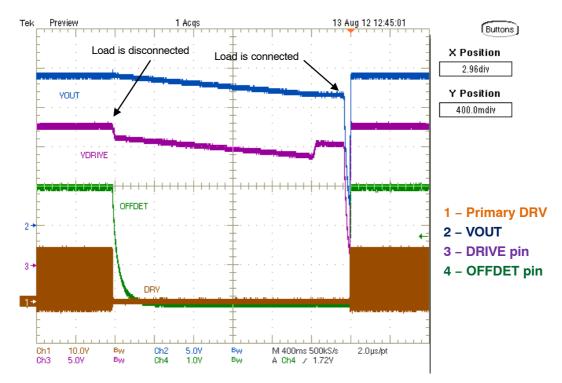


Figure 13. V_{IN} = 230 V_{AC}, I_{OUT} = 0 A, 20 Ω Load Resistor is connected to the Output in Off Mode V_{OUT} quickly drops below V_{MIN} voltage and primary side starts to operate again. The DRIVE waveform shows the point when voltage OTA stops sinking current, because VSNS voltage drops below V_{REF} level.

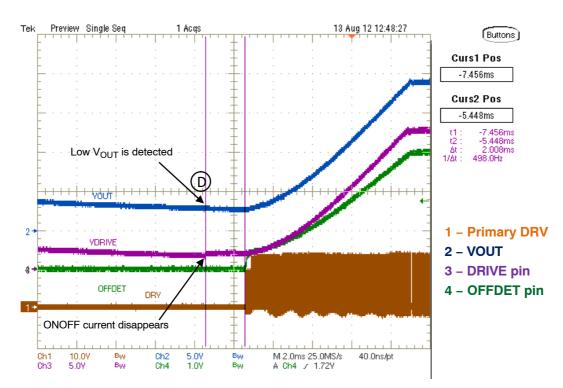


Figure 14. $V_{IN} = 230 V_{AC}$, $I_{OUT} = 0 A$, zoomed Situation from Figure 13. Cursors show time (3.13 ms) that is necessary to switch primary side from OFF mode to normal operation. The DRIVE waveform shows a small voltage change when V_{OUT} is lower than V_{MIN} and ONOFF current is switched off.

Load Detection Speed Up Circuit

When a load is connected to the SMPS in off mode, the output capacitors have to be discharged below VMIN level in order to re-start the primary side. The output capacitor discharging may take too long for some applications. Figure 15 shows an external speed up circuit (load detection circuit) that consists of D112, R124, R125, Q100, C6 and removed R123. This circuit uses the NCP4354A OFFDET pin. When the OFFDET voltage goes above 10% of V_{CC} threshold, off mode is ended. Raising the OFFDET voltage can be used to end OFF mode sooner than waiting for V_{OUT} to drop below V_{MIN} level. When there is no load in off mode,

output capacitors C8, C9, C10 are discharged slower than VCC capacitors C6 and C109, so at VCC the voltage is VOUT-VD109 and transistor Q100 is not conducting. Once a load is connected to the SMPS output in OFF mode, the output capacitors start to be discharged faster by the load than the VCC capacitors are discharged by $I_{\rm CC}$. The voltage difference between output capacitors and VCC capacitors forces Q100 to conduct current through R124 into the OFFDET divider. OFFDET voltage is increased by additional current and when it crosses 10% of VCC threshold, off mode is ended.

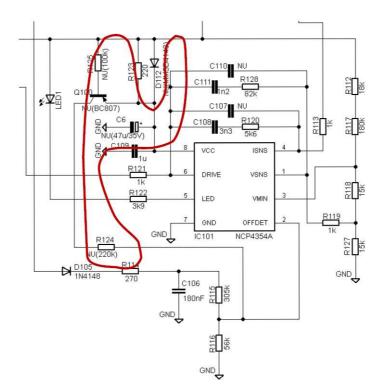


Figure 15. Speed up Circuit Schematic

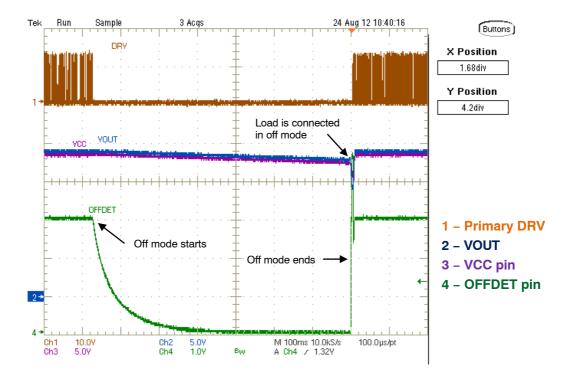


Figure 16. V_{IN} = 230 VAC, I_{OUT} = 0 A \rightarrow 1 A, Load is connected to the Output of Off Mode

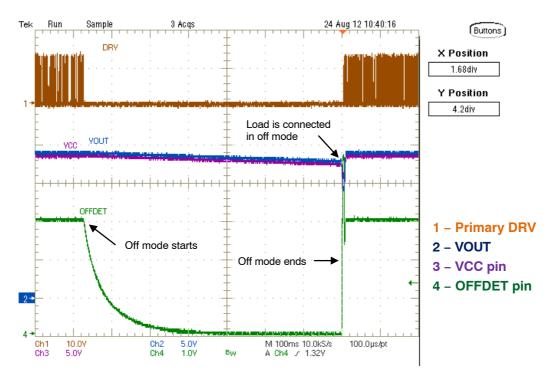


Figure 17. Zoomed Situation from Figure 16. Cursors show time (4 ms) that elapsed from load connection to primary side turn-on.

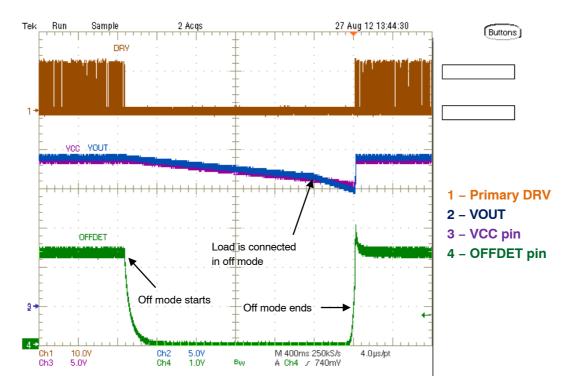


Figure 18. V_{IN} = 230 VAC, R_{LOAD} = 2 k $\Omega \rightarrow \infty \Omega \rightarrow 2$ k Ω , Load is connected to the Output in Off Mode

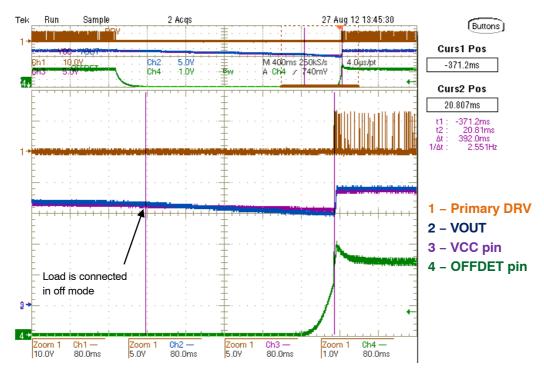
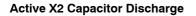


Figure 19. Zoomed Situation from Figure 18. Cursors show time (392 ms) that elapsed from load connection to primary side turn-on.



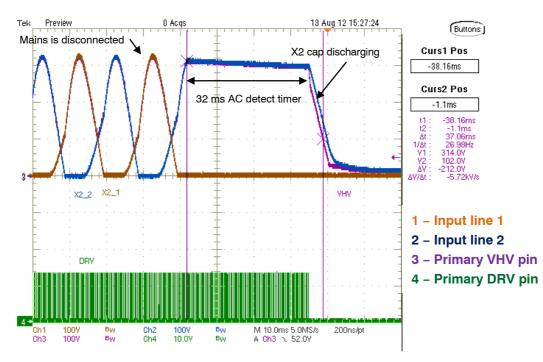


Figure 20. V_{IN} = 230 V_{AC} , I_{OUT} = 1.0 A, when the AC mains is disconnected, 32 ms detection timer is started. After this time, the X2 cap is discharged. Discharging time is much shorter than required by safety standards (37 ms << 1 s)

Transient Response

Output Current Transients

Current slew rate is 125 mA / 1 μs for all transients.

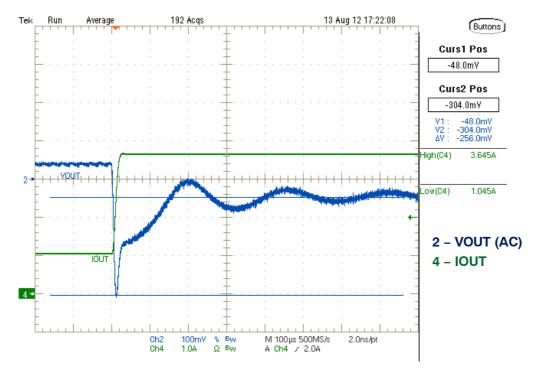


Figure 21. V_{IN} = 115 V_{AC}, I_{OUT} = 1.0 – 3.5 A, V_{OUT} $_{DROP}$ = 256 mV

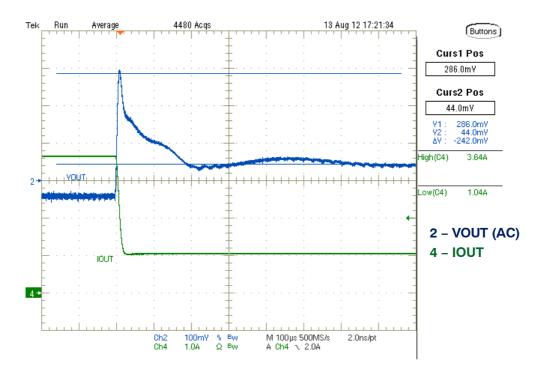


Figure 22. V_{IN} = 115 V_{AC}, I_{OUT} = 3.5 – 1.0 A, V_{OUT_OVERSHOOT} = 242 mV

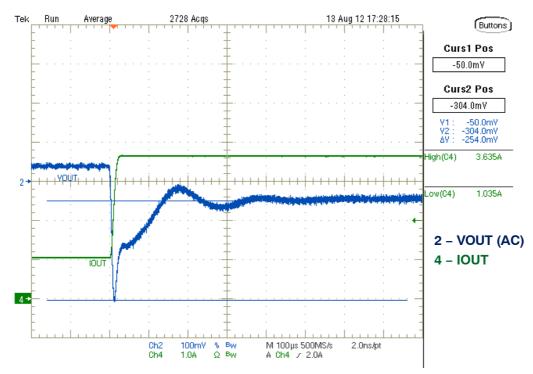


Figure 23. V_{IN} = 230 V_{AC} , I_{OUT} = 1.0 – 3.5 A, V_{OUT_DROP} = 254 mV

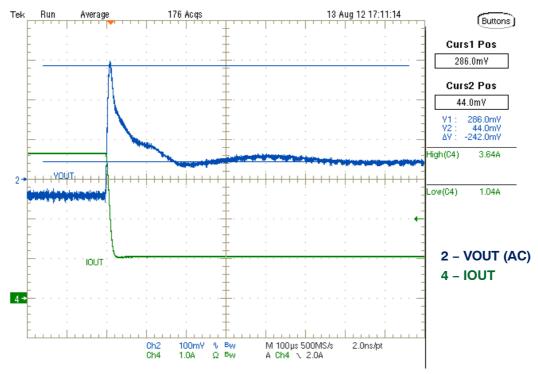


Figure 24. V_{IN} = 230 V_{AC} , I_{OUT} = 3.5 – 1.0 A, $V_{OUT_OVERSHOOT}$ = 242 mV

Output Voltage Transients

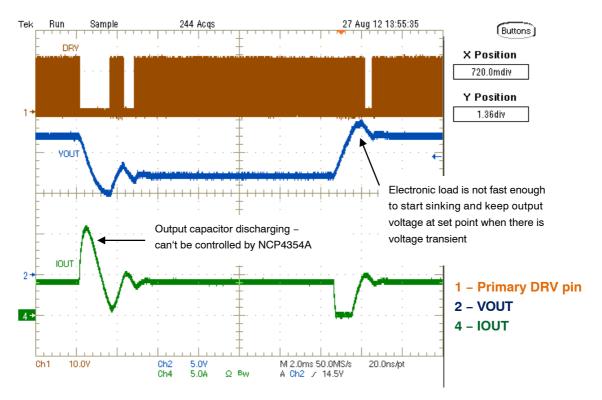


Figure 25. V_{IN} = 230 V_{AC} , V_{OUT} = 12 – 17 V

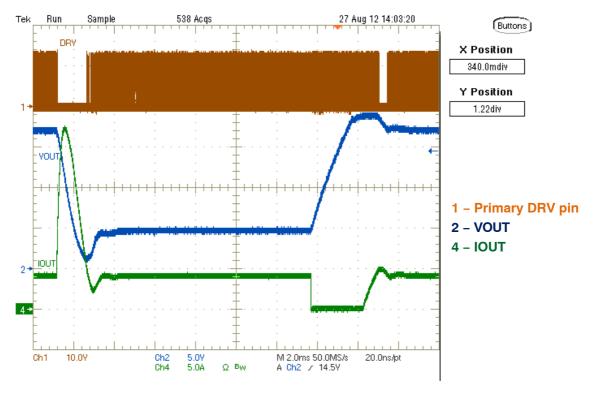
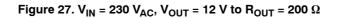


Figure 26. V_{IN} = 230 V_{AC} , V_{OUT} = 5 – 17 V

Tek Run Sample 89 Acqs 27 Aug 12 13:57:53 (Buttons) DBV X Position 720.0mdiv **Y** Position 1.36div YOUT 1 – Primary DRV pin 2 – VOUT IOUT 4 – IOUT 2 Output capacitor discharging - can't be controlled by NCP4354A 5.0V 2.0A Ch1 10.07 Ch2 Ch4 M 2.0ms 50.0MS/s 20.0ns/pt ΩBW A Ch2 / 14.5V

Output Voltage to Current Transient



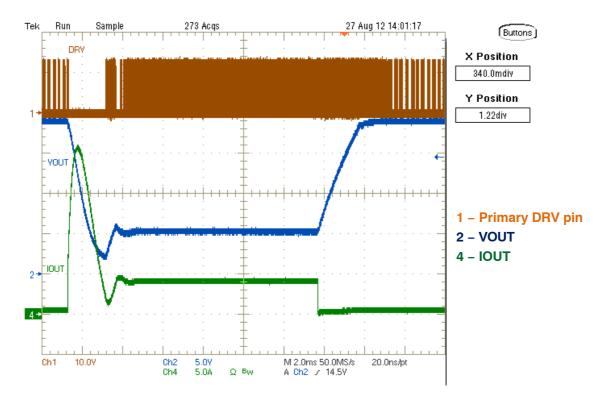


Figure 28. V_{IN} = 230 V_{AC}, V_{OUT} = 5 V to R_{OUT} = 40 Ω

Open Loop Transfer Characteristics

Voltage Control Loop Transfer Characteristic Phase margin is never lower than 50° Gain margin is never lower than 13 dB Crossover frequency is between 0.6 – 0.75 kHz

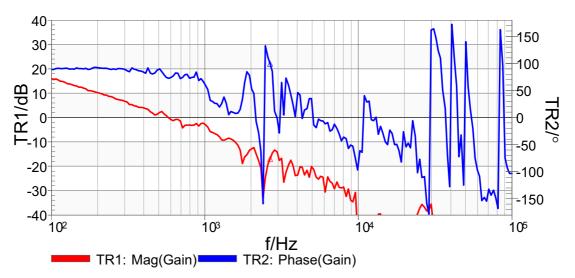


Figure 29. V_{IN} = 85 V_{AC}, I_{OUT} = 100 mA

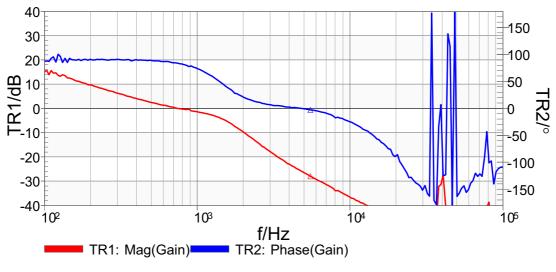
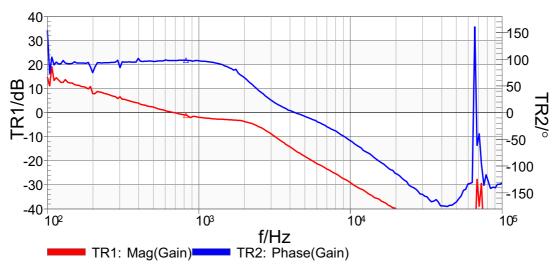
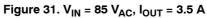
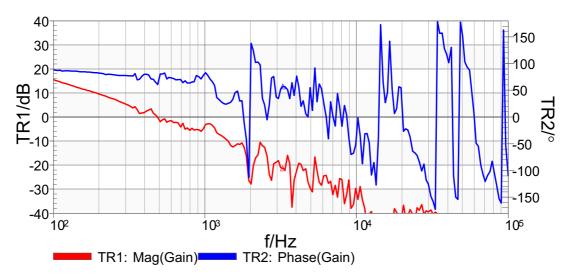
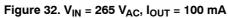


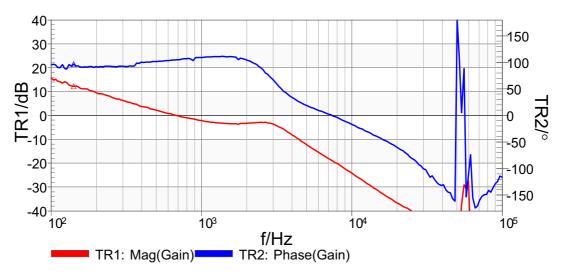
Figure 30. V_{IN} = 85 V_{AC} , I_{OUT} = 1.0 A



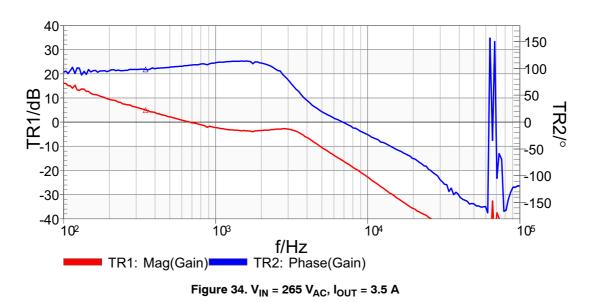




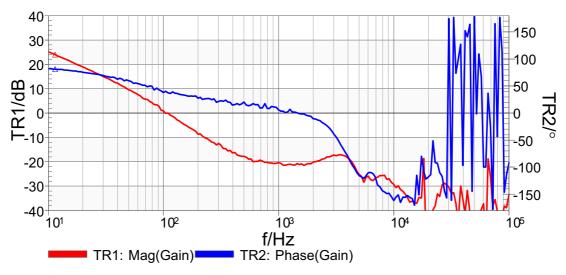


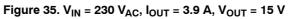


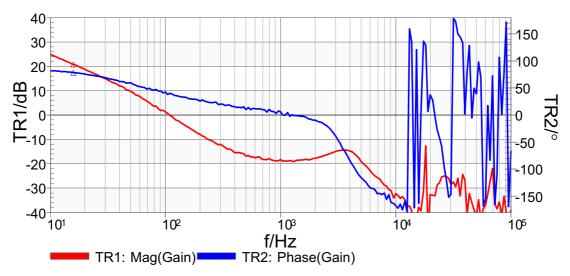


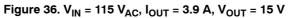


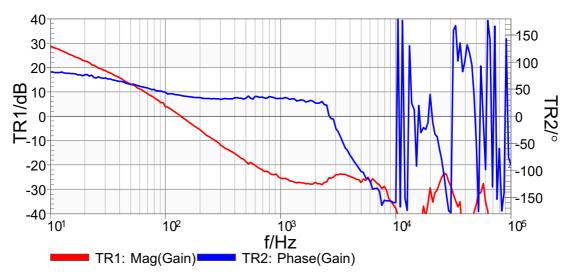
Current Control Loop Transfer Characteristic Phase margin is never lower than 35° Gain margin is never lower than 18 dB Crossover frequency is between 100 – 200 Hz

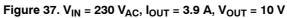


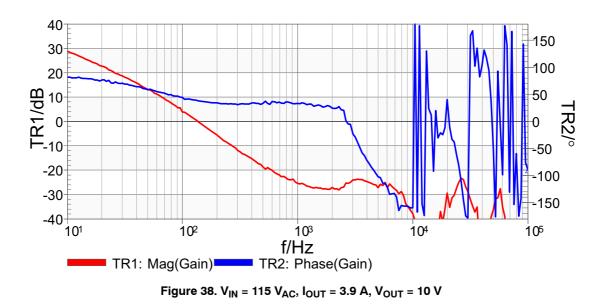


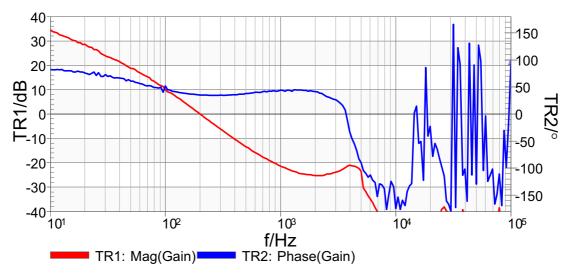


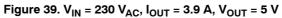












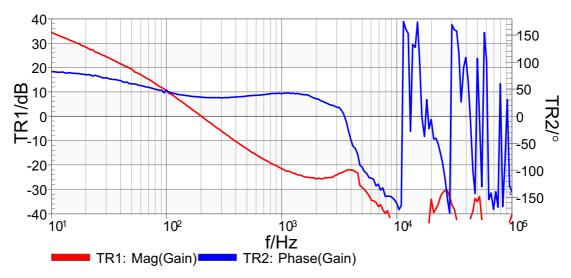


Figure 40. V_{IN} = 115 $V_{\text{AC}},\,I_{\text{OUT}}$ = 3.9 A, V_{OUT} = 5 V

Conducted Emission Quasi-peak

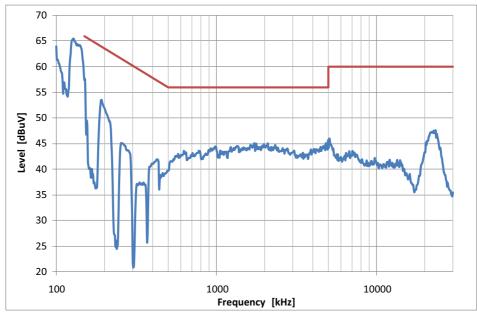


Figure 41. V_{IN} = 115 V_{AC} , I_{OUT} = 3.5 A

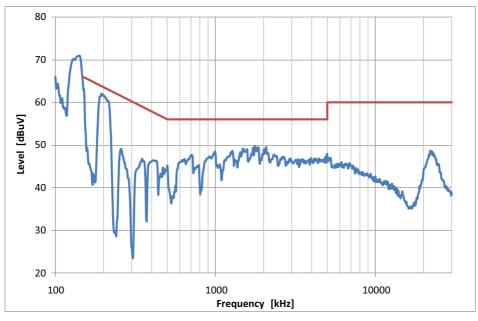


Figure 42. V_{IN} = 230 V_{AC} , I_{OUT} = 3.5 A

Result Summary

The NCP1246 and NCP4354 controllers allow building cost effective, easy to design and high efficiency power supplies with very low no load input power consumption.

Special thanks go to companies Coilcraft, Epcos and Würth that provided samples of their components for this evaluation board. **Top Side Assembly**

