Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NCP4523

CMOS 3CH-LDOs for RF Unit

The NCP4523 Series are multi voltage regulator ICs with high output voltage accuracy, extremely low supply current, low noise, low ON−resistance and high ripple rejection by CMOS process. The NCP4523 Series contain three voltage regulators. Each of these voltage regulators in the NCP4523 Series consists of a voltage reference unit, an error amplifier, resistors for setting output voltage, a current limit circuit and a chip enable circuit.

The chip enable function contributes to prolong battery life. Further, regulators in the NCP4523 Series are with low dropout voltage, excellent load transient response and line transient response, thus the NCP4523 series are very suitable for the power supply for hand−held communication equipment.

The output voltage of each regulator is fixed with high accuracy by laser trim.

Since the package for these ICs is SSOP−8, high density mounting of the ICs on boards is possible.

Features

- Ultra−Low Supply Current
- Low Standby Current
- Low Dropout Voltage
- High Ripple Rejection, Typical 70 dB (f = 1.0 kHz)
- High Output Voltage Accuracy, ±2.0%
- Excellent Load Transient Response and Line Transient Response
- Small Package 8−Pin SSOP
- Maximum Input Voltage 6.0 V
- Pb−Free Packages are Available

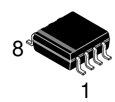
Applications

- Power Source for Cellular Phones such as GSM, CDMA and Personal Handy−Phone System
- Power Source for Electrical Appliances such as Cameras, VCRs, Camcorders, etc.
- Power Source for Battery−Powered Equipment

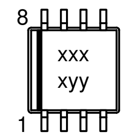
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

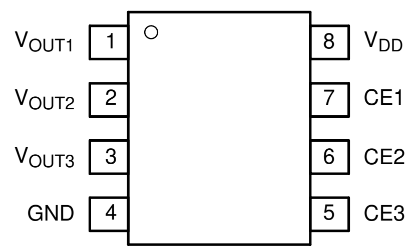


SSOP−8
G SUFFIX
CASE 487



xxxx = Product Code
yy = Lot Number

PIN ASSIGNMENT



(Top View)
SSOP−8

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 22 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 22 of this data sheet.

September, 2005 − Rev. 6

Publication Order Number:
NCP4523/D

PIN DESCRIPTION

Pin Number		
NCP4523G SSOP−8	Symbol	Description
1	V_{OUT1}	Output Pin
2	V_{OUT2}	Output Pin
3	V_{OUT3}	Output Pin
4	GND	Ground Pin
5	CE3	Chip Enable Pin
6	CE2	Chip Enable Pin
7	CE1	Chip Enable Pin
8	V_{DD}	Input Pin

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	7.0	V
Input Voltage (CE Pin)	CE	−0.3 ~ V_{IN} + 0.3	V
Output Voltage	V_{OUT}	−0.3 ~ V_{IN} + 0.3	V
Output Current (V_{OUT1})	I_{OUT1}	200	mA
Output Current (V_{OUT2})	I_{OUT2}	100	mA
Output Current (V_{OUT3})	I_{OUT3}	100	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opt}	−40 ~ 85	°C
Storage Temperature Range	T_{stg}	−55 ~ 125	°C
Electrostatic Discharge Sensitivity (ESD) Human Body Model (HBM) Machine Model (MM)	ESD	 2000 200	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS

VR1 (T_{opt} = 25°C)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Output Voltage	$V_{IN} - V_{OUT}$ = 1.0 V 1.0 mA ≤ I_{OUT} ≤ 30 mA	V_{OUT}	×0.98	–	×1.02	V
Output Current	$V_{IN} - V_{OUT}$ = 1.0 V	I_{OUT}	150	–	–	mA
Load Regulation	$V_{IN} - V_{OUT}$ = 1.0 V 1.0 mA ≤ I_{OUT} ≤ 80 mA	$\Delta V_{OUT}/\Delta I_{OUT}$	–	12	40	mV
Dropout Voltage	Refer to Electrical Characteristic by Output Voltage (VR1)	V_{DIF}	–	–	–	–
Supply Current	$V_{IN} - V_{OUT}$ = 1.0 V	I_{SS}	–	70	120	μA
Supply Current (Standby)	$V_{IN} - V_{OUT}$ = 1.0 V V_{CE} = GND	Istandby	–	0.1	1.0	μA
Line Regulation	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.0 V I_{OUT} = 30 mA	$\Delta V_{OUT}/\Delta V_{IN}$	–	0.05	0.20	%/V
Ripple Rejection	f = 1.0 kHz, sinusoidal 0.5 Vp−p $V_{IN} - V_{OUT}$ = 1.0 V	RR	–	70	–	dB
Input Voltage	–	V_{IN}	–	–	6.0	V
Output Voltage Temperature Coefficient	I_{OUT} = 50 mA −40°C ≤ T_{opt} ≤ 85°C	$\Delta V_{OUT}/\Delta T$	–	±100	–	ppm/°C
Short Current Limit	V_{OUT} = 0 V	I_{LIM}	–	50	–	mA
CE Pull−down Resistance	–	R_{DN}	2.5	5.0	10	MΩ
CE Input Voltage “H”	–	V_{CEH}	1.5	–	V_{IN}	V
CE Input Voltage “L”	–	V_{CEL}	0.00	–	0.25	V
Output Noise	BW = 10 Hz – 100 kHz	en	–	60	–	μVrms

ELECTRICAL CHARACTERISTICS BY OUTPUT VOLTAGE (VR1)

Output Voltage V_{OUT} (V)	Dropout Voltage V_{DIF} (V)		
	Condition	Typ	Max
2.0 ≤ V_{OUT} ≤ 2.4	I_{OUT} = 150 mA	0.35	0.55
2.5 ≤ V_{OUT} ≤ 2.7		0.30	0.45
2.8 ≤ V_{OUT} ≤ 3.3		0.22	0.35

ELECTRICAL CHARACTERISTICS

VR2 (T_{opt} = 25°C)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Output Voltage	V_{IN} – V_{OUT} = 1.0 V 1.0 mA ≤ I_{OUT} ≤ 30 mA	V_{OUT}	×0.98	–	×1.02	V
Output Current	V_{IN} – V_{OUT} = 1.0 V	I_{OUT}	80	–	–	mA
Load Regulation	V_{IN} – V_{OUT} = 1.0 V 1.0 mA ≤ I_{OUT} ≤ 50 mA	$\Delta V_{OUT}/\Delta I_{OUT}$	–	12	40	mV
Dropout Voltage	Refer to Electrical Characteristic by Output Voltage (VR2)	V_{DIF}	–	–	–	–
Supply Current	V_{IN} – V_{OUT} = 1.0 V	I_{SS}	–	70	120	μA
Supply Current (Standby)	V_{IN} – V_{OUT} = 1.0 V V_{CE} = GND	Istandby	–	0.1	1.0	μA
Line Regulation	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.0 V I ≤ = 30 mA	$\Delta V_{OUT}/\Delta V_{IN}$	–	0.05	0.20	V
Ripple Rejection	f = 1.0 kHz, sinusoidal 0.5 Vp−p V_{IN} – V_{OUT} = 1.0 V	RR	–	70	–	dB
Input Voltage	–	V_{IN}	–	–	6.0	V
Output Voltage Temperature Coefficient	I_{OUT} = 30 mA −40°C ≤ T_{opt} ≤ 85°C	$\Delta V_{OUT}/\Delta T$	–	±100	–	ppm/°C
Short Current Limit	V_{OUT} = 0 V	I_{LIM}	–	50	–	mA
CE Pull−down Resistance	–	R_{DN}	2.5	5.0	10	MΩ
CE Input Voltage “H”	–	V_{CEH}	1.5	–	V_{IN}	V
CE Input Voltage “L”	–	V_{CEL}	0.00	–	0.25	V
Output Noise	BW = 10 Hz – 100 kHz	en	–	60	–	μVrms

ELECTRICAL CHARACTERISTICS BY OUTPUT VOLTAGE (VR2)

Output Voltage V_{OUT} (V)	Dropout Voltage V_{DIF} (V)		
	Condition	Typ	Max
2.0 ≤ V_{OUT} ≤ 2.4	I_{OUT} = 80 mA	0.22	0.38
2.5 ≤ V_{OUT} ≤ 2.7		0.20	0.38
2.8 ≤ V_{OUT} ≤ 3.3		0.16	0.24

ELECTRICAL CHARACTERISTICS

VR3 (T_{opt} = 25°C)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Output Voltage	$V_{IN} - V_{OUT}$ = 1.0 V 1.0 mA ≤ 30 mA	V_{OUT}	×0.98	–	×1.02	V
Output Current	$V_{IN} - V_{OUT}$ = 1.0 V	I_{OUT}	80	–	–	mA
Load Regulation	$V_{IN} - V_{OUT}$ = 1.0 V 1.0 mA ≤ I_{OUT} ≤ 50 mA	$\Delta V_{OUT}/\Delta I_{OUT}$	–	12	40	mV
Dropout Voltage	Refer to Electrical Characteristic by Dropout Voltage (VR3)	V_{DIF}	–	–	–	–
Supply Current	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 6.0 V I_{OUT} = 30 mA	I_{SS}	–	70	120	μA
Supply Current (Standby)	f = 1.0 kHz, sinusoidal 0.5 Vp−p $V_{IN} - V_{OUT}$ = 1.0 V	Istandby	–	0.1	1.0	μA
Line Regulation	–	$\Delta V_{OUT}/\Delta V_{IN}$	–	0.05	0.20	%/V
Ripple Rejection	I_{OUT} = 30 mA −40°C ≤ T_{opt} ≤ 85°C	RR	–	70	–	dB
Input Voltage	V_{OUT} = 0 V	V_{IN}	–	–	6.0	V
Output Voltage Temperature Coefficient	–	$\Delta V_{OUT}/\Delta T$	–	±100	–	ppm/°C
Short Current Limit	BW = 10 Hz – 100 kHz	I_{LIM}	–	50	–	mA
CE Pull−down Resistance	–	R_{DN}	2.5	5.0	10	MΩ
CE Input Voltage “H”	–	V_{CEH}	1.5	–	V_{IN}	V
CE Input Voltage “L”	–	V_{CEL}	0.00	–	0.25	V
Output Noise	–	en	–	60	–	μVrms

ELECTRICAL CHARACTERISTICS BY OUTPUT VOLTAGE (VR3)

Output Voltage V_{OUT} (V)	Dropout Voltage V_{DIF} (V)		
	Condition	Typ	Max
2.0 ≤ V_{OUT} ≤ 2.4	I_{OUT} = 80 mA	0.24	0.38
2.5 ≤ V_{OUT} ≤ 2.7		0.22	0.28
2.8 ≤ V_{OUT} ≤ 3.3		0.16	0.24

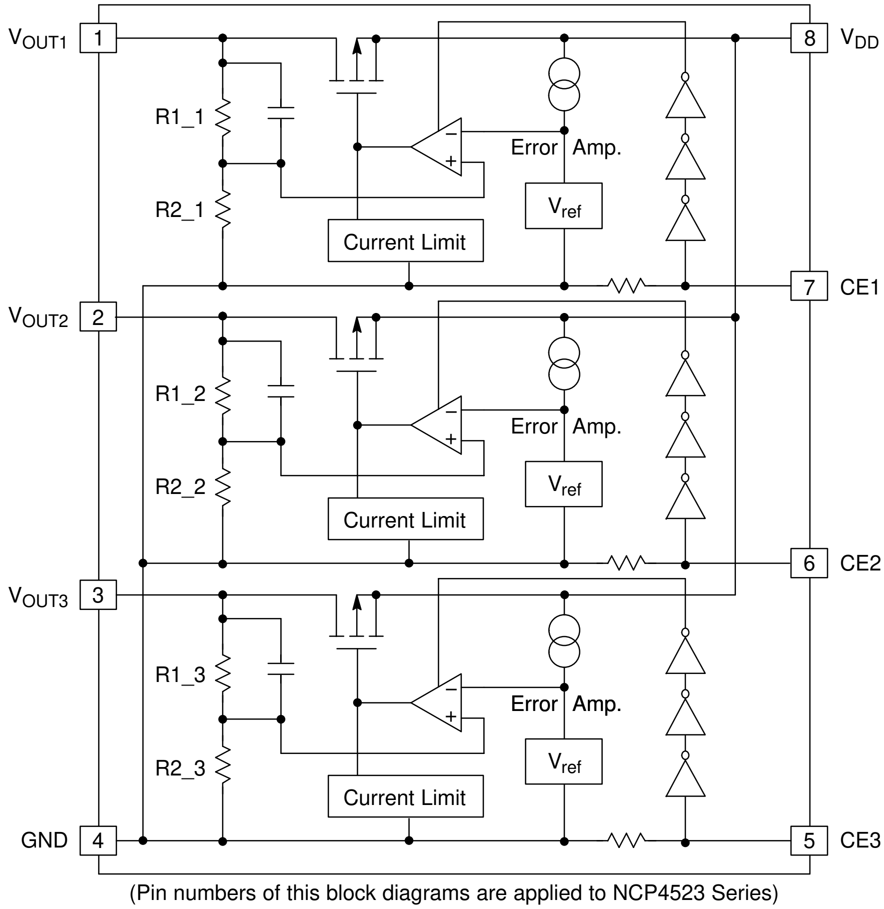


Figure 1. Block Diagram

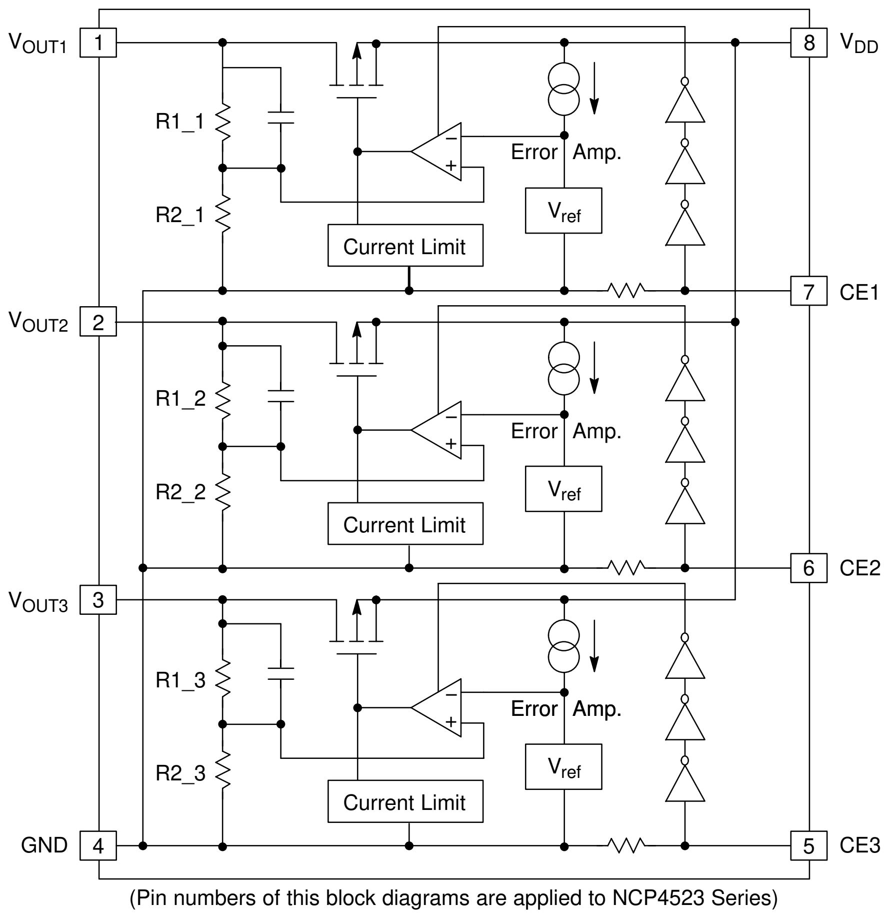


Figure 2. Operation

Fluctuation of each regulator's output voltage, or $V_{OUT1, 2, 3}$ is detected individually. Then it is put back to an error amplifier through feedback resistors, or R1_1, R2_1, R1_2, R2_2, R1_3, R2_3 and compared with a reference voltage and compensated for the result and make a constant voltage.

In each regulator, short protection is made with a current limit circuit and standby mode is available by a chip enable circuit.

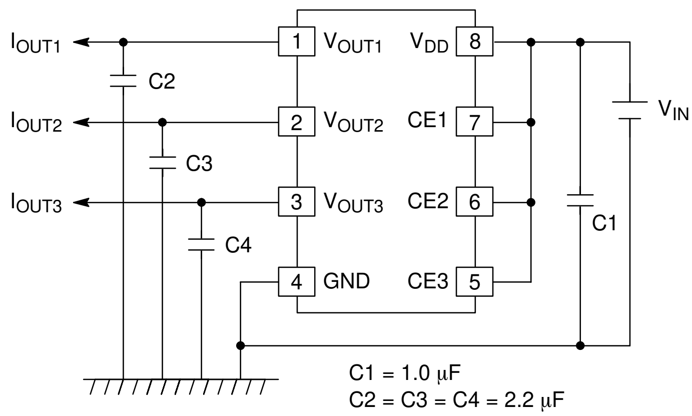


Figure 3. Basic Test Circuit

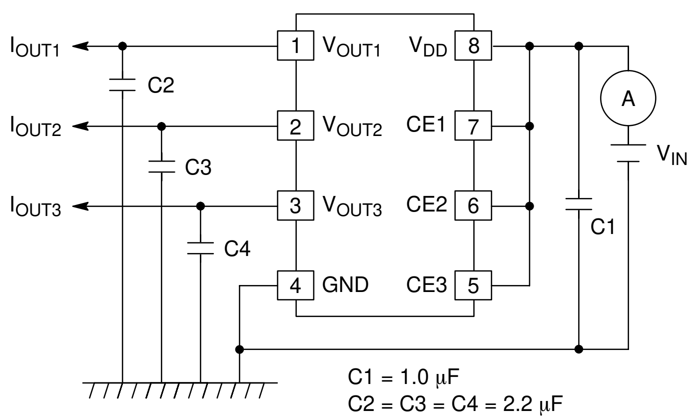


Figure 4. Test Circuit for Supply Current

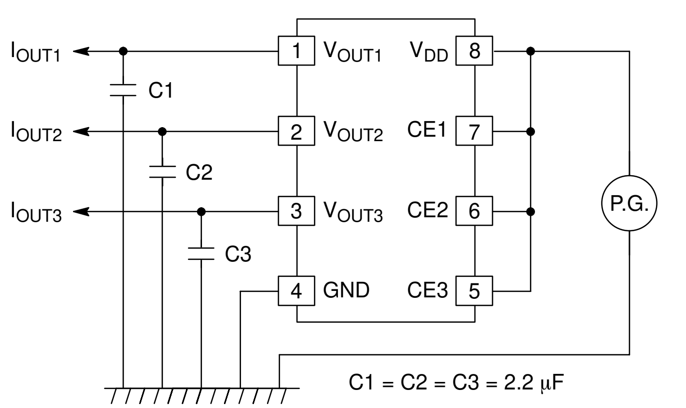


Figure 5. Test Circuit for Line Transient Response

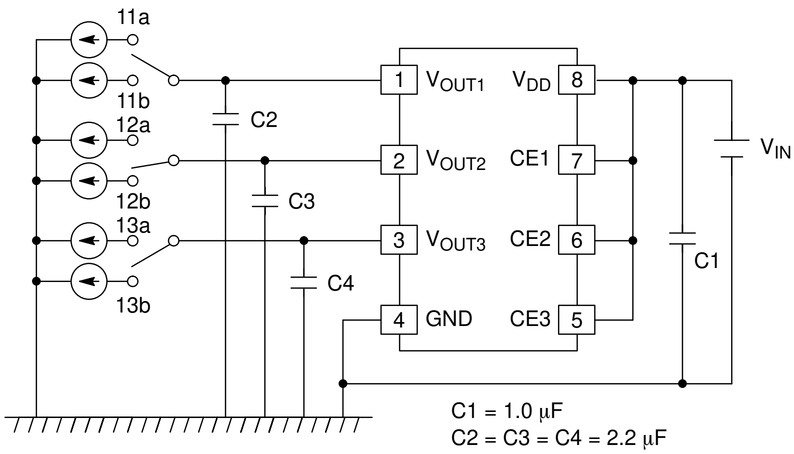


Figure 6. Test Circuit for Load Transient Response

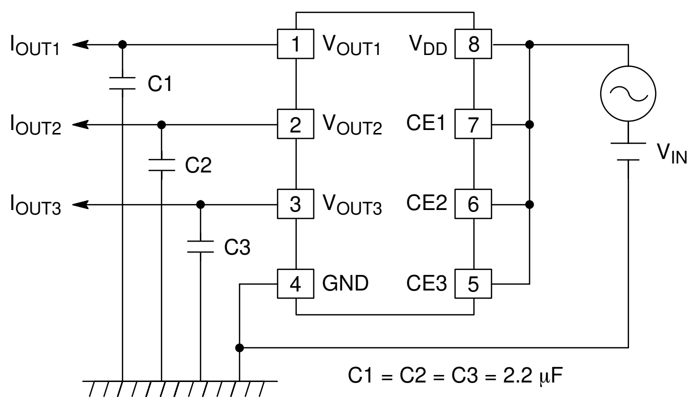


Figure 7. Test Circuit for Ripple Rejection

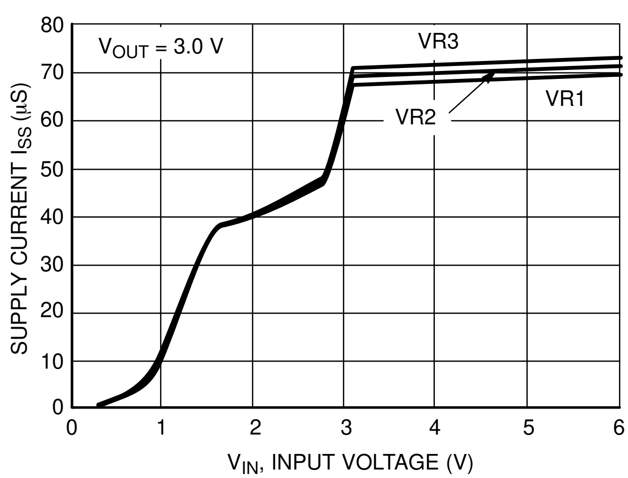


Figure 8. Supply Current vs Input Voltage

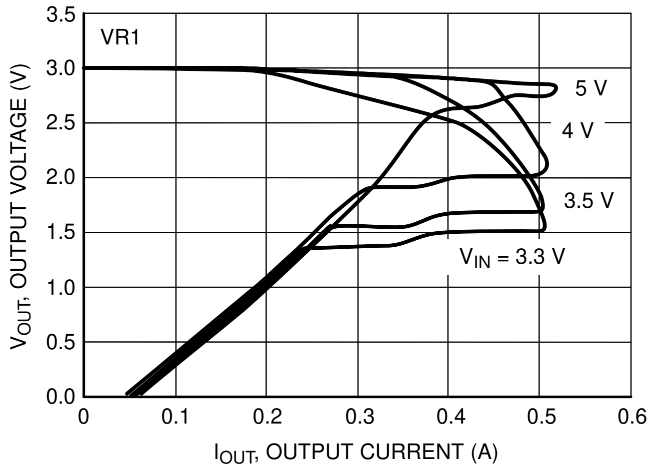


Figure 9. Output Voltage vs. Output Current

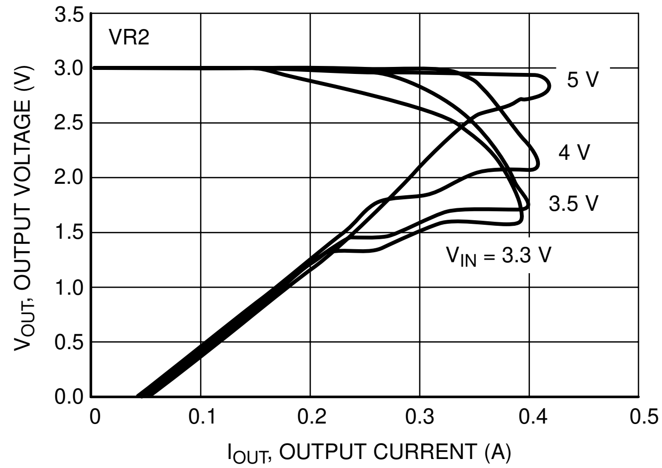


Figure 10. Output Voltage vs. Output Current

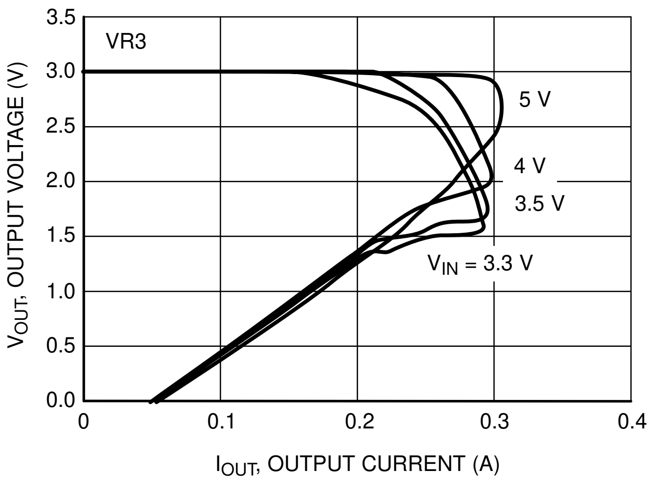


Figure 11. Output Voltage vs. Output Current

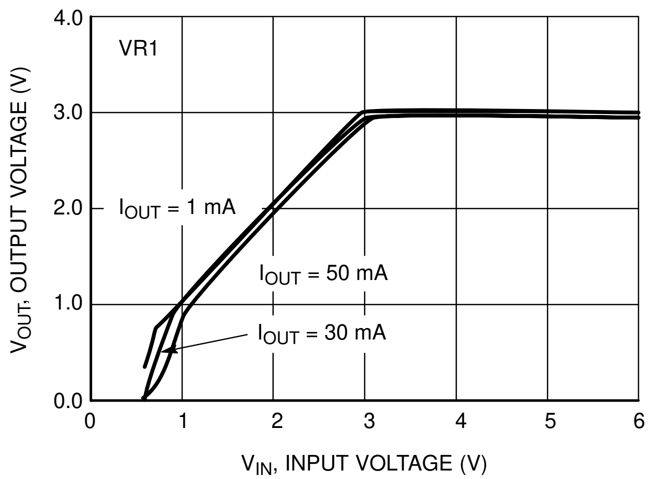


Figure 12. Output Voltage vs. Input Voltage

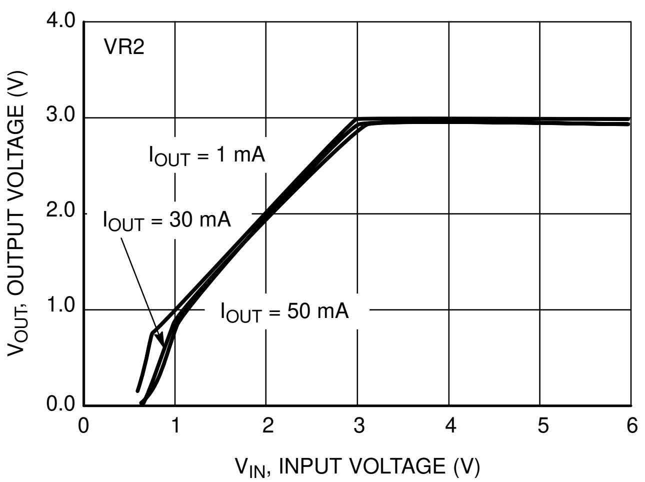


Figure 13. Output Voltage vs. Input Voltage

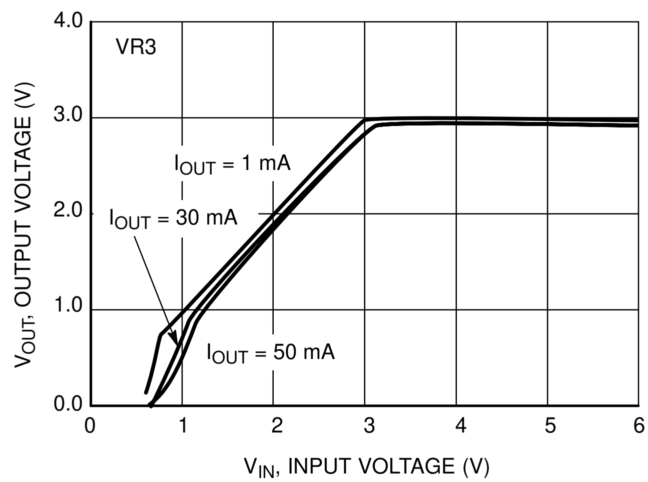


Figure 14. Output Voltage vs. Input Voltage

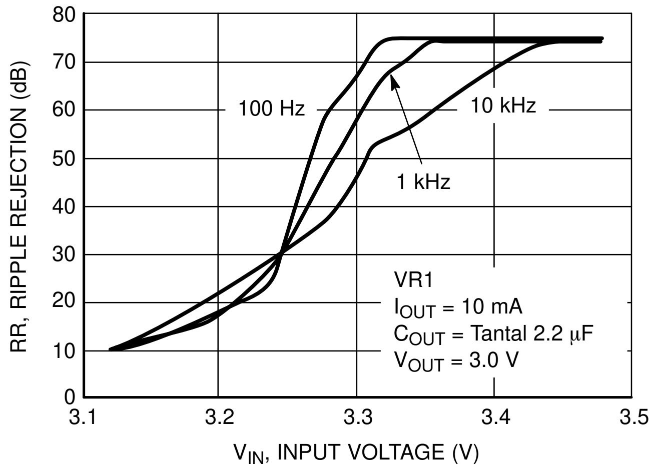


Figure 15. Ripple Rejection vs. Input Voltage (DC Bias)

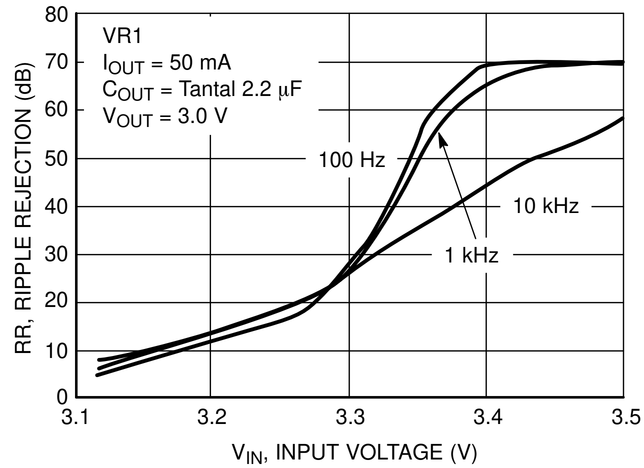


Figure 16. Ripple Rejection vs. Input Voltage (DC Bias)

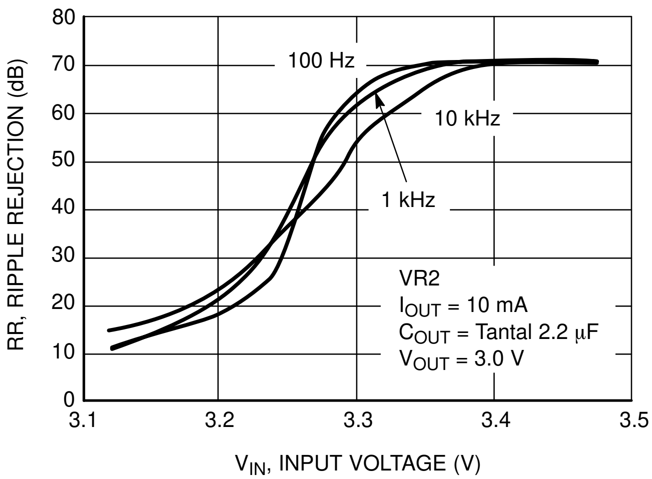


Figure 17. Ripple Rejection vs. Input Voltage (DC Bias)

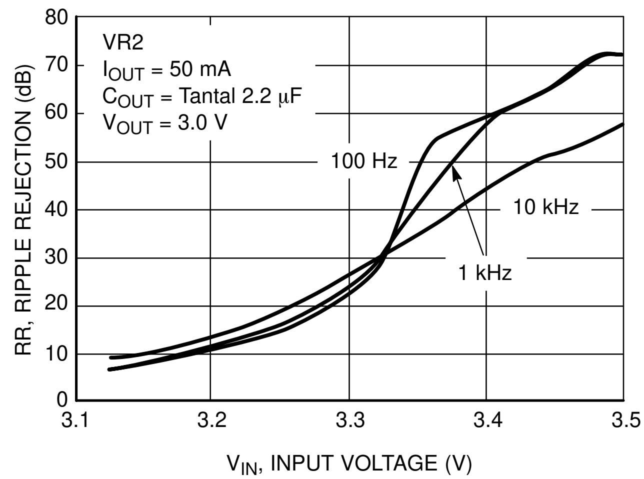


Figure 18. Ripple Rejection vs. Input Voltage (DC Bias)

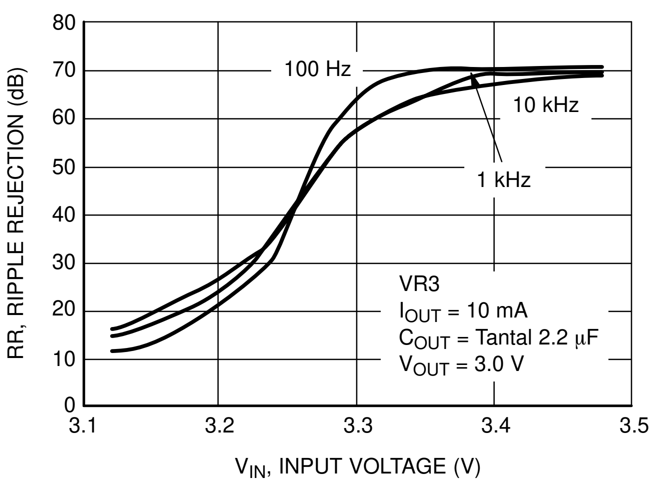


Figure 19. Ripple Rejection vs. Input Voltage (DC Bias)

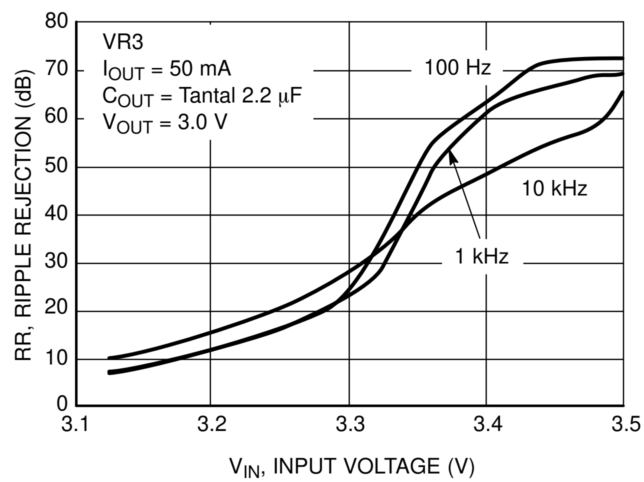


Figure 20. Ripple Rejection vs. Input Voltage (DC Bias)

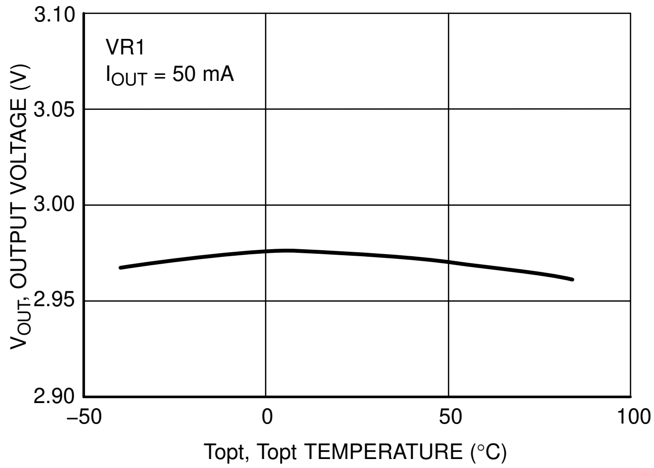


Figure 21. Output Voltage vs. Temperature

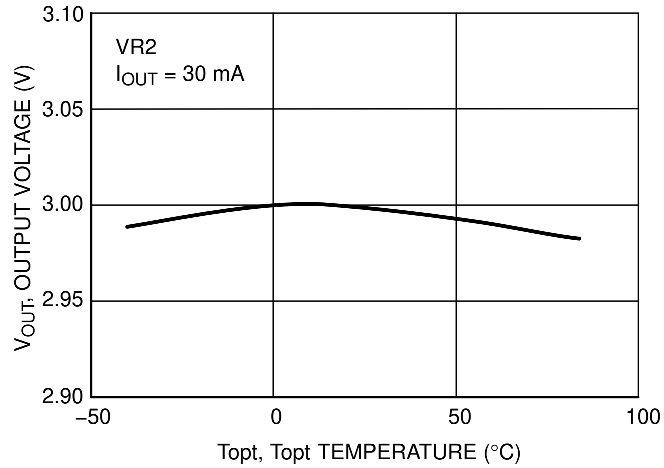


Figure 22. Output Voltage vs. Temperature

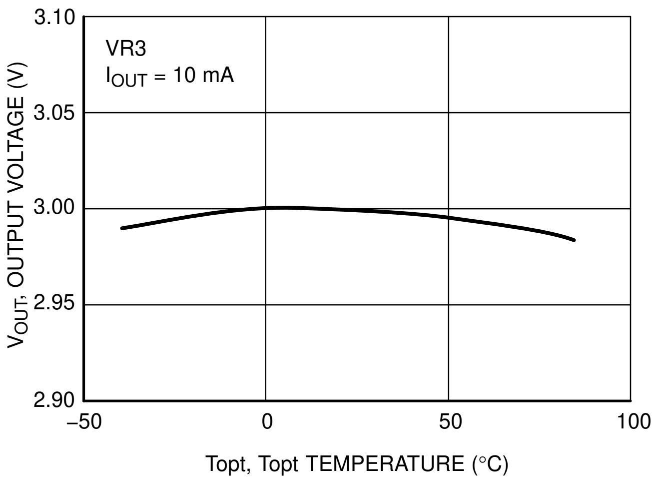


Figure 23. Output Voltage vs. Temperature

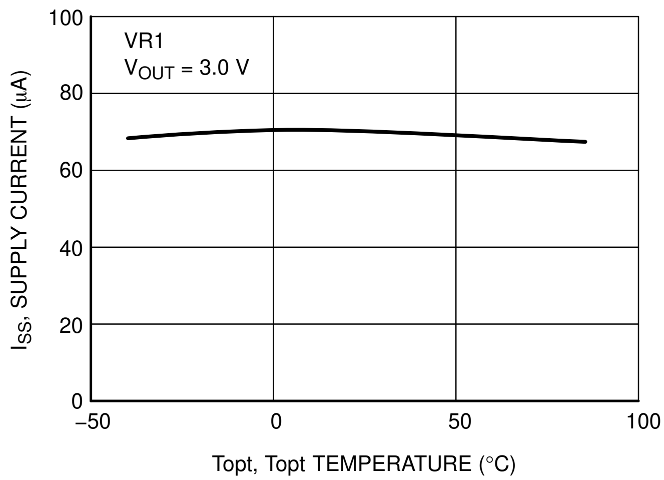


Figure 24. Supply Current vs. Temperature

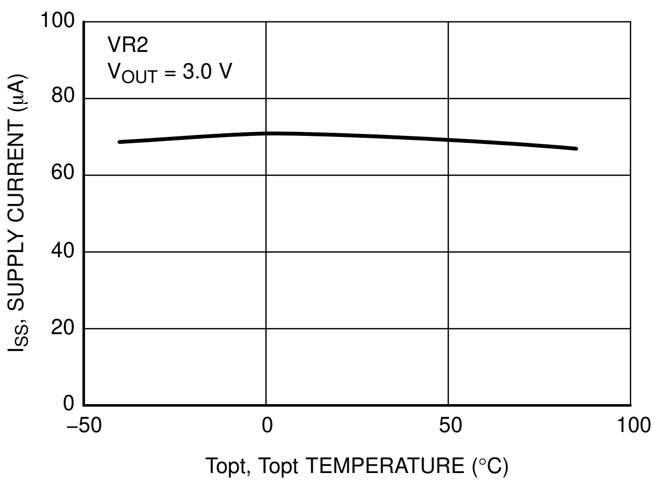


Figure 25. Supply Current vs. Temperature

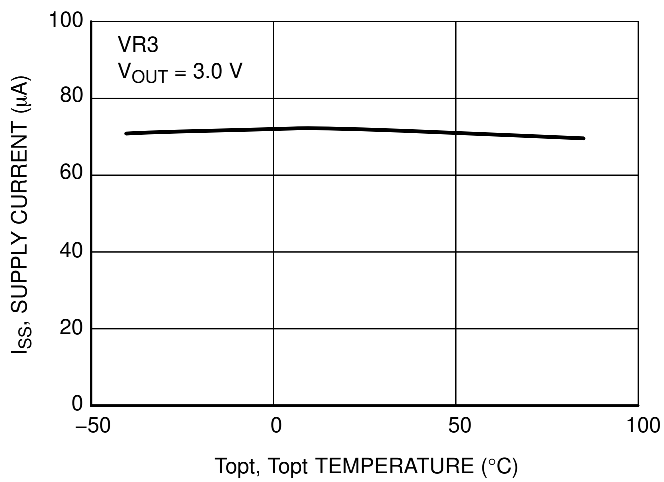


Figure 26. Supply Current vs. Temperature

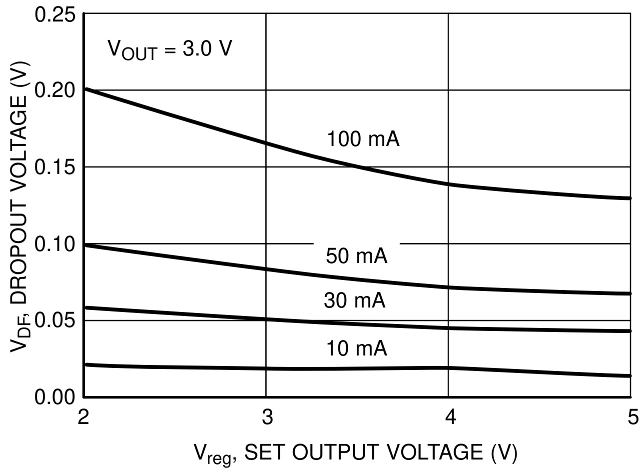


Figure 27. Dropout Voltage vs. Set Output Voltage

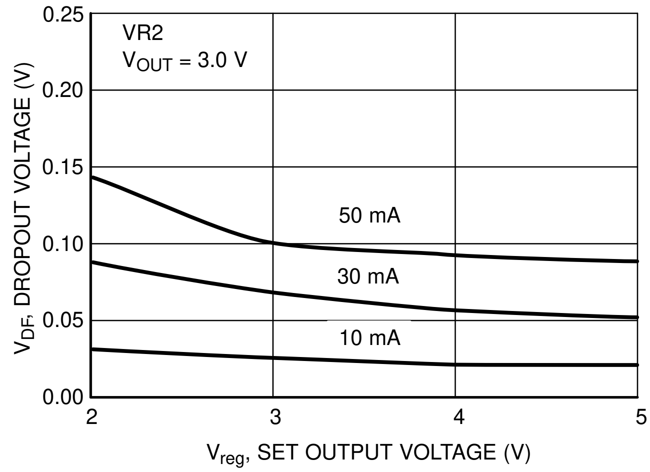


Figure 28. Dropout Voltage vs. Set Output Voltage

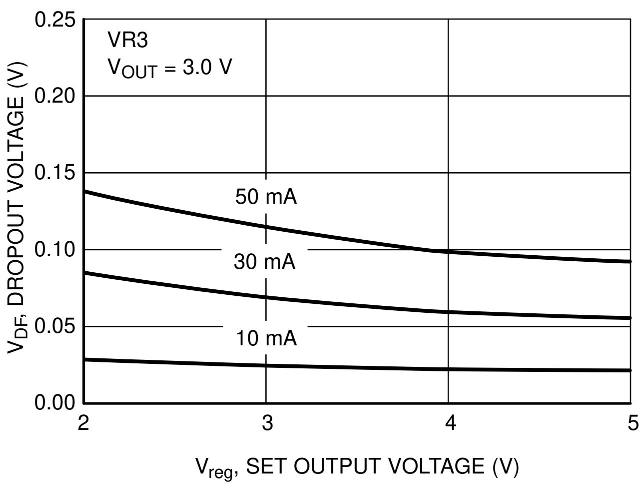


Figure 29. Dropout Voltage vs. Set Output Voltage

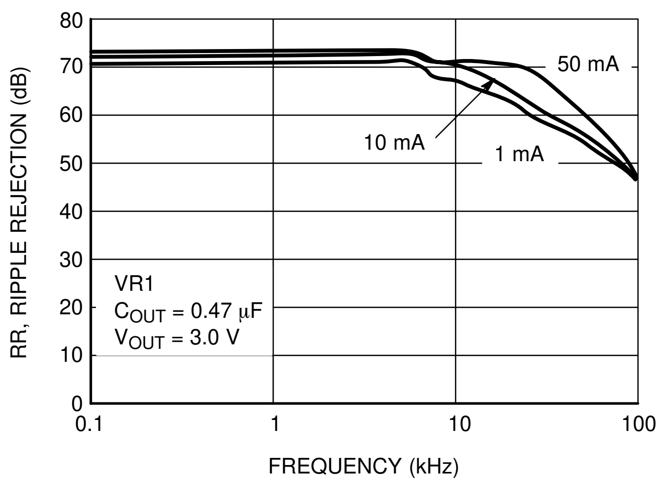


Figure 30. Ripple Rejection vs. Frequency

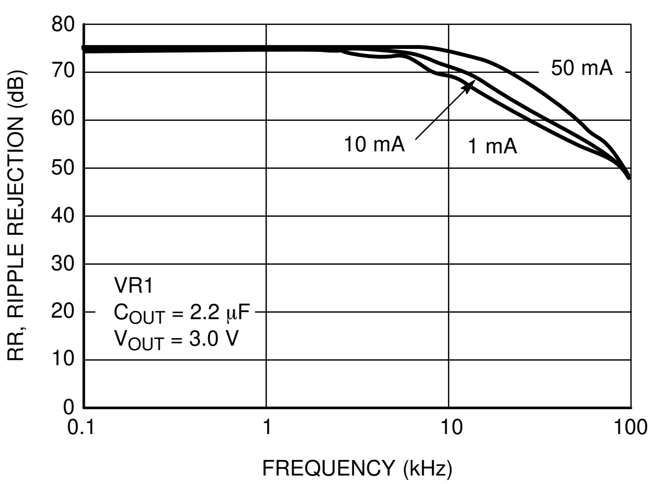


Figure 31. Ripple Rejection vs. Frequency

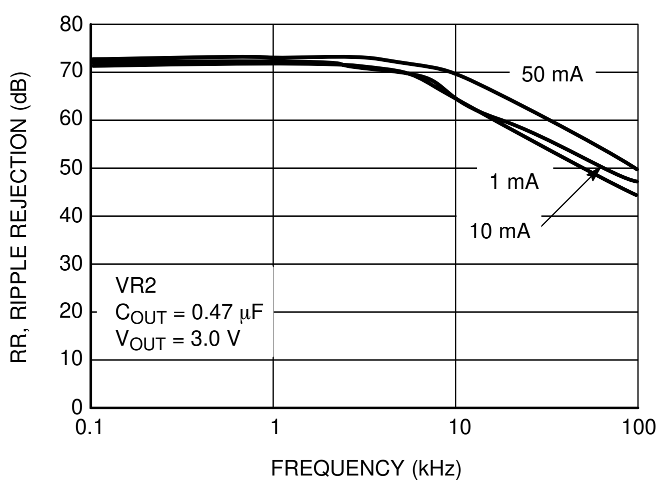


Figure 32. Ripple Rejection vs. Frequency

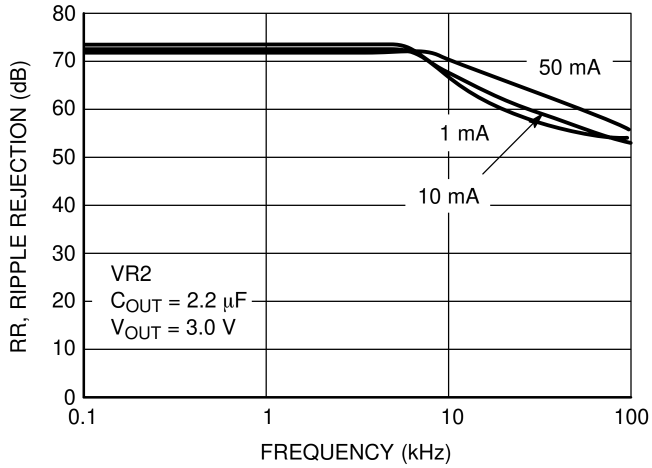


Figure 33. Ripple Rejection vs. Frequency

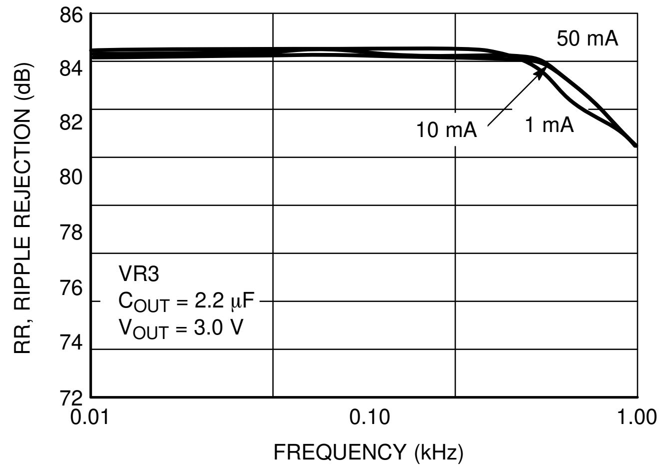


Figure 34. Ripple Rejection vs. Frequency

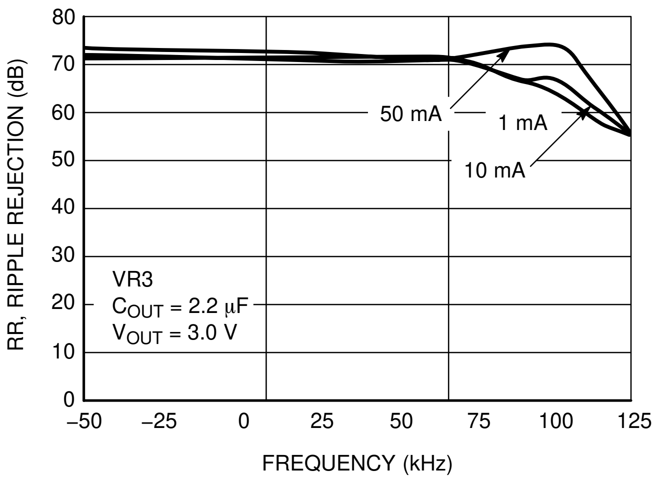


Figure 35. Ripple Rejection vs. Frequency

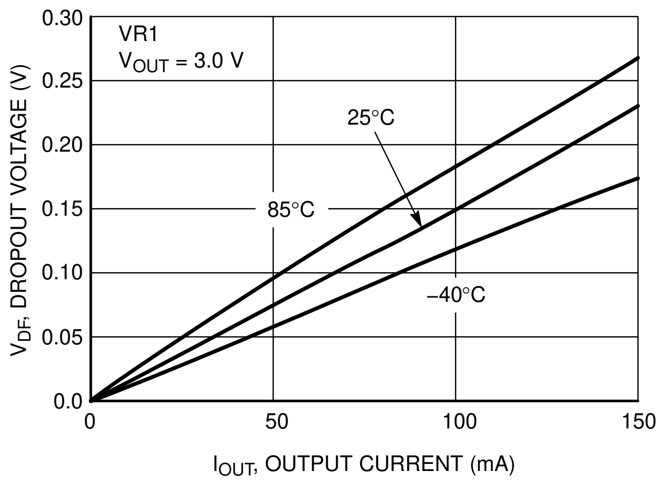


Figure 36. Dropout Voltage vs. Output Current

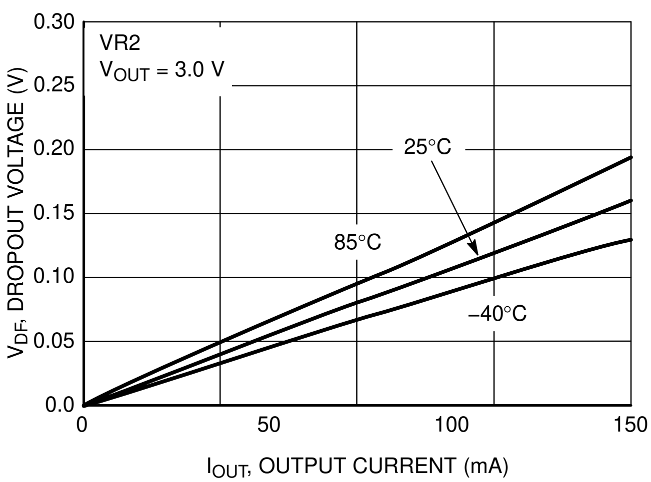


Figure 37. Dropout Voltage vs. Output Current

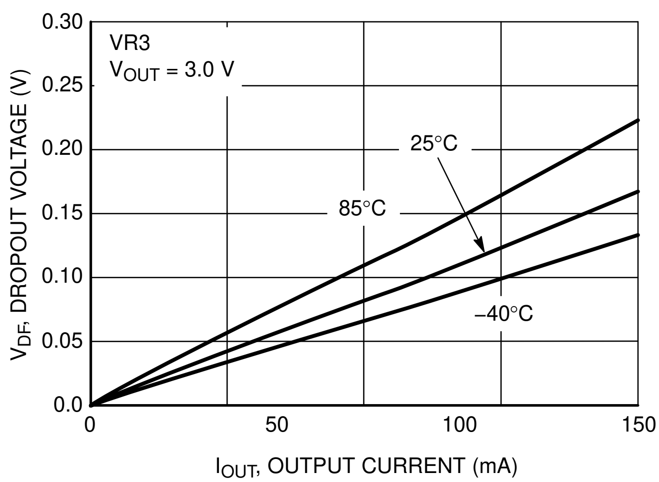


Figure 38. Dropout Voltage vs. Output Current

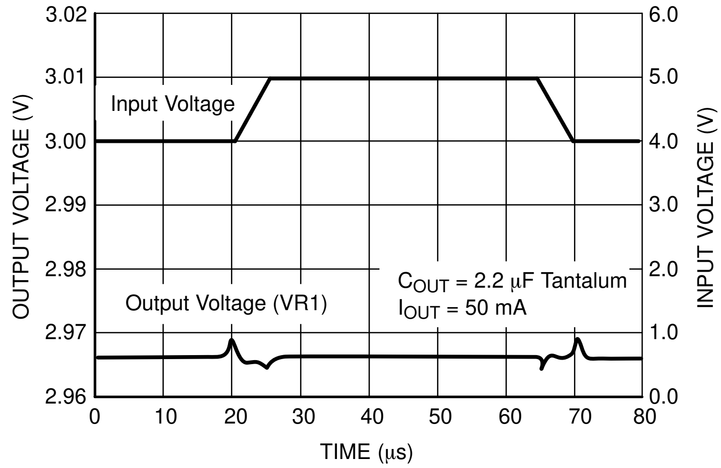


Figure 39. Line Transient Response

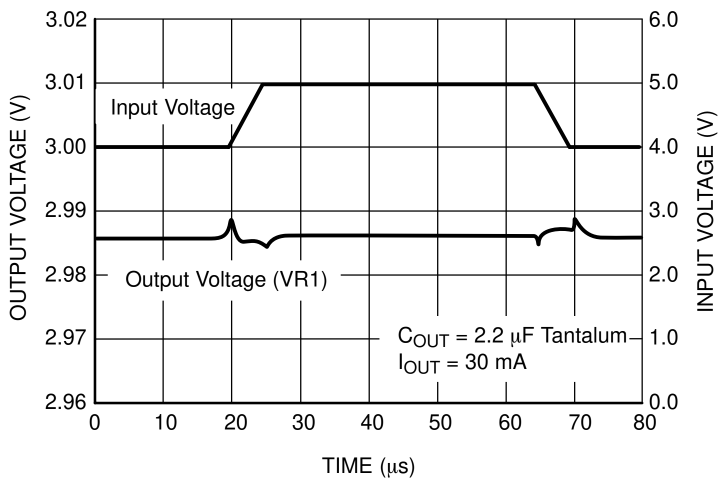


Figure 40. Line Transient Response

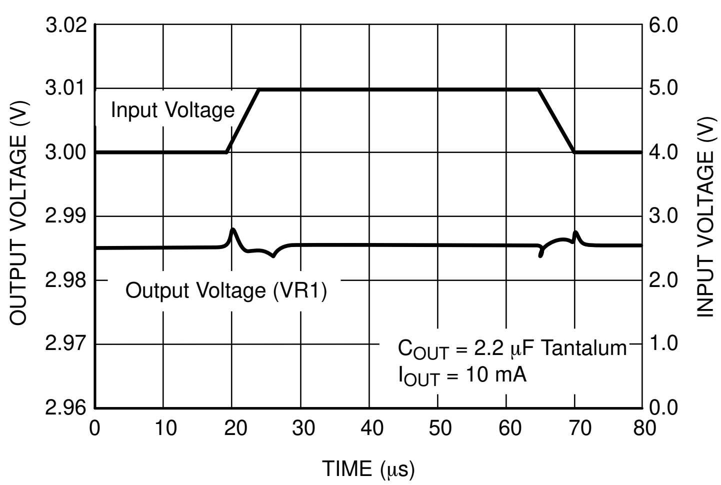


Figure 41. Line Transient Response

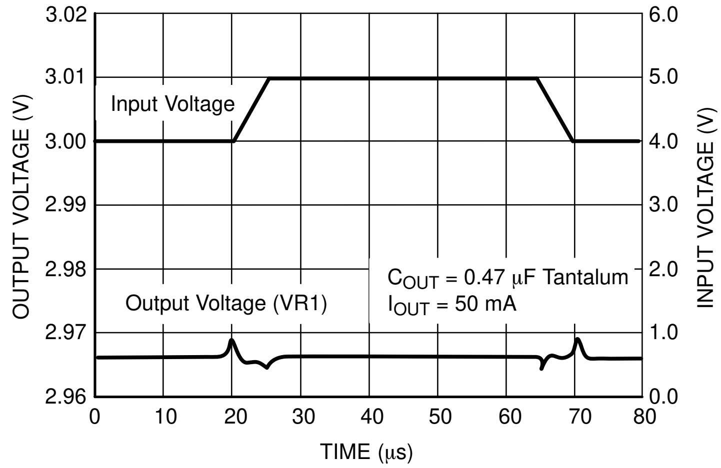


Figure 42. Line Transient Response

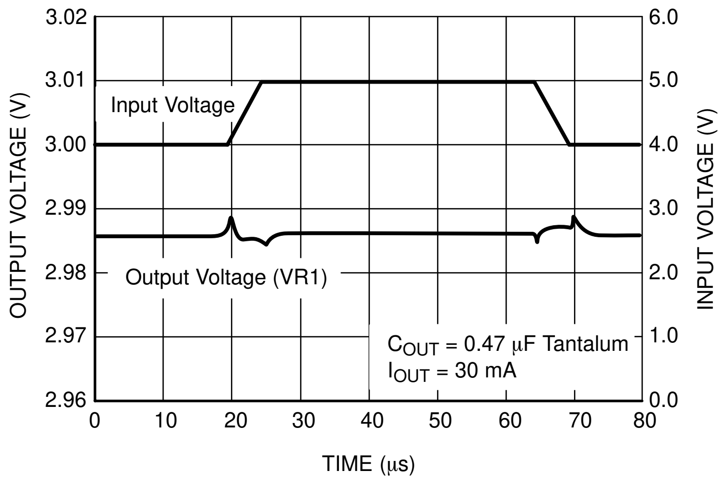


Figure 43. Line Transient Response

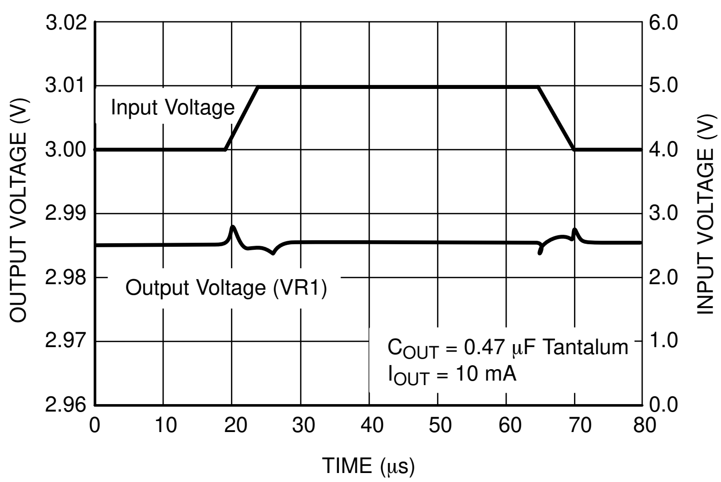


Figure 44. Line Transient Response

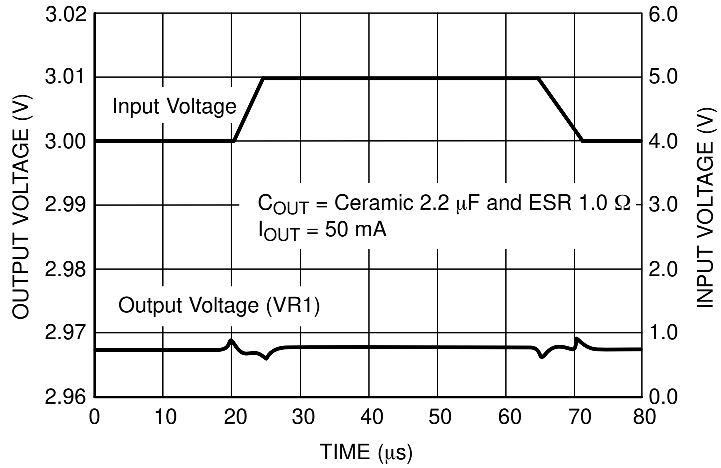


Figure 45. Line Transient Response

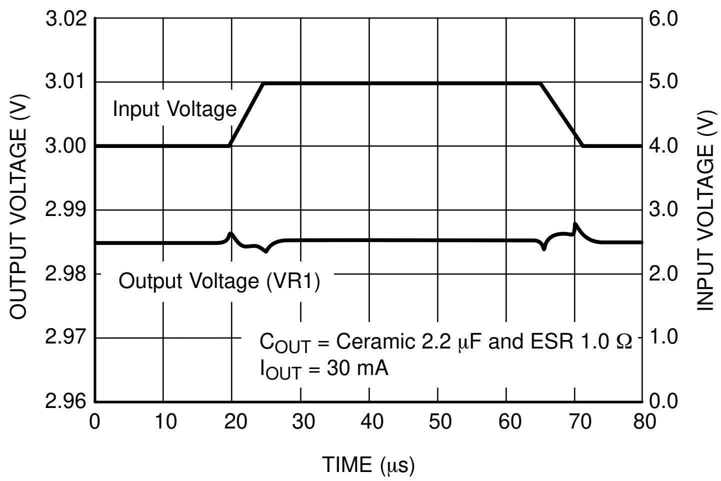


Figure 46. Line Transient Response

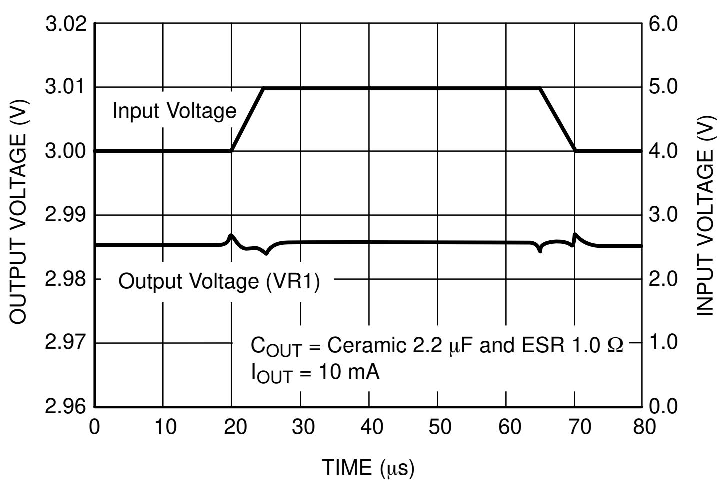


Figure 47. Line Transient Response

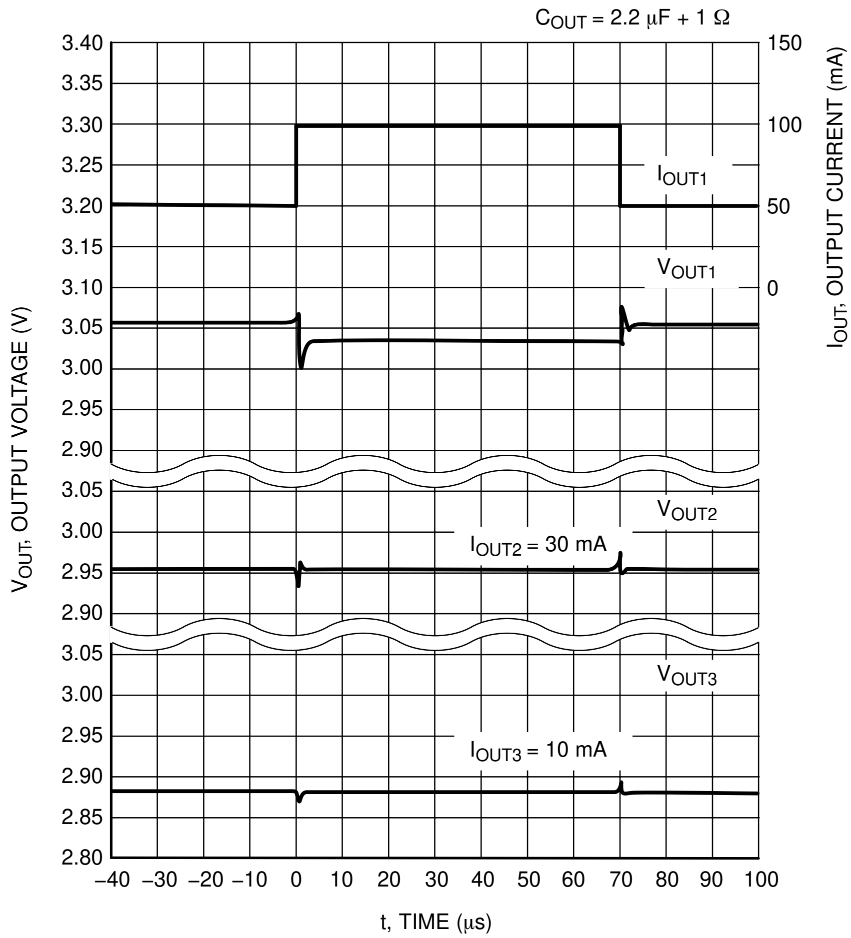


Figure 48. Load Transient Response

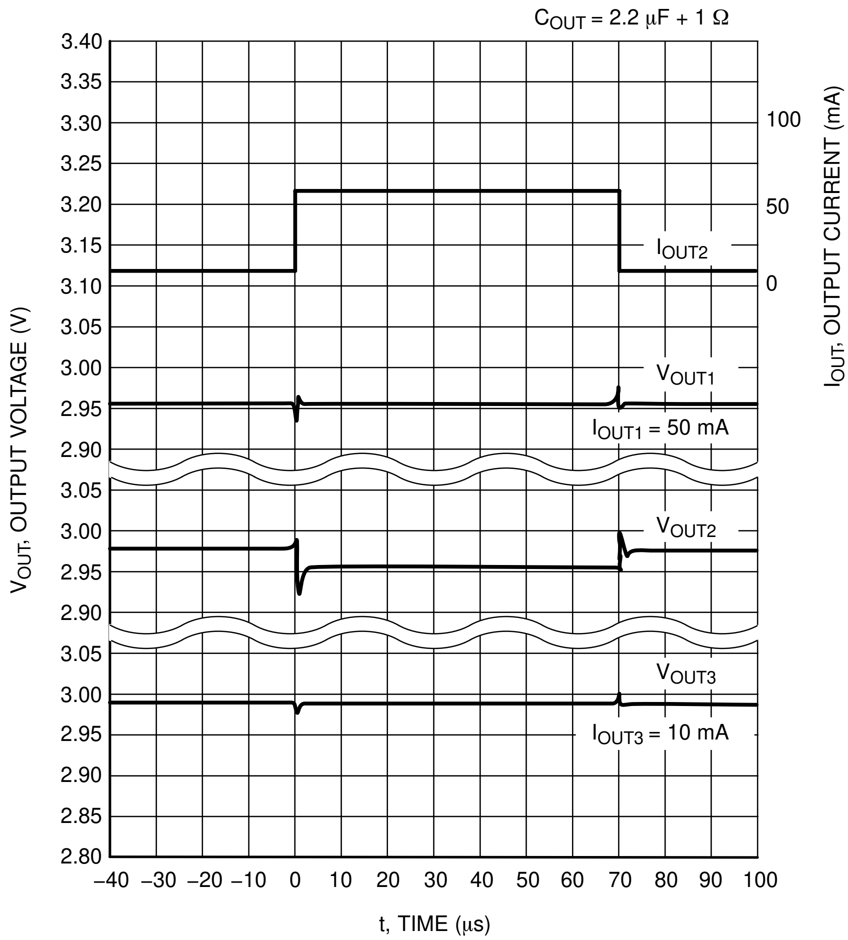


Figure 49. Load Transient Response

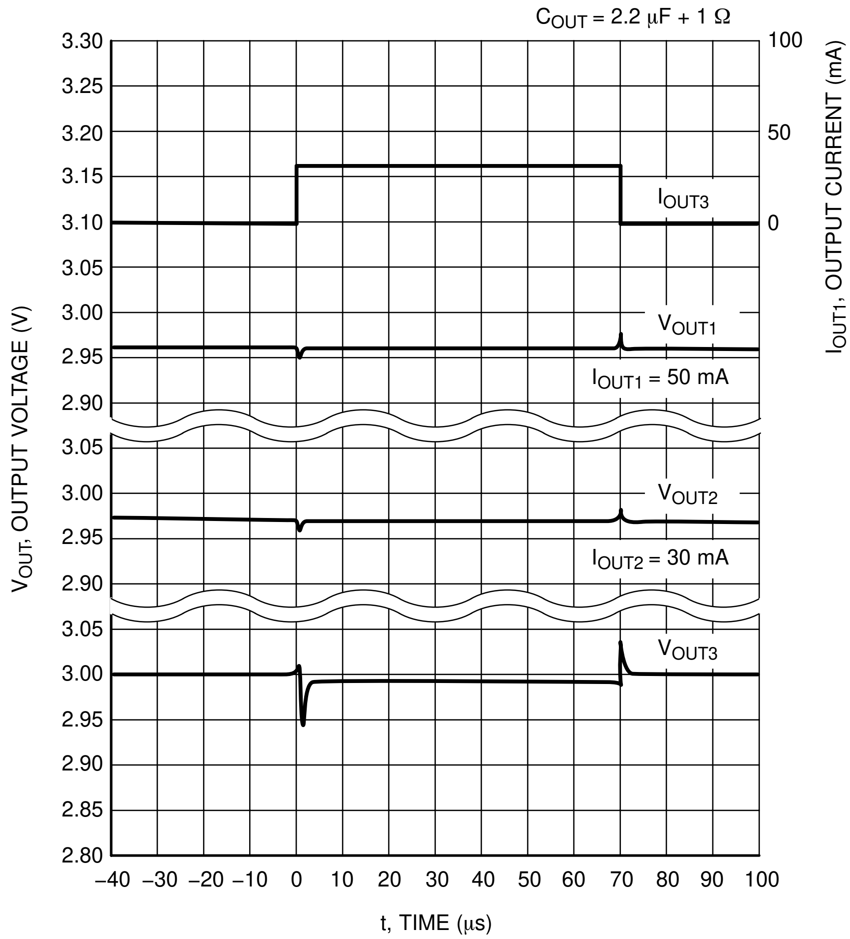


Figure 50. Load Transient Response

Technical Notes

(Pin numbers of the diagram below are applied to NCP4523)

To use this IC with ceramic capacitors, ESR should be set in the range of the following graphs. Test circuit for Noise level measurement is shown below.

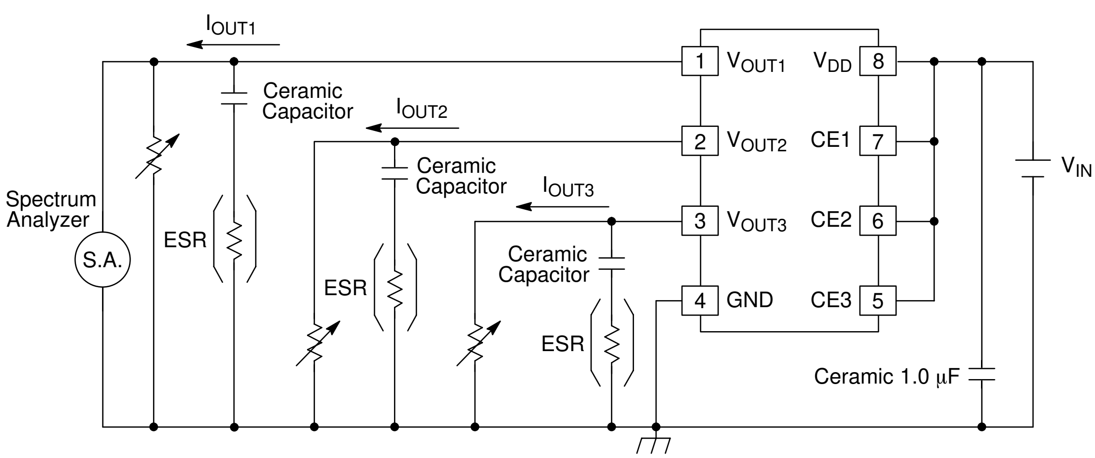


Figure 51.

Noise level is measured with a spectrum analyzer and hatched area shows stable areas of which noise level is approximately equal or less than 40 μV (Avg.). The relation between Load Current (I_{OUT}) and Equivalent Series Resistors (ESR) value of external output capacitor with the stable area is shown below.

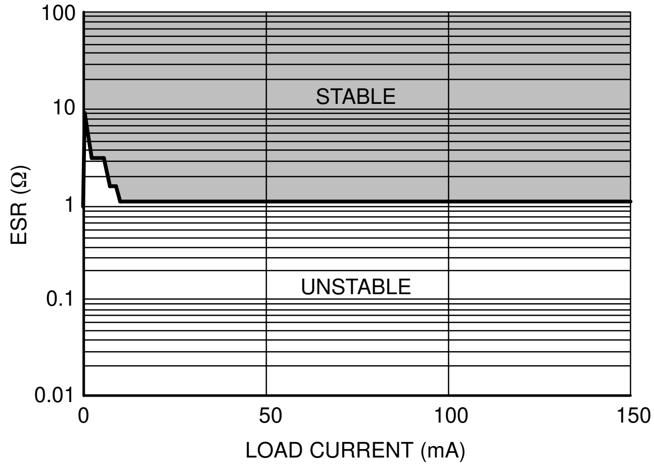


Figure 52. Ceramic Capacitor 1.0 μF

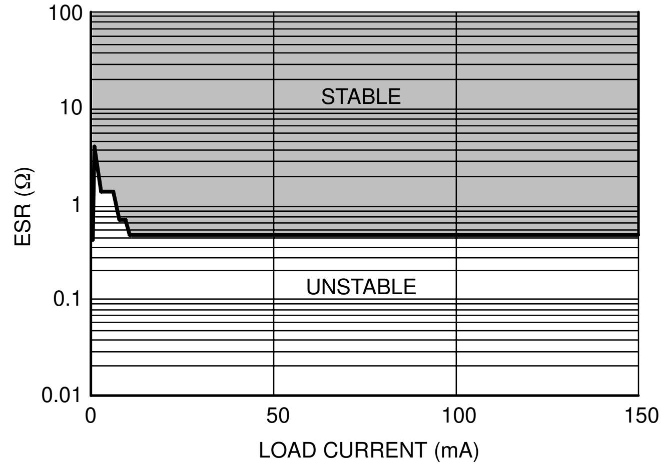


Figure 53. Ceramic Capacitor 2.2 μF

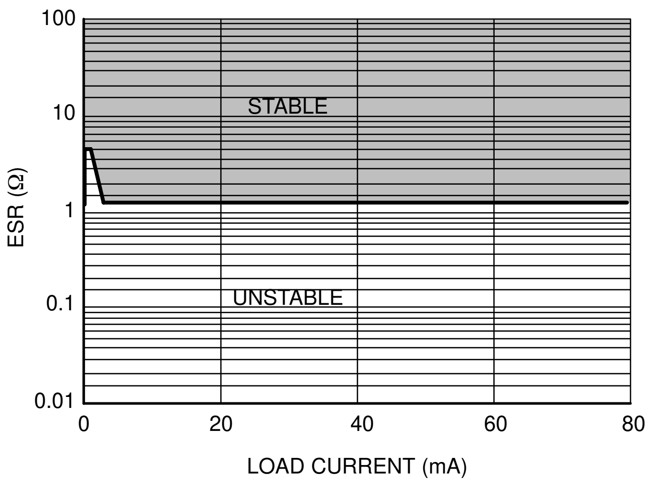


Figure 54. Ceramic Capacitor 1.0 μF

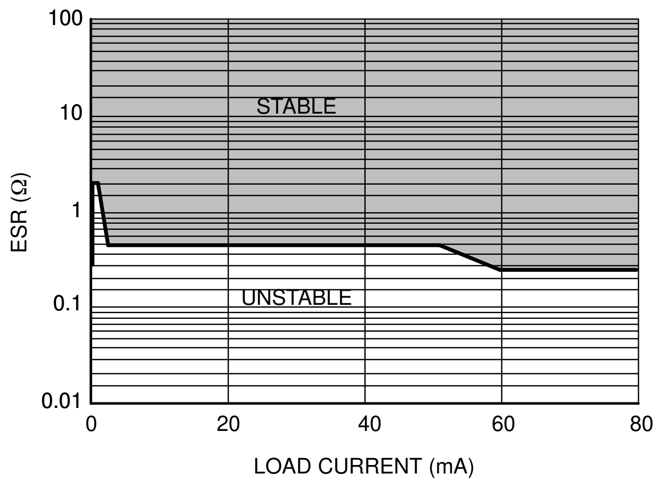


Figure 55. Ceramic Capacitor 2.2 μF

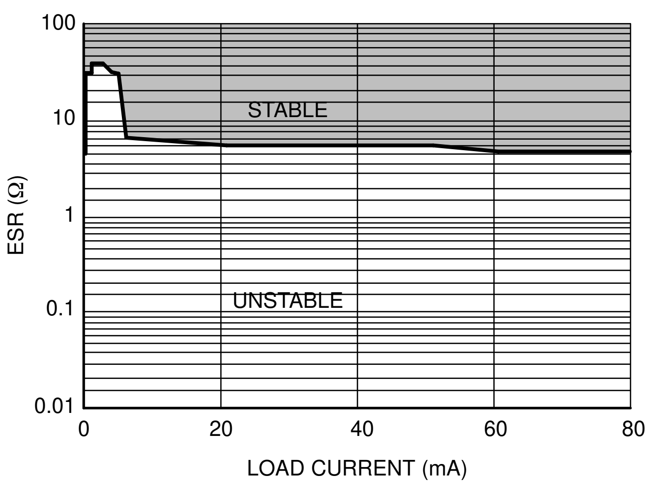


Figure 56. Ceramic Capacitor 1.0 μF

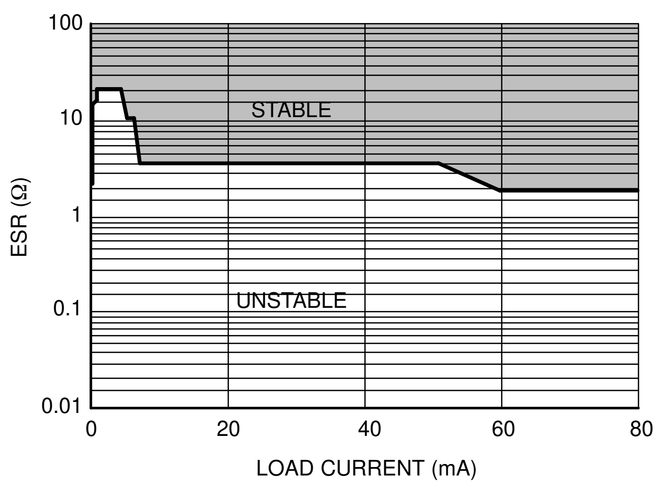


Figure 57. Ceramic Capacitor 2.2 μF

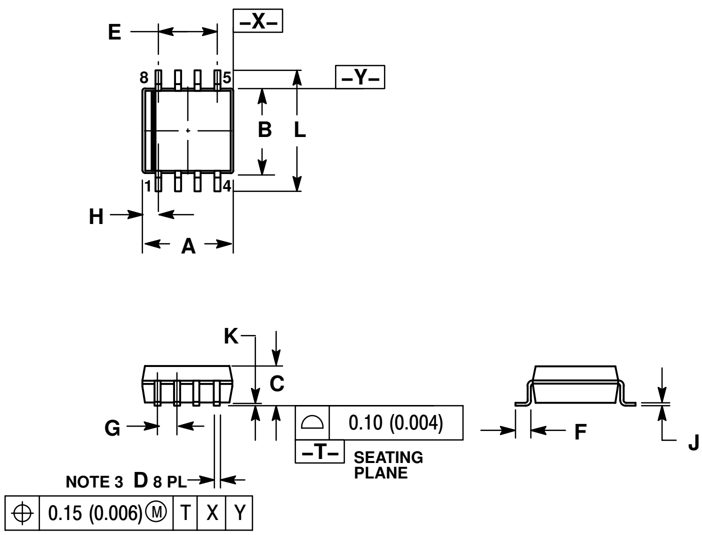
ORDERING INFORMATION

Device	S/N for Voltage Setting	Output Voltage			Marking	Package	Shipping†
		VR1	VR2	VR2	Product Code		
NCP4523G1T1	1	2.8	2.8	2.8	B01A	SSOP−8	3000 Tape and Reel
NCP4523G1T1G	1	2.8	2.8	2.8	B01A	SSOP−8 (Pb−Free)	3000 Tape and Reel
NCP4523G3T1	3	3.0	3.0	3.0	B03A	SSOP−8	3000 Tape and Reel
NCP4523G3T1G	3	3.0	3.0	3.0	B03A	SSOP−8 (Pb−Free)	3000 Tape and Reel
NCP4523G20T1	20	2.35	2.8	2.8	B20A	SSOP−8	3000 Tape and Reel
NCP4523G20T1G	20	2.35	2.8	2.8	B20A	SSOP−8 (Pb−Free)	3000 Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

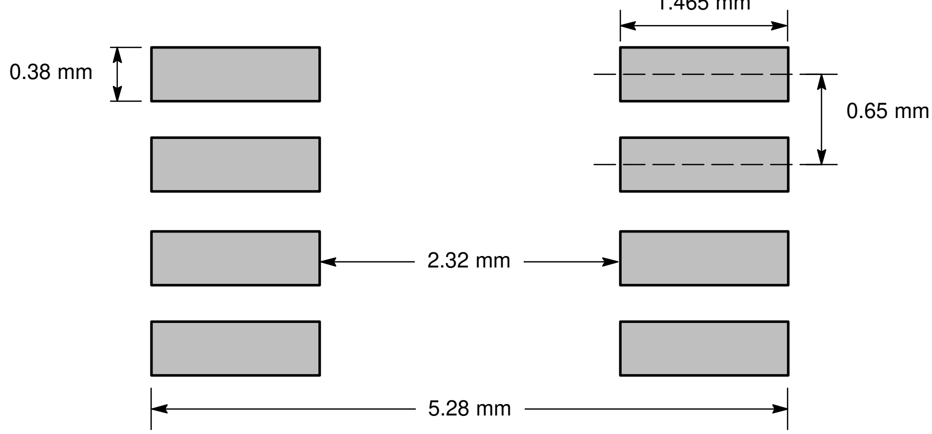
SSOP−8
G SUFFIX
CASE 487−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.106	0.122	2.70	3.10
B	0.102	0.118	2.60	3.00
C	0.039	0.051	1.00	1.30
D	0.004	0.012	0.10	0.30
E	0.073	0.081	1.85	2.05
F	0.012	0.024	0.30	0.60
G	0.026 TYP		0.65 TYP	
H	0.019 TYP		0.475 TYP	
J	0.004	0.006	0.11	0.14
K	0.000	0.008	0.00	0.20
L	0.150	0.165	3.80	4.20

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.