Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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NCP5322A

Two-Phase Buck Controller with Integrated Gate Drivers and 5-Bit DAC

The NCP5322A is a second−generation, two−phase step down controller which incorporates all control functions required to power high performance processors and high current power supplies. Proprietary multi−phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications. Enhanced V^{2}™ control architecture provides the fastest possible transient response, excellent overall regulation, and ease of use. The NCP5322A is a second−generation PWM controller because it optimizes transient response by combining traditional Enhanced V^{2} with an internal PWM ramp and fast−feedback directly from V_{CORE} to the internal PWM comparator. These enhancements provide greater design flexibility, facilitate use and reduce output voltage jitter.

The NCP5322A multi−phase architecture reduces output voltage and input current ripple, allowing for a significant reduction in filter size and inductor values with a corresponding increase in inductor current slew rate. This approach allows a considerable reduction in input and output capacitor requirements, as well as reducing overall solution size and cost.

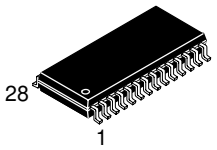
Features

- Enhanced V^{2} Control Method with Internal Ramp
- Internal PWM Ramp
- Fast−Feedback Directly from V_{CORE}
- 5−Bit DAC with 1.0% Accuracy
- Adjustable Output Voltage Positioning
- 4 On−Board Gate Drivers
- 200 kHz to 800 kHz Operation Set by Resistor
- Current Sensed through Buck Inductors or Sense Resistors
- Hiccup Mode Current Limit
- Individual Current Limits for Each Phase
- On−Board Current Sense Amplifiers
- 3.3 V, 1.0 mA Reference Output
- 5.0 V and/or 12 V Operation
- On/Off Control (through Soft Start Pin)
- Power Good Output with Internal Delay
- Pb−Free Packages are Available

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

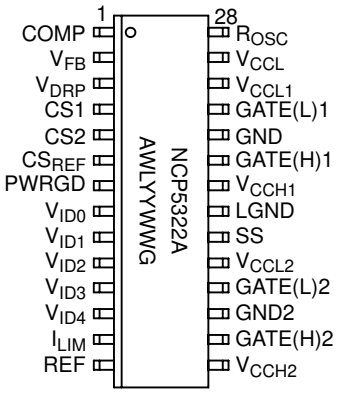
ON Semiconductor®

http://onsemi.com



SO−28L
DW SUFFIX
CASE 751F

PIN CONNECTIONS AND MARKING DIAGRAM

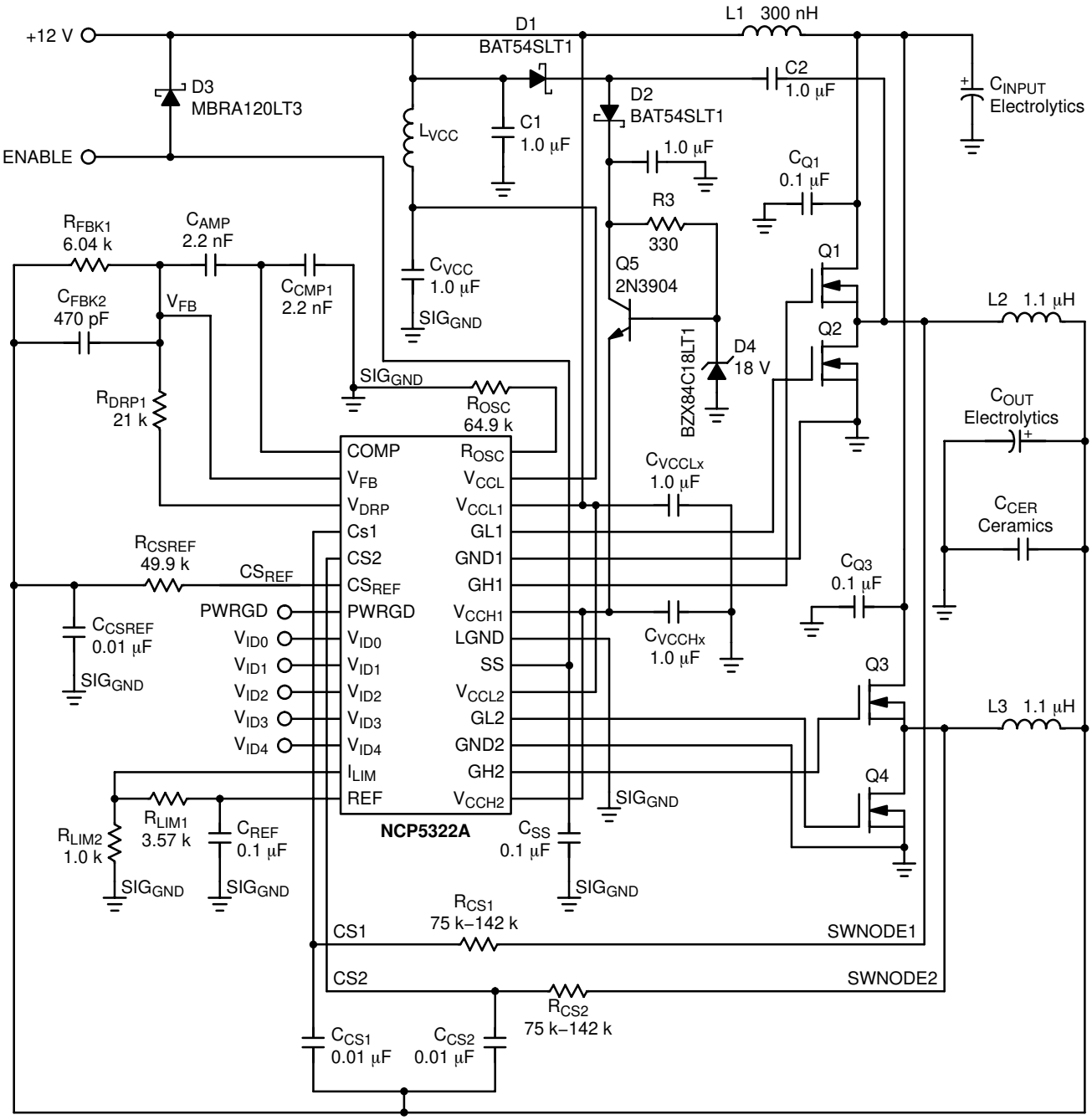


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP5322ADW	SO−28L	26 Units/Rail
NCP5322ADWG	SO−28L (Pb−Free)	26 Units/Rail
NCP5322ADWR2	SO−28L	1000 Tape & Reel
NCP5322ADWR2G	SO−28L (Pb−Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



Recommended Components:

L1: Coiltronics P/N CTX15−14771 or T30−26 core with 3T of #16 AWG

L2: Coiltronics P/N *TBD* or T50−52B with 5T of #16 AWG Bifilar

C_{INPUT}: 3 × Sanyo Oscon 16SP270M (270 μF, 16 V, 4.4 A_{RMS}, 18 mΩ)

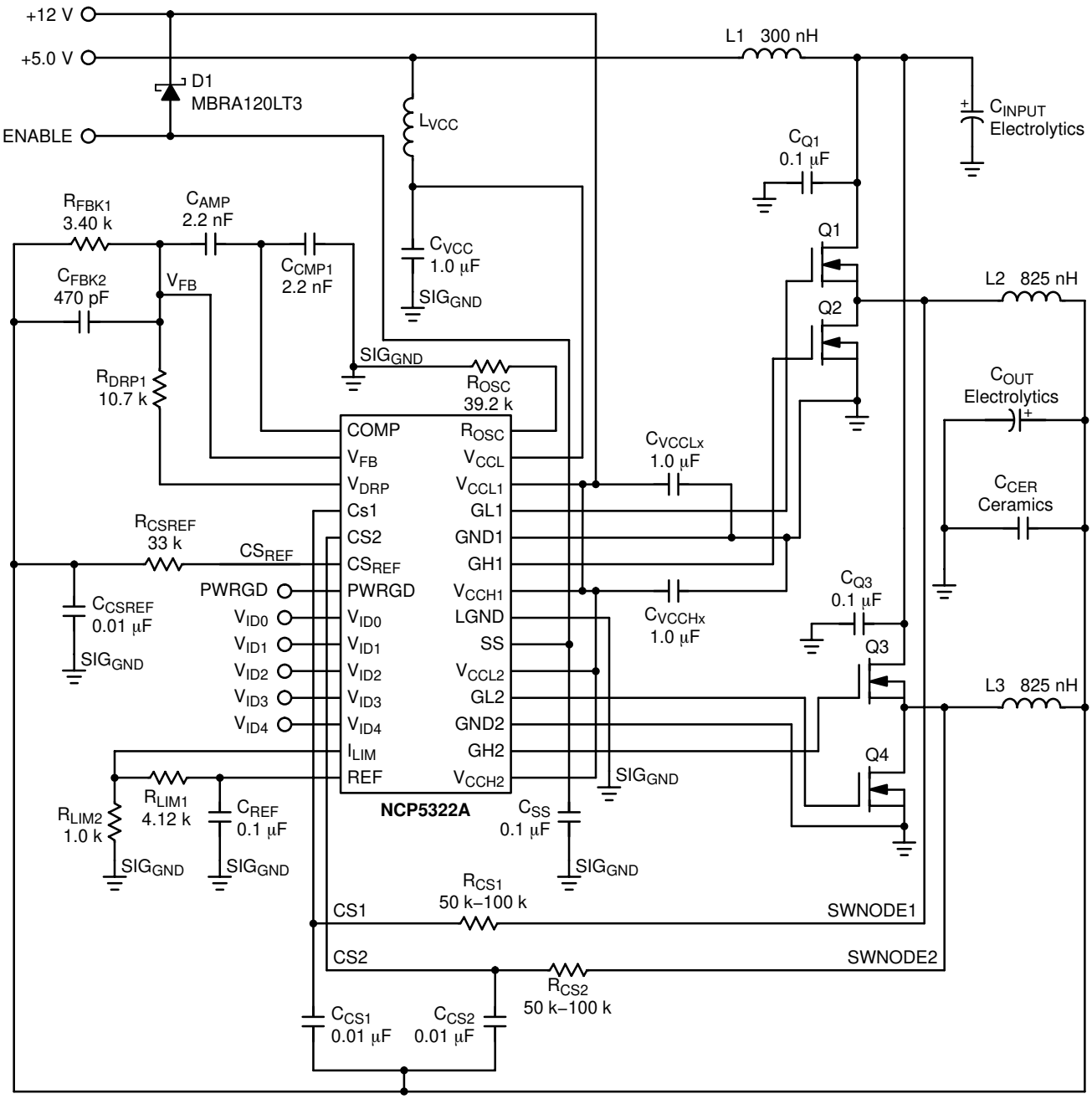
C_{OUT}: 10 × Rubycon 16MBZ1500M10x20 (1500 μF, 16 V, 13 mΩ)
or 8 × Sanyo Oscon 4SP820M (820 μF, 4 V, 12 mΩ)

$C_{CERAMICS}$: 12 × Panasonic ECJ−3YB0J106K (10 μF, 6.3 V)

Q1−Q4: ON Semiconductor NTB85N03 (28 V, 85 A)

L_{VCC}: Murata P/N BLM21P221SG (220 Ω at 100 MHz)

Figure 1. Application Diagram, 12 V Only to 1.6 V at 45 A, 220 kHz



Recommended Components:
L1: Coiltronics P/N CTX15−14771 or T30−26 core with 3T of #16 AWG
L2: Coiltronics P/N CTX22−15401 or T50−52 with 5T of #16 AWG Bifilar
L_{VCC}: Murata P/N BLM21P221SG (220 Ω at 100 MHz)
Q1−Q4: ON Semiconductor NTB85N03 (28 V, 85 A)

Figure 2. Alternate Application Diagram, 5.0 V (with 12 V Bias) to 1.6 V at 45 A, 335 kHz

MAXIMUM RATINGS*

Rating		Value	Unit
Operating Junction Temperature		150	°C
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1): Pb Devices (Note 2): Pb−Free Devices	230 peak 260 Peak	°C
Package Thermal Resistance: Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$		 15 75	 °C/W °C/W
Storage Temperature Range		−65 to +150	°C
ESD Susceptibility (Human Body Model)		2.0	kV
JEDEC Moisture Sensitivity	Pb Devices Pb−Free Devices	Level 1 Level 2	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.
2. 60 second maximum above 217°C.

*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP	6.0 V	−0.3 V	1.0 mA	1.0 mA
V_{FB}	6.0 V	−0.3 V	1.0 mA	1.0 mA
V_{DRP}	6.0 V	−0.3 V	1.0 mA	1.0 mA
CS1, CS2	6.0 V	−0.3 V	1.0 mA	1.0 mA
CS_{REF}	6.0 V	−0.3 V	1.0 mA	1.0 mA
R_{OSC}	6.0 V	−0.3 V	1.0 mA	1.0 mA
PWRGD	6.0 V	−0.3 V	1.0 mA	8.0 mA
VID Pins	6.0 V	−0.3 V	1.0 mA	1.0 mA
I_{LIM}	6.0 V	−0.3 V	1.0 mA	1.0 mA
REF	6.0 V	−0.3 V	1.0 mA	20 mA
SS	6.0 V	−0.3 V	1.0 mA	1.0 mA
V_{CCL}	16 V	−0.3 V	N/A	50 mA
V_{CCHx}	20 V	−0.3 V	N/A	1.5 A for 1.0 μs, 200 mA DC
V_{CCLx}	16 V	−0.3 V	N/A	1.5 A for 1.0 μs, 200 mA DC
GATE(H)x	20 V	−2.0 V for 100 ns, −0.3 V DC	1.5 A for 1.0 μs, 200 mA DC	1.5 A for 1.0 μs, 200 mA DC
GATE(L)x	16 V	−2.0 V for 100 ns, −0.3 V DC	1.5 A for 1.0 μs, 200 mA DC	1.5 A for 1.0 μs, 200 mA DC
GND1, GND2	0.3 V	−0.3 V	2.0 A for 1.0 μs, 200 mA DC	N/A
LGND	0 V	0 V	50 mA	N/A

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; 9.0 V < $V_{CCH1} = V_{CCH2}$ < 20 V; 4.5 V < $V_{CCL} = V_{CCL1} = V_{CCL2}$ < 14 V; C_{GATE} = 3.3 nF, $R_{R(OSC)}$ = 32.4 kΩ, C_{COMP} = 1.0 nF, C_{REF} = 0.1 μF, C_{SS} = 0.1 μF, DAC Code 10000 (1.45 V), C_{VCC} = 1.0 μF; unless otherwise specified.)

Characteristic					Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC									
Accuracy (all codes)					Measure V_{FB} = COMP			± 1.0	%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}					
1	1	1	1	1	–	Fault Mode – Output Off			V
1	1	1	1	0	–	1.089	1.100	1.111	V
1	1	1	0	1	–	1.114	1.125	1.136	V
1	1	1	0	0	–	1.139	1.150	1.162	V
1	1	0	1	1	–	1.163	1.175	1.187	V
1	1	0	1	0	–	1.188	1.200	1.212	V
1	1	0	0	1	–	1.213	1.225	1.237	V
1	1	0	0	0	–	1.238	1.250	1.263	V
1	0	1	1	1	–	1.262	1.275	1.288	V
1	0	1	1	0	–	1.287	1.300	1.313	V
1	0	1	0	1	–	1.312	1.325	1.338	V
1	0	1	0	0	–	1.337	1.350	1.364	V
1	0	0	1	1	–	1.361	1.375	1.389	V
1	0	0	1	0	–	1.386	1.400	1.414	V
1	0	0	0	1	–	1.411	1.425	1.439	V
1	0	0	0	0	–	1.436	1.450	1.465	V
0	1	1	1	1	–	1.460	1.475	1.490	V
0	1	1	1	0	–	1.485	1.500	1.515	V
0	1	1	0	1	–	1.510	1.525	1.540	V
0	1	1	0	0	–	1.535	1.550	1.566	V
0	1	0	1	1	–	1.559	1.575	1.591	V
0	1	0	1	0	–	1.584	1.600	1.616	V
0	1	0	0	1	–	1.609	1.625	1.641	V
0	1	0	0	0	–	1.634	1.650	1.667	V
0	0	1	1	1	–	1.658	1.675	1.692	V
0	0	1	1	0	–	1.683	1.700	1.717	V
0	0	1	0	1	–	1.708	1.725	1.742	V
0	0	1	0	0	–	1.733	1.750	1.768	V
0	0	0	1	1	–	1.757	1.775	1.793	V
0	0	0	1	0	–	1.782	1.800	1.818	V
0	0	0	0	1	–	1.807	1.825	1.843	V
0	0	0	0	0	–	1.832	1.850	1.869	V
Input Threshold					V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	1.00	1.25	1.50	V
Input Pull–up Resistance					V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	25	50	100	kΩ
Pull–up Voltage					–	3.15	3.30	3.45	V

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; 9.0 V < $V_{CCH1} = V_{CCH2}$ < 20 V; 4.5 V < $V_{CCL} = V_{CCL1} = V_{CCL2}$ < 14 V; C_{GATE} = 3.3 nF, $R_{R(OSC)}$ = 32.4 kΩ, C_{COMP} = 1.0 nF, C_{REF} = 0.1 μF, C_{SS} = 0.1 μF, DAC Code 10000 (1.45 V), C_{VCC} = 1.0 μF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Power Good Output					
Power Good Fault Delay	CS_{REF} = DAC to DAC ± 15%	60	120	240	μs
PWRGD Low Voltage	CS_{REF} = 1.0 V, I_{PWRGD} = 4.0 mA	–	0.25	0.40	V
Output Leakage Current	CS_{REF} = 1.45 V, PWRGD = 5.5 V	–	0.1	10	μA
Lower Threshold	–	–15	–12	–9.0	%
Upper Threshold	–	9.0	12	15	%
Voltage Feedback Error Amplifier					
V_{FB} Bias Current	1.0 V < V_{FB} < 1.9 V. Note 3.	9.0	10.3	11.5	μA
COMP Source Current	COMP = 0.5 V to 2.0 V; V_{FB} = 1.8 V; DAC = 00000	15	30	60	μA
COMP Sink Current	COMP = 0.5 V to 2.0 V; V_{FB} = 1.9 V; DAC = 00000	15	30	60	μA
COMP Clamp Voltage	SS = 0.25 V to 2.5 V; V_{FB} = LGND; Measure COMP	–	–	SS Voltage	V
COMP Max Voltage	COMP Open; V_{FB} = 1.8 V; DAC = 00000	2.4	2.7	–	V
COMP Min Voltage	COMP Open; V_{FB} = 1.9 V; DAC = 00000	–	0.1	0.2	V
Transconductance	–10 μA < I_{COMP} < +10 μA	–	32	–	mmho
Output Impedance	–	–	2.5	–	MΩ
Open Loop DC Gain	Note 4.	60	90	–	dB
Unity Gain Bandwidth	0.01 μF COMP Capacitor	–	400	–	kHz
PSRR @ 1.0 kHz	–	–	70	–	dB
Soft Start					
Soft Start Charge Current	0.2 V ≤ SS ≤ 3.0 V	15	30	50	μA
Soft Start Discharge Current	0.2 V ≤ SS ≤ 3.0 V	4.0	7.5	13	μA
Hiccup Mode Charge/Discharge Ratio	–	3.0	4.0	–	–
Soft Start Clamp Voltage	–	3.3	4.0	4.2	V
Soft Start Discharge Threshold Voltage	–	0.20	0.27	0.34	V
PWM Comparators					
Minimum Pulse Width	CS1 = CS2 = CS_{REF}	–	350	475	ns
Channel Start Up Offset	V(CS1) = V(CS2) = V(V_{FB}) = V(CS_{REF}) = 0 V; Measure V(COMP) when GATE(H)1, GATE(H)2, switch high	0.3	0.4	0.5	V
GATE(H) and GATE(L)					
High Voltage (AC)	Measure V_{CCLX} – GATE(L)$_X$ or V_{CCHX} – GATE(H)$_X$. Note 4.	–	0	1.0	V
Low Voltage (AC)	Measure GATE(L)$_X$ or GATE(H)$_X$. Note 4.	–	0	0.5	V
Rise Time GATE(H)$_X$	1.0 V < GATE < 8.0 V; V_{CCHX} = 10 V	–	35	80	ns

3. The V_{FB} Bias Current changes with the value of R_{OSC} per Figure 5.
4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; 9.0 V < $V_{CCH1} = V_{CCH2}$ < 20 V; 4.5 V < $V_{CCL} = V_{CCL1} = V_{CCL2}$ < 14 V; C_{GATE} = 3.3 nF, $R_{R(OSC)}$ = 32.4 kΩ, C_{COMP} = 1.0 nF, C_{REF} = 0.1 μF, C_{SS} = 0.1 μF, DAC Code 10000 (1.45 V), C_{VCC} = 1.0 μF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
GATE(H) and GATE(L)					
Rise Time GATE(L)$_X$	1.0 V < GATE < 8.0 V; V_{CCLX} = 10 V	–	35	80	ns
Fall Time GATE(H)$_X$	8.0 V > GATE > 1.0 V; V_{CCHX} = 10 V	–	35	80	ns
Fall Time GATE(L)$_X$	8.0 V > GATE > 1.0 V; V_{CCLX} = 10 V	–	35	80	ns
GATE(H)x to GATE(L)x Delay	GATE(H)$_X$ < 2.0 V, GATE(L)$_X$ > 2.0 V	30	65	110	ns
GATE(L)x to GATE(H)x Delay	GATE(L)$_X$ < 2.0 V, GATE(H)$_X$ > 2.0 V	30	65	110	ns
GATE Pull−Down	Force 100 μA into GATE with no power applied to V_{CCHX} and V_{CCLX} = 2.0 V.	–	1.2	1.6	V
Oscillator					
Switching Frequency	Measure any phase (R_{OSC} = 32.4 k)	340	400	460	kHz
Switching Frequency	Measure any phase (R_{OSC} = 63.4 k). Note 5.	150	200	250	kHz
Switching Frequency	Measure any phase (R_{OSC} = 16.2 k). Note 5.	600	800	1000	kHz
R_{OSC} Voltage	–	–	1.0	–	V
Phase Delay	–	165	180	195	deg
Adaptive Voltage Positioning					
V_{DRP} Output Voltage to DAC_{OUT} Offset	CS1 = CS2 = CS_{REF}, V_{FB} = COMP Measure V_{DRP} – COMP	−15	–	15	mV
V_{DRP} Operating Voltage Range	Measure V_{DRP} – GND, Note 5.	–	–	2.3	V
Maximum V_{DRP} Voltage	(CS1 = CS2) – CS_{REF} = 50 mV, V_{FB} = COMP, Measure V_{DRP} – COMP	260	330	400	mV
Current Sense Amp to V_{DRP} Gain	–	2.6	3.3	4.0	V/V
Current Sensing and Sharing					
CS1−CS2 Input Bias Current	V(CSx) = V(CS_{REF}) = 0 V	–	0.1	2.0	μA
CS_{REF} Input Bias Current	V(CSx) = V(CS_{REF}) = 0 V	–	0.3	4.0	μA
Current Sense Amplifier Gain	–	3.15	3.5	3.9	V/V
Current Sense Amp Mismatch (The Sum of Gain and Offset Errors.)	0 ≤ (CSx – CS_{REF}) ≤ 50 mV. Note 5.	−5.0	–	5.0	mV
Current Sense Input to I_{LIM} Gain	0.25 V < I_{LIM} < 1.00 V	5.5	6.75	8.5	V/V
Current Limit Filter Slew Rate	–	4.0	10	26	mV/μs
I_{LIM} Operating Voltage Range	Note 5.	–	–	1.3	V
I_{LIM} Bias Current	0 < I_{LIM} < 1.0 V	–	0.1	1.0	μA
Single Phase Pulse−by−Pulse Current Limit	Measure V(CSx) – V(CS_{REF}) that Trips Pulse−by−Pulse Limit	90	105	135	mV
Current Share Amplifier Bandwidth	Note 5.	1.0	–	–	MHz
General Electrical Specifications					
V_{CCL} Operating Current	V_{FB} = COMP (no switching)	–	22	26	mA
V_{CCL1} or V_{CCL2} Operating Current	V_{FB} = COMP (no switching)	–	4.5	5.5	mA

5. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; 9.0 V < V_{CCH1} = V_{CCH2} < 20 V; 4.5 V < V_{CCL} = V_{CCL1} = V_{CCL2} < 14 V; C_{GATE} = 3.3 nF, $R_{R(OSC)}$ = 32.4 kΩ, C_{COMP} = 1.0 nF, C_{REF} = 0.1 μF, C_{SS} = 0.1 μF, DAC Code 10000 (1.45 V), C_{VCC} = 1.0 μF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
General Electrical Specifications					
V_{CCH1} or V_{CCH2} Operating Current	V_{FB} = COMP (no switching)	–	3.2	4.5	mA
V_{CCL} Start Threshold	GATEs switching, Soft Start charging	4.05	4.3	4.5	V
V_{CCL} Stop Threshold	GATEs stop switching, Soft Start discharging	3.75	4.1	4.35	V
V_{CCL} Hysteresis	GATEs not switching, Soft Start not charging	100	200	300	mV
V_{CCH1} Start Threshold	GATEs switching, Soft Start charging	1.8	2.0	2.2	V
V_{CCH1} Stop Threshold	GATEs stop switching, Soft Start discharging	1.55	1.75	1.90	V
V_{CCH1} Hysteresis	GATEs not switching, Soft Start not charging	100	200	300	mV
Reference Output					
V_{REF} Output Voltage	0 mA < I(V_{REF}) < 1.0 mA	3.2	3.3	3.4	V
Internal Ramp					
Ramp Height @ 50% PWM Duty−Cycle	CS1 = CS2 = CS_{REF}.	–	125	–	mV

PACKAGE PIN DESCRIPTION

PACKAGE PIN # SO−28L	PIN SYMBOL	FUNCTION
1	COMP	Output of the error amplifier and input for the PWM comparators.
2	V_{FB}	Voltage Feedback Pin. To use Adaptive Voltage Positioning (AVP) select an offset voltage at light load and connect a resistor between V_{FB} and V_{OUT}. The input current of the V_{FB} pin and the resistor value determine output voltage offset for zero output current. Short V_{FB} to V_{OUT} for no AVP.
3	V_{DRP}	Current sense output for AVP. The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to V_{FB} to set amount AVP or leave this pin open for no AVP. This pin's maximum working voltage is 2.3 Vdc.
4−5	CS1−CS2	Current sense inputs. Connect current sense network for the corresponding phase to each input. The input voltages to these pins must be kept within 105 mV of CS_{REF} or pulse−by−pulse current limit will be tripped.
6	CS_{REF}	Reference for Current Sense Amplifiers, input to the Power Good comparators, and fast feedback connection to the PWM comparator. To balance input offset voltages between the inverting and noninverting inputs of the Current Sense Amplifiers, connect a resistor between CS_{REF} and the output voltage. The value should be 1/3 of the value of the resistors connected to the CSx pins. The input voltage to this pin must not exceed the maximum DAC (VID) setting by more than 100 mV or the internal PWM comparator may saturate.
7	PWRGD	Power Good Output. Open collector output goes low when CS_{REF} (V_{OUT}) is out of regulation.
8−12	V_{ID4}−V_{ID0}	Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open.

PACKAGE PIN DESCRIPTION (continued)

PACKAGE PIN # SO−28L	PIN SYMBOL	FUNCTION
13	I_{LIM}	Sets threshold for current limit. Connect to reference through a resistive divider. This pin's maximum working voltage is 1.3 Vdc.
14	REF	Reference output. Decouple with 0.1 μF to LGND.
15	V_{CCH2}	Power for GATE(H)2.
16	GATE(H)2	High side driver #2.
17	GND2	Return for #2 drivers.
18	GATE(L)2	Low side driver #2.
19	V_{CCL2}	Power for GATE(L)2.
20	SS	Soft Start capacitor pin. The Soft Start capacitor controls both Soft Start time and hiccup mode frequency. The COMP pin is clamped below Soft Start during Start−Up and hiccup mode.
21	LGND	Return for internal control circuits and IC substrate connection.
22	V_{CCH1}	Power for GATE(H)1. UVLO Sense for High Side Driver supply connects to this pin.
23	GATE(H)1	High side driver #1.
24	GND1	Return #1 drivers.
25	GATE(L)1	Low side driver #1.
26	V_{CCL1}	Power for GATE(L)1.
27	V_{CCL}	Power for internal control circuits. UVLO Sense for Logic connects to this pin.
28	R_{OSC}	A resistor from this pin to ground sets operating frequency and V_{FB} bias current.

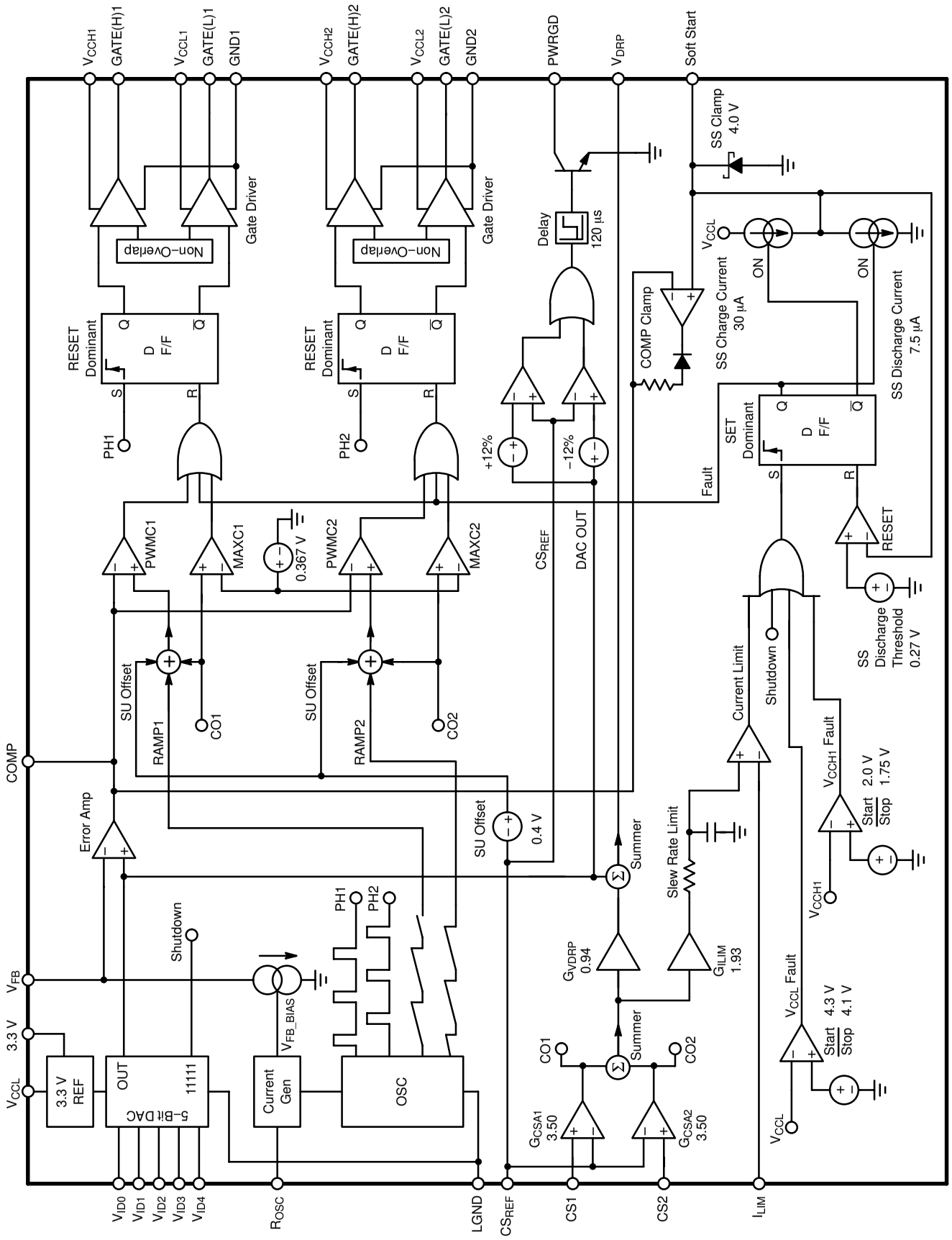


Figure 3. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

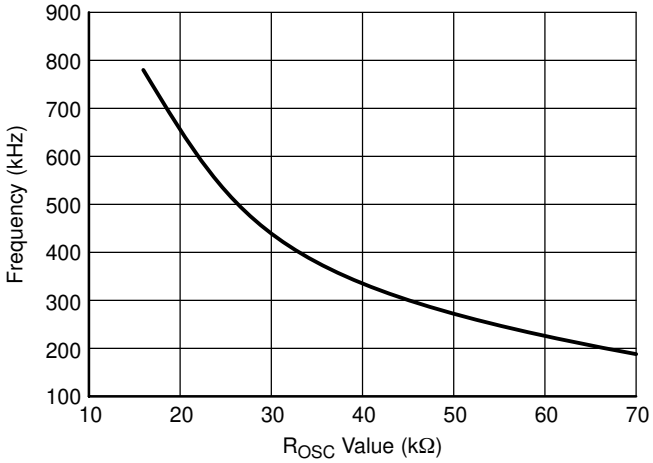


Figure 4. Oscillator Frequency vs. R_{OSC} Value

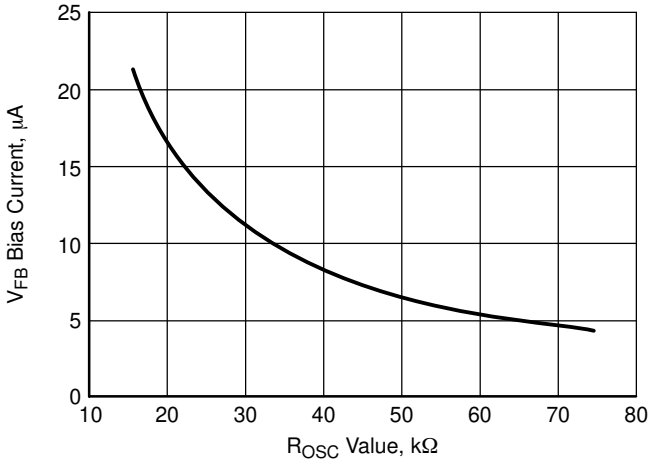


Figure 5. V_{FB} Bias Current vs. R_{OSC} Value

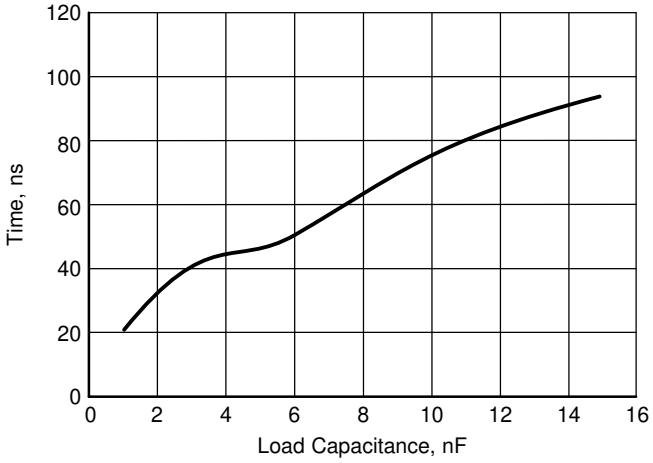


Figure 6. GATE(H) Rise Time vs. Load Capacitance Measured from 1.0 V to 4.0 V with V_{CC} at 5.0 V

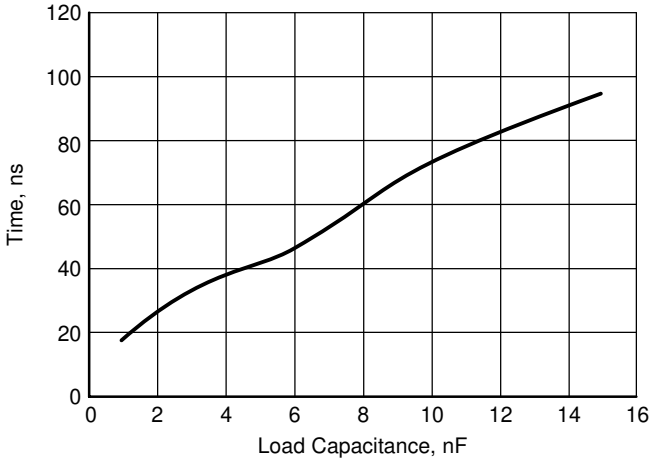


Figure 7. GATE(H) Fall Time vs. Load Capacitance Measured from 4.0 V to 1.0 V with V_{CC} at 5.0 V

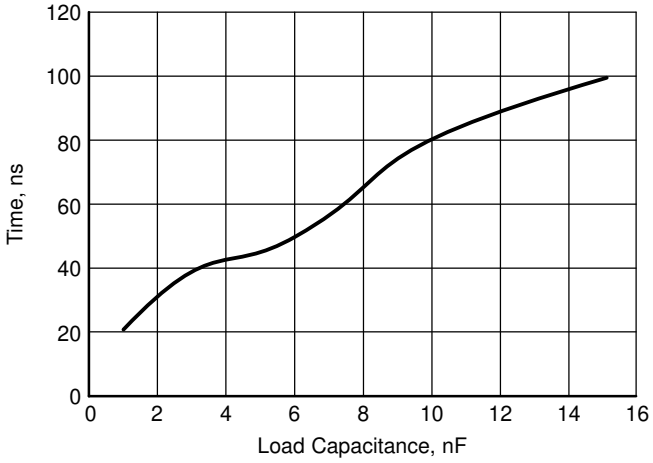


Figure 8. GATE(L) Rise Time vs. Load Capacitance Measured from 1.0 V to 4.0 V with V_{CC} at 5.0 V

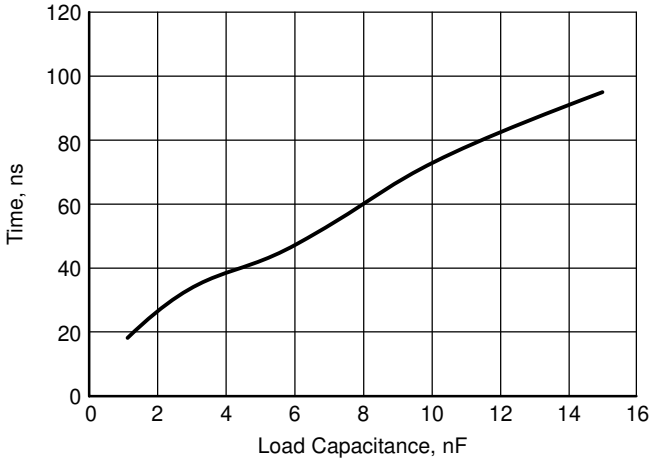


Figure 9. GATE(L) Fall Time vs. Load Capacitance Measured from 4.0 V to 1.0 V with V_{CC} at 5.0 V

APPLICATIONS INFORMATION

Overview

The NCP5322A DC/DC controller from ON Semiconductor was developed using the Enhanced V^2 topology to meet requirements of low voltage, high current loads with fast transient requirements. Enhanced V^2 combines the original V^2 topology with peak current−mode control for fast transient response and current sensing capability. The addition of an internal PWM ramp and implementation of fast−feedback directly from V_{CORE} has improved transient response and simplified design. The NCP5322A includes Power Good (PWRGD) and MOSFET gate drivers to provide a "fully integrated solution" to simplify design, minimize circuit board area, and reduce overall system cost.

Two advantages of a multi−phase converter over a single−phase converter are current sharing and increased apparent output frequency. Current sharing allows the designer to use less inductance in each phase than would be required in a single−phase converter. The smaller inductor will produce larger ripple currents but the total per phase power dissipation is reduced because the RMS current is lower. Transient response is improved because the control loop will measure and adjust the current faster in a smaller output inductor. Increased apparent output frequency is desirable because the off time and the ripple voltage of the two−phase converter will be less than that of a single−phase converter.

Fixed Frequency Multi−Phase Control

In a multi−phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The NCP5322A controller uses two−phase, fixed frequency, Enhanced V^2 architecture to measure and control currents in individual phases. Each phase is delayed 180° from the previous phase. Normally, GATE(H) transitions to a high voltage at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal, the internal ramp and the output voltage ripple trip the PWM comparator and bring GATE(H) low. Once GATE(H) goes low, it will remain low until the beginning of the next oscillator cycle. While GATE(H) is high, the Enhanced V^2 loop will respond to line and load variations. On the other hand, once GATE(H) is low, the loop can not respond until the beginning of the next PWM cycle. Therefore, constant frequency Enhanced V^2 will typically respond to disturbances within the off−time of the converter.

The Enhanced V^2 architecture measures and adjusts the output current in each phase. An additional input (CSn) for inductor current information has been added to the V^2 loop for each phase as shown in Figure 10. The triangular inductor current is measured differentially across RS, amplified by CSA and summed with the Channel Startup Offset, the Internal Ramp, and the Output Voltage at the non−inverting input of the PWM comparator. The purpose of the Internal Ramp is to compensate for propagation delays in the NCP5322A. This provides greater design flexibility by allowing smaller external ramps, lower minimum pulse widths, higher frequency operation, and PWM duty cycles above 50% without external slope compensation. As the sum of the inductor current and the internal ramp increase, the voltage on the positive pin of the PWM comparator rises and terminates the PWM cycle. If the inductor starts a cycle with higher current, the PWM cycle will terminate earlier providing negative feedback. The NCP5322A provides a CSn input for each phase, but the CS_{REF} and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same CS_{REF} and COMP pins, so that a phase with a larger current signal will turn off earlier than a phase with a smaller current signal.

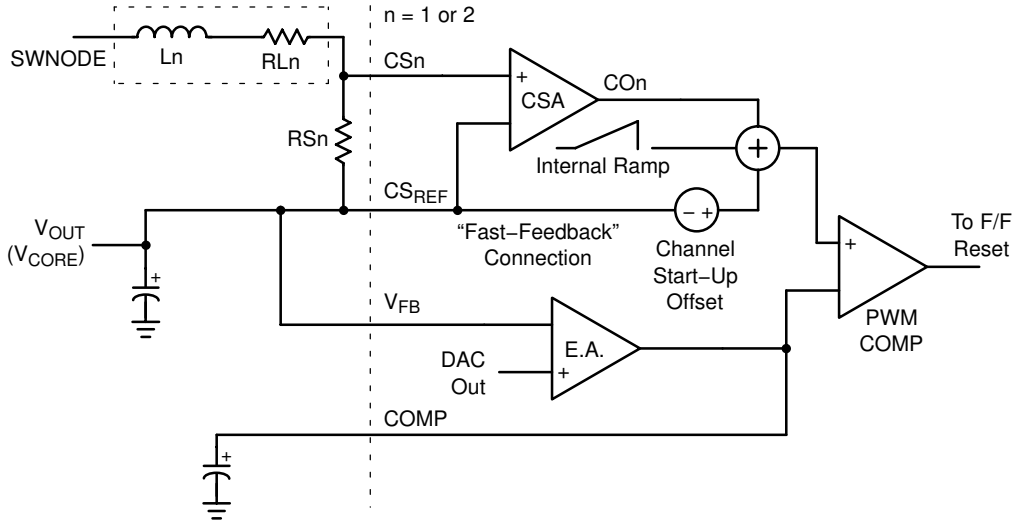


Figure 10. Enhanced V^2 Control Employing Resistive Current Sensing and Additional Internal Ramp

Enhanced V^2 responds to disturbances in V_{CORE} by employing both "slow" and "fast" voltage regulation. The internal error amplifier performs the slow regulation. Depending on the gain and frequency compensation set by the amplifier's external components, the error amplifier will typically begin to ramp its output to react to changes in the output voltage in 1−2 PWM cycles. Fast voltage feedback is implemented by a direct connection from V_{CORE} to the non−inverting pin of the PWM comparator via the summation with the inductor current, internal ramp, and Offset. A rapid increase in load current will produce a negative offset at V_{CORE} and at the output of the summer. This will cause the PWM duty cycle to increase almost instantly. Fast feedback will typically adjust the PWM duty cycle in 1 PWM cycle.

As shown in Figure 10, an internal ramp (nominally 125 mV at a 50% duty cycle) is added to the inductor current ramp at the positive terminal of the PWM comparator. This additional ramp compensates for propagation time delays from the current sense amplifier (CSA), the PWM comparator, and the MOSFET gate drivers. As a result, the minimum ON time of the controller is reduced and lower duty cycles may be achieved at higher frequencies. Also, the additional ramp reduces the reliance on the inductor current ramp and allows greater flexibility when choosing the output inductor and the $R_{CSn}C_{CSn}$ (n = 1 or 2) time constant of the feedback components from V_{CORE} to the CSn pin.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. When the average output current is zero, the COMP pin will be:

$$V_{COMP} = V_{OUT} @ 0\ A + Channel\_Startup\_Offset + Int\_Ramp + G_{CSA} \cdot Ext\_Ramp/2$$

Int_Ramp is the "partial" internal ramp value at the corresponding duty cycle, Ext_Ramp is the peak−to−peak external steady−state ramp at 0 A, G_{CSA} is the Current Sense Amplifier Gain (nominally 3.5 V/V), and the Channel Startup Offset is typically 0.40 V. The magnitude of the Ext_Ramp can be calculated from:

$$Ext\_Ramp = D \cdot (V_{IN} - V_{OUT})/(R_{CSn} \cdot C_{CSn} \cdot f_{SW})$$

For example, if V_{OUT} at 0 A is set to 1.630 V with AVP and the input voltage is 12.0 V, the duty cycle (D) will be 1.630/12.0 or 13.6%. Int_Ramp will be 125 mV • 13.6/50 = 34 mV. Realistic values for R_{CSn}, C_{CSn} and f_{SW} are 60 kΩ, 0.01 μF, and 220 kHz − using these and the previously mentioned formula, Ext_Ramp will be 10.6 mV.

$$V_{COMP} = 1.630\ V + 0.40\ V + 34\ mV + 3.5\ V/V \cdot 10.6\ mV/2 = 2.083\ Vdc.$$

If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as:

$$\Delta V = R_S \cdot G_{CSA} \cdot \Delta I_{OUT}.$$

The single−phase power stage output impedance is:

$$Single\ Stage\ Impedance = \Delta V_{OUT}/\Delta I_{OUT} = R_S \cdot G_{CSA}$$

The multi−phase power stage output impedance is the single−phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few microseconds of a transient before the feedback loop has repositioned the COMP pin.

The peak output current can be calculated from:

$$I_{OUT,PEAK} = (V_{COMP} - V_{OUT} - Offset)/(R_S \cdot G_{CSA})$$

Figure 11 shows the step response of the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides a portion of the PWM ramp through the Current Sense Amplifier. The PWM cycle ends when the sum of the current ramp, the "partial" internal ramp voltage signal and Offset exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the V_{FB} pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the average current signal level (CSn output) is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.

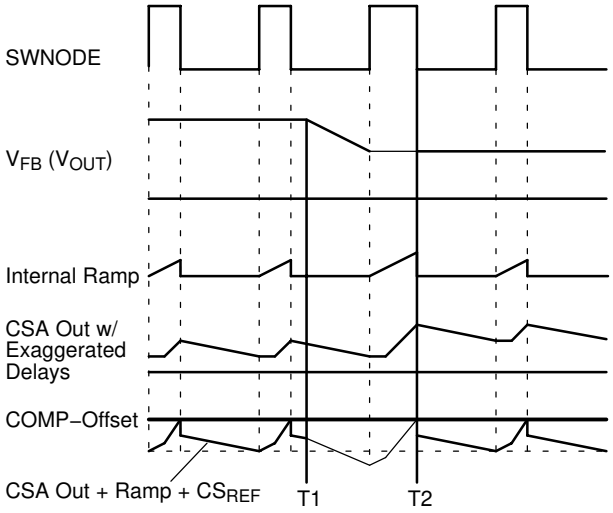


Figure 11. Open Loop Operation

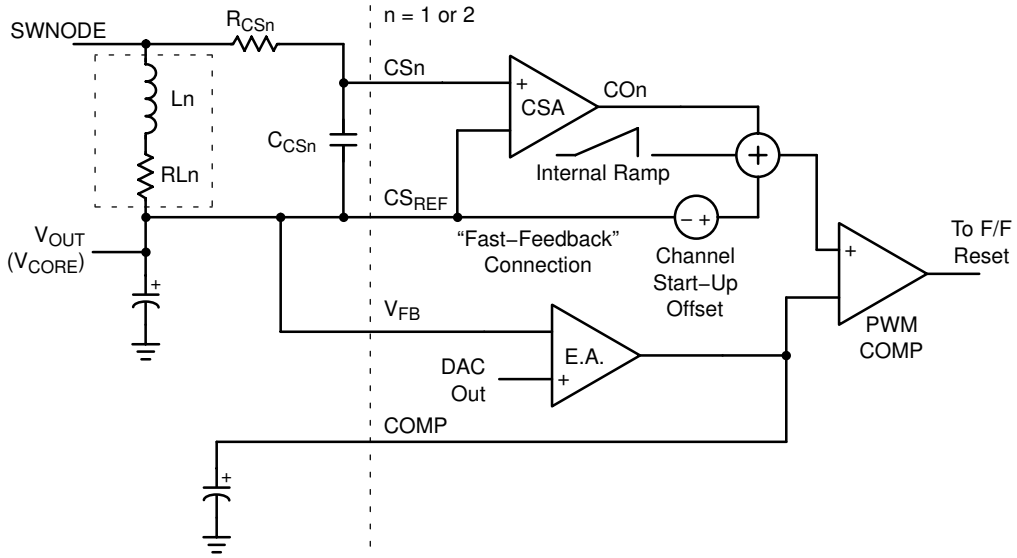


Figure 12. Enhanced V^2 Control Employing Lossless Inductive Current Sensing and Internal Ramp

Inductive Current Sensing

For lossless sensing, current can be sensed across the inductor as shown in Figure 12. In the diagram, L is the output inductance and R_L is the inherent inductor resistance. To compensate the current sense signal, the values of R_{CSn} and C_{CSn} are chosen so that $L/R_L = R_{CSn} \bullet C_{CSn}$. If this criteria is met, the current sense signal will be the same shape as the inductor current and the voltage signal at CSn will represent the instantaneous value of inductor current. Also, the circuit can be analyzed as if a sense resistor of value R_L was used as a sense resistor (R_S).

When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of 0.39% per °C. The increase in winding resistance at higher temperatures should be considered when setting the I_{LIM} threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 10.

Current Sharing Accuracy

Printed circuit board (PCB) traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at relatively the same point for each phase and the connection to the CS_{REF} pin should be made so that no phase is favored. In some cases, especially with inductive sensing, resistance of the PCB can be useful for increasing the current sense resistance. The total current sense resistance used for calculations must include any PCB trace resistance between the CSn input and the CS_{REF} input that carries inductor current.

Current Sense Amplifier (CSA) input mismatch and the value of the current sense component will determine the accuracy of the current sharing between phases. The worst case Current Sense Amplifier input mismatch is ±5.0 mV and will typically be within 3.0 mV. The difference in peak currents between phases will be the CSA input mismatch divided by the current sense resistance. If all current sense components are of equal resistance a 3.0 mV mismatch with a 2.0 mΩ sense resistance will produce a 1.5 A difference in current between phases.

External Ramp Size and Current Sensing

The internal ramp allows flexibility of current sense time constant. Typically, the current sense $R_{CSn} \bullet C_{CSn}$ time constant (n = 1 or 2) should be equal to or slower than the inductor's time constant. If RC is chosen to be smaller (faster) than L/R_L, the AC or transient portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $R_{CSn} \bullet C_{CSn}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $R_{CSn} \bullet C_{CSn}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During a positive current transient, the COMP pin will be required to undershoot in response to the current signal in order to maintain the output voltage. Similarly, the V_{DRP} signal will overshoot which will produce too much transient droop in the output voltage. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.

The waveforms in Figure 13 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of L = 500 nH, R_L = 1.6 mΩ, R_{CSn} = 20 k and C_{CSn} = 0.01 μF. For ideal current signal compensation the value of R_{CSn} should be 31 kΩ. Due to the faster than ideal RC time constant there is an overshoot of 50% and the overshoot decays with a 200 μs time constant. With this compensation the I_{LIM} pin threshold must be set more than 50% above the full load current to avoid triggering hiccup mode during a large output load step.

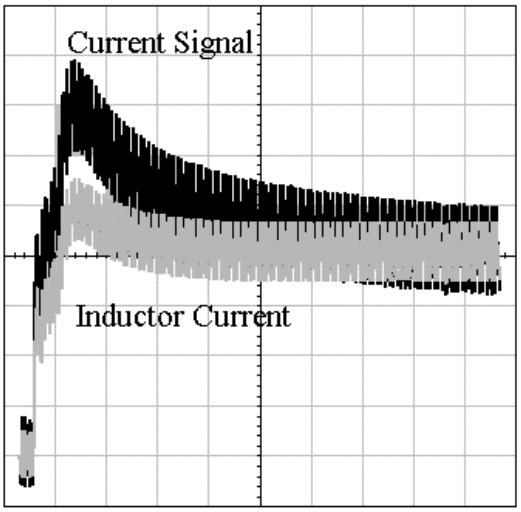


Figure 13. Inductive Sensing Waveform During a Load Step with Fast RC Time Constant (50 μs/div)

Current Limit

Two levels of overcurrent protection are provided. First, if the voltage on the Current Sense pins (either CS1 or CS2) exceeds CS_{REF} by more than a fixed threshold (Single Pulse Current Limit), the PWM comparator is turned off. This provides fast peak current protection for individual phases. Second, the individual phase currents are summed and low−pass filtered to compare an averaged current signal to a user adjustable voltage on the I_{LIM} pin. If the I_{LIM} voltage is exceeded, the fault latch trips and the Soft Start capacitor is discharged until the Soft−Start pin reaches 0.27 V. Then Soft Start begins. The converter will continue to operate in a low current hiccup mode until the fault condition is corrected.

Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced V^2 control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns, causing the top MOSFET to shut OFF and the synchronous (lower) MOSFET to turn ON. This results in a "crowbar" action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during load transients. Adaptive voltage positioning can reduce peak−to−peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is applied. Similarly, the output voltage can be set lower than nominal during heavy loads to reduce overshoot

when the load current is removed. For low current applications a droop resistor can provide fast accurate adaptive positioning. However, at high currents the loss in a droop resistor becomes excessive. For example; in a 50 A converter a 1 mΩ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond to changes in load current. Figure 14 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.

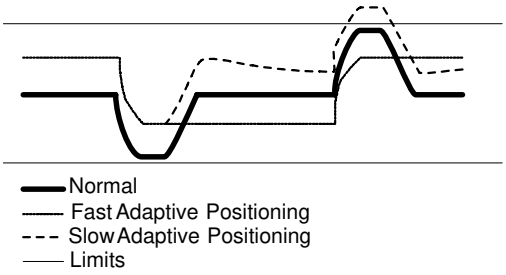


Figure 14. Adaptive Positioning

The controller can be configured to adjust the output voltage based on the output current of the converter. (Refer to the application diagram in Figure 1). To set the no−load positioning, a resistor is placed between the output voltage and V_{FB} pin. The V_{FB} bias current will develop a voltage across the resistor to adjust the no−load output voltage. The V_{FB} bias current is dependent on the value of R_{OSC} as shown in the datasheet.

During no load conditions the V_{DRP} pin is at the same voltage as the V_{FB} pin, so none of the V_{FB} bias current flows through the V_{DRP} resistor. When output current increases the V_{DRP} pin increases proportionally and the V_{DRP} pin current offsets the V_{FB} bias current and causes the output voltage to decrease.

The response during the first few microseconds of a load transient are controlled primarily by power stage output impedance and the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the total ramp size and the error amp compensation. If the current signal size is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

Error Amp Compensation & Tuning

The transconductance error amplifier requires a capacitor (C_{CMP1} in the Applications Diagram) between the COMP pin and GND. This capacitor stabilizes the transconductance error amplifier. Values less than 1 nF may cause oscillations of the COMP voltage. These oscillations will increase the output voltage jitter.

The capacitor (C_{AMP}) between the COMP pin and the inverting error amplifier input (the V_{FB} pin) and the parallel combination of the resistors R_{FBK1} and R_{DRP1} determine the bandwidth of the error amplifier. The gain of the error amplifier crosses 0 dB at a high enough frequency to give a quick transient response, but well below the switching frequency to minimize ripple and noise on the COMP pin. A capacitor in parallel with the V_{FB} resistor (C_{FBK2}) adds a zero to boost phase near the crossover frequency to improve loop stability.

Setting−up and tuning the error amplifier is a three step process. First, the no−load and full−load adaptive voltage positioning (AVP) are set using R_{FBK1} and R_{DRP1}, respectively. Second, the current sense time constant and error amplifier gain are adjusted with R_{CSn} and C_{AMP} while monitoring V_{OUT} during transient loading. Lastly, the peak−to−peak voltage ripple on the COMP pin is examined when the converter is fully loaded to insure low output voltage jitter. The details of this process are covered in the Design Procedure section.

Undervoltage Lockout (UVLO)

The controller has undervoltage lockout functions connected to two pins. One, intended for the logic and low−side drivers, with approximately a 4.2 V turn−on threshold is connected to the V_{CCL} pin. A second, for the high side drivers, with approximately a 1.875 V threshold, is connected to the V_{CCH1} pin.

The UVLO threshold for the high side drivers varies with the part type. In many applications this function will be disabled or will only check that the applicable supply is on − not that is at a high enough voltage to run the converter. See individual datasheets for more information on UVLO.

Soft Start Enable, and Hiccup Mode

A capacitor between the Soft Start pin and GND controls Soft Start and Hiccup mode slopes. A 0.1 μF capacitor with the 30 μA charge current will allow the output to ramp up at 0.3 V/ms or 1.6 V in 5.3 ms at start−up.

When a fault is detected due to an overcurrent condition the converter will enter a low duty cycle hiccup mode. During hiccup mode the converter will not switch from the time a fault is detected until the Soft Start capacitor has discharged below the Soft Start Discharge Threshold and then charged back up above the Channel Start Up Offset.

The Soft Start pin will disable the converter when pulled below the maximum Soft Start Discharge Threshold (nominally 0.27 V).

Power Good (PWRGD)

The open−collector Power Good (PWRGD) pin is driven by a "window−comparator" monitoring V_{CORE}. This comparator will transition HIGH if V_{CORE} is within ±12% of the nominal VID setting. After a 120 μs delay, the

comparators output will saturate the open−collector output transistor and the PWRGD pin will be pulled LOW.

Layout Guidelines

With the fast rise, high output currents of microprocessor applications, parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically, a multi−layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to route the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.

The current sense signals are typically tens of milli−volts. Noise pick−up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as the switch node and gate drive signals. If the current signals are taken from a location other than directly at the inductor any additional resistance between the pick−off point and the inductor appears as part of the inherent inductor resistances and should be considered in design calculations. The capacitors for the current feedback networks should be placed as close to the current sense pins as practical. After placing the NCP5322A control IC, follow these guidelines to optimize the layout and routing:

1. Place the 1 μF power supply bypass (ceramic) capacitors close to their associated pins: V_{CCL}, V_{CCH1} (and/or V_{CCH2}), V_{CCL1} (and/or V_{CCL2}).
2. Place the MOSFETs to minimize the length of the Gate traces. Orient the MOSFETs such that the Drain connections are away from the controller and the Gate connections are closest to the controller.
3. Place the components associated with the internal error amplifier (R_{FBK1}, C_{FBK2}, C_{AMP}, R_{CMP1}, C_{CMP1}, R_{DRP1}) to minimize the trace lengths to the pins V_{FB}, V_{DRP} and COMP.
4. Place the current sense components (R_{CS1}, R_{CS2}, C_{CS1}, C_{CS2}, R_{CSREF}, C_{CSREF}) near the CS1, CS2, and CS_{REF} pins.
5. Place the frequency setting resistor (R_{OSC}) close to the R_{OSC} pin. The R_{OSC} pin is very sensitive to noise. Route noisy traces, such as the SWNODEs and GATE traces, away from the R_{OSC} pin and resistor.
6. Place the Soft Start capacitor (C_{SS}) near the Soft Start pin.
7. Place the MOSFETs and output inductors to reduce the size of the noisy SWNODEs. There is a trade−off between reducing the size of the SWNODEs for noise reduction and providing adequate heat−sinking for the synchronous MOSFETs.
8. Place the input inductor and input capacitor(s) near the Drain of the control (upper) MOSFETs. There is a trade−off between reducing the size of this node to save board area and providing adequate heat−sinking for the control MOSFETs.
9. Place the output capacitors (electrolytic and ceramic) close to the processor socket or output connector.
10. The trace from the SWNODEs to the current sense components (R_{CS1}, R_{CS2}) will be very noisy. Route this away from more sensitive, low−level traces. The Ground layer can be used to help isolate this trace.
11. The Gate traces are very noisy. Route these away from more sensitive, low−level traces. Keep each Gate signal on one layer and insure that there is an uninterrupted return path directly below the Gate trace. The Ground layer can be used to help isolate these traces.
12. Don't "daisy chain" connections to Ground from one via. Allow each connection to Ground to have its own via as close to the component as possible.
13. Use a slot in the ground plane from the bulk output capacitors back to the input power connector to prevent high currents from flowing beneath the control IC. This slot should extend length−wise under the control IC and separate the connections to "signal ground" and "power ground." Examples of signal ground include the capacitors at COMP, CS_{REF}, Soft−Start (SS), V_{CCL}, and REF, the resistors at R_{OSC} and I_{LIM}, and the LGND pin to the controller. Examples of power ground include the capacitors to V_{CCH1} (and/or V_{CCH2}) and V_{CCL1} (and/or V_{CCL2}), the Source of the synchronous MOSFET, and the GND1 and GND2 pins of the controller.
14. The CS_{REF} sense point should be equidistant between the output inductors to equalize the PCB resistance added to the current sense paths. This will insure acceptable current sharing. Also, route the CS_{REF} connection away from noisy traces such as the SWNODEs and GATE traces. If noise from the SWNODEs or GATE signals capacitively couples to the CS_{REF} trace the external ramps will be very noisy and voltage jitter will result.
15. Ideally, the SWNODEs are exactly the same shape and the current sense points (connections to R_{CS1}

and R_{CS2}) are made at identical locations to equalize the PCB resistance added to the current sense paths. This will help to insure acceptable current sharing.

16. Place the 0.1 μF ceramic capacitors, C_{Q1} and C_{Q2}, close to the drains of the MOSFETs Q1 and Q2, respectively.

Design Procedure

1. Output Capacitor Selection

The output capacitors filter the current from the output inductor and provide a low impedance for transient load current changes. Typically, microprocessor applications will require both bulk (electrolytic, tantalum) and low impedance, high frequency (ceramic) types of capacitors. The bulk capacitors provide "hold up" during transient loading. The low impedance capacitors reduce steady−state ripple and bypass the bulk capacitance when the output current changes very quickly. The microprocessor manufacturers usually specify a minimum number of ceramic capacitors. The designer must determine the number of bulk capacitors.

Choose the number of bulk output capacitors to meet the peak transient requirements. The formula below can be used to provide a starting point for the minimum number of bulk capacitors ($N_{OUT,MIN}$):

$$N_{OUT,MIN} = \text{ESR per capacitor} \cdot \frac{\Delta I_{O,MAX}}{\Delta V_{O,MAX}} \quad (1)$$

In reality, both the ESR and ESL of the bulk capacitors determine the voltage change during a load transient according to:

$$\Delta V_{O,MAX} = (\Delta I_{O,MAX}/\Delta t) \cdot ESL + \Delta I_{O,MAX} \cdot ESR \quad (2)$$

Unfortunately, capacitor manufacturers do not specify the ESL of their components and the inductance added by the PCB traces is highly dependent on the layout and routing. Therefore, it is necessary to start a design with slightly more than the minimum number of bulk capacitors and perform transient testing or careful modeling/simulation to determine the final number of bulk capacitors.

2. Output Inductor Selection

The output inductor may be the most critical component in the converter because it will directly effect the choice of other components and dictate both the steady−state and transient performance of the converter. When selecting an inductor the designer must consider factors such as DC current, peak current, output voltage ripple, core material, magnetic saturation, temperature, physical size, and cost (usually the primary concern).

In general, the output inductance value should be as low and physically small as possible to provide the best transient response and minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, too low an inductance value will result in very large ripple currents in the power components (MOSFETs, capacitors, etc) resulting in increased dissipation and lower converter efficiency. Also, increased ripple currents will force the designer to use higher rated MOSFETs, oversize the thermal solution, and use more, higher rated input and output capacitors − the converter cost will be adversely effected.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. Equation 3 may be used to calculate the minimum inductor value to produce a given maximum ripple current (α) per phase. The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the maximum ripple current.

$$Lo_{MIN} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{(\alpha \cdot I_{O,MAX} \cdot V_{IN} \cdot f_{SW})} \quad (3)$$

α is the ripple current as a percentage of the maximum output current *per phase* (α = 0.15 for ±15%, α = 0.25 for ±25%, etc). If the minimum inductor value is used, the inductor current will swing ±α% about its value at the center (1/2 the DC output current for a two−phase converter). Therefore, for a two−phase converter, the inductor must be designed or selected such that it will not saturate with a peak current of $(1 + \alpha) \bullet I_{O,MAX}/2$.

The maximum inductor value is limited by the transient response of the converter. If the converter is to have a fast transient response then the inductor should be made as small as possible. If the inductor is too large its current will change too slowly, the output voltage will droop excessively, more bulk capacitors will be required, and the converter cost will be increased. For a given inductor value, its interesting to determine the times required to increase or decrease the current.

For increasing current:

$$\Delta t_{INC} = Lo \cdot \Delta I_O/(V_{IN} - V_{OUT}) \quad (3.1)$$

For decreasing current:

$$\Delta t_{DEC} = Lo \cdot \Delta I_O/(V_{OUT}) \quad (3.2)$$

For typical processor applications with output voltages less than half the input voltage, the current will be increased much more quickly than it can be decreased. It may be more difficult for the converter to stay within the regulation limits when the load is removed than when it is applied − excessive overshoot may result.

The output voltage ripple can be calculated using the output inductor value derived in this Section (Lo_{MIN}), the number of output capacitors ($N_{OUT,MIN}$) and the per capacitor ESR determined in the previous Section:

$$V_{OUT,P-P} = (\text{ESR per cap} / N_{OUT,MIN}) \cdot \{(V_{IN} - \#Phases \cdot V_{OUT}) \cdot D / (Lo_{MIN} \cdot f_{SW})\} \quad (4)$$

This formula assumes steady−state conditions with no more than one phase on at any time. The second term in Equation 4 is the total ripple current seen by the output capacitors. The total output ripple current is the “time summation” of the two individual phase currents that are 180 degrees out−of−phase. As the inductor current in one phase ramps upward, current in the other phase ramps downward and provides a canceling of currents during part of the switching cycle. Therefore, the total output ripple current and voltage are reduced in a multi−phase converter.

3. Input Capacitor Selection

The choice and number of input capacitors is primarily determined by their voltage and ripple current ratings. The designer must choose capacitors that will support the worst case input voltage with adequate margin. To calculate the number of input capacitors one must first determine the total RMS input ripple current. To this end, begin by calculating the average input current to the converter:

$$I_{IN,AVG} = I_{O,MAX} \cdot D/\eta \quad (5)$$

where:

D is the duty cycle of the converter, $D = V_{OUT}/V_{IN}$.

η is the specified minimum efficiency.

$I_{O,MAX}$ is the maximum converter output current.

The input capacitors will discharge when the control FET is ON and charge when the control FET is OFF as shown in Figure 15.

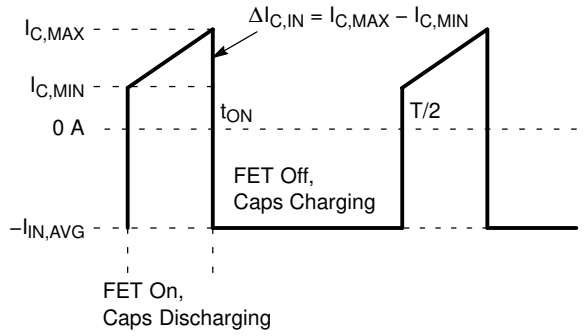


Figure 15. Input Capacitor Current for a Two−Phase Converter

The following equations will determine the maximum and minimum currents delivered by the input capacitors:

$$I_{C,MAX} = I_{Lo,MAX}/\eta - I_{IN,AVG} \quad (6)$$

$$I_{C,MIN} = I_{Lo,MIN}/\eta - I_{IN,AVG} \quad (7)$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = I_{O,MAX}/2 + \Delta I_{Lo}/2 \quad (8)$$

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = I_{O,MAX}/2 - \Delta I_{Lo}/2 \quad (9)$$

ΔI_{Lo} is the peak−to−peak ripple current in the output inductor of value Lo:

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \cdot D/(Lo \cdot f_{SW}) \quad (10)$$

For the two−phase converter, the input capacitor(s) RMS current is then:

$$I_{CIN,RMS} = [2D \cdot (I_{C,MIN}^2 + I_{C,MIN} \cdot \Delta I_{C,IN} + \Delta I_{C,IN}^2/3) + I_{IN,AVG}^2 \cdot (1 - 2D)]^{1/2} \quad (11)$$

Select the number of input capacitors (N_{IN}) to provide the RMS input current ($I_{CIN,RMS}$) based on the RMS ripple current rating per capacitor ($I_{RMS,RATED}$):

$$N_{IN} = I_{CIN,RMS}/I_{RMS,RATED} \quad (12)$$

For a two−phase converter with perfect efficiency ($\eta = 1$), the worst case input ripple−current will occur when the converter is operating at a 25% duty cycle. At this operating point, the parallel combination of input capacitors must support an RMS ripple current equal to 25% of the converter’s DC output current. At other duty cycles, the ripple−current will be less. For example, at a duty cycle of either 10% or 40%, the two−phase input ripple−current will be approximately 20% of the converter’s DC output current.

In general, capacitor manufacturers require derating to the specified ripple−current based on the ambient temperature. More capacitors will be required because of the current derating. The designer should be cognizant of the ESR of the input capacitors. The input capacitor power loss can be calculated from:

$$P_{CIN} = I_{CIN,RMS}^2 \cdot ESR\_per\_capacitor/N_{IN} \quad (13)$$

Low ESR capacitors are recommended to minimize losses and reduce capacitor heating. The life of an electrolytic capacitor is reduced 50% for every 10°C rise in the capacitor’s temperature.

4. Input Inductor Selection

The use of an inductor between the input capacitors and the power source will accomplish two objectives. First, it will isolate the voltage source and the system from the noise generated in the switching supply. Second, it will limit the inrush current into the input capacitors at power up. Large inrush currents will reduce the expected life of the input capacitors. The inductor’s limiting effect on the input current slew rate becomes increasingly beneficial during load transients.

The worst case input current slew rate will occur during the first few PWM cycles immediately after a step−load change is applied as shown in Figure 16. When the load is applied, the output voltage is pulled down very quickly. Current through the output inductors will not change instantaneously so the initial transient load current must be conducted by the output capacitors. The output voltage will step downward depending on the magnitude of the output

current ($I_{O,MAX}$), the per capacitor ESR of the output capacitors (ESR_{OUT}), and the number of the output capacitors (N_{OUT}) as shown in Figure 16. Assuming the load current is shared equally between the two phases, the output voltage at full, transient load will be:

$$V_{OUT,FULL-LOAD} = V_{OUT,NO-LOAD} - (I_{O,MAX}/2) \cdot ESR_{OUT}/N_{OUT} \quad (14)$$

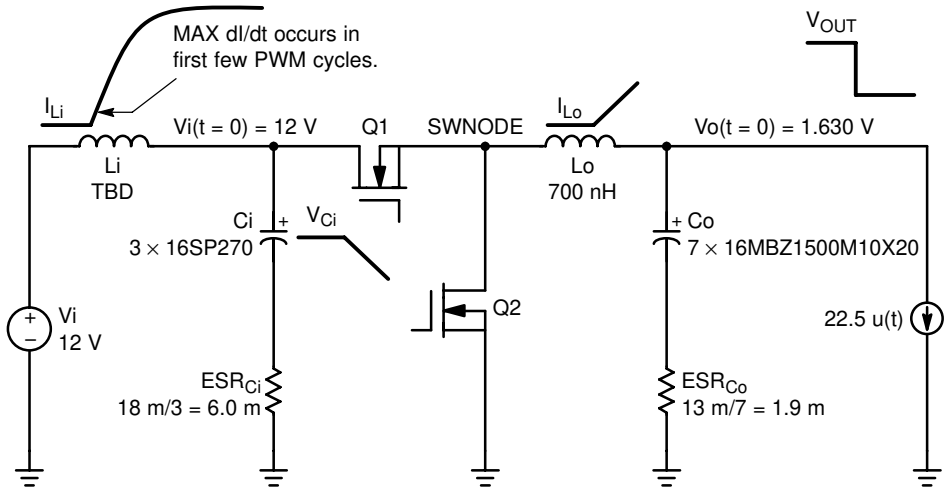


Figure 16. Calculating the Input Inductance

When the control MOSFET (Q1 in Figure 16) turns ON, the input voltage will be applied to the opposite terminal of the output inductor (the SWNODE). At that instant, the voltage across the output inductor can be calculated as:

$$\Delta V_{Lo} = V_{IN} - V_{OUT,FULL-LOAD} = V_{IN} - V_{OUT,NO-LOAD} + (I_{O,MAX}/2) \cdot ESR_{OUT}/N_{OUT} \quad (15)$$

The differential voltage across the output inductor will cause its current to increase linearly with time. The slew rate of this current can be calculated from:

$$dI_{Lo}/dt = \Delta V_{Lo}/Lo \quad (16)$$

Current changes slowly in the input inductor so the input capacitors must initially deliver the vast majority of the input current. The amount of voltage drop across the input capacitors (ΔV_{Ci}) is determined by the number of input capacitors (N_{IN}), their per capacitor ESR (ESR_{IN}), and the current in the output inductor according to:

$$\Delta V_{Ci} = ESR_{IN}/N_{IN} \cdot dI_{Lo}/dt \cdot t_{ON} = ESR_{IN}/N_{IN} \cdot dI_{Lo}/dt \cdot D/f_{SW} \quad (17)$$

Before the load is applied, the voltage across the input inductor (V_{Li}) is very small – the input capacitors charge to the input voltage, V_{IN}. After the load is applied the voltage drop across the input capacitors, ΔV_{Ci}, appears across the input inductor as well. Knowing this, the minimum value of the input inductor can be calculated from:

$$Li_{MIN} = V_{Li} / dI_{IN}/dt_{MAX} = \Delta V_{Ci} / dI_{IN}/dt_{MAX} \quad (18)$$

dI_{IN}/dt_{MAX} is the maximum allowable input current slew rate.

The input inductance value calculated from Equation 18 is relatively conservative. It assumes the supply voltage is very "stiff" and does not account for any parasitic elements that will limit dI/dt such as stray inductance. Also, the ESR values of the capacitors specified by the manufacturer's data sheets are worst case high limits. In reality input voltage "sag," lower capacitor ESRs, and stray inductance will help reduce the slew rate of the input current.

As with the output inductor, the input inductor must support the maximum current without saturating the magnetic. Also, for an inexpensive iron powder core, such as the –26 or –52 from Micrometals, the inductance "swing" with DC bias must be taken into account – inductance will decrease as the DC input current increases. At the maximum input current, the inductance must not decrease below the minimum value or the dI/dt will be higher than expected.

5. MOSFET & Heatsink Selection

Power dissipation, package size, and thermal solution drive MOSFET selection. To adequately size the heat sink, the design must first predict the MOSFET power dissipation. Once the dissipation is known, the heat sink thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded

at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the non−overlap time of the gate drivers.

For the upper or control MOSFET, the power dissipation can be approximated from:

$$P_{D,CONTROL} = (I_{RMS,CNTL}^2 \cdot R_{DS(on)}) + (I_{Lo,MAX} \cdot Q_{switch}/I_g \cdot V_{IN} \cdot f_{SW}) + (Q_{oss}/2 \cdot V_{IN} \cdot f_{SW}) + (V_{IN} \cdot Q_{RR} \cdot f_{SW}) \quad (19)$$

The first term represents the conduction or IR losses when the MOSFET is ON while the second term represents the switching losses. The third term is the losses associated with the *control and synchronous* MOSFET output charge when the control MOSFET turns ON. The output losses are caused by both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovery time of the body diode in the *synchronous* MOSFET. The first two terms are usually adequate to predict the majority of the losses.

Where $I_{RMS,CNTL}$ is the RMS value of the trapezoidal current in the control MOSFET:

$$I_{RMS,CNTL} = [D \cdot (I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (20)$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = I_{O,MAX}/2 + \Delta I_{Lo}/2 \quad (21)$$

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = I_{O,MAX}/2 - \Delta I_{Lo}/2 \quad (22)$$

$I_{O,MAX}$ is the maximum converter output current.

D is the duty cycle of the converter:

$$D = V_{OUT}/V_{IN} \quad (23)$$

ΔI_{Lo} is the peak−to−peak ripple current in the output inductor of value Lo:

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \cdot D/(Lo \cdot f_{SW}) \quad (24)$$

$R_{DS(on)}$ is the ON resistance of the MOSFET at the applied gate drive voltage.

Q_{switch} is the post gate threshold portion of the gate−to−source charge plus the gate−to−drain charge. This may be specified in the data sheet or approximated from the gate−charge curve as shown in the Figure 17.

$$Q_{switch} = Q_{gs2} + Q_{gd} \quad (25)$$

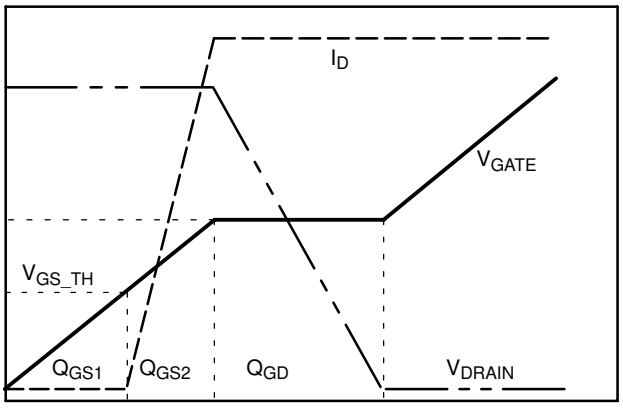


Figure 17. MOSFET Switching Characteristics

I_g is the output current from the gate driver IC.

V_{IN} is the input voltage to the converter.

f_{sw} is the switching frequency of the converter.

Q_G is the MOSFET total gate charge to obtain $R_{DS(on)}$. Commonly specified in the data sheet.

V_g is the gate drive voltage.

Q_{RR} is the reverse recovery charge of the *lower* MOSFET.

Q_{oss} is the MOSFET output charge specified in the data sheet.

For the lower or synchronous MOSFET, the power dissipation can be approximated from:

$$P_{D,SYNCH} = (I_{RMS,SYNCH}^2 \cdot R_{DS(on)}) + (Vf_{diode} \cdot I_{O,MAX}/2 \cdot t\_nonoverlap \cdot f_{SW}) \quad (26)$$

The first term represents the conduction or IR losses when the MOSFET is ON and the second term represents the diode losses that occur during the gate non−overlap time.

All terms were defined in the previous discussion for the control MOSFET with the exception of:

$$I_{RMS,SYNCH} = [(1 - D) \cdot (I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (27)$$

where:

Vf_{diode} is the forward voltage of the MOSFET's intrinsic diode at the converter output current.

t_nonoverlap is the non−overlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the control IC.

When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature

$$\theta_T < (T_J - T_A)/P_D \quad (28)$$

where;

θ_T is the total thermal impedance ($\theta_{JC} + \theta_{SA}$).

θ_{JC} is the junction−to−case thermal impedance of the MOSFET.

θ_{SA} is the sink−to−ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET (no thermal "pad" is used).

T_J is the specified maximum allowed junction temperature.

T_A is the worst case ambient operating temperature.

For TO−220 and TO−263 packages, standard FR−4 copper clad circuit boards will have approximate thermal resistances (θ_{SA}) as shown below:

Pad Size (in^2/mm^2)	Single−Sided 1 oz. Copper
0.5/323	60−65°C/W
0.75/484	55−60°C/W
1.0/645	50−55°C/W
1.5/968	45−50°C/W
2.0/1290	38−42°C/W
2.5/1612	33−37°C/W

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e. worst case MOSFET $R_{DS(on)}$). Also, the inductors and capacitors share the MOSFET's heatsinks and will add heat and raise the temperature of the circuit board and MOSFET. For any new design, its advisable to have as much heatsink area as possible – all too often new designs are found to be too hot and require re−design to add heatsinking.

6. Adaptive Voltage Positioning

There are two resistors that determine the Adaptive Voltage Positioning: R_{FBK1} and R_{DRP}. R_{FBK1} establishes the no−load "high" voltage position and R_{DRP} determines the full−load "droop" voltage.

Resistor R_{FBK1} is connected between V_{CORE} and the V_{FB} pin of the controller. At no load, this resistor will conduct the internal bias current of the V_{FB} pin and develop a voltage drop from V_{CORE} to the V_{FB} pin. Because the error amplifier regulates V_{FB} to the DAC setting, the output voltage, V_{CORE}, will be higher by the amount $IBIAS_{VFB} \bullet R_{FBK1}$. This condition is shown in Figure 18.

To calculate R_{FBK1} the designer must specify the no−load voltage increase above the VID setting ($\Delta V_{NO-LOAD}$) and determine the V_{FB} bias current. Usually, the no−load voltage increase is specified in the design guide for the processor that is available from the manufacturer. The V_{FB} bias current is determined by the value of the resistor from R_{OSC} to ground (see Figure 5 in the data sheet for a graph of $IBIAS_{VFB}$ versus R_{OSC}). The value of R_{FBK1} can then be calculated:

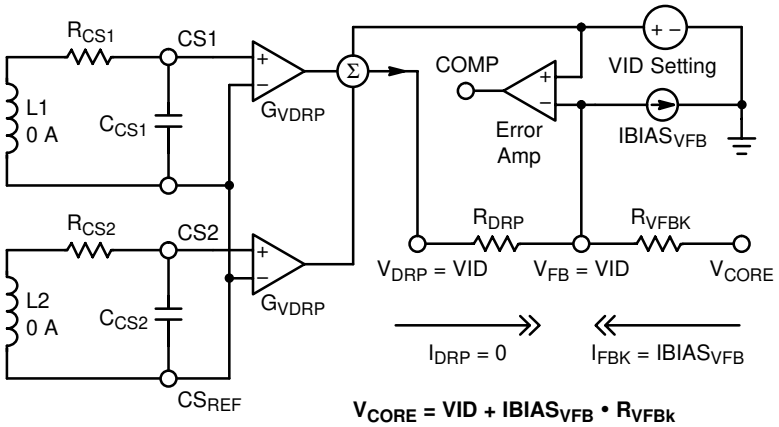


Figure 18. AVP Circuitry at No−Load

$$R_{FBK1} = \Delta V_{NO-LOAD}/IBIAS_{VFB} \quad (29)$$

Resistor R_{DRP} is connected between the V_{DRP} and the V_{FB} pins. At no−load, the V_{DRP} and the V_{FB} pins will both be at the DAC voltage so this resistor will conduct zero current. However, at full−load, the voltage at the V_{DRP} pin will increase proportional to the output inductor's current while V_{FB} will still be regulated to the DAC voltage. Current will be conducted from V_{DRP} to V_{FB} by R_{DRP}. This current will be large enough to supply the V_{FB} bias current and cause a voltage drop from V_{FB} to Vcore across R_{FBK} – the converter's output voltage will be reduced. This condition is shown in Figure 19.

To determine the value of R_{DRP} the designer must specify the full−load voltage reduction *from the VID* (DAC) setting ($\Delta V_{OUT,FULL-LOAD}$) and predict the voltage increase at the V_{DRP} pin at full−load. Usually, the full−load voltage reduction is specified in the design guide for the processor that is available from the manufacturer. To predict the

voltage increase at the V_{DRP} pin at full−load (ΔV_{DRP}), the designer must consider the output inductor's resistance (R_L), the PCB trace resistance between the current sense points (R_{PCB}), and the controller IC's gain from the current sense to the V_{DRP} pin (G_{VDRP}):

$$\Delta V_{DRP} = I_{O,MAX} \cdot (R_L + R_{PCB}) \cdot G_{VDRP} \quad (30)$$

The value of R_{DRP} can then be calculated:

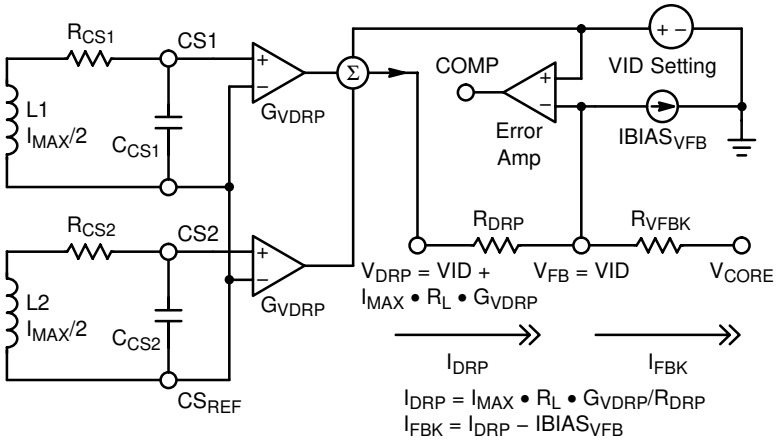
$$R_{DRP} = \frac{\Delta V_{DRP}}{(IBIAS_{VFB} + \Delta V_{OUT,FULL-LOAD}/R_{FBK1})} \quad (31)$$

$\Delta V_{OUT,FULL-LOAD}$ is the full−load voltage reduction from the VID (DAC) setting. $\Delta V_{OUT,FULL-LOAD}$ is *not* the voltage change from the no−load AVP setting.

7. Current Sensing

For inductive current sensing, choose the current sense network (R_{CSn}, C_{CSn}, n = 1 or 2) to satisfy

$$R_{CSn} \cdot C_{CSn} = Lo/(R_L + R_{PCB}) \quad (32)$$



$$V_{CORE} = VID - (I_{DRP} - IBIAS_{VFB}) \cdot R_{VFBK}$$
$$= VID - I_{MAX} \cdot R_L \cdot G_{VDRP} \cdot R_{FBK}/R_{DRP} + IBIAS_{VFB} \cdot R_{FBK}$$

Figure 19. AVP Circuitry at Full−Load

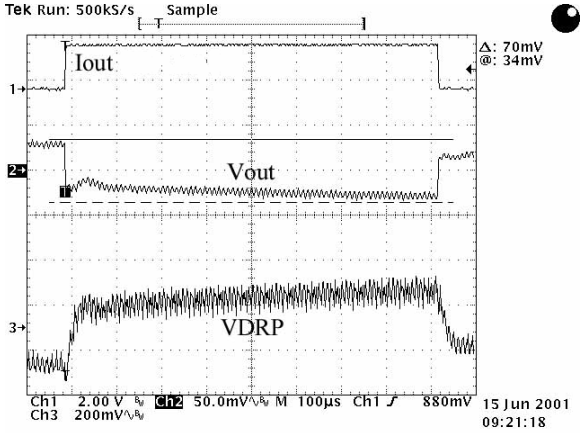


Figure 20. V_{DRP} Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Too Long (Slow): V_{DRP} and V_{OUT} Respond Too Slowly.

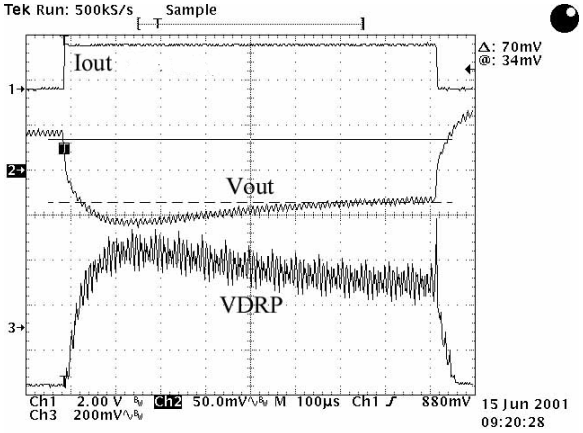


Figure 21. V_{DRP} Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Too Short (Fast): V_{DRP} and V_{OUT} Both Overshoot.

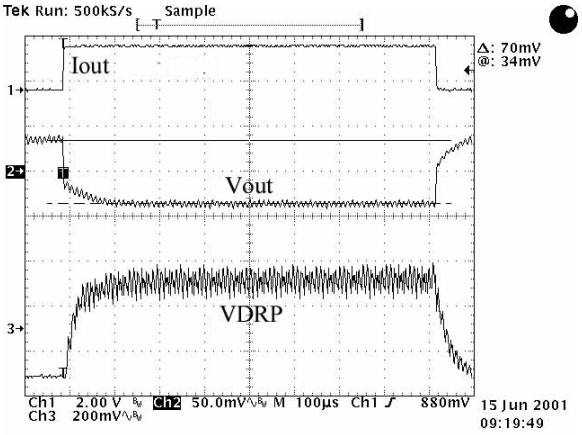


Figure 22. V_{DRP} Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Optimal: V_{DRP} and V_{OUT} Respond to the Load Current Quickly Without Overshooting.

For resistive current sensing, choose the current sense network (R_{CSn}, C_{CSn}, n = 1 or 2) to satisfy

$$R_{CSn} \cdot C_{CSn} = Lo/(R_{sense}) \quad (33)$$

This will provide an adequate starting point for R_{CSn} and C_{CSn}. After the converter is constructed, the value of R_{CSn} (and/or C_{CSn}) should be fine−tuned in the lab by observing the V_{DRP} signal during a step change in load current. The R_{CSn} • C_{CSn} network should be tuned to provide a "square−wave" at the V_{DRP} output pin with maximum rise time and minimal overshoot as shown in Figure 22.

Equation 32 will be most accurate for better iron powder core material (such as the −8 from Micrometals). This material is very consistent with DC current and frequency. Less expensive core materials (such as the −52 from Micrometals) change their characteristics with DC current, AC flux density, and frequency. This material will yield acceptable converter performance if the current sense time constant is set lower (longer) than anticipated. As a rule of thumb, use approximately twice the resistance (R_{CSn}) or twice the capacitance (C_{CSn}) when using the less expensive core material.

8. Error Amplifier Tuning

After the steady−state (static) AVP has been set and the current sense network has been optimized the Error Amplifier must be tuned. Basically, the gain of the Error Amplifier should be adjusted to provide an acceptable transient response by increasing or decreasing the Error Amplifier's feedback capacitor (C_{AMP} in the Applications Diagram). The bandwidth of the control loop will vary directly with the gain of the error amplifier.

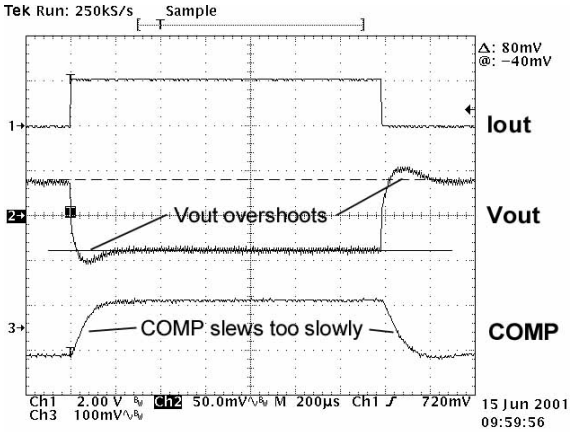


Figure 23. The Value of C_{AMP} Is Too High and the Loop Gain/Bandwidth Too Low. COMP Slews Too Slowly Which Results in Overshoot in V_{OUT}.

If C_{AMP} is too large the loop gain/bandwidth will be low, the COMP pin will slew too slowly, and the output voltage will overshoot as shown in Figure 23. On the other hand, if C_{AMP} is too small the loop gain/bandwidth will be high, the COMP pin will slew very quickly and overshoot. Integrator

"wind up" is the cause of the overshoot. In this case the output voltage will transition more slowly because COMP spikes upward as shown in Figure 24. Too much loop gain/bandwidth increase the risk of instability. In general, one should use the lowest loop gain/bandwidth as possible to achieve acceptable transient response − this will insure good stability. If C_{AMP} is optimal the COMP pin will slew quickly but not overshoot and the output voltage will monotonically settle as shown in Figure 25.

After the control loop is tuned to provide an acceptable transient response the steady−state voltage ripple on the COMP pin should be examined. When the converter is operating at full, steady−state load, the peak−to−peak voltage ripple on the COMP pin should be less than 20 mV_{PP} as shown in Figure 26. Less than 10 mV_{PP} is ideal. Excessive ripple on the COMP pin will contribute to output voltage jitter.

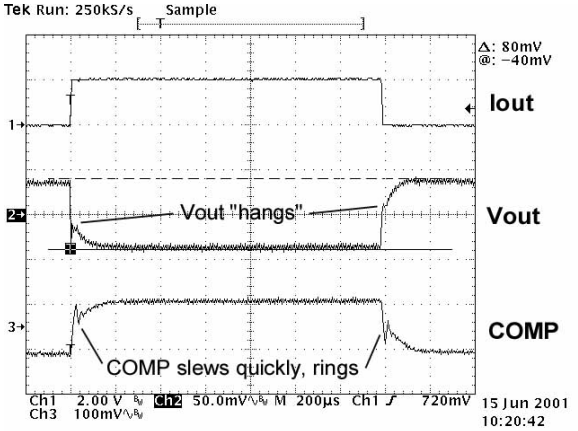


Figure 24. The Value of C_{AMP} Is Too Low and the Loop Gain/Bandwidth Too High. COMP Moves Too Quickly, Which Is Evident from the Small Spike in Its Voltage When the Load Is Applied or Removed. The Output Voltage Transitions More Slowly Because of the COMP Spike.

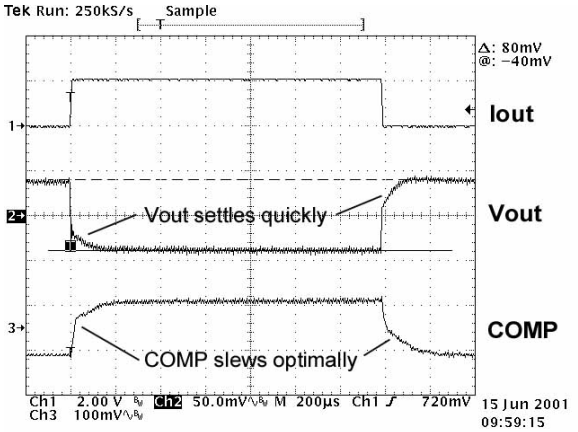


Figure 25. The Value of C_{AMP} Is Optimal. COMP Slews Quickly Without Spiking or Ringing. V_{OUT} Does Not Overshoot and Monotonically Settles to Its Final Value.

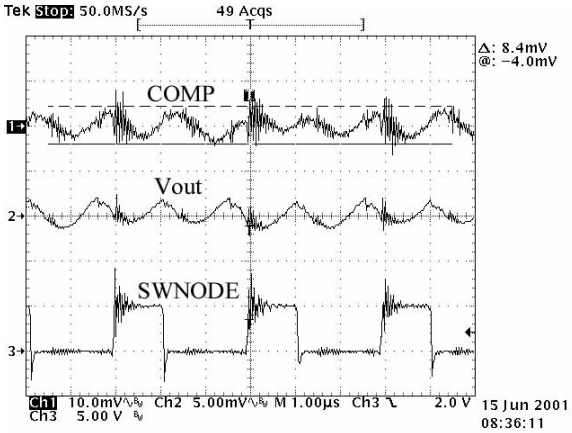


Figure 26. At Full−Load (28 A) the Peak−to−Peak Voltage Ripple on the COMP Pin Should Be Less than 20 mV for a Well−Tuned/Stable Controller. Higher COMP Voltage Ripple Will Contribute to Output Voltage Jitter.

9. Current Limit Setting

When the output of the current sense amplifier (CO1 or CO2 in the block diagram) exceeds the voltage on the I_{LIM} pin the part will enter hiccup mode. For inductive sensing, the I_{LIM} pin voltage should be set based on the inductor's maximum resistance (R_{LMAX}). The design must consider the inductor's resistance increase due to current heating and ambient temperature rise. Also, depending on the current sense points, the circuit board may add additional resistance. In general, the temperature coefficient of copper is +0.393% per °C. If using a current sense resistor (R_{SENSE}), the I_{LIM} pin voltage should be set based on the maximum value of the sense resistor. To set the level of the I_{LIM} pin:

$$V_{ILIM} = (I_{OUT,LIM} + \Delta I_{Lo}/2) \cdot R \cdot G_{ILIM} \quad (34)$$

where:

$I_{OUT,LIM}$ is the current limit threshold of the converter;
$\Delta I_{Lo}/2$ is half the inductor ripple current;
R is either (R_{LMAX} + R_{PCB}) or R_{SENSE};
G_{ILIM} is the current sense to I_{LIM} gain.

For the overcurrent protection to work properly, the current sense time constant (RC) should be slightly larger than the RL time constant. If the RC time constant is too fast, during step load changes the sensed current waveform will appear larger than the actual inductor current and will probably trip the current limit at a lower level than expected.

10. PWM Comparator Input Voltage

The voltage at the positive input terminal of the PWM comparator (see Figure 10 or 12) is limited by the internal voltage supply of the controller (3.3 V), the size of the internal ramp, and the magnitude of the channel startup offset voltage. To prevent the PWM comparator from saturating, the differential input voltage from CS_{REF} to CSn (n = 1 or 2) must satisfy the following equation: