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# NCP5386, NCP5386A, NCP5386B

## 1/2 Phase Controller for CPU and Chipset Applications

The NCP5386 is a one- or two-phase buck controller which combines differential voltage and current sensing, and adaptive voltage positioning to power both AMD and Intel processors and chipsets. Dual-edge pulse-width modulation (PWM) combined with inductor current sensing reduces system cost by providing the fastest initial response to transient load events. Dual-edge multi-phase modulation reduces total bulk and ceramic output capacitance required to satisfy transient load-line regulation.

A high performance operational error amplifier is provided, which allows easy compensation of the system. The proprietary method of Dynamic Reference Injection makes the error amplifier compensation virtually independent of the system response to VID changes, eliminating tradeoffs between overshoot and dynamic VID performance.

### Features

- Meets Intel's VR 10.0 and 11.0, and AMD Specifications
- No load Intel VR Offset of -19 mV (NCP5386), +20 mV (NCP5386A), and 0 mV (NCP5386B)
- Dual-Edge PWM for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Supports both VR11 and Legacy Soft-Start Modes
- Dynamic Reference Injection (Patent# 7057381)
- DAC Range from 0.5 V to 1.6 V
- $\pm 0.5\%$  System Voltage Accuracy from 1.0 V to 1.6 V
- True Differential Remote Voltage Sensing Amplifier
- Phase-to-Phase Current Balancing
- "Lossless" Differential Inductor Current Sensing
- Differential Current Sense Amplifiers for each Phase
- Adaptive Voltage Positioning (AVP)
- Frequency Range: 100 kHz – 1.0 MHz
- OVP with Resettable, 8 Event Delayed Latch
- Threshold Sensitive Enable Pin for  $V_{TT}$  Sensing
- Power Good Output with Internal Delays
- Programmable Soft-Start Time
- This is a Pb-Free Device\*

### Applications

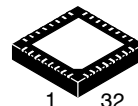
- Desktop Processors and Chipsets
- Server Processors and Chipsets
- DDR

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



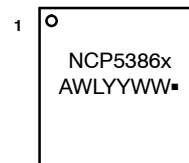
ON Semiconductor®

<http://onsemi.com>



QFN32, 5 x 5\*  
MN SUFFIX  
CASE 485AF

### MARKING DIAGRAMS



\*Pin 33 is the thermal pad on the bottom of the device.

NCP5386 = Specific Device Code  
x = Blank, A or B  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
▪ = Pb-Free Package

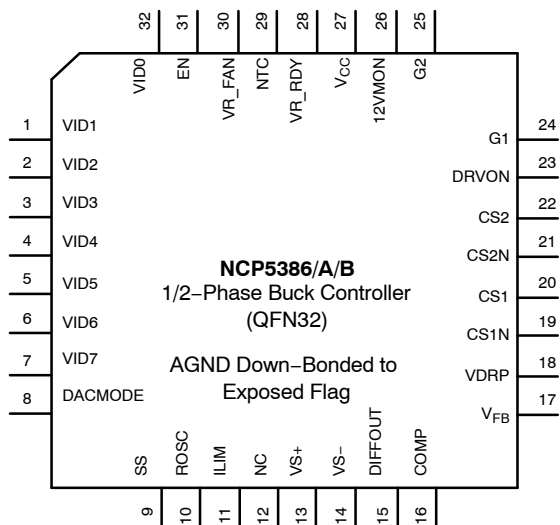
### ORDERING INFORMATION

Device	Package	Shipping†
NCP5386MNR2G*	QFN32 (Pb-Free)	2500 / Tape & Reel
NCP5386AMNR2G*	QFN32 (Pb-Free)	2500 / Tape & Reel
NCP5386BMNR2G*	QFN32 (Pb-Free)	2500 / Tape & Reel

\*Temperature Range: 0°C to 85°C

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NCP5386, NCP5386A, NCP5386B



**Figure 1. Pin Connections**  
(Top View)

# NCP5386, NCP5386A, NCP5386B

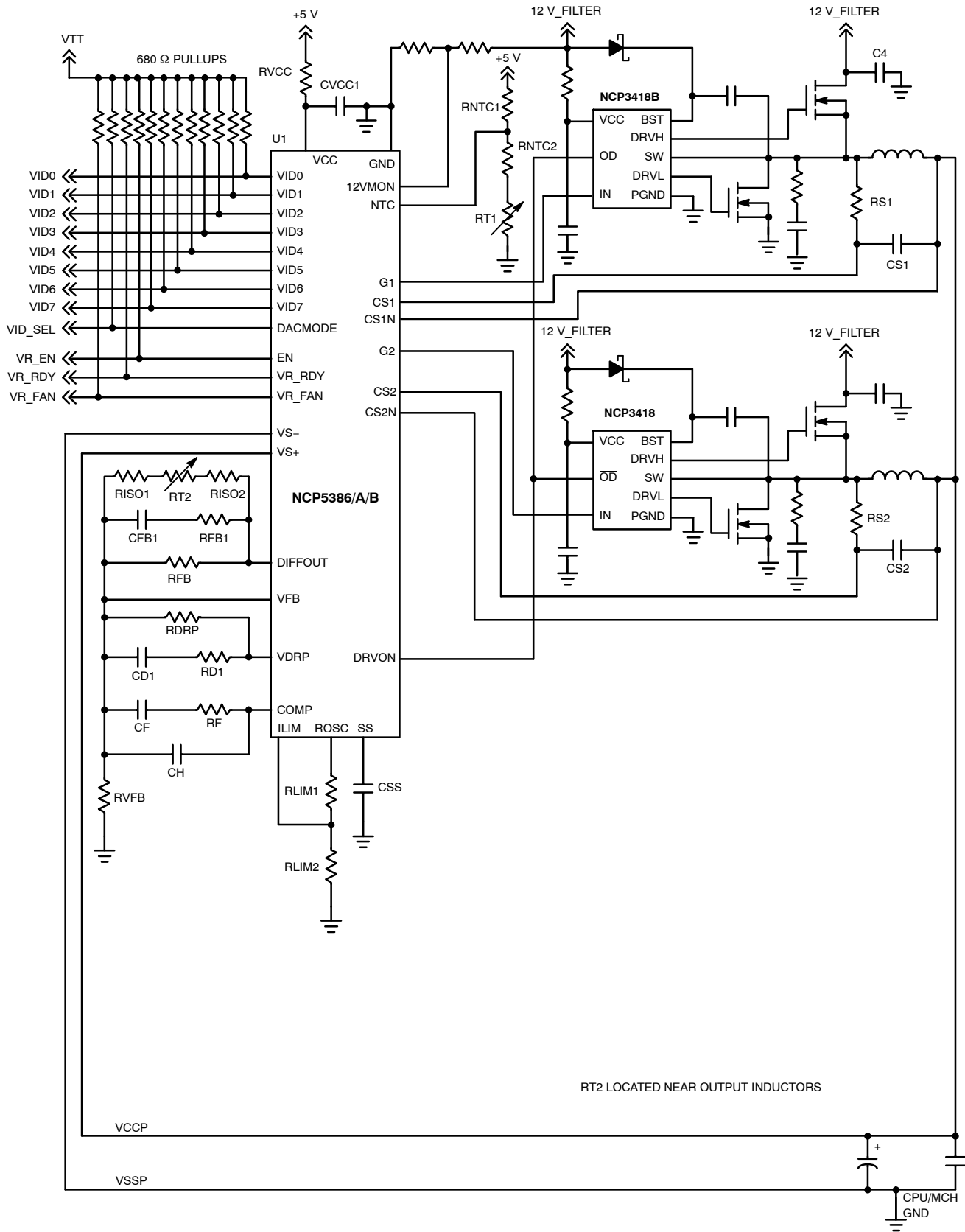


Figure 2. 2-Phase Application Schematic

# NCP5386, NCP5386A, NCP5386B

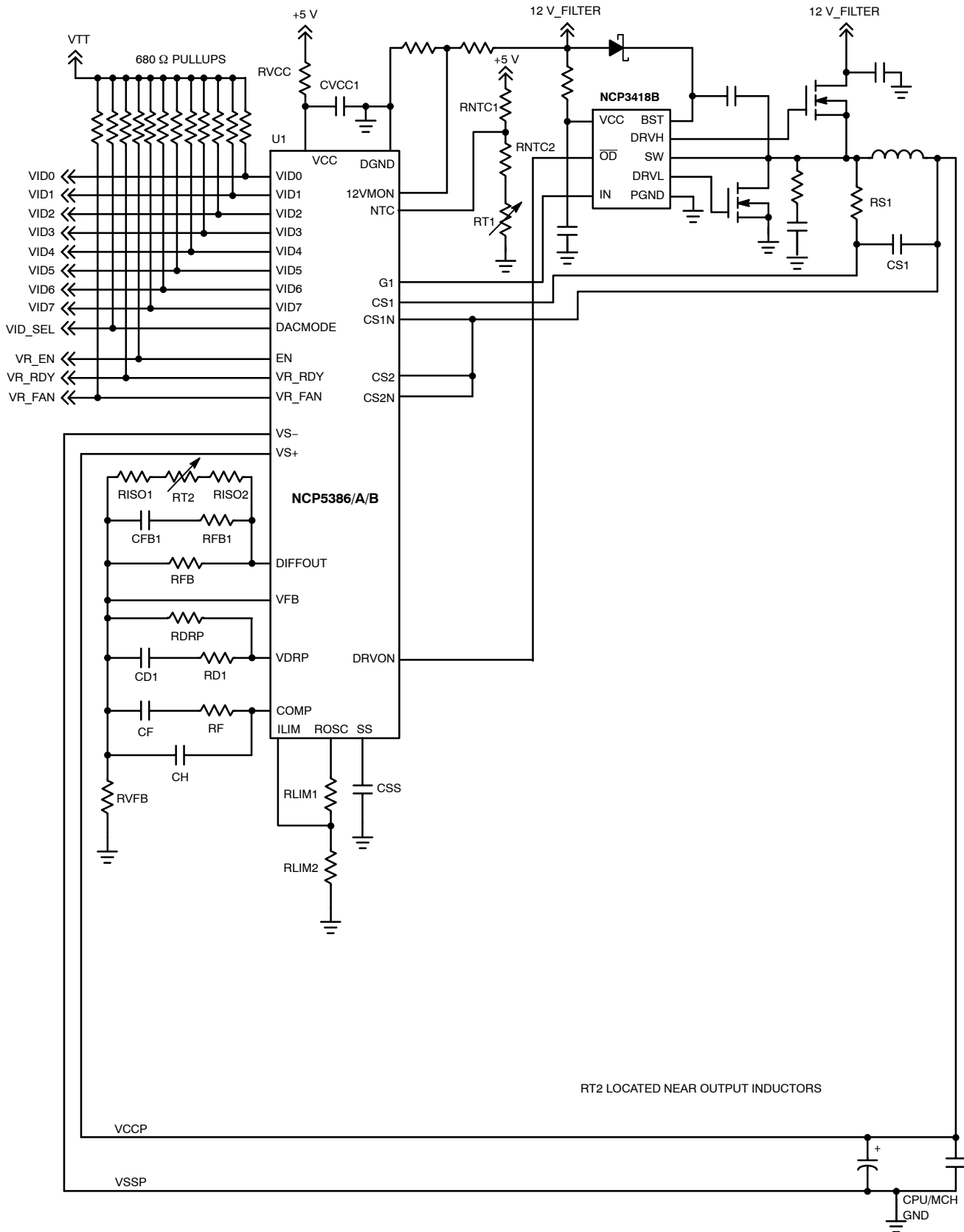


Figure 3. 1-Phase Application Schematic

NCP5386, NCP5386A, NCP5386B

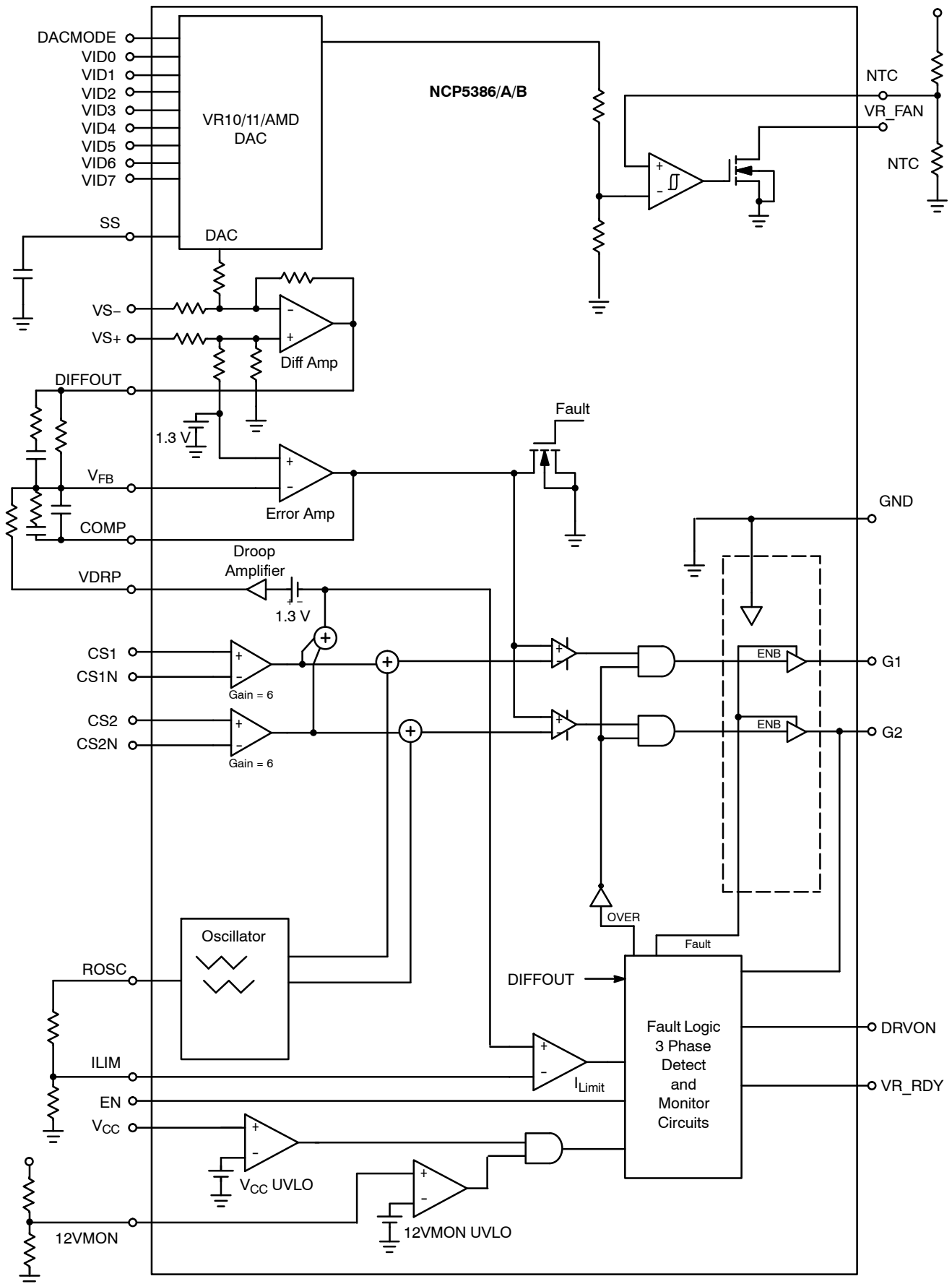


Figure 4. Simplified Block Diagram

## NCP5386, NCP5386A, NCP5386B

### PIN DESCRIPTIONS

QFN32		Description
Pin No.	Symbol	
32, 1 – 7	VID0–VID7	Voltage ID DAC inputs
8	DACMODE	VRM select bit
9	SS	A capacitor from this pin to ground programs the soft–start time.
10	ROSC	A resistance from this pin to ground programs the oscillator frequency. Also, this pin supplies an output voltage of 2 V which may be used to form a voltage divider to the ILIM pin to set the over–current shutdown threshold as shown in the Applications Schematics.
11	ILIM	Overcurrent shutdown threshold. To program the shutdown threshold, connect this pin to the ROSC pin via a resistor divider as shown in the Applications Schematics. To disable the over–current feature, connect this pin directly to the ROSC pin. To guarantee correct operation, this pin should only be connected to the voltage generated by the ROSC pin; do not connect this pin to any externally generated voltages.
12	NC	Do not connect anything to this pin.
13	VS+	Non–inverting input to the internal differential remote sense amplifier
14	VS–	Inverting input to the internal differential remote sense amplifier
15	DIFFOUT	Output of the differential remote sense amplifier
16	COMP	Output of the error amplifier, and the non–inverting input of the PWM comparators
17	V <sub>FB</sub>	Error amplifier inverting input. Connect a resistor from this pin to DIFFOUT. The value of this resistor and the amount of current from the droop resistor (RDRP) will set the amount of output voltage droop (AVP) during load.
18	VDRP	Current signal output for Adaptive Voltage Positioning (AVP). The voltage of this pin above the 1.3 V internal offset voltage is proportional to the output current. Connect a resistor from this pin to V <sub>FB</sub> to set the amount of AVP current into the feedback resistor (R <sub>FB</sub> ) to produce an output voltage droop. Leave this pin open for no AVP.
19, 21	CS1N, CS2N	Inverting input to current sense amplifier.
20, 22	CS1, CS2	Non–inverting input to current sense amplifier.
23	DRVON	Output to enable Gate Drivers
24, 25	G1, G2	PWM output pulses to gate drivers
26	12VMON	Second UVLO monitor for monitoring the power stage supply rail
27	V <sub>CC</sub>	Power for the internal control circuits.
28	VR_RDY	Voltage Regulator Ready (Power Good) output. Open drain output that indicates the output is regulating.
29	NTC	Remote temperature sense connection. Connect an NTC thermistor from this pin to GND and a resistor from this pin to V <sub>REF</sub> . As the NTC's temperature increases, the voltage on this pin will decrease.
30	VR_FAN	Open drain output that will be low impedance when the voltage at the NTC pin is above the specified threshold. This pin will transition to a high impedance state when the voltage at the NTC pin decreases below the specified threshold. This pin requires an external pull–up resistor.
31	EN	Pull this pin high to enable controller. Pull this pin low to disable controller. Either an open–collector output (with a pull–up resistor) or a logic gate (CMOS or totem–pole output) may be used to drive this pin. A Low–to–High transition on this pin will initiate a soft start. Connect this pin directly to V <sub>REF</sub> if the Enable function is not required. 20 MHz filtering at this pin is required.
33	GND	Power supply return (QFN Flag)

# NCP5386, NCP5386A, NCP5386B

## MAXIMUM RATINGS

### Electrical Information

Pin Symbol	V <sub>MAX</sub> (V)	V <sub>MIN</sub> (V)	I <sub>SOURCE</sub> (mA)	I <sub>SINK</sub> (mA)
COMP	5.5	-0.3	10	10
VDRP	5.5	-0.3	5	5
VS+	2.0	GND - 300 mV	1	1
VS-	2.0	GND - 300 mV	1	1
DIFFOUT	5.5	-0.3	20	20
VR_RDY, VR_FAN	5.5	-0.3	N/A	20
V <sub>CC</sub>	7.0	-0.3	N/A	20
ROSC	5.5	-0.3	1	N/A
DACMODE, EN	3.5	-0.3	0	0
All Other Pins	5.5	-0.3	-	-

\*All signals reference to GND unless otherwise noted.

### Thermal Information

Rating	Symbol	Value	Unit
Thermal Characteristic, QFN Package (Note 1)	R <sub>θJA</sub>	56	°C/W
Operating Junction Temperature Range (Note 2)	T <sub>J</sub>	0 to 125	°C
Operating Ambient Temperature Range	T <sub>A</sub>	0 to 85	°C
Maximum Storage Temperature Range	T <sub>STG</sub>	-55 to +150	°C
Moisture Sensitivity Level, QFN Package	MSL	1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

\*The maximum package power dissipation must be observed.

1. JESD 51-5 (1S2P Direct-Attach Method) with 0 Airflow.
2. JESD 51-7 (1S2P Direct-Attach Method) with 0 Airflow.

## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T<sub>A</sub> < 85°C; 4.75 V < V<sub>CC</sub> < 5.25 V; All DAC Codes; C<sub>VCC</sub> = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
<b>Error Amplifier</b>					
Input Bias Current		-200	-	200	nA
Input Offset Voltage (Note 3)		-1.0	-	1.0	mV
Open Loop DC Gain (Note 3)	C <sub>L</sub> = 60 pF to GND, R <sub>L</sub> = 10 kΩ to GND	-	100	-	dB
Open Loop Unity Gain Bandwidth (Note 3)	C <sub>L</sub> = 60 pF to GND, R <sub>L</sub> = 10 kΩ to GND	-	15	-	MHz
Open Loop Phase Margin (Note 3)	C <sub>L</sub> = 60 pF to GND, R <sub>L</sub> = 10 kΩ to GND	-	70	-	°
Slew Rate (Note 3)	ΔV <sub>IN</sub> = 100 mV, G = -10 V/V, 1.5 V < COMP < 2.5 V, C <sub>L</sub> = 60 pF, DC Load = ±125 μA	-	5	-	V/μs
Maximum Output Voltage	10 mV of Overdrive I <sub>SOURCE</sub> = 2.0 mA	2.20	V <sub>CC</sub> - 20 mV	-	V
Minimum Output Voltage	10 mV of Overdrive I <sub>SINK</sub> = 2.0 mA	-	0.01	0.5	V

3. Guaranteed by design. Not tested in production.



# NCP5386, NCP5386A, NCP5386B

## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated:  $0^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ ;  $4.75\text{ V} < V_{\text{CC}} < 5.25\text{ V}$ ; All DAC Codes;  $C_{\text{VCC}} = 0.1\ \mu\text{F}$ )

Parameter	Test Conditions	Min	Typ	Max	Units
<b>Error Amplifier</b>					
Output Source Current (Note 3)	10 mV Input Overdrive COMP = 2.0 V	2.0	–	–	mA
Output Sink Current (Note 3)	10 mV Input Overdrive COMP = 1.0 V	2.0	–	–	mA

### Differential Summing Amplifier

VS+ Input Resistance	DRVON = Low DRVON = High	– –	1.5 17	– –	k $\Omega$
VS+ Input Bias Voltage	DRVON = Low DRVON = High	– –	0.05 0.65	– –	V
VS– Bias Current	VS– = 0 V	–	33	–	$\mu\text{A}$
VS+ Input Voltage Range	$0.95 \leq \Delta\text{DIFFOUT} / \Delta\text{VS–} \leq 1.05$ $0.5\text{ V} \leq \text{DIFFOUT} \leq 2.0\text{ V}$	–0.3	–	2.0	V
VS– Input Voltage Range	$0.95 \leq \Delta\text{DIFFOUT} / \Delta\text{VS–} \leq 1.05$ $0.5\text{ V} \leq \text{DIFFOUT} \leq 2.0\text{ V}$	–0.3	–	0.3	V
DC Gain VS+ to DIFFOUT	$0\text{ V} \leq \text{DAC} - \text{VS+} \leq 0.3\text{ V}$	0.99	–	1.01	V/V
DAC Accuracy (measured at VS+)	Closed loop measurement including error amplifier. (See Figure 20) $1.0 \leq \text{DAC} \leq 1.6$ $0.8 \leq \text{DAC} \leq 1.0$ $0.5 \leq \text{DAC} \leq 0.8$	–0.5 –5 –8	– – –	0.5 5 8	% mV mV
–3dB Bandwidth (Note 3)	$C_L = 80\text{ pF}$ to GND, $R_L = 10\text{ k}\Omega$ to GND	–	10	–	MHz
Slew Rate (Note 3)	$\Delta V_{\text{IN}} = 100\text{ mV}$ , DIFFOUT = 1.3 V to 1.2 V	–	5.0	–	V/ $\mu\text{s}$
Maximum Output Voltage	VS+ – DAC = 1.0 V $I_{\text{SOURCE}} = 2.0\text{ mA}$	2.0	3.0	–	V
Minimum Output Voltage	VS+ – DAC = –0.8 V $I_{\text{SINK}} = 2.0\text{ mA}$	–	0.01	0.5	V
Output Source Current (Note 3)	VS+ – DAC = 1.0 V DIFFOUT = 1.0 V	2.0	–	–	mA
Output Sink Current	VS+ – DAC = –0.8 V DIFFOUT = 1.0 V	2.0	–	–	mA

### Internal Offset Voltage

VDRP pin offset voltage AND Error Amp input voltage		–	1.30		V
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### VDRP Adaptive Voltage–Positioning Amplifier

Current Sense Input to VDRP Gain	$-60\text{ mV} < (\text{CSx} - \text{CSxN}) < +60\text{ mV}$ (Each CS Input Independently)	5.64	5.79	5.95	V/V
Current Sense Input to VDRP –3dB Bandwidth (Note 3)	$C_L = 30\text{ pF}$ to GND, $R_L = 10\text{ k}\Omega$ to GND	–	4	–	MHz
VDRP Output Slew Rate (Note 3)	$\Delta V_{\text{IN}} = 25\text{ mV}$ $1.3\text{ V} < \text{VDRP} < 1.9\text{ V}$ , $C_L = 330\text{ pF}$ to GND, $R_L = 1\text{ k}\Omega$ to $10\text{ k}\Omega$ connected to 1.3 V	2.5	–	–	V/ $\mu\text{s}$
VDRP Output Voltage Offset from Internal Offset Voltage	CSx– CSxN = 1.3 V	–15	–	+15	mV
Maximum VDRP Output Voltage	CSx – CSxN = 0.1 V (all phases), $I_{\text{SOURCE}} = 1.0\text{ mA}$	2.6	3.0	–	V

3. Guaranteed by design. Not tested in production.

# NCP5386, NCP5386A, NCP5386B

## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated:  $0^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ ;  $4.75\text{ V} < V_{\text{CC}} < 5.25\text{ V}$ ; All DAC Codes;  $C_{\text{VCC}} = 0.1\ \mu\text{F}$ )

Parameter	Test Conditions	Min	Typ	Max	Units
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### VDRP Adaptive Voltage-Positioning Amplifier

Minimum VDRP Output Voltage	$CSx - CSxN = -0.033\text{ V}$ (all phases), $I_{\text{SINK}} = 1.0\text{ mA}$	-	0.1	0.5	V
Output Source Current (Note 3)	VDRP = 2.0 V	-	1.3	-	mA
Output Sink Current (Note 3)	VDRP = 1.0 V	-	25	-	mA

### Current Sense Amplifiers

Input Bias Current	$CSx = CSxN = 1.4\text{ V}$	-200	-	200	nA
Common Mode Input Voltage Range		-0.3	-	2.0	V
Differential Mode Input Voltage Range (Note 3)		-120	-	120	mV
Input Referred Offset Voltage (Note 3)	$CSx = CSxN = 1.0\text{ V}$	-1.0	-	1.0	mV
Current Sense Input to PWM Gain	$0\text{ V} < (CSx - CSxN) < 0.1\text{ V}$	-	6.0	-	V/V

### Oscillator

Switching Frequency Range (Note 3)		100	-	1000	kHz
Switching Frequency Accuracy	ROSC = 50 k $\Omega$ 25 k $\Omega$ 10 k $\Omega$	196 380 803	- - -	226 420 981	kHz
Switching Frequency Tolerance (Note 3)	$200\text{ kHz} < F_{\text{SW}} < 600\text{ kHz}$ $100\text{ kHz} < F_{\text{SW}} < 1\text{ MHz}$	- -	5 10	- -	%
ROSC Output Voltage	$10\ \mu\text{A} \leq I_{\text{ROSC}} \leq 200\ \mu\text{A}$	1.950	2.010	2.065	V

### Modulators (PWM Comparators)

Minimum Pulse Width (Note 3)	$F_S = 800\text{ kHz}$	-	30	40	ns
Propagation Delay (Note 3)		-	20	-	ns
Magnitude of the PWM Ramp		-	1.0	-	V
0% Duty Cycle	COMP voltage when the PWM outputs remain LOW	-	1.3	-	V
100% Duty Cycle	COMP voltage when the PWM outputs remain HIGH	-	2.3	-	V
PWM Linear Duty Cycle (Note 3)		-	90	-	%
PWM Phase Angle Error		-15	-	15	$^{\circ}$

### VR\_RDY (Power Good) Output

VR_RDY Saturation Voltage	$I_{\text{VR\_RDY}} = 10\text{ mA}$	-	-	0.4	V
VR_RDY Rise Time	External pullup of 680 $\Omega$ to 1.25 V, $C_L = 45\text{ pF}$ , $\Delta V_O = 10\%$ to 90%	-	-	150	ns
VR_RDY High – Output Leakage Current	VR_RDY = 5.0 V	-	-	1.0	$\mu\text{A}$
VR_RDY Upper Threshold Voltage	VCore increasing, DAC = 1.3 V	-	300	-	mV below DAC
VR_RDY Lower Threshold Voltage	VCore decreasing, DAC = 1.3 V	-	350	-	mV below DAC
VR_RDY Rising Delay	VCore increasing	-	-	3	ms
VR_RDY Falling Delay	VCore decreasing	-	-	250	ns

### PWM Outputs

Output High Voltage	Sourcing 500 $\mu\text{A}$	3.0	-	$V_{\text{CC}}$	V
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# NCP5386, NCP5386A, NCP5386B

## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated:  $0^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ ;  $4.75\text{ V} < V_{\text{CC}} < 5.25\text{ V}$ ; All DAC Codes;  $C_{V_{\text{CC}}} = 0.1\ \mu\text{F}$ )

Parameter	Test Conditions	Min	Typ	Max	Units
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### PWM Outputs

Output Low Voltage	Sinking 500 $\mu\text{A}$	–	–	0.15	V
Rise Time	$C_L = 20\ \text{pF}$ , $\Delta V_O = 0.3\ \text{to}\ 2.0\ \text{V}$	–	–	20	ns
Fall Time	$C_L = 20\ \text{pF}$ , $\Delta V_O = V_{\text{max}}\ \text{to}\ 0.7\ \text{V}$	–	–	20	ns
Tri-State Output Leakage	$G_x = 2.5\ \text{V}$ , $x = 1 - 4$	–	–	1.5	$\mu\text{A}$
Output Impedance – Sourcing	Maximum Resistance to $V_{\text{CC}}$	–	320	–	$\Omega$
Output Impedance – Sinking	Maximum Resistance to GND	–	140	–	$\Omega$

### DRVON

Output High Voltage	Sourcing 500 $\mu\text{A}$	3.0	–	$V_{\text{CC}}$	V
Output Low Voltage	Sinking 500 $\mu\text{A}$	–	–	0.7	mV
Rise Time	$C_L\ (\text{PCB}) = 20\ \text{pF}$ , $\Delta V_O = 10\% \text{ to } 90\%$	–	24	30	ns
Fall Time	$C_L = 20\ \text{pF}$ , $\Delta V_O = 10\% \text{ to } 90\%$	–	11	20	ns
Internal Pulldown Resistance		–	70	–	k $\Omega$

### Soft-Start

Soft-Start Pin Source Current		3.75	5.0	6.25	$\mu\text{A}$
Soft-Start Ramp Time	$C_{\text{SS}} = 0.01\ \mu\text{F}$ ; Time to 1.05 V	–	2.2	–	ms
Soft-Start Pin Discharge Voltage	DRVON pin = LO (Fault)	–	–	25	mV
VR11 Dwell Time at $V_{\text{BOOT}}$	$C_{\text{SS}} = 0.01\ \mu\text{F}$	50	–	500	$\mu\text{s}$

### DACMODE Input

Input Range for AMD Operating Mode		2.3	–	3.5	V
Input Range for VR11 Operating Mode		0.9	–	1.7	V
Input Range for VR10 Operating Mode		0	–	0.5	V

### Enable Input

Enable High Input Leakage Current	$EN = 3.3\ \text{V}$	–	–	1.0	$\mu\text{A}$
Rising Threshold	$V_{\text{UPPER}}$	0.800	–	0.920	V
Falling Threshold	$V_{\text{LOWER}}$	0.670	–	0.830	V
Hysteresis	$V_{\text{UPPER}} - V_{\text{LOWER}}$	–	130	–	mV
Enable Delay Time	Time from Enable transitioning HI to initiation of Soft-Start	1.0	–	5.0	ms
Disable Delay Time	EN Low to DRVON Low	–	150	200	ns

### Current Limit

Current Sense Amp to $I_{\text{LIM}}$ Gain	$20\ \text{mV} < (\text{CS}_x - \text{CS}_x\text{N}) < 60\ \text{mV}$ (Each CS Input Independently)	5.7	5.95	6.2	V/V
ILIM Pin Input Bias Current	$V_{\text{LIM}} = 2.0\ \text{V}$	–	–	1.0	$\mu\text{A}$
ILIM Pin Working Voltage Range		0.2	–	2.0	V
ILIM Offset Voltage	Offset extrapolated to $\text{CS}_x - \text{CS}_x\text{N} = 0$ , referred to ILIM pin	–33	17	67	mV
Delay (Note 3)		–	300	–	ns

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# NCP5386, NCP5386A, NCP5386B

## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated:  $0^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ ;  $4.75\text{ V} < V_{\text{CC}} < 5.25\text{ V}$ ; All DAC Codes;  $C_{\text{VCC}} = 0.1\ \mu\text{F}$ )

Parameter	Test Conditions	Min	Typ	Max	Units
<b>Overvoltage Protection</b>					
Overvoltage Threshold		DAC+ 160	–	DAC+ 200	mV
Delay (Note 3)		–	100	–	ns
<b>Undervoltage Protection</b>					
$V_{\text{CC}}$ UVLO Start Threshold		4	–	4.5	V
$V_{\text{CC}}$ UVLO Stop Threshold		3.8	–	4.3	V
$V_{\text{CC}}$ UVLO Hysteresis		100	215	–	mV
<b>VID Inputs</b>					
Upper Threshold	$V_{\text{UPPER}}$	–	–	800	mV
Lower Threshold	$V_{\text{LOWER}}$	300	–	–	mV
Input Bias Current		–	–	500	nA
Delay before Latching VID Change (VID De-Skewing) (Note 3)	Measured from the edge of the first VID change	500	–	800	ns
<b>Internal DAC Slew Rate Limiter</b>					
Positive Slew Rate Limit	$V_{\text{ID}}$ Step of +500 mV	–	6.3	–	mV/ $\mu\text{s}$
Negative Slew Rate Limit	$V_{\text{ID}}$ Step of –500 mV	–	–6.3	–	mV/ $\mu\text{s}$
<b>Input Supply Current</b>					
$V_{\text{CC}}$ Operating Current	EN = LOW, No PWM	–	–	20	mA
<b>Temperature Sensing</b>					
VR_FAN Upper Voltage Threshold	Fraction of $V_{\text{REF}}$ voltage above which VR_FAN output pulls low	–	$0.4 \times V_{\text{REF}}$	–	–
VR_FAN Lower Voltage Threshold	Fraction of $V_{\text{REF}}$ voltage below which VR_FAN output is open	–	$0.33 \times V_{\text{REF}}$	–	–
VR_FAN Output Saturation Voltage	$I_{\text{SINK}} = 4\text{ mA}$	–	–	0.3	V
VR_FAN Output Leakage Current	High Impedance State	–	–	1	$\mu\text{A}$
NTC Pin Bias Current		–	–	1	$\mu\text{A}$
<b>12VMON</b>					
12VMON (Rising Threshold)	Sufficient power stage supply voltage	0.728	–	0.821	V
12VMON (Falling Threshold)	Insufficient power stage supply voltage	0.643	–	0.725	V

3. Guaranteed by design. Not tested in production.

# NCP5386, NCP5386A, NCP5386B

## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T<sub>A</sub> < 85°C; 4.75 V < V<sub>CC</sub> < 5.25 V; All DAC Codes; C<sub>VCC</sub> = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
<b>VRM11 DAC</b>					
System Voltage Accuracy	1.0 V < DAC < 1.6 V 0.8 V < DAC < 1.0 V 0.5 V < DAC < 0.8 V	-	-	±0.5 ±5 ±8	% mV mV
No Load Offset Voltage from Nominal DAC Specification (NCP5386)	With CS Input ΔV <sub>IN</sub> = 0 V	-	-19	-	mV
No Load Offset Voltage from Nominal DAC Specification (NCP5386A)	With CS Input ΔV <sub>IN</sub> = 0 V	-	+20	-	mV
No Load Offset Voltage from Nominal DAC Specification (NCP5386B)	With CS Input ΔV <sub>IN</sub> = 0 V	-	50	-	mV

**Table 1: VRM11 VID Codes**

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	0	0	0	0	0	0	0	OFF	00
0	0	0	0	0	0	0	1	OFF	01
0	0	0	0	0	0	1	0	1.60000	02
0	0	0	0	0	0	1	1	1.59375	03
0	0	0	0	0	1	0	0	1.58750	04
0	0	0	0	0	1	0	1	1.58125	05
0	0	0	0	0	1	1	0	1.57500	06
0	0	0	0	0	1	1	1	1.56875	07
0	0	0	0	1	0	0	0	1.56250	08
0	0	0	0	1	0	0	1	1.55625	09
0	0	0	0	1	0	1	0	1.55000	0A
0	0	0	0	1	0	1	1	1.54375	0B
0	0	0	0	1	1	0	0	1.53750	0C
0	0	0	0	1	1	0	1	1.53125	0D
0	0	0	0	1	1	1	0	1.52500	0E
0	0	0	0	1	1	1	1	1.51875	0F
0	0	0	1	0	0	0	0	1.51250	10
0	0	0	1	0	0	0	1	1.50625	11
0	0	0	1	0	0	1	0	1.50000	12
0	0	0	1	0	0	1	1	1.49375	13
0	0	0	1	0	1	0	0	1.48750	14
0	0	0	1	0	1	0	1	1.48125	15
0	0	0	1	0	1	1	0	1.47500	16
0	0	0	1	0	1	1	1	1.46875	17
0	0	0	1	1	0	0	0	1.46250	18
0	0	0	1	1	0	0	1	1.45625	19
0	0	0	1	1	0	1	0	1.45000	1A
0	0	0	1	1	0	1	1	1.44375	1B
0	0	0	1	1	1	0	0	1.43750	1C
0	0	0	1	1	1	0	1	1.43125	1D
0	0	0	1	1	1	1	0	1.42500	1E
0	0	0	1	1	1	1	1	1.41875	1F
0	0	1	0	0	0	0	0	1.41250	20
0	0	1	0	0	0	0	1	1.40625	21
0	0	1	0	0	0	1	0	1.40000	22
0	0	1	0	0	0	1	1	1.39375	23

# NCP5386, NCP5386A, NCP5386B

**Table 1: VRM11 VID Codes**

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	0	1	0	0	1	0	0	1.38750	24
0	0	1	0	0	1	0	1	1.38125	25
0	0	1	0	0	1	1	0	1.37500	26
0	0	1	0	0	1	1	1	1.36875	27
0	0	1	0	1	0	0	0	1.36250	28
0	0	1	0	1	0	0	1	1.35625	29
0	0	1	0	1	0	1	0	1.35000	2A
0	0	1	0	1	0	1	1	1.34375	2B
0	0	1	0	1	1	0	0	1.33750	2C
0	0	1	0	1	1	0	1	1.33125	2D
0	0	1	0	1	1	1	0	1.32500	2E
0	0	1	0	1	1	1	1	1.31875	2F
0	0	1	1	0	0	0	0	1.31250	30
0	0	1	1	0	0	0	1	1.30625	31
0	0	1	1	0	0	1	0	1.30000	32
0	0	1	1	0	0	1	1	1.29375	33
0	0	1	1	0	1	0	0	1.28750	34
0	0	1	1	0	1	0	1	1.28125	35
0	0	1	1	0	1	1	0	1.27500	36
0	0	1	1	0	1	1	1	1.26875	37
0	0	1	1	1	0	0	0	1.26250	38
0	0	1	1	1	0	0	1	1.25625	39
0	0	1	1	1	0	1	0	1.25000	3A
0	0	1	1	1	0	1	1	1.24375	3B
0	0	1	1	1	1	0	0	1.23750	3C
0	0	1	1	1	1	0	1	1.23125	3D
0	0	1	1	1	1	1	0	1.22500	3E
0	0	1	1	1	1	1	1	1.21875	3F
0	1	0	0	0	0	0	0	1.21250	40
0	1	0	0	0	0	0	1	1.20625	41
0	1	0	0	0	0	1	0	1.20000	42
0	1	0	0	0	0	1	1	1.19375	43
0	1	0	0	0	1	0	0	1.18750	44
0	1	0	0	0	1	0	1	1.18125	45
0	1	0	0	0	1	1	0	1.17500	46
0	1	0	0	0	1	1	1	1.16875	47
0	1	0	0	1	0	0	0	1.16250	48
0	1	0	0	1	0	0	1	1.15625	49
0	1	0	0	1	0	1	0	1.15000	4A
0	1	0	0	1	0	1	1	1.14375	4B
0	1	0	0	1	1	0	0	1.13750	4C
0	1	0	0	1	1	0	1	1.13125	4D
0	1	0	0	1	1	1	0	1.12500	4E
0	1	0	0	1	1	1	1	1.11875	4F
0	1	0	1	0	0	0	0	1.11250	50
0	1	0	1	0	0	0	1	1.10625	51
0	1	0	1	0	0	1	0	1.10000	52
0	1	0	1	0	0	1	1	1.09375	53
0	1	0	1	0	1	0	0	1.08750	54
0	1	0	1	0	1	0	1	1.08125	55

# NCP5386, NCP5386A, NCP5386B

**Table 1: VRM11 VID Codes**

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	1	0	1	0	1	1	0	1.07500	56
0	1	0	1	0	1	1	1	1.06875	57
0	1	0	1	1	0	0	0	1.06250	58
0	1	0	1	1	0	0	1	1.05625	59
0	1	0	1	1	0	1	0	1.05000	5A
0	1	0	1	1	0	1	1	1.04375	5B
0	1	0	1	1	1	0	0	1.03750	5C
0	1	0	1	1	1	0	1	1.03125	5D
0	1	0	1	1	1	1	0	1.02500	5E
0	1	0	1	1	1	1	1	1.01875	5F
0	1	1	0	0	0	0	0	1.01250	60
0	1	1	0	0	0	0	1	1.00625	61
0	1	1	0	0	0	1	0	1.00000	62
0	1	1	0	0	0	1	1	0.99375	63
0	1	1	0	0	1	0	0	0.98750	64
0	1	1	0	0	1	0	1	0.98125	65
0	1	1	0	0	1	1	0	0.97500	66
0	1	1	0	0	1	1	1	0.96875	67
0	1	1	0	1	0	0	0	0.96250	68
0	1	1	0	1	0	0	1	0.95625	69
0	1	1	0	1	0	1	0	0.95000	6A
0	1	1	0	1	0	1	1	0.94375	6B
0	1	1	0	1	1	0	0	0.93750	6C
0	1	1	0	1	1	0	1	0.93125	6D
0	1	1	0	1	1	1	0	0.92500	6E
0	1	1	0	1	1	1	1	0.91875	6F
0	1	1	1	0	0	0	0	0.91250	70
0	1	1	1	0	0	0	1	0.90625	71
0	1	1	1	0	0	1	0	0.90000	72
0	1	1	1	0	0	1	1	0.89375	73
0	1	1	1	0	1	0	0	0.88750	74
0	1	1	1	0	1	0	1	0.88125	75
0	1	1	1	0	1	1	0	0.87500	76
0	1	1	1	0	1	1	1	0.86875	77
0	1	1	1	1	0	0	0	0.86250	78
0	1	1	1	1	0	0	1	0.85625	79
0	1	1	1	1	0	1	0	0.85000	7A
0	1	1	1	1	0	1	1	0.84375	7B
0	1	1	1	1	1	0	0	0.83750	7C
0	1	1	1	1	1	0	1	0.83125	7D
0	1	1	1	1	1	1	0	0.82500	7E
0	1	1	1	1	1	1	1	0.81875	7F
1	0	0	0	0	0	0	0	0.81250	80
1	0	0	0	0	0	0	1	0.80625	81
1	0	0	0	0	0	1	0	0.80000	82
1	0	0	0	0	0	1	1	0.79375	83
1	0	0	0	0	1	0	0	0.78750	84
1	0	0	0	0	1	0	1	0.78125	85
1	0	0	0	0	1	1	0	0.77500	86
1	0	0	0	0	1	1	1	0.76875	87

# NCP5386, NCP5386A, NCP5386B

**Table 1: VRM11 VID Codes**

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
1	0	0	0	1	0	0	0	0.76250	88
1	0	0	0	1	0	0	1	0.75625	89
1	0	0	0	1	0	1	0	0.75000	8A
1	0	0	0	1	0	1	1	0.74375	8B
1	0	0	0	1	1	0	0	0.73750	8C
1	0	0	0	1	1	0	1	0.73125	8D
1	0	0	0	1	1	1	0	0.72500	8E
1	0	0	0	1	1	1	1	0.71875	8F
1	0	0	1	0	0	0	0	0.71250	90
1	0	0	1	0	0	0	1	0.70625	91
1	0	0	1	0	0	1	0	0.70000	92
1	0	0	1	0	0	1	1	0.69375	93
1	0	0	1	0	1	0	0	0.68750	94
1	0	0	1	0	1	0	1	0.68125	95
1	0	0	1	0	1	1	0	0.67500	96
1	0	0	1	0	1	1	1	0.66875	97
1	0	0	1	1	0	0	0	0.66250	98
1	0	0	1	1	0	0	1	0.65625	99
1	0	0	1	1	0	1	0	0.65000	9A
1	0	0	1	1	0	1	1	0.64375	9B
1	0	0	1	1	1	0	0	0.63750	9C
1	0	0	1	1	1	0	1	0.63125	9D
1	0	0	1	1	1	1	0	0.62500	9E
1	0	0	1	1	1	1	1	0.61875	9F
1	0	1	0	0	0	0	0	0.61250	A0
1	0	1	0	0	0	0	1	0.60625	A1
1	0	1	0	0	0	1	0	0.60000	A2
1	0	1	0	0	0	1	1	0.59375	A3
1	0	1	0	0	1	0	0	0.58750	A4
1	0	1	0	0	1	0	1	0.58125	A5
1	0	1	0	0	1	1	0	0.57500	A6
1	0	1	0	0	1	1	1	0.56875	A7
1	0	1	0	1	0	0	0	0.56250	A8
1	0	1	0	1	0	0	1	0.55625	A9
1	0	1	0	1	0	1	0	0.55000	AA
1	0	1	0	1	0	1	1	0.54375	AB
1	0	1	0	1	1	0	0	0.53750	AC
1	0	1	0	1	1	0	1	0.53125	AD
1	0	1	0	1	1	1	0	0.52500	AE
1	0	1	0	1	1	1	1	0.51875	AF
1	0	1	1	0	0	0	0	0.51250	B0
1	0	1	1	0	0	0	1	0.50625	B1
1	0	1	1	0	0	1	0	0.50000	B2
1	1	1	1	1	1	1	0	OFF	FE
1	1	1	1	1	1	1	1	OFF	FF
								OFF	B3 to FD



# NCP5386, NCP5386A, NCP5386B

## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T<sub>A</sub> < 85°C; 4.75 V < V<sub>CC</sub> < 5.25 V; All DAC Codes; C<sub>VCC</sub> = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
<b>VRM10 DAC</b>					
System Voltage Accuracy	1.0 V < DAC < 1.6 V 0.83125 V < DAC < 1.0 V	-	-	±0.5 ±5	% mV
No Load Offset Voltage from Nominal DAC Specification	With CS Input ΔV <sub>IN</sub> = 0 V	-	-19	-	mV
No Load Offset Voltage from Nominal DAC Specification (NCP5386A)	With CS Input ΔV <sub>IN</sub> = 0 V	-	+20	-	mV
No Load Offset Voltage from Nominal DAC Specification (NCP5386B)	With CS Input ΔV <sub>IN</sub> = 0 V	-	50	-	mV

**Table 2: VRM10 VID Codes**

VID4 400 mV	VID3 200 mV	VID2 100 mV	VID1 50 mV	VID0 25 mV	VID5 12.5 mV	VID6 6.25 mV	Nominal DAC Voltage (V)
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375
0	1	1	1	1	0	1	1.48750
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375

# NCP5386, NCP5386A, NCP5386B

**Table 2: VRM10 VID Codes**

VID4 400 mV	VID3 200 mV	VID2 100 mV	VID1 50 mV	VID0 25 mV	VID5 12.5 mV	VID6 6.25 mV	Nominal DAC Voltage (V)
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875
1	0	1	0	0	0	1	1.36250
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000

# NCP5386, NCP5386A, NCP5386B

**Table 2: VRM10 VID Codes**

VID4 400 mV	VID3 200 mV	VID2 100 mV	VID1 50 mV	VID0 25 mV	VID5 12.5 mV	VID6 6.25 mV	Nominal DAC Voltage (V)
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375
0	0	1	0	0	0	1	0.98750
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.96250
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.88750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

# NCP5386, NCP5386A, NCP5386B

## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T<sub>A</sub> < 85°C; 4.75 V < V<sub>CC</sub> < 5.25 V; All DAC Codes; C<sub>VCC</sub> = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
<b>AMD DAC</b>					
System Voltage Accuracy	0.8 V < DAC < 1.55 V	-	-	±0.5	%
No Load Offset Voltage from Nominal DAC Specification	With CS Input ΔV <sub>IN</sub> = 0 V	-	20	-	mV

**Table 3: AMD VID Codes**

VID4	VID3	VID2	VID1	VID0	Nominal V <sub>OUT</sub> (V)	Tolerance
0	0	0	0	0	1.550	±0.5 %
0	0	0	0	1	1.525	±0.5 %
0	0	0	1	0	1.500	±0.5 %
0	0	0	1	1	1.475	±0.5 %
0	0	1	0	0	1.450	±0.5 %
0	0	1	0	1	1.425	±0.5 %
0	0	1	1	0	1.400	±0.5 %
0	0	1	1	1	1.375	±0.5 %
0	1	0	0	0	1.350	±0.5 %
0	1	0	0	1	1.325	±0.5 %
0	1	0	1	0	1.300	±0.5 %
0	1	0	1	1	1.275	±0.5 %
0	1	1	0	0	1.250	±0.5 %
0	1	1	0	1	1.225	±0.5 %
0	1	1	1	0	1.200	±0.5 %
0	1	1	1	1	1.175	±0.5 %
1	0	0	0	0	1.150	±0.5 %
1	0	0	0	1	1.125	±0.5 %
1	0	0	1	0	1.100	±0.5 %
1	0	0	1	1	1.075	±0.5 %
1	0	1	0	0	1.050	±0.5 %
1	0	1	0	1	1.025	±0.5 %
1	0	1	1	0	1.000	±0.5 %
1	0	1	1	1	0.975	±5.0 mV
1	1	0	0	0	0.950	±5.0 mV
1	1	0	0	1	0.925	±5.0 mV
1	1	0	1	0	0.900	±5.0 mV
1	1	0	1	1	0.875	±5.0 mV
1	1	1	0	0	0.850	±5.0 mV
1	1	1	0	1	0.825	±5.0 mV
1	1	1	1	0	0.800	±5.0 mV
1	1	1	1	1	Shutdown	-

TYPICAL CHARACTERISTICS

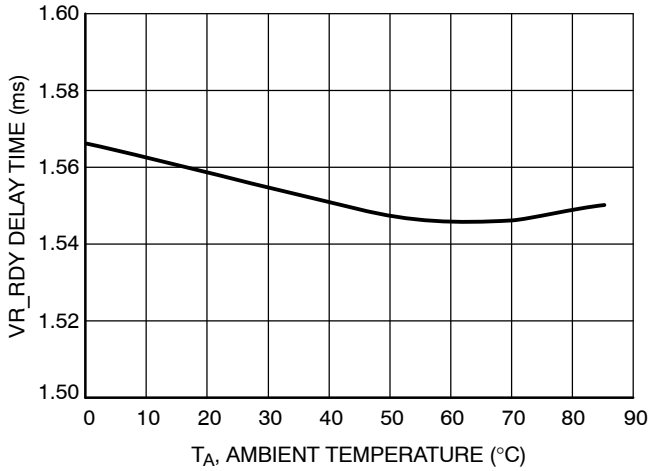


Figure 5. PWM Output Resistance vs. Ambient Temperature

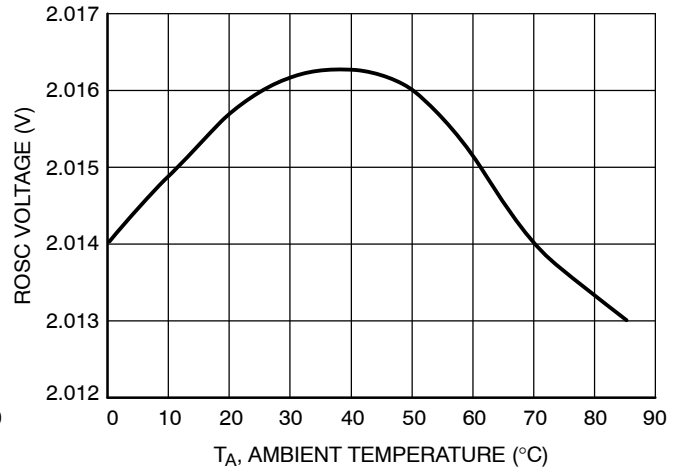


Figure 6. ROSC Voltage vs. Ambient Temperature

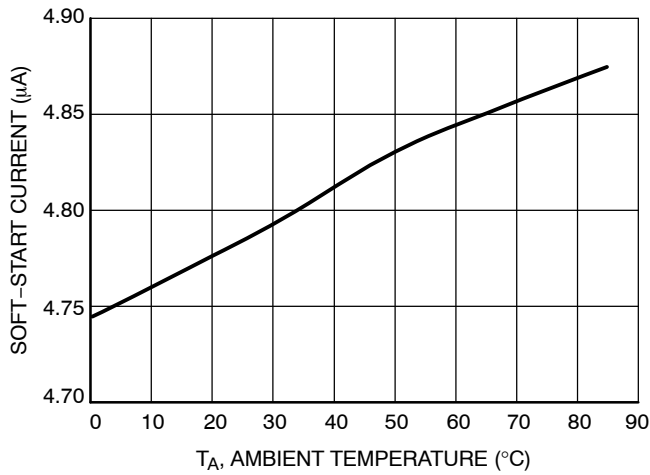


Figure 7. Soft-start Current vs. Ambient Temperature

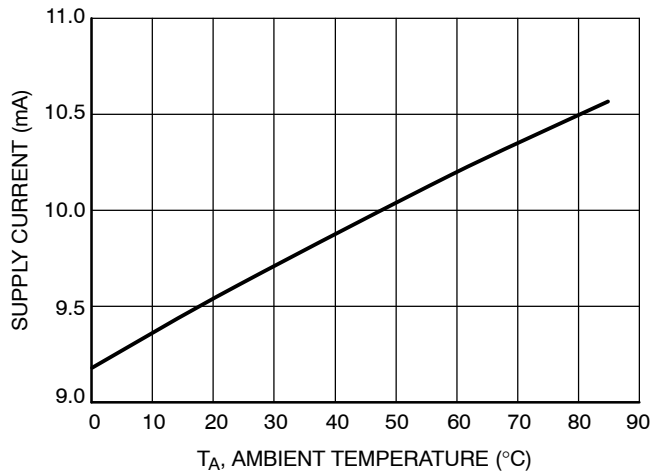


Figure 8. Supply Current vs. Ambient Temperature

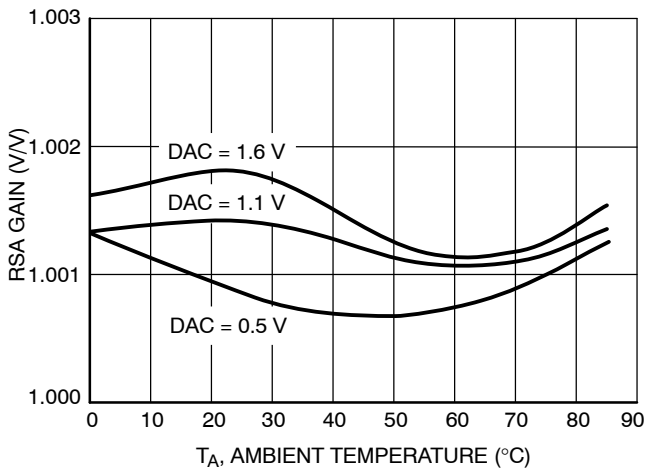


Figure 9. RSA Gain vs. Ambient Temperature

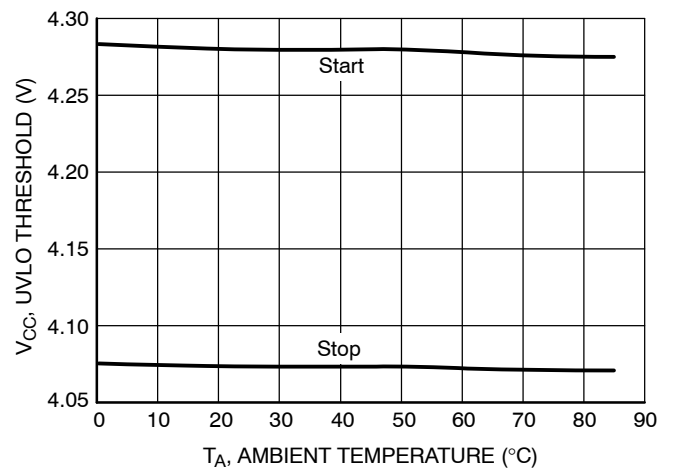


Figure 10. UVLO Threshold vs. Ambient Temperature

TYPICAL CHARACTERISTICS

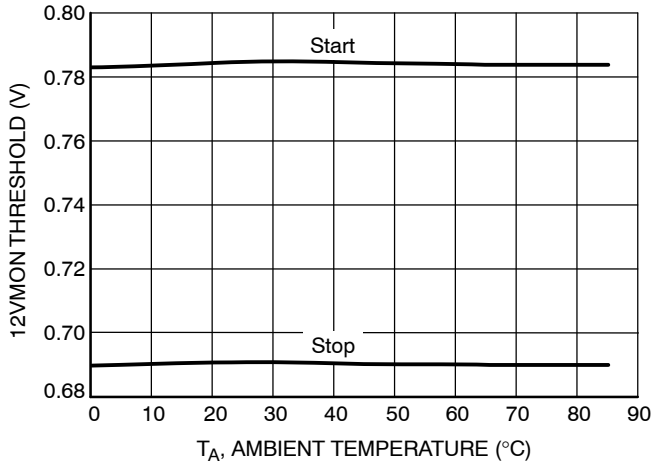


Figure 11. 12VMON Threshold vs. Ambient Temperature

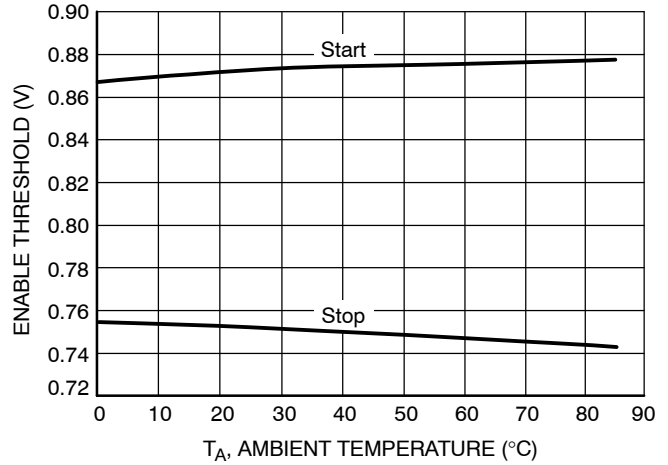


Figure 12. Enable Threshold vs. Ambient Temperature

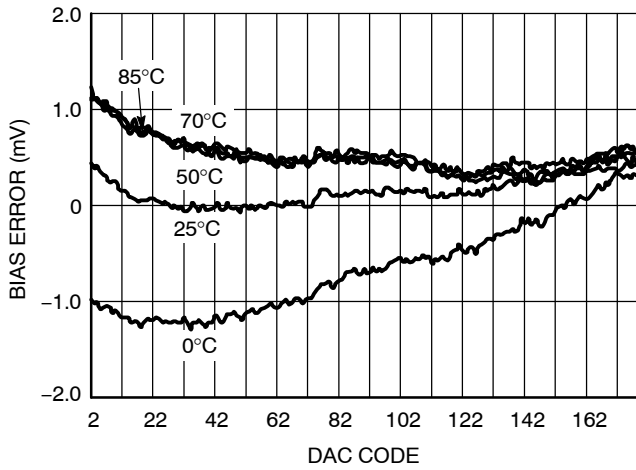


Figure 13. RSA Bias

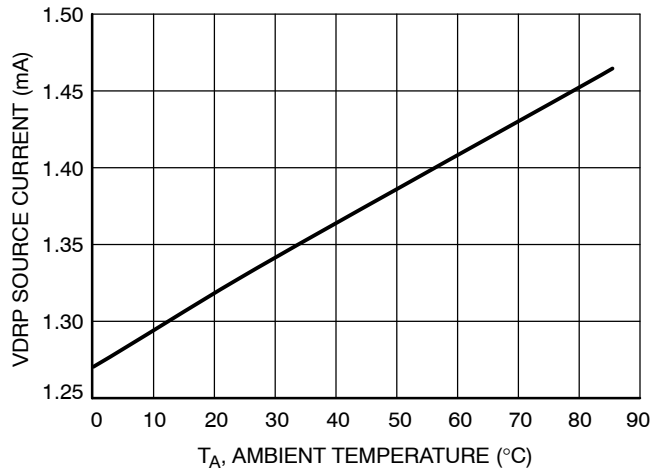


Figure 14. VDRP Source Current vs. Ambient Temperature

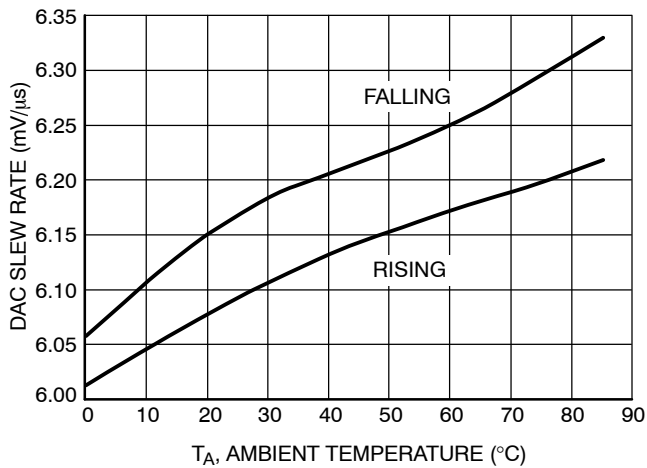


Figure 15. DAC Slew Rate vs. Ambient Temperature

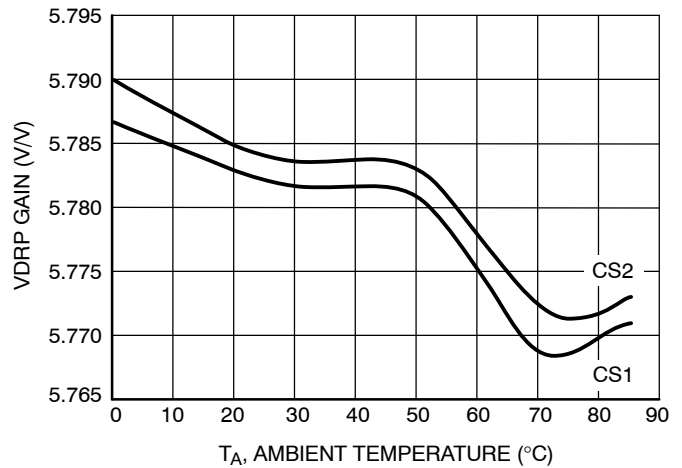


Figure 16. VDRP Gain vs. Ambient Temperature

TYPICAL CHARACTERISTICS

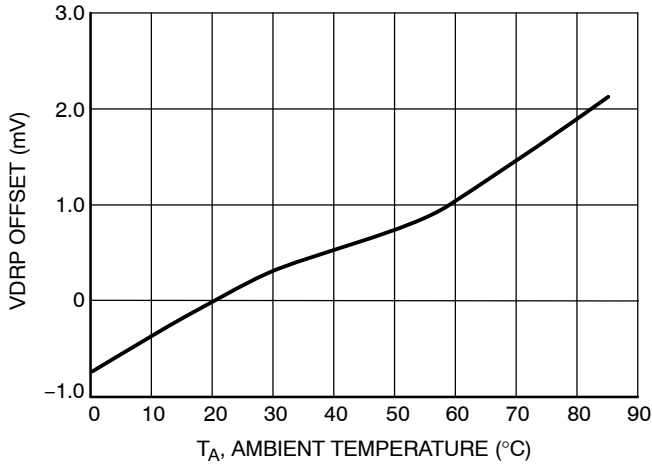


Figure 17. VDRP Offset vs. Ambient Temperature

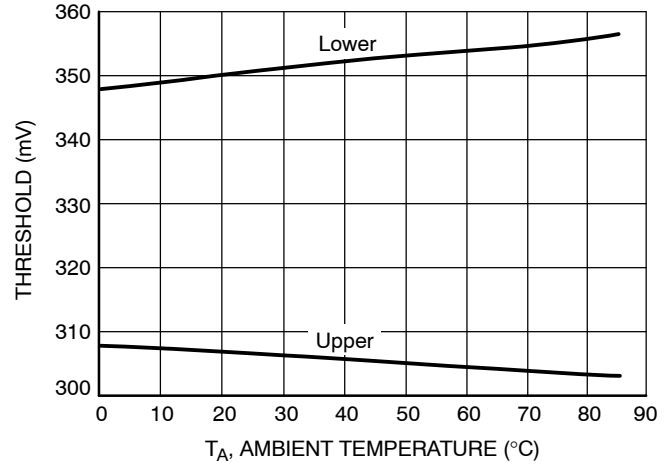


Figure 18. VR\_RDY Thresholds vs. Ambient Temperature

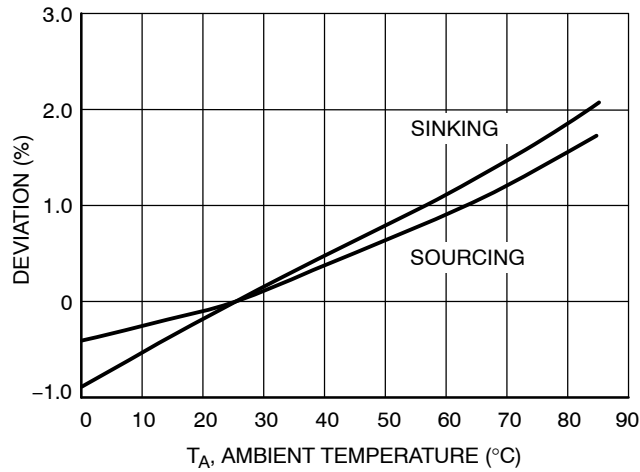


Figure 19. PWM Output Resistance vs. Ambient Temperature

**FUNCTIONAL DESCRIPTION**

**General**

The NCP5386/A/B dual edge modulated multiphase PWM controller is specifically designed with the necessary features for a high current VR10, VR11 or AMD CPU and chipset power system. The IC consists of the following blocks: Precision Programmable DAC, Differential Remote Voltage Sense Amplifier, High Performance Voltage Error Amplifier, Differential Current Feedback Amplifiers, Precision Oscillator and Triangle Wave Generators, and PWM Comparators. Protection features include Undervoltage Lockout, Soft-Start, Overcurrent Protection, Overvoltage Protection, and Power Good Monitor.

**Remote Output Sensing Amplifier (RSA)**

A true differential amplifier allows the NCP5386/A/B to measure VCore voltage feedback with respect to the Vcore ground reference point by connecting the Vcore reference point to VS+, and the Vcore ground reference point to VS-. This configuration keeps ground potential differences between the local controller ground and the Vcore ground reference point from affecting regulation of Vcore between VCore and VCore ground reference points. The RSA also subtracts the DAC (minus VID offset) voltage, thereby producing an unamplified output error voltage at the DIFFOUT pin. This output also has a 1.3 V bias voltage to allow both positive and negative error voltages.

**Precision Programmable DAC**

A precision programmable DAC is provided. This DAC has 0.5% accuracy over the entire operating temperature range of the part. The DAC can be programmed to support either Intel VR10 or VR11 or AMD K8 specifications. A program selection pin is provided to accomplish this. This pin also sets the startup mode of operation. Connect this pin to 1.25 V to select the VR11 DAC table and startup mode. Connect this pin to ground to select the VR10 DAC table and the VR11 startup mode. Connect this pin to VREF to select the AMD DAC table and startup mode.

**High Performance Voltage Error Amplifier**

The error amplifier is designed to provide high slew rate and bandwidth. Although not required when operating as the controller of a voltage regulator, a capacitor from COMP to VFB is required for stable unity gain test configurations.

**Gate Driver Outputs and 1/2 Phase Operation**

The part can be configured to run in 1- or 2-Phase mode. In 2-phase mode, phases 1 and 2 should be used to drive the external gate drivers as shown in the 2-phase Applications

Schematic. In 1-Phase mode, gate output G2 must be left open as shown in the 1-phase Applications Schematic. The CS2 and CS2N inputs should be connected to CS1N. The following truth table summarizes the modes of operation:

Mode	Gate Output Connections	
	G1	G2
1-Phase	Normal	OPEN
2-Phase	Normal	Normal

**These are the only allowable connection schemes to program the modes of operation.**

**Differential Current Sense Amplifiers**

Two differential amplifiers are provided to sense the output current of each phase. The inputs of each current sense amplifier must be connected across the current sensing element of the phase controlled by the corresponding gate output (G1 or G2). **If a phase is unused, the differential inputs to that phase's current sense amplifier must be shorted together and connected to CS1N as shown in the 1-Phase Application Schematics.**

A voltage is generated across the current sense element (such as an inductor or sense resistor) by the current flowing in that phase. The output of the current sense amplifiers are used to control three functions. First, the output controls the adaptive voltage positioning, where the output voltage is actively controlled according to the output current. In this function, all of the current sense outputs are summed so that the total output current is used for output voltage positioning. Second, the output signal is fed to the current limit circuit. This again is the summed current of all phases in operation. Finally, the individual phase current is connected to the PWM comparator. In this way current balance is accomplished.

**Oscillator and Triangle Wave Generator**

A programmable precision oscillator is provided. The oscillator's frequency is programmed by the resistance connected from the ROSC pin to ground. The user will usually form this resistance from two resistors in order to create a voltage divider that uses the ROSC output voltage as the reference for creating the current limit setpoint voltage. The oscillator frequency range is 100 kHz/phase to 1.0 MHz/phase. The oscillator generates up to 4 triangle waveforms (symmetrical rising and falling slopes) between 1.3 V and 2.3 V. The triangle waves have a phase delay between them such that for 2-phase operation the PWM outputs are separated by 180 angular degrees, respectively.



**PWM Comparators with Hysteresis**

Four PWM comparators receive the error amplifier output signal at their noninverting input. Each comparator receives one of the triangle waves offset by 1.3 V at its inverting input. The output of the comparator generates the PWM outputs G1 and G2.

During steady state operation, the duty cycle will center on the valley of the triangle waveform, with steady state duty cycle calculated by  $V_{OUT}/V_{IN}$ . During a transient event, both high and low comparator output transitions shift phase to the points where the error amplifier output intersects the down and up ramp of the triangle wave.

**PROTECTION FEATURES**

**Undervoltage Lockout**

An undervoltage lockout (UVLO) senses the  $V_{CC}$  input. During powerup, the input voltage to the controller is monitored, and the PWM outputs and the soft-start circuit are disabled until the input voltage exceeds the threshold voltage of the UVLO comparator. The UVLO comparator incorporates hysteresis to avoid chattering, since  $V_{CC}$  is likely to decrease as soon as the converter initiates soft-start.

**Overcurrent Shutdown**

A programmable overcurrent function is incorporated within the IC. A comparator and latch make up this function. The inverting input of the comparator is connected to the ILIM pin. The voltage at this pin sets the maximum output current the converter can produce. The ROSC pin provides a convenient and accurate reference voltage from which a resistor divider can create the overcurrent setpoint voltage. Although not actually disabled, tying the ILIM pin directly to the ROSC pin sets the limit above useful levels – effectively disabling overcurrent shutdown. The comparator noninverting input is the summed current information from the current sense

amplifiers. The overcurrent latch is set when the current information exceeds the voltage at the ILIM pin. The outputs are immediately disabled, the VR\_RDY and DRVON pins are pulled low, and the soft-start is pulled low. The outputs will remain disabled until the  $V_{CC}$  voltage is removed and re-applied, or the ENABLE input is brought low and then high.

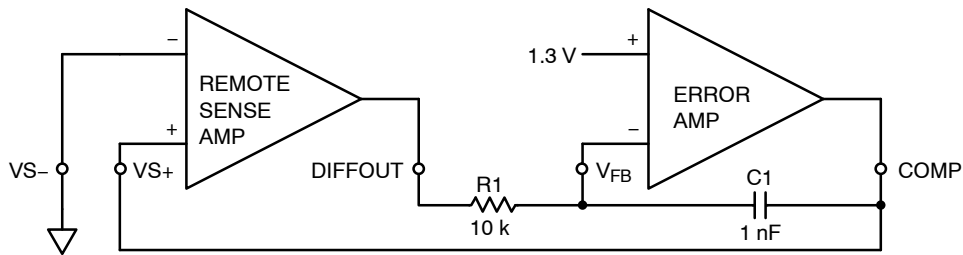
**Overvoltage Protection and Power Good Monitor**

An output voltage monitor is incorporated. During normal operation, if the voltage at the DIFFOUT pin exceeds 1.3 V, the VR\_RDY pin goes low, the DRVON signal remains high, the PWM outputs are set low. The outputs will remain disabled until the  $V_{CC}$  voltage is removed and reapplied. During normal operation, if the output voltage falls more than 300 mV below the DAC setting, the VR\_RDY pin will be set low until the output rises.

**Soft-Start**

The NCP5386 incorporates an externally programmable soft-start. The soft-start circuit works by controlling the ramp-up of the DAC voltage during powerup. The initial soft-start pin voltage is 0 V. The soft-start circuitry clamps the DAC input of the Remote Sense Amplifier to the SS pin voltage until the SS pin voltage exceeds the DAC setting minus VID offset thereafter. The soft-start pin is pulled to 0 V.

There are two possible soft-start modes: AMD and VR11. AMD mode simply ramps  $V_{core}$  from 0 V directly to the DAC setting at the rate set by the capacitor connected to the SS pin. The VR11 mode ramps  $V_{core}$  to 1.1 V at the SS capacitor charge rate, pauses at 1.1 V for 170  $\mu$ s, reads the VID pins to determine the DAC setting, then ramps  $V_{core}$  to the final DAC setting at the Dynamic VID slew rate of 7.3 mV/ $\mu$ s. Typical AMD and VR11 soft-start sequences are shown in the following graphs.



**Figure 20. DAC Servo Evaluation Circuit**

# NCP5386, NCP5386A, NCP5386B

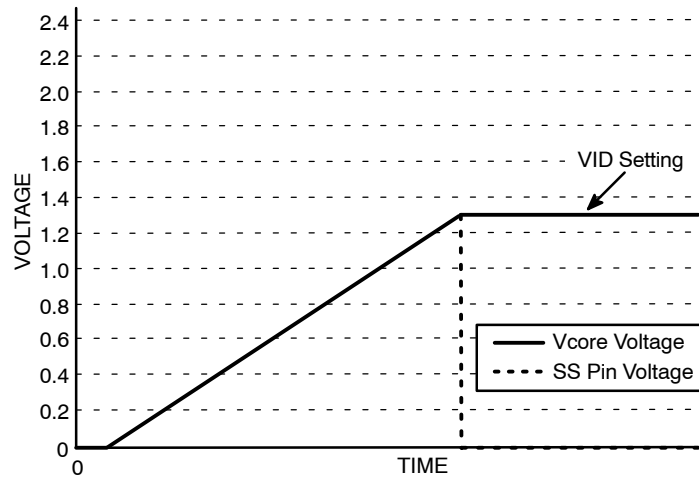


Figure 21. Typical AMD Soft-Start Sequence to Vcore = 1.3 V

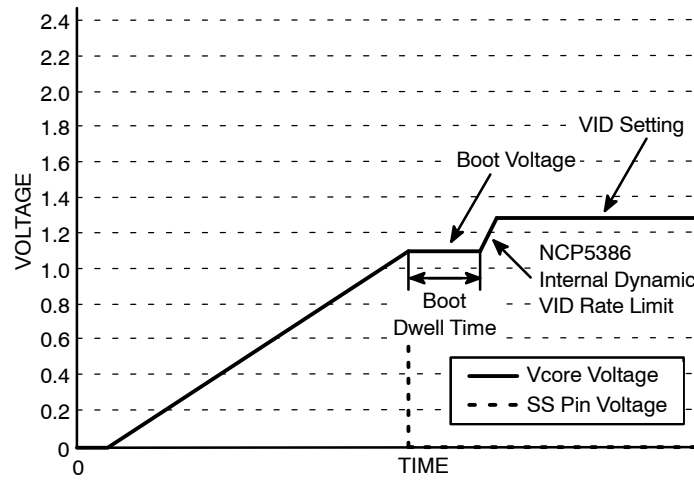


Figure 22. Typical VR10 & VR11 Soft-Start Sequence to Vcore = 1.3 V