Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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NCP5387

2/3/4 Phase Controller for CPU Applications

The NCP5387 is a two−, three−, or four−phase buck controller which combines differential voltage and current sensing, and adaptive voltage positioning to power both AMD and Intel processors. Dual−edge pulse−width modulation (PWM) combined with inductor current sensing reduces system cost by providing the fastest initial response to transient load events. Dual−edge multi−phase modulation reduces total bulk and ceramic output capacitance required to satisfy transient load−line regulation.

A high performance operational error amplifier is provided, which allows easy compensation of the system. The proprietary method of Dynamic Reference Injection (Patented) makes the error amplifier compensation virtually independent of the system response to VID changes, eliminating tradeoffs between overshoot and dynamic VID performance.

Features

- Meets Intel's VR 10.0 and 11.0 and AMD Specifications
- Dual−Edge PWM for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Supports both VR11 and Legacy Soft−Start Modes
- Dynamic Reference Injection (Patented)
- DAC Range from 0.5 V to 1.6 V
- ±0.5% System Voltage Accuracy from 1.0 V to 1.6 V
- True Differential Remote Voltage Sensing Amplifier
- Phase−to−Phase Current Balancing
- "Lossless" Differential Inductor Current Sensing
- Differential Current Sense Amplifiers for each Phase
- Adaptive Voltage Positioning (AVP)
- Frequency Range: 100 kHz – 1.0 MHz
- OVP with Resettable, 8 Event Delayed Latch
- Threshold Sensitive Enable Pin for VTT Sensing
- Power Good Output with Internal Delays
- Programmable Soft−Start Time
- This is a Pb−Free Device*

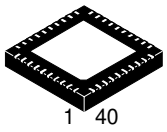
Applications

- Desktop Processors

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com



40 PIN QFN, 6x6
MN SUFFIX
CASE 488AR

MARKING DIAGRAM

NCP5387 = Specific Device Code
AA = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪/G = Pb−Free Package

*Pin 41 is the thermal pad on the bottom of the device.

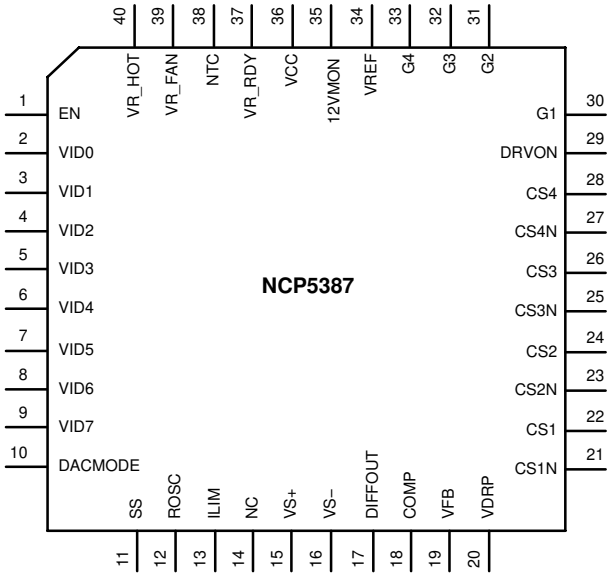
ORDERING INFORMATION

Device	Package	Shipping†
NCP5387MNR2G*	QFN−40 (Pb−Free)	2500 / Tape & Reel

*Temperature Range: 0°C to 85°C

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN CONNECTIONS



(Top View)

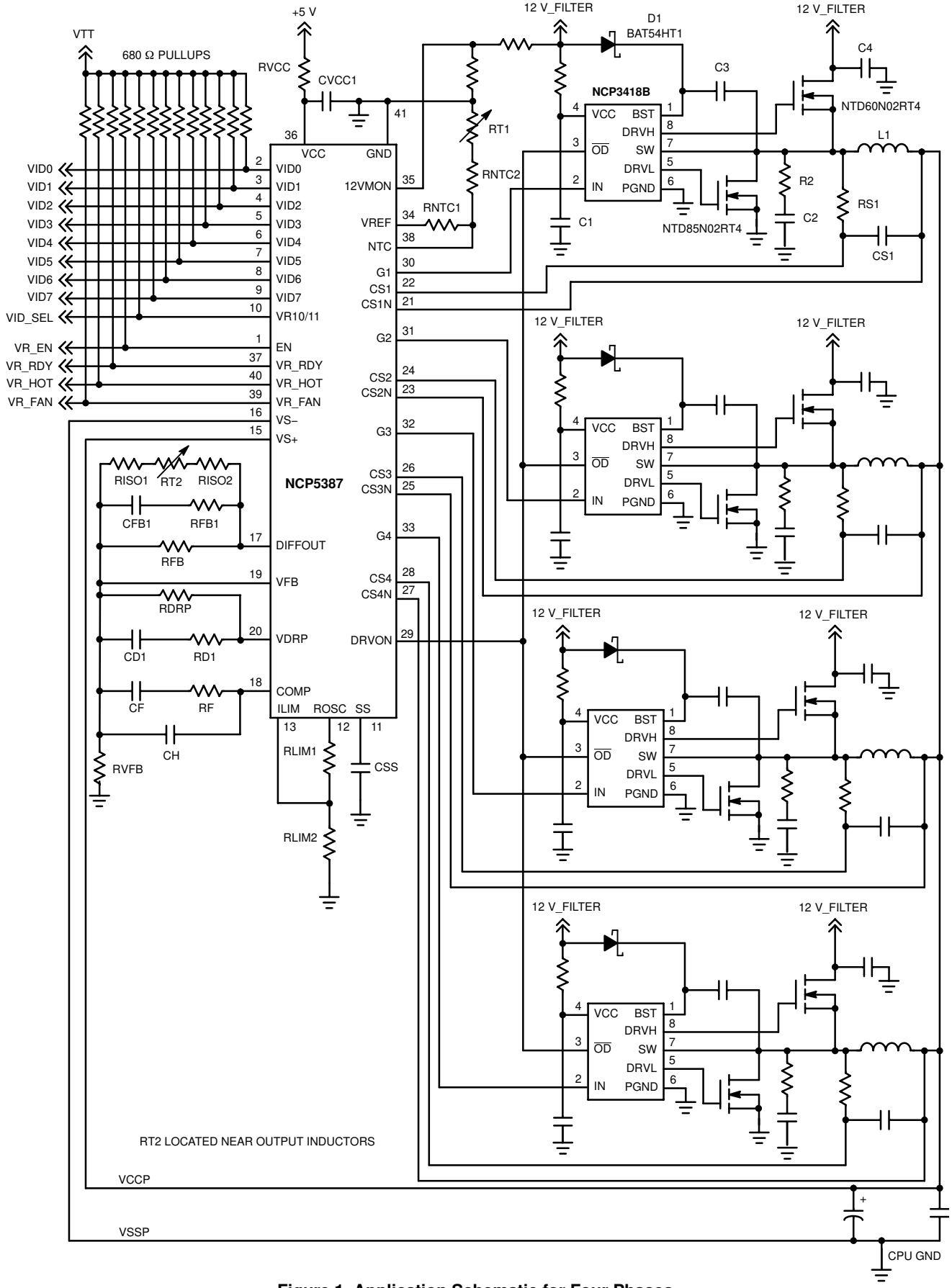


Figure 1. Application Schematic for Four Phases

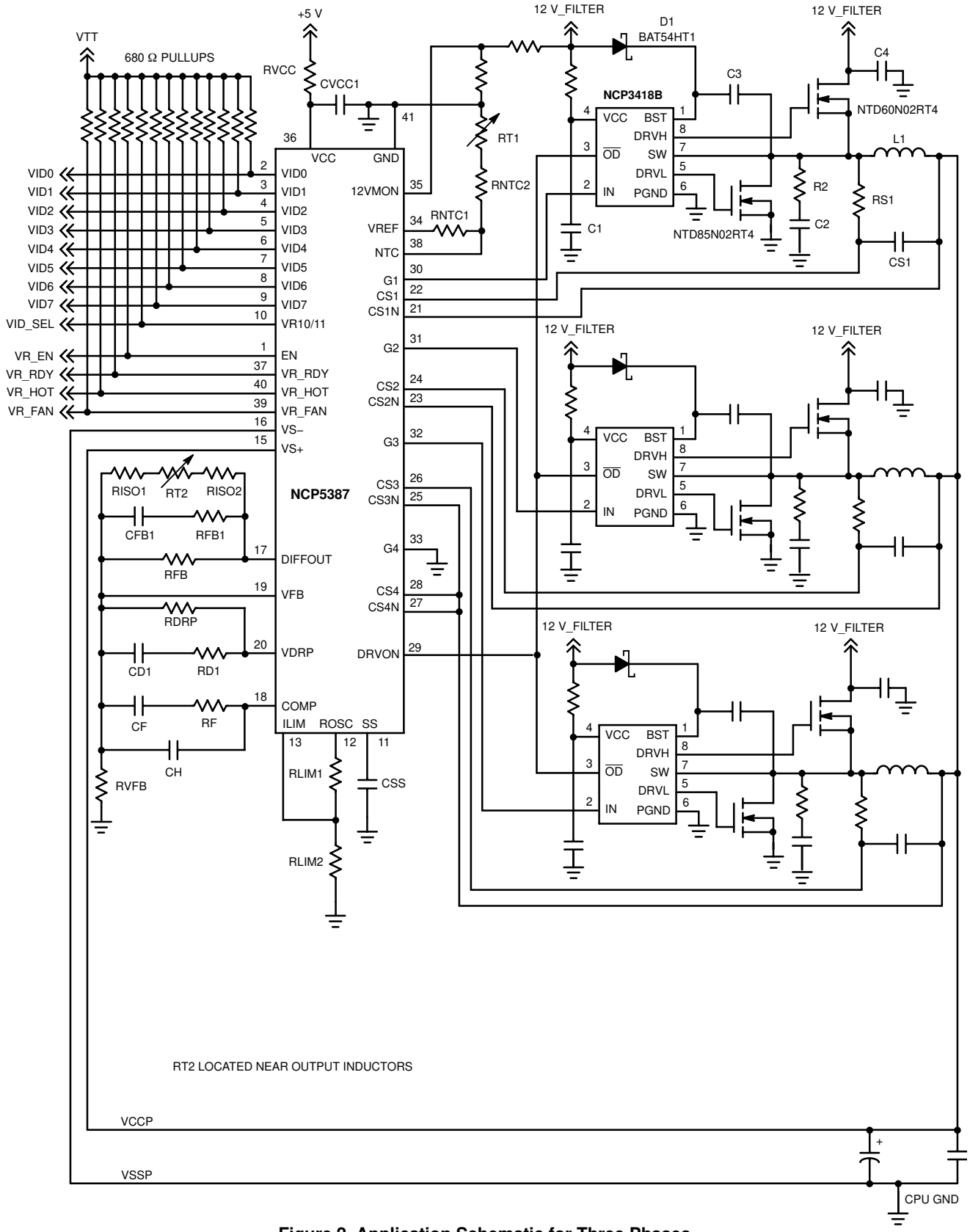


Figure 2. Application Schematic for Three Phases

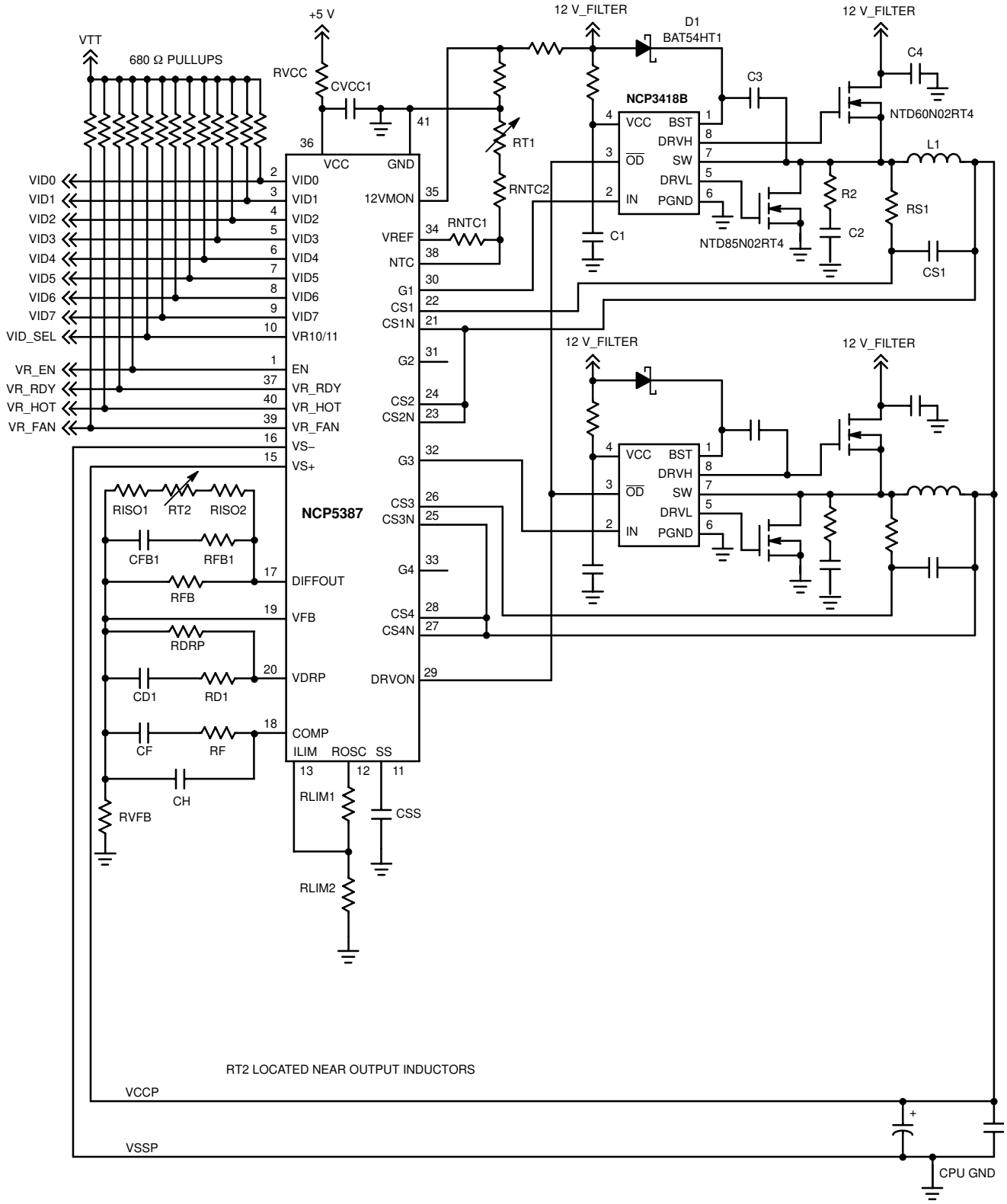


Figure 3. Application Schematic for Two Phases

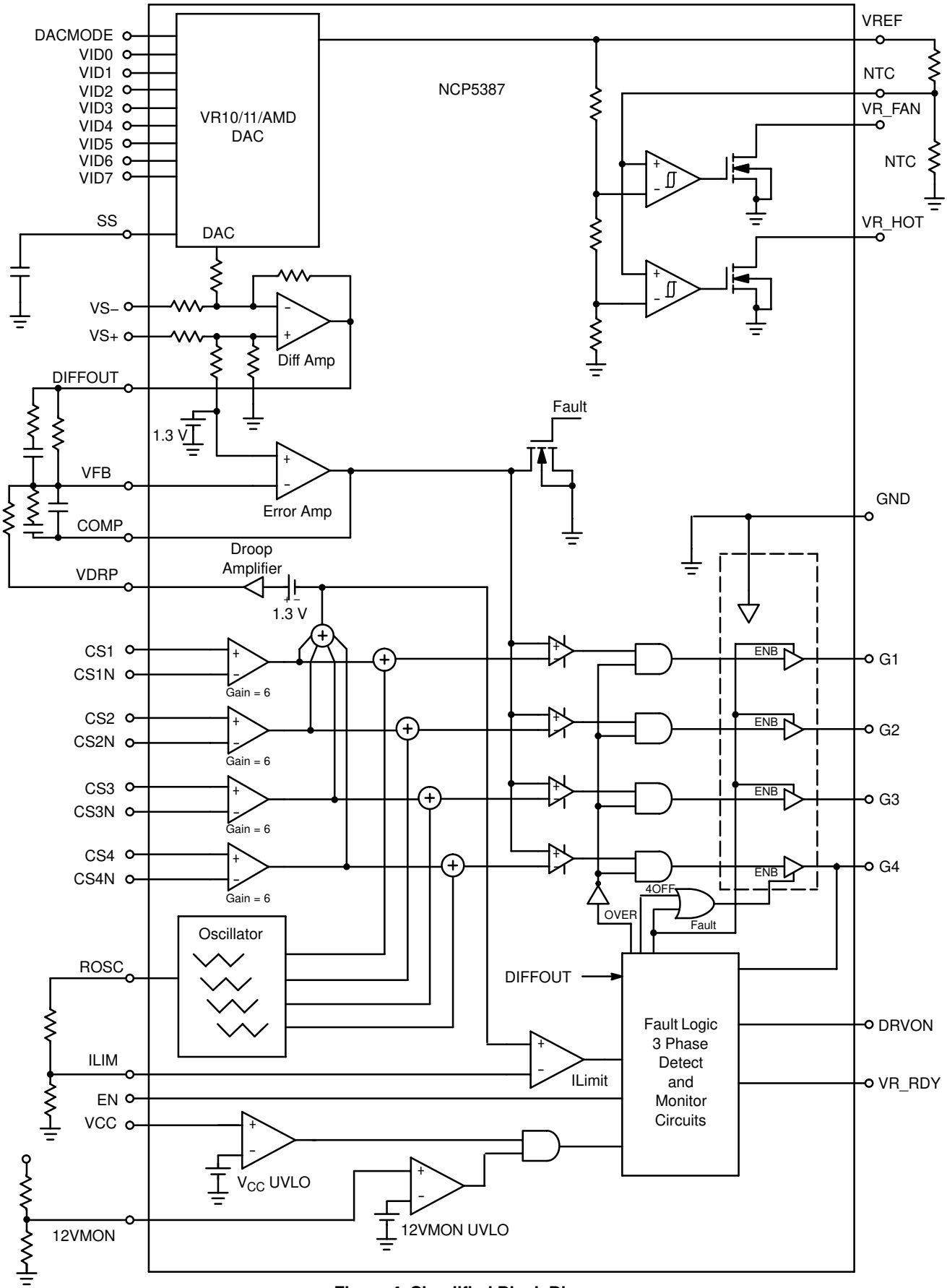


Figure 4. Simplified Block Diagram

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	EN	Pull this pin high to enable controller. Pull this pin low to disable controller. Either an open−collector output (with a pull−up resistor) or a logic gate (CMOS or totem−pole output) may be used to drive this pin. A Low−to−High transition on this pin will initiate a soft start. Connect this pin directly to VREF if the Enable function is not required. 20 MHz filtering at this pin is required.
2 – 9	VID0−VID7	Voltage ID DAC inputs
10	DACMODE	VRM select bit
11	SS	A capacitor from this pin to ground programs the soft−start time.
12	ROSC	A resistance from this pin to ground programs the oscillator frequency. Also, this pin supplies an output voltage of 2 V which may be used to form a voltage divider to the ILIM pin to set the over−current shutdown threshold as shown in the Applications Schematics.
13	ILIM	Over−current shutdown threshold. To program the shutdown threshold, connect this pin to the ROSC pin via a resistor divider as shown in the Applications Schematics. To disable the over−current feature, connect this pin directly to the ROSC pin. To guarantee correct operation, this pin should only be connected to the voltage generated by the ROSC pin; do not connect this pin to any externally generated voltages.
14	NC	Do not connect anything to this pin.
15	VS+	Non−inverting input to the internal differential remote sense amplifier
16	VS−	Inverting input to the internal differential remote sense amplifier
17	DIFFOUT	Output of the differential remote sense amplifier
18	COMP	Output of the error amplifier, and the non−inverting input of the PWM comparators
19	VFB	Error amplifier inverting input. Connect a resistor from this pin to DIFFOUT. The value of this resistor and the amount of current from the droop resistor (RDRP) will set the amount of output voltage droop (AVP) during load.
20	VDRP	Current signal output for Adaptive Voltage Positioning (AVP). The voltage of this pin above the 1.3 V internal offset voltage is proportional to the output current. Connect a resistor from this pin to VFB to set the amount of AVP current into the feedback resistor (RFB) to produce an output voltage droop. Leave this pin open for no AVP.
21, 23, 25, 27	CSxN	Inverting input to current sense amplifier #x, x = 1, 2, 3, 4.
22, 24, 26, 28	CSx	Non−inverting input to current sense amplifier #x, x = 1, 2, 3, 4.
29	DRVON	Output to enable Gate Drivers
30 – 33	G1 – G4	PWM output pulses to gate drivers
34	VREF	Voltage reference output. This pin is used for remote temperature sensing as shown in the Applications Schematic.
35	12VMON	Second UVLO monitor for monitoring the power stage supply rail
36	VCC	Power for the internal control circuits.
37	VR_RDY	Voltage Regulator Ready (Power Good) output. Open drain output that is high when the output is regulating.
38	NTC	Remote temperature sense connection. Connect an NTC thermistor from this pin to GND and a resistor from this pin to VREF. As the NTC's temperature increases, the voltage on this pin will decrease.
39	VR_FAN	Open drain output that will be low impedance when the voltage at the NTC pin is above the specified threshold. This pin will transition to a high impedance state when the voltage at the NTC pin decreases below the specified threshold. This pin requires an external pull−up resistor.
40	VR_HOT	Open drain output that will be low impedance when the voltage at the NTC pin is above the specified threshold. This pin will transition to a high impedance state when the voltage at the NTC pin decreases below the specified threshold. This pin requires an external pull−up resistor.
41	GND	Power supply return (QFN Flag)

MAXIMUM RATINGS

Electrical Information

Pin Symbol	V_{MAX} (V)	V_{MIN} (V)	I_{SOURCE} (mA)	I_{SINK} (mA)
COMP	5.5	–0.3	10	10
VDRP	5.5	–0.3	5	5
VS+	2.0	GND – 300 mV	1	1
VS–	2.0	GND – 300 mV	1	1
DIFFOUT	5.5	–0.3	20	20
VR_RDY, VR_HOT, VR_FAN	5.5	–0.3	N/A	20
VCC	7.0	–0.3	N/A	10
ROSC	5.5	–0.3	1	N/A
DACMODE, EN	3.5	–0.3	0	0
V_{REF}	5.5	–0.3	0.5	N/A
All Other Pins	5.5	–0.3	–	–

*All signals reference to GND unless otherwise noted.

Thermal Information

Rating	Symbol	Value	Unit
Thermal Characteristic, QFN Package (Note 1)	$R_{\theta JA}$	34	°C/W
Operating Junction Temperature Range (Note 2)	T_J	0 to 125	°C
Operating Ambient Temperature Range	T_A	0 to 85	°C
Maximum Storage Temperature Range	T_{STG}	–55 to +150	°C
Moisture Sensitivity Level, QFN Package	MSL	3	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*The maximum package power dissipation must be observed.

1. JESD 51–5 (1S2P Direct–Attach Method) with 0 Airflow.
2. JESD 51–7 (1S2P Direct–Attach Method) with 0 Airflow.

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
Error Amplifier					
Input Bias Current		–200	–	200	nA
Input Offset Voltage (Note 3)		–1.0	–	1.0	mV
Open Loop DC Gain (Note 3)	C_L = 60 pF to GND, R_L = 10 kΩ to GND	–	100	–	dB
Open Loop Unity Gain Bandwidth (Note 3)	C_L = 60 pF to GND, R_L = 10 kΩ to GND	–	15	–	MHz
Open Loop Phase Margin (Note 3)	C_L = 60 pF to GND, R_L = 10 kΩ to GND	–	70	–	°
Slew Rate (Note 3)	ΔV_{in} = 100 mV, G = –10 V/V, 1.5 V < COMP < 2.5 V, C_L = 60 pF, DC Load = ±125 μA	–	5	–	V/μs
Maximum Output Voltage	10 mV of Overdrive I_{SOURCE} = 2.0 mA	2.20	V_{CC}–20 mV	–	V
Minimum Output Voltage	10 mV of Overdrive I_{SINK} = 2.0 mA	–	0.01	0.5	V
Output Source Current (Note 3)	10 mV Input Overdrive COMP = 2.0 V	2.0	–	–	mA
Output Sink Current (Note 3)	10 mV Input Overdrive COMP = 1.0 V	2.0	–	–	mA
Differential Summing Amplifier					
VS+ Input Resistance	DRVON = Low DRVON = High	– –	1.5 17	– –	kΩ
VS+ Input Bias Voltage	DRVON = Low DRVON = High	– –	0.05 0.65	– –	V
VS– Bias Current	VS– = 0 V	–	33	–	μA
VS+ Input Voltage Range	0.95 ≤ ΔDIFFOUT / ΔVS– ≤ 1.05 0.5 V ≤ DIFFOUT ≤ 2.0 V	–0.3	–	2.0	V
VS– Input Voltage Range	0.95 ≤ ΔDIFFOUT / ΔVS– ≤ 1.05 0.5 V ≤ DIFFOUT ≤ 2.0 V	–0.3	–	0.3	V
DC Gain VS+ to DIFFOUT	0 V ≤ DAC – VS+ ≤ 0.3 V	0.98	1.0	1.025	V/V
DAC Accuracy (measured at VS+)	Closed loop measurement including error amplifier. (See Figure 25) 1.0 ≤ DAC ≤ 1.6 0.8 ≤ DAC ≤ 1.0 0.5 ≤ DAC ≤ 0.8	 –0.5 –5 –8	 – – –	 0.5 5 8	 % mV mV
–3dB Bandwidth (Note 3)	C_L = 80 pF to GND, R_L = 10 kΩ to GND	–	10	–	MHz
Slew Rate (Note 3)	ΔV_{in} = 100 mV, DIFFOUT = 1.3 V to 1.2 V	–	5	–	V/μs
Maximum Output Voltage	VS+ – DAC = 1.0 V I_{SOURCE} = 2.0 mA	2.0	3.0	–	V
Minimum Output Voltage	VS+ – DAC = –0.8 V I_{SINK} = 2.0 mA	–	0.01	0.5	V
Output Source Current (Note 3)	VS+ – DAC = 1.0 V DIFFOUT = 1.0 V	2.0	–	–	mA
Output Sink Current (Note 3)	VS+ – DAC = –0.8 V DIFFOUT = 1.0 V	2.0	–	–	mA

3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
Internal Offset Voltage					
VDRP pin offset voltage AND Error Amp input voltage		–	1.30		V
VDRP Adaptive Voltage–Positioning Amplifier					
Current Sense Input to VDRP Gain	–60 mV < (CSx–CSxN) < +60 mV (Each CS Input Independently)	5.64	5.79	5.95	V/V
Current Sense Input to VDRP –3dB Bandwidth (Note 3)	C_L = 30 pF to GND, R_L = 10 kΩ to GND	–	4	–	MHz
VDRP Output Slew Rate (Note 3)	ΔVin = 25 mV 1.3 V < VDRP < 1.9 V, C_L = 330 pF to GND, R_L = 1 kΩ to 10 kΩ connected to 1.3 V	2.5	–	–	V/μs
VDRP Output Voltage Offset from Internal Offset Voltage	CSx= CSxN = 1.3 V	–15	–	+15	mV
Maximum VDRP Output Voltage	CSx – CSxN = 0.1 V (all phases), I_{SOURCE} = 1.0 mA	2.6	3.0	–	V
Minimum VDRP Output Voltage	CSx – CSxN = –0.033 V (all phases), I_{SINK} = 1.0 mA	–	0.1	0.5	V
Output Source Current (Note 3)	VDRP = 2.0 V	–	1.3	–	mA
Output Sink Current (Note 3)	VDRP = 1.0 V	–	25	–	mA
Current Sense Amplifiers					
Input Bias Current	CSx = CSxN = 1.4 V	–200	–	200	nA
Common Mode Input Voltage Range		–0.3	–	2.0	V
Differential Mode Input Voltage Range (Note 3)		–120	–	120	mV
Input Referred Offset Voltage (Note 3)	CSx = CSxN = 1.0 V	–1.0	–	1.0	mV
Current Sense Input to PWM Gain	0 V < (CSx – CSxN) < 0.1 V	–	6.0	–	V/V
Oscillator					
Switching Frequency Range (Note 3)		100	–	1000	kHz
Switching Frequency Accuracy, 2– or 4–phase	ROSC = 50 kΩ ROSC = 25 kΩ ROSC = 10 kΩ	196 380 803	– – –	226 420 981	kHz
Switching Frequency Accuracy, 3–phase	ROSC = 50 kΩ ROSC = 25 kΩ ROSC = 10 kΩ	196 370 757	– – –	230 430 963	kHz
Switching Frequency Tolerance, 2 and 4 Phase Operation (Note 3)	200 kHz < FSW < 600 kHz 100 kHz < FSW <1 MHz	– –	5 10	– –	%
Switching Frequency Tolerance, 3 Phase Operation (Note 3)	200 kHz < FSW < 600 kHz 100 kHz < FSW <1 MHz	– –	10 15	– –	%
ROSC Output Voltage	40 μA ≤ I_{ROSC} ≤ 200 μA	1.95	2.01	2.065	V

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
Modulators (PWM Comparators)					
Minimum Pulse Width (Note 3)	Fs = 800 kHz	–	30	40	ns
Propagation Delay (Note 3)		–	20	–	ns
Magnitude of the PWM Ramp		–	1.0	–	V
0% Duty Cycle	COMP voltage when the PWM outputs remain LOW	–	1.3	–	V
100% Duty Cycle	COMP voltage when the PWM outputs remain HIGH	–	2.3	–	V
PWM Linear Duty Cycle (Note 3)		–	90	–	%
PWM Phase Angle Error		–15	–	15	°
VR_RDY (Power Good) Output					
VR_RDY Saturation Voltage	I_{VR_RDY} = 10 mA	–	–	0.4	V
VR_RDY Rise Time	External pullup of 680 kΩ to 1.25 V, C_L = 45 pF, ΔVo = 10% to 90%	–	–	150	ns
VR_RDY High – Output Leakage Current	VR_RDY = 5.0 V	–	–	1.0	μA
VR_RDY Upper Threshold Voltage	VCORE increasing, DAC = 1.3 V	–	300	–	mV below DAC
VR_RDY Lower Threshold Voltage	VCORE decreasing, DAC = 1.3 V	–	350	–	mV below DAC
VR_RDY Rising Delay	VCORE increasing	–	–	3	ms
VR_RDY Falling Delay	VCORE decreasing	–	–	250	ns
PWM Outputs					
Output High Voltage	Sourcing 500 μA	3.0	–	V_{CC}	V
Output Low Voltage	Sinking 500 μA	–	–	0.15	V
Rise Time	C_L = 20 pF, ΔVo = 0.3 to 2.0 V	–	–	20	ns
Fall Time	C_L = 20 pF, ΔVo = Vmax to 0.7 V	–	–	20	ns
Tri–State Output Leakage	Gx = 2.5 V, x = 1 – 4	–	–	1.5	μA
Output Impedance – Sourcing	Max Resistance to V_{CC}	–	320	–	Ω
Output Impedance – Sinking	Max Resistance to GND	–	140	–	Ω
2/3/4 Phase Detection					
Gate Pin Source Current		–	84	–	μA
Gate Pin Threshold Voltage		–	225	–	mV
Phase Detect Timer		–	20	–	μs
DRVON					
Output High Voltage	Sourcing 500 μA	3.0	–	V_{CC}	V
Output Low Voltage	Sinking 500 μA	–	–	0.7	mV
Rise Time	C_L (PCB) = 20 pF, ΔVo = 10% to 90%	–	24	30	ns
Fall Time	C_L = 20 pF, ΔVo = 10% to 90%	–	11	20	ns
Internal Pulldown Resistance		–	70	–	kΩ

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
Soft−Start					
Soft−Start Pin Source Current		3.75	5.0	6.25	μA
Soft−Start Ramp Time	C_{SS} = 0.01 μF; Time to 1.05 V	–	2.2	–	ms
Soft−Start Pin Discharge Voltage	DRVON pin = LO (Fault)	–	–	25	mV
VR11 Dwell Time at V_{BOOT}	C_{SS} = 0.01 μF	50	–	500	μs
DACMODE Input					
Input Range for AMD Operating Mode		2.3	–	3.5	V
Input Range for VR11 Operating Mode		0.9	–	1.7	V
Input Range for VR10 Operating Mode		0	–	0.5	V
Enable Input					
Enable High Input Leakage Current	EN = 3.3 V	–	–	1.0	μA
Rising Threshold	V_{UPPER}	0.800	–	0.920	V
Falling Threshold	V_{LOWER}	0.670	–	0.830	V
Hysteresis	$V_{UPPER} - V_{LOWER}$	–	130	–	mV
Enable Delay Time	Time from Enable transitioning HI to initiation of Soft−Start	1.0	–	5.0	ms
Disable Delay Time	EN Low to DRVON Low	–	150	200	ns
Current Limit					
Current Sense Amp to ILIM Gain	20 mV < (CSx − CSxN) < 60 mV (Each CS Input Independently)	5.7	5.95	6.2	V/V
ILIM Pin Input Bias Current	V_{ILIM} = 2.0 V	–	–	1.0	μA
ILIM Pin Working Voltage Range (Note 3)		0.2	–	2.0	V
ILIM Offset Voltage	Offset extrapolated to CSx − CSxN = 0, referred to ILIM pin	−33	17	67	mV
Delay (Note 3)		–	300	–	ns
Overvoltage Protection					
Overvoltage Threshold		DAC+ 160	–	DAC+ 200	mV
Delay (Note 3)		–	100	–	ns
Undervoltage Protection					
V_{CC} UVLO Start Threshold		4	–	4.5	V
V_{CC} UVLO Stop Threshold		3.8	–	4.3	V
V_{CC} UVLO Hysteresis		100	215	–	mV
VID Inputs					
Upper Threshold	V_{UPPER}	–	–	800	mV
Lower Threshold	V_{LOWER}	300	–	–	mV
Input Bias Current		–	–	500	nA
Delay before Latching VID Change (VID De−Skewing) (Note 3)	Measured from the edge of the first VID change	500	–	800	ns
Internal DAC Slew Rate Limiter					
Positive Slew Rate Limit	V_{ID} Step of +500 mV	–	6.3	–	mV/μs
Negative Slew Rate Limit	V_{ID} Step of −500 mV	–	−6.3	–	mV/μs

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage Reference (V_{REF})					
V_{REF} Output Voltage	0 μA ≤ I_{VREF} ≤ 500 μA	2.469	2.52	2.569	V
Input Supply Current					
V_{CC} Operating Current	EN = LOW, No PWM	–	–	20	mA
Temperature Sensing					
VR_FAN Upper Voltage Threshold	Fraction of V_{REF} voltage above which VR_FAN output pulls low	–	0.4 x V_{REF}	–	–
VR_FAN Lower Voltage Threshold	Fraction of V_{REF} voltage below which VR_FAN output is open	–	0.33 x V_{REF}	–	–
VR_HOT Upper Voltage Threshold	Fraction of V_{REF} voltage above which VR_HOT output pulls low	–	0.33 x V_{REF}	–	–
VR_HOT Lower Voltage Threshold	Fraction of V_{REF} voltage below which VR_HOT output is open	–	0.27 x V_{REF}	–	–
VR_FAN Output Saturation Voltage	I_{SINK} = 4 mA	–	–	0.3	V
VR_FAN Output Leakage Current	High Impedance State	–	–	1	μA
VR_HOT Saturation Output Voltage	I_{SINK} = 4 mA	–	–	0.3	V
VR_HOT Output Leakage Current	High Impedance State	–	–	1	μA
NTC Pin Bias Current		–	–	1	μA
12VMON					
12VMON (Rising Threshold)	Sufficient power stage supply voltage	0.728	–	0.821	V
12VMON (Falling Threshold)	Insufficient power stage supply voltage	0.643	–	0.725	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
VRM11 DAC					
System Voltage Accuracy	1.0 V < DAC < 1.6 V 0.8 V < DAC < 1.0 V 0.5 V < DAC < 0.8 V	–	–	±0.5 ±5 ±8	% mV mV
No Load Offset Voltage from Nominal DAC Specification	With CS Input ΔV_{in} = 0 V	–	–19	–	mV

Table 1: VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	0	0	0	0	0	0	0	OFF	00
0	0	0	0	0	0	0	1	OFF	01
0	0	0	0	0	0	1	0	1.60000	02
0	0	0	0	0	0	1	1	1.59375	03
0	0	0	0	0	1	0	0	1.58750	04
0	0	0	0	0	1	0	1	1.58125	05
0	0	0	0	0	1	1	0	1.57500	06
0	0	0	0	0	1	1	1	1.56875	07
0	0	0	0	1	0	0	0	1.56250	08
0	0	0	0	1	0	0	1	1.55625	09
0	0	0	0	1	0	1	0	1.55000	0A
0	0	0	0	1	0	1	1	1.54375	0B
0	0	0	0	1	1	0	0	1.53750	0C
0	0	0	0	1	1	0	1	1.53125	0D
0	0	0	0	1	1	1	0	1.52500	0E
0	0	0	0	1	1	1	1	1.51875	0F
0	0	0	1	0	0	0	0	1.51250	10
0	0	0	1	0	0	0	1	1.50625	11
0	0	0	1	0	0	1	0	1.50000	12
0	0	0	1	0	0	1	1	1.49375	13
0	0	0	1	0	1	0	0	1.48750	14
0	0	0	1	0	1	0	1	1.48125	15
0	0	0	1	0	1	1	0	1.47500	16
0	0	0	1	0	1	1	1	1.46875	17
0	0	0	1	1	0	0	0	1.46250	18
0	0	0	1	1	0	0	1	1.45625	19
0	0	0	1	1	0	1	0	1.45000	1A
0	0	0	1	1	0	1	1	1.44375	1B
0	0	0	1	1	1	0	0	1.43750	1C
0	0	0	1	1	1	0	1	1.43125	1D
0	0	0	1	1	1	1	0	1.42500	1E
0	0	0	1	1	1	1	1	1.41875	1F
0	0	1	0	0	0	0	0	1.41250	20
0	0	1	0	0	0	0	1	1.40625	21
0	0	1	0	0	0	1	0	1.40000	22
0	0	1	0	0	0	1	1	1.39375	23
0	0	1	0	0	1	0	0	1.38750	24

Table 1: VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	0	1	0	0	1	0	1	1.38125	25
0	0	1	0	0	1	1	0	1.37500	26
0	0	1	0	0	1	1	1	1.36875	27
0	0	1	0	1	0	0	0	1.36250	28
0	0	1	0	1	0	0	1	1.35625	29
0	0	1	0	1	0	1	0	1.35000	2A
0	0	1	0	1	0	1	1	1.34375	2B
0	0	1	0	1	1	0	0	1.33750	2C
0	0	1	0	1	1	0	1	1.33125	2D
0	0	1	0	1	1	1	0	1.32500	2E
0	0	1	0	1	1	1	1	1.31875	2F
0	0	1	1	0	0	0	0	1.31250	30
0	0	1	1	0	0	0	1	1.30625	31
0	0	1	1	0	0	1	0	1.30000	32
0	0	1	1	0	0	1	1	1.29375	33
0	0	1	1	0	1	0	0	1.28750	34
0	0	1	1	0	1	0	1	1.28125	35
0	0	1	1	0	1	1	0	1.27500	36
0	0	1	1	0	1	1	1	1.26875	37
0	0	1	1	1	0	0	0	1.26250	38
0	0	1	1	1	0	0	1	1.25625	39
0	0	1	1	1	0	1	0	1.25000	3A
0	0	1	1	1	0	1	1	1.24375	3B
0	0	1	1	1	1	0	0	1.23750	3C
0	0	1	1	1	1	0	1	1.23125	3D
0	0	1	1	1	1	1	0	1.22500	3E
0	0	1	1	1	1	1	1	1.21875	3F
0	1	0	0	0	0	0	0	1.21250	40
0	1	0	0	0	0	0	1	1.20625	41
0	1	0	0	0	0	1	0	1.20000	42
0	1	0	0	0	0	1	1	1.19375	43
0	1	0	0	0	1	0	0	1.18750	44
0	1	0	0	0	1	0	1	1.18125	45
0	1	0	0	0	1	1	0	1.17500	46
0	1	0	0	0	1	1	1	1.16875	47
0	1	0	0	1	0	0	0	1.16250	48
0	1	0	0	1	0	0	1	1.15625	49
0	1	0	0	1	0	1	0	1.15000	4A
0	1	0	0	1	0	1	1	1.14375	4B
0	1	0	0	1	1	0	0	1.13750	4C
0	1	0	0	1	1	0	1	1.13125	4D
0	1	0	0	1	1	1	0	1.12500	4E
0	1	0	0	1	1	1	1	1.11875	4F
0	1	0	1	0	0	0	0	1.11250	50
0	1	0	1	0	0	0	1	1.10625	51
0	1	0	1	0	0	1	0	1.10000	52

Table 1: VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
0	1	0	1	0	0	1	1	1.09375	53
0	1	0	1	0	1	0	0	1.08750	54
0	1	0	1	0	1	0	1	1.08125	55
0	1	0	1	0	1	1	0	1.07500	56
0	1	0	1	0	1	1	1	1.06875	57
0	1	0	1	1	0	0	0	1.06250	58
0	1	0	1	1	0	0	1	1.05625	59
0	1	0	1	1	0	1	0	1.05000	5A
0	1	0	1	1	0	1	1	1.04375	5B
0	1	0	1	1	1	0	0	1.03750	5C
0	1	0	1	1	1	0	1	1.03125	5D
0	1	0	1	1	1	1	0	1.02500	5E
0	1	0	1	1	1	1	1	1.01875	5F
0	1	1	0	0	0	0	0	1.01250	60
0	1	1	0	0	0	0	1	1.00625	61
0	1	1	0	0	0	1	0	1.00000	62
0	1	1	0	0	0	1	1	0.99375	63
0	1	1	0	0	1	0	0	0.98750	64
0	1	1	0	0	1	0	1	0.98125	65
0	1	1	0	0	1	1	0	0.97500	66
0	1	1	0	0	1	1	1	0.96875	67
0	1	1	0	1	0	0	0	0.96250	68
0	1	1	0	1	0	0	1	0.95625	69
0	1	1	0	1	0	1	0	0.95000	6A
0	1	1	0	1	0	1	1	0.94375	6B
0	1	1	0	1	1	0	0	0.93750	6C
0	1	1	0	1	1	0	1	0.93125	6D
0	1	1	0	1	1	1	0	0.92500	6E
0	1	1	0	1	1	1	1	0.91875	6F
0	1	1	1	0	0	0	0	0.91250	70
0	1	1	1	0	0	0	1	0.90625	71
0	1	1	1	0	0	1	0	0.90000	72
0	1	1	1	0	0	1	1	0.89375	73
0	1	1	1	0	1	0	0	0.88750	74
0	1	1	1	0	1	0	1	0.88125	75
0	1	1	1	0	1	1	0	0.87500	76
0	1	1	1	0	1	1	1	0.86875	77
0	1	1	1	1	0	0	0	0.86250	78
0	1	1	1	1	0	0	1	0.85625	79
0	1	1	1	1	0	1	0	0.85000	7A
0	1	1	1	1	0	1	1	0.84375	7B
0	1	1	1	1	1	0	0	0.83750	7C
0	1	1	1	1	1	0	1	0.83125	7D
0	1	1	1	1	1	1	0	0.82500	7E
0	1	1	1	1	1	1	1	0.81875	7F
1	0	0	0	0	0	0	0	0.81250	80

Table 1: VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
1	0	0	0	0	0	0	1	0.80625	81
1	0	0	0	0	0	1	0	0.80000	82
1	0	0	0	0	0	1	1	0.79375	83
1	0	0	0	0	1	0	0	0.78750	84
1	0	0	0	0	1	0	1	0.78125	85
1	0	0	0	0	1	1	0	0.77500	86
1	0	0	0	0	1	1	1	0.76875	87
1	0	0	0	1	0	0	0	0.76250	88
1	0	0	0	1	0	0	1	0.75625	89
1	0	0	0	1	0	1	0	0.75000	8A
1	0	0	0	1	0	1	1	0.74375	8B
1	0	0	0	1	1	0	0	0.73750	8C
1	0	0	0	1	1	0	1	0.73125	8D
1	0	0	0	1	1	1	0	0.72500	8E
1	0	0	0	1	1	1	1	0.71875	8F
1	0	0	1	0	0	0	0	0.71250	90
1	0	0	1	0	0	0	1	0.70625	91
1	0	0	1	0	0	1	0	0.70000	92
1	0	0	1	0	0	1	1	0.69375	93
1	0	0	1	0	1	0	0	0.68750	94
1	0	0	1	0	1	0	1	0.68125	95
1	0	0	1	0	1	1	0	0.67500	96
1	0	0	1	0	1	1	1	0.66875	97
1	0	0	1	1	0	0	0	0.66250	98
1	0	0	1	1	0	0	1	0.65625	99
1	0	0	1	1	0	1	0	0.65000	9A
1	0	0	1	1	0	1	1	0.64375	9B
1	0	0	1	1	1	0	0	0.63750	9C
1	0	0	1	1	1	0	1	0.63125	9D
1	0	0	1	1	1	1	0	0.62500	9E
1	0	0	1	1	1	1	1	0.61875	9F
1	0	1	0	0	0	0	0	0.61250	A0
1	0	1	0	0	0	0	1	0.60625	A1
1	0	1	0	0	0	1	0	0.60000	A2
1	0	1	0	0	0	1	1	0.59375	A3
1	0	1	0	0	1	0	0	0.58750	A4
1	0	1	0	0	1	0	1	0.58125	A5
1	0	1	0	0	1	1	0	0.57500	A6
1	0	1	0	0	1	1	1	0.56875	A7
1	0	1	0	1	0	0	0	0.56250	A8
1	0	1	0	1	0	0	1	0.55625	A9
1	0	1	0	1	0	1	0	0.55000	AA
1	0	1	0	1	0	1	1	0.54375	AB
1	0	1	0	1	1	0	0	0.53750	AC
1	0	1	0	1	1	0	1	0.53125	AD
1	0	1	0	1	1	1	0	0.52500	AE

Table 1: VRM11 VID Codes

VID7 800 mV	VID6 400 mV	VID5 200 mV	VID4 100 mV	VID3 50 mV	VID2 25 mV	VID1 12.5 mV	VID0 6.25 mV	Voltage (V)	HEX
1	0	1	0	1	1	1	1	0.51875	AF
1	0	1	1	0	0	0	0	0.51250	B0
1	0	1	1	0	0	0	1	0.50625	B1
1	0	1	1	0	0	1	0	0.50000	B2
1	1	1	1	1	1	1	0	OFF	FE
1	1	1	1	1	1	1	1	OFF	FF
								OFF	B3 to FD

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
VRM10 DAC					
System Voltage Accuracy	1.0 V < DAC < 1.6 V 0.83125 V < DAC < 1.0 V	–	–	±0.5 ±5	% mV
No Load Offset Voltage from Nominal DAC Specification	With CS Input ΔV_{in} = 0 V	–	–19	–	mV

Table 2: VRM10 VID Codes

VID4 400 mV	VID3 200 mV	VID2 100 mV	VID1 50 mV	VID0 25 mV	VID5 12.5 mV	VID6 6.25 mV	Nominal DAC Voltage (V)
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375
0	1	1	1	1	0	1	1.48750
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875

Table 2: VRM10 VID Codes

VID4 400 mV	VID3 200 mV	VID2 100 mV	VID1 50 mV	VID0 25 mV	VID5 12.5 mV	VID6 6.25 mV	Nominal DAC Voltage (V)
1	0	1	0	0	0	1	1.36250
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF

Table 2: VRM10 VID Codes

VID4 400 mV	VID3 200 mV	VID2 100 mV	VID1 50 mV	VID0 25 mV	VID5 12.5 mV	VID6 6.25 mV	Nominal DAC Voltage (V)
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375
0	0	1	0	0	0	1	0.98750
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.96250
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.88750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: 0°C < T_A < 85°C; 4.75 V < V_{CC} < 5.25 V; All DAC Codes; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Units
AMD DAC					
System Voltage Accuracy	1.0 V < DAC < 1.55 V 0.8 V < DAC < 1.0 V	–	–	±0.5 ±5.0	% mV
No Load Offset Voltage from Nominal DAC Specification	With CS Input ΔV_{in} = 0 V	–	0	–	mV

Table 3: AMD VID Codes

VID4	VID3	VID2	VID1	VID0	Nominal V_{OUT} (V)	Tolerance
0	0	0	0	0	1.550	±0.5 %
0	0	0	0	1	1.525	±0.5 %
0	0	0	1	0	1.500	±0.5 %
0	0	0	1	1	1.475	±0.5 %
0	0	1	0	0	1.450	±0.5 %
0	0	1	0	1	1.425	±0.5 %
0	0	1	1	0	1.400	±0.5 %
0	0	1	1	1	1.375	±0.5 %
0	1	0	0	0	1.350	±0.5 %
0	1	0	0	1	1.325	±0.5 %
0	1	0	1	0	1.300	±0.5 %
0	1	0	1	1	1.275	±0.5 %
0	1	1	0	0	1.250	±0.5 %
0	1	1	0	1	1.225	±0.5 %
0	1	1	1	0	1.200	±0.5 %
0	1	1	1	1	1.175	±0.5 %
1	0	0	0	0	1.150	±0.5 %
1	0	0	0	1	1.125	±0.5 %
1	0	0	1	0	1.100	±0.5 %
1	0	0	1	1	1.075	±0.5 %
1	0	1	0	0	1.050	±0.5 %
1	0	1	0	1	1.025	±0.5 %
1	0	1	1	0	1.000	±0.5 %
1	0	1	1	1	0.975	±5.0 mV
1	1	0	0	0	0.950	±5.0 mV
1	1	0	0	1	0.925	±5.0 mV
1	1	0	1	0	0.900	±5.0 mV
1	1	0	1	1	0.875	±5.0 mV
1	1	1	0	0	0.850	±5.0 mV
1	1	1	0	1	0.825	±5.0 mV
1	1	1	1	0	0.800	±5.0 mV
1	1	1	1	1	Shutdown	–

TYPICAL CHARACTERISTICS

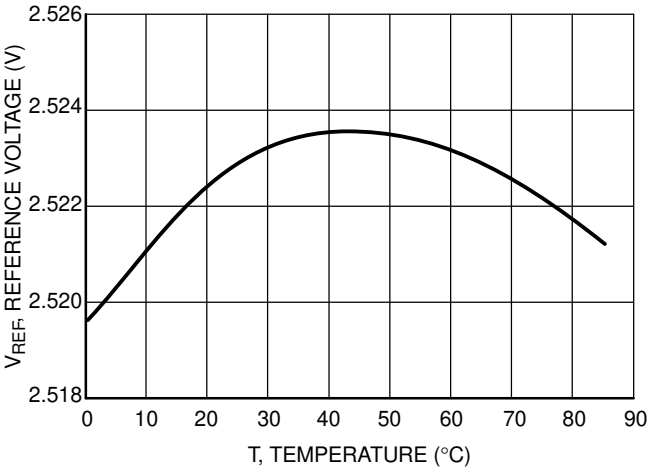


Figure 5. Voltage Reference (VREF) vs. Temperature

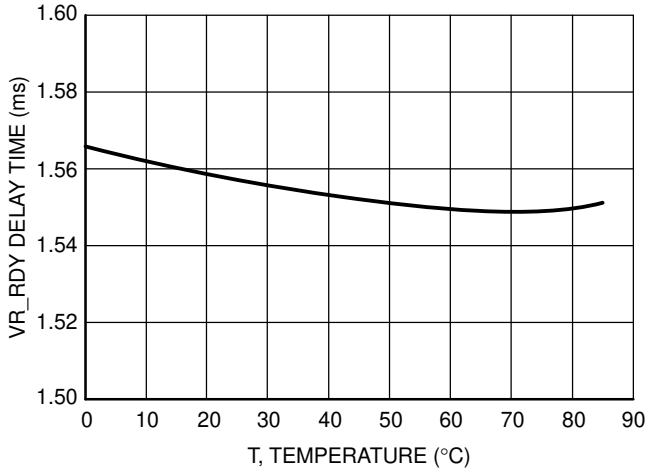


Figure 6. VR Ready Delay Time vs. Temperature

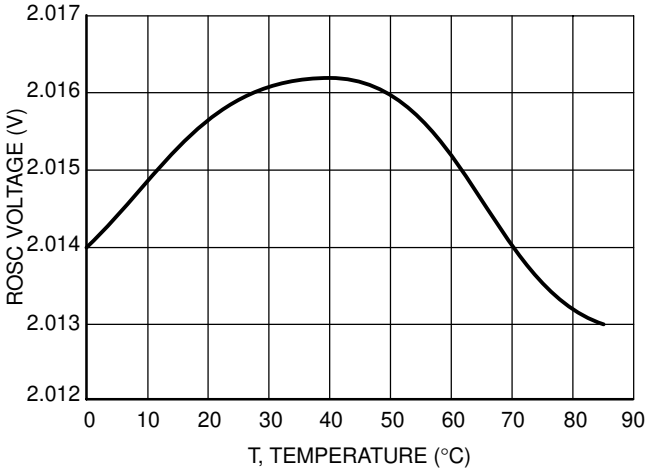


Figure 7. ROSC Voltage vs. Temperature

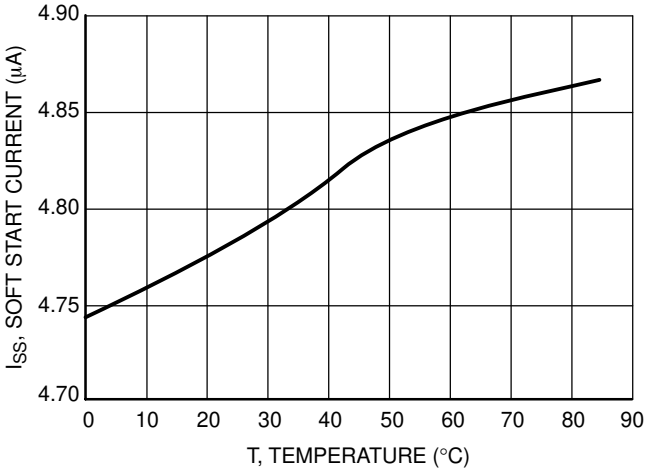


Figure 8. Soft Start Current vs. Temperature

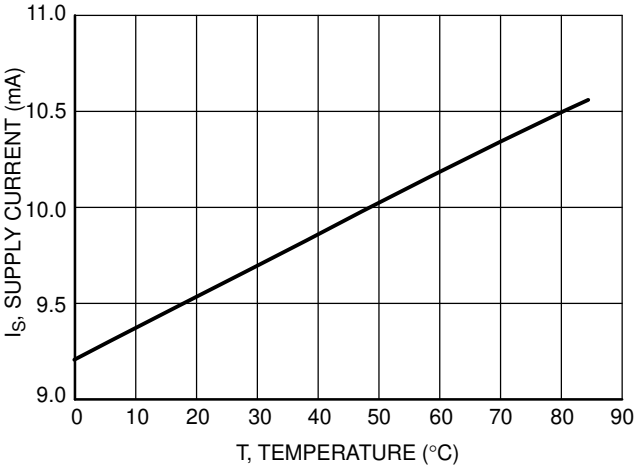


Figure 9. Supply Current vs. Temperature

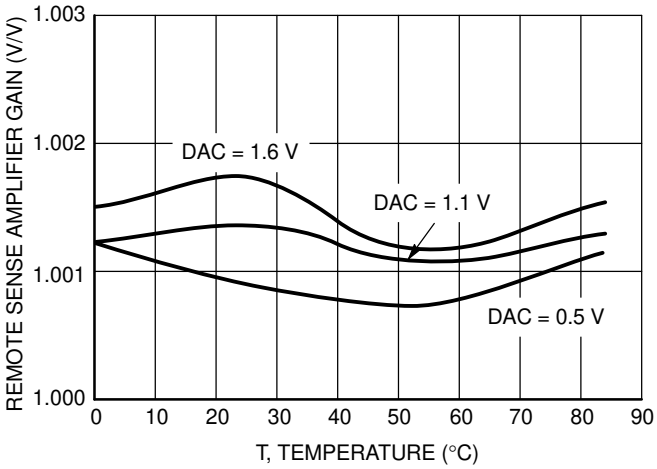


Figure 10. Remote Sense Amplifier Gain vs. Temperature

TYPICAL CHARACTERISTICS

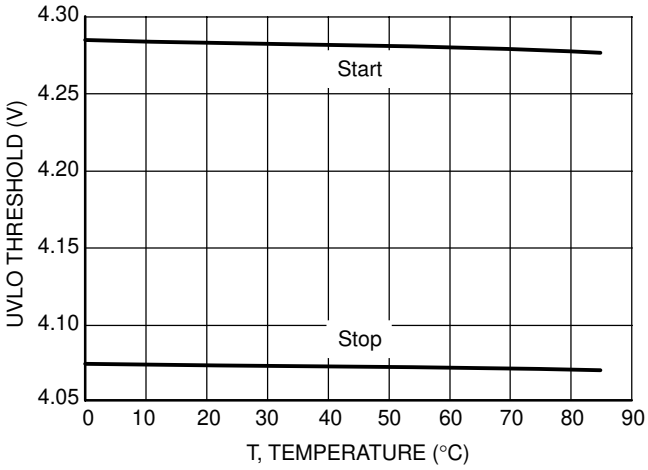


Figure 11. UVLO Threshold vs. Temperature

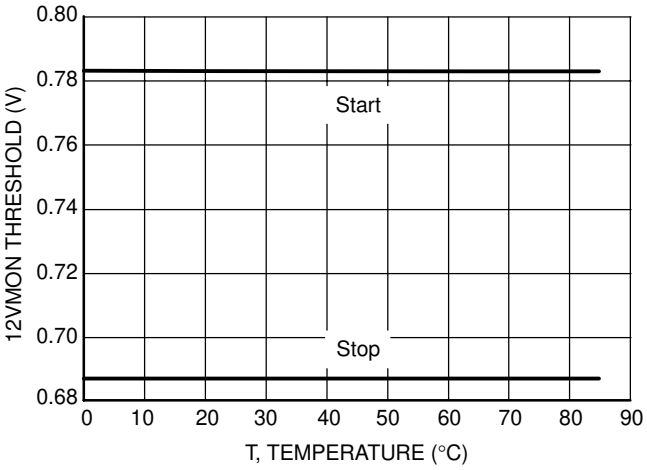


Figure 12. 12VMON Threshold vs. Temperature

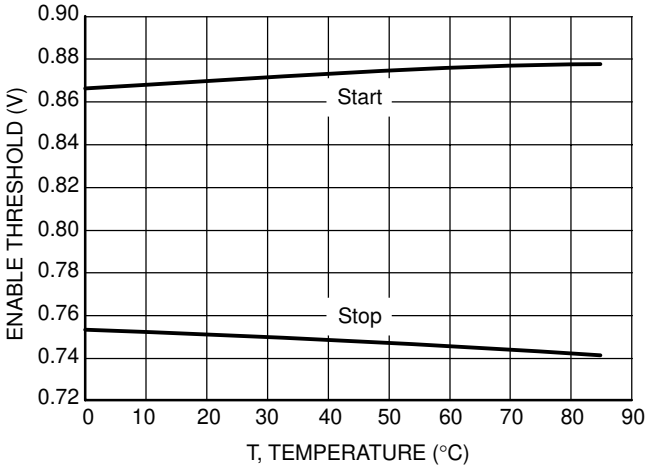


Figure 13. Enable Threshold vs. Temperature

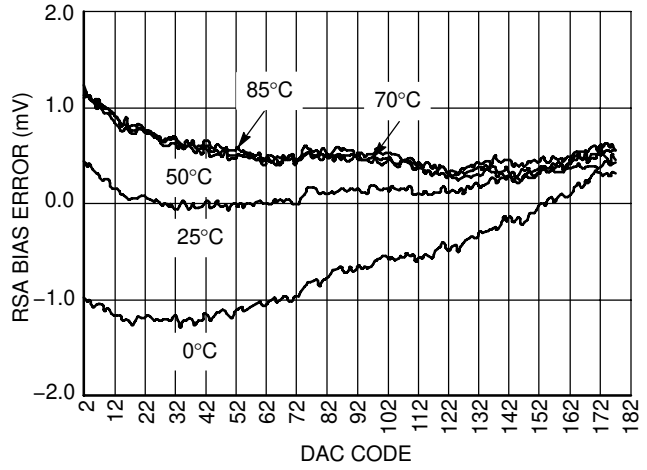


Figure 14. Remote Sense Amplifier Bias Error vs. DAC Code

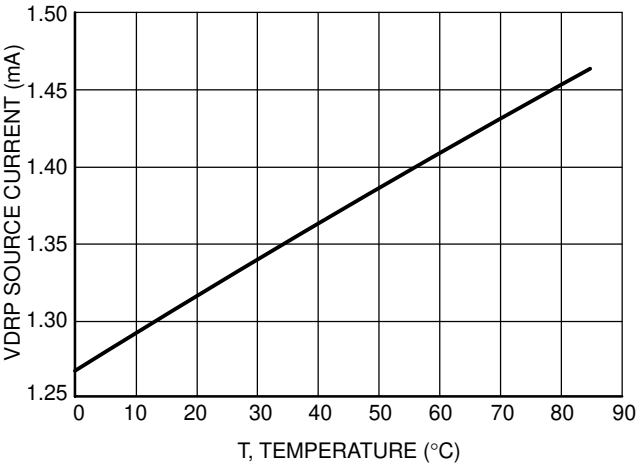


Figure 15. VDRP Source Current vs. Temperature

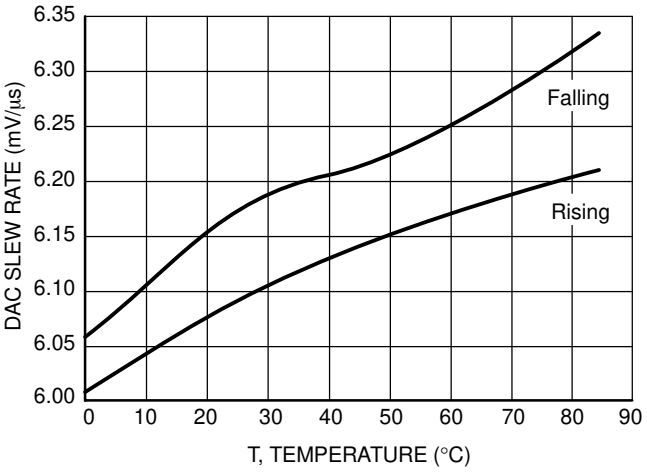


Figure 16. DAC Slew Rate vs. Temperature

TYPICAL CHARACTERISTICS

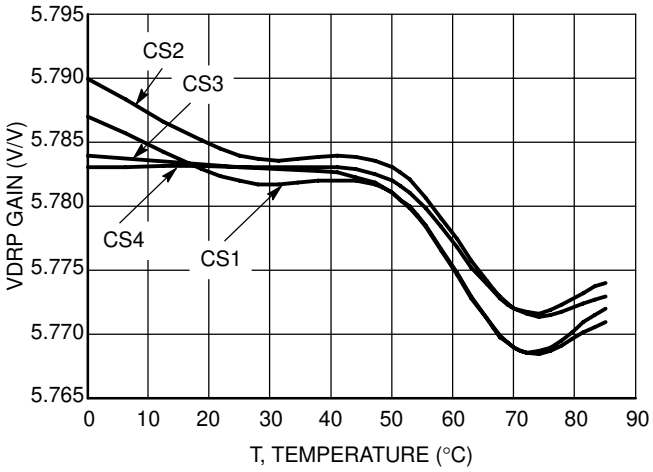


Figure 17. VDRP Gain vs. Temperature

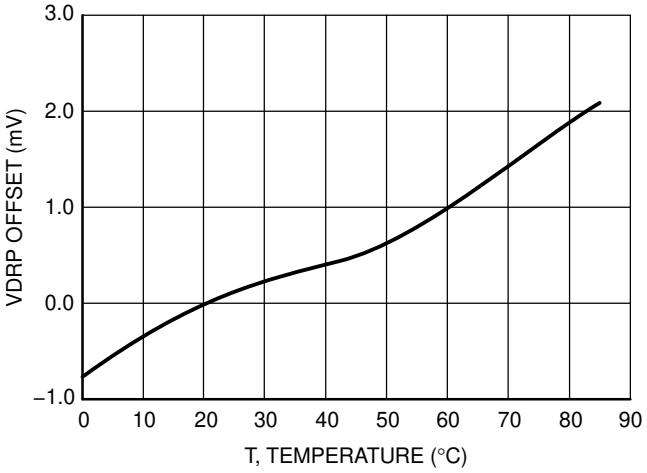


Figure 18. VDRP Offset vs. Temperature

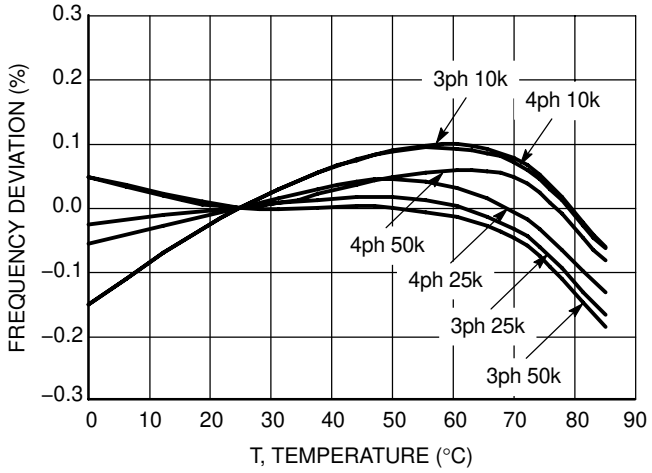


Figure 19. Switching Frequency Deviation vs. Temperature

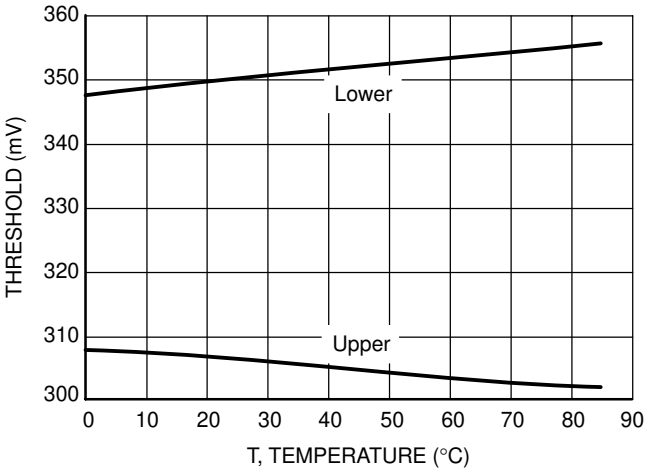


Figure 20. VR_RDY Thresholds vs. Temperature

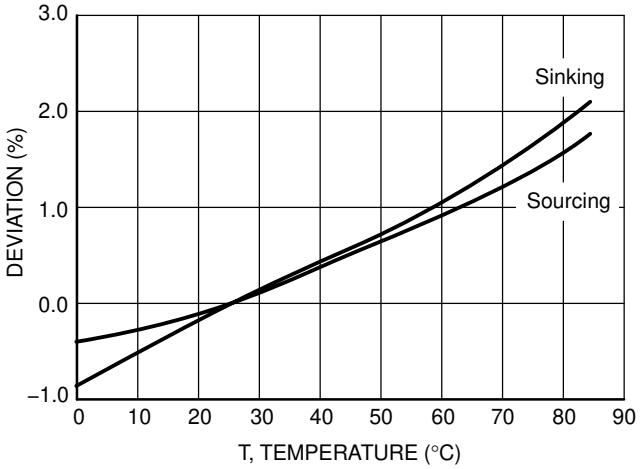


Figure 21. PWM Output Resistance Deviation vs. Temperature

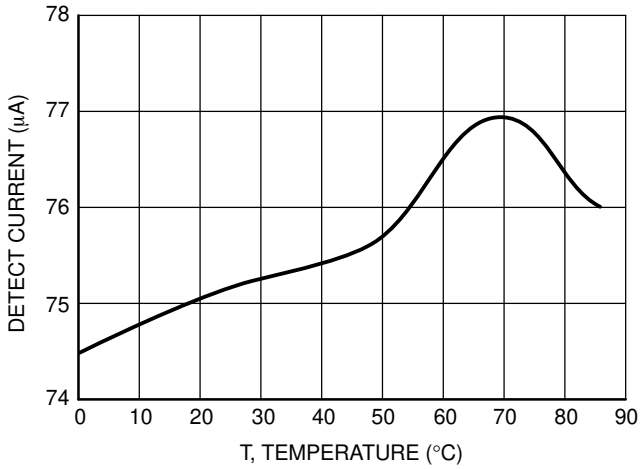


Figure 22. 2/3/4 Phase Detect Current vs. Temperature