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NCP5608

Multiple LED Charge Pump Driver

The NCP5608 is a high efficiency boost converter operating in current loop, based on a charge pump multi mode, to drive White LED. The current mode regulation allows a uniform and programmable brightness of the LEDs. The chip has been optimized for small ceramic capacitors, capable to supply up to 2.0 W output power.

Features

- 2.7 to 5.5 V Input Voltage Range
- Up to 500 mA Output Current
- Capable to Drive 8 LED
- Multi Mode Charge Pump Based Converter
- I2C Serial Link Protocol
- Consistent High Efficiency
- Independently Block Programmable Output Currents
- Programmable 3 or 4 Operating Backlight LED at Zero Extra Losses
- Constant Output Current Regulation
- Built−in Dimming Function
- Tight Automatic LED Current Matching
- Thermal Shutdown Protection
- Low Battery Return Noise
- This is a Pb−Free Device*

Typical Applications

- LED Display Back Light Control
- Keyboard Back Light
- High Power Photo Flash
- Multiple Displays

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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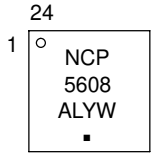
http://onsemi.com

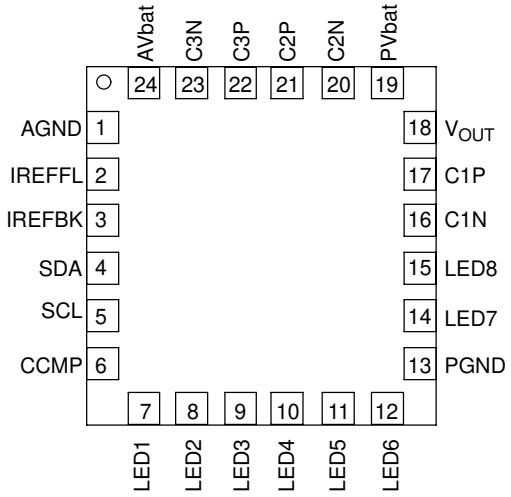
24 PIN TQFN (4x4)
MT SUFFIX
CASE 511AA

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP5608MTR2G	TQFN24 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

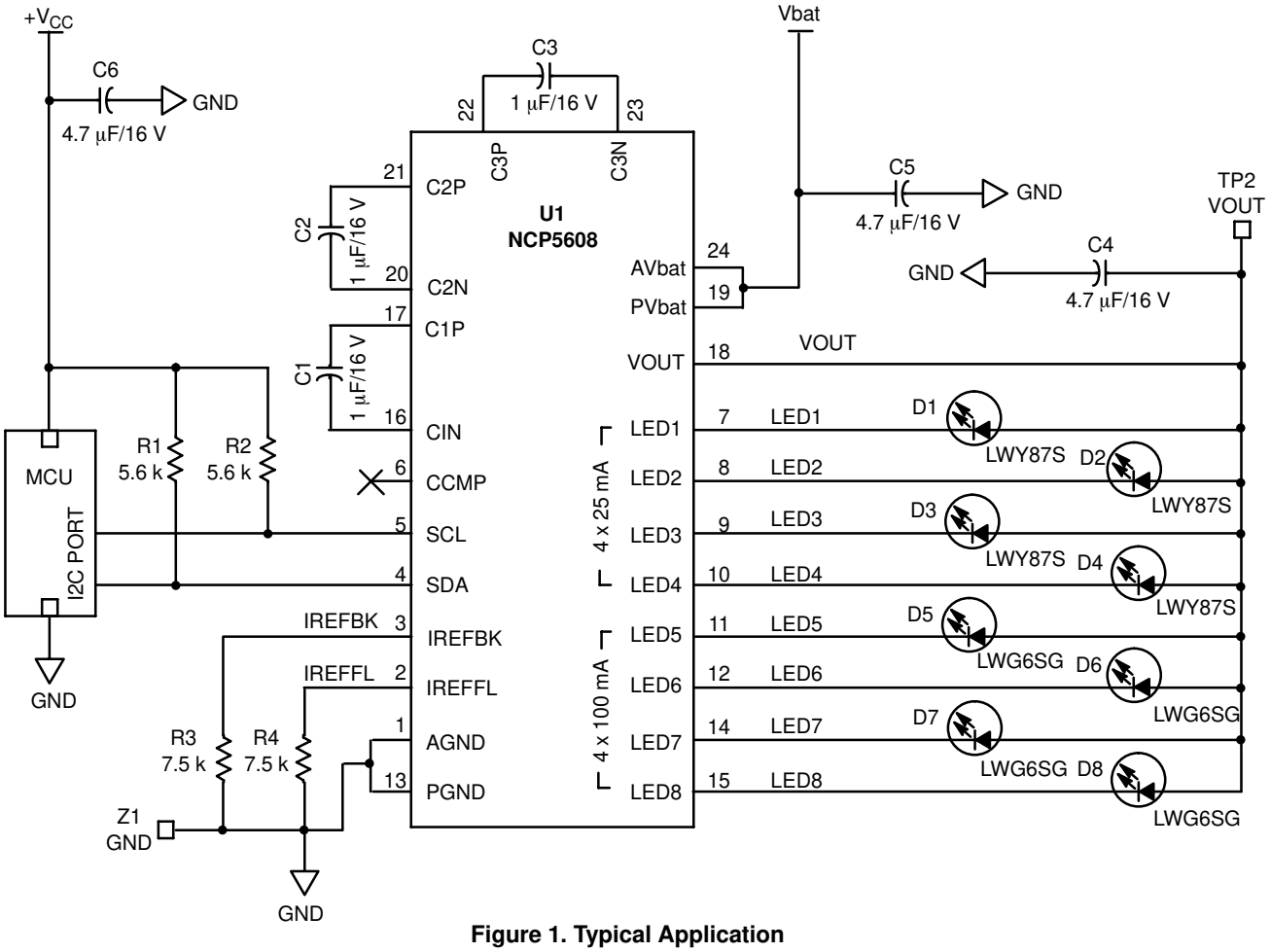


Figure 1. Typical Application

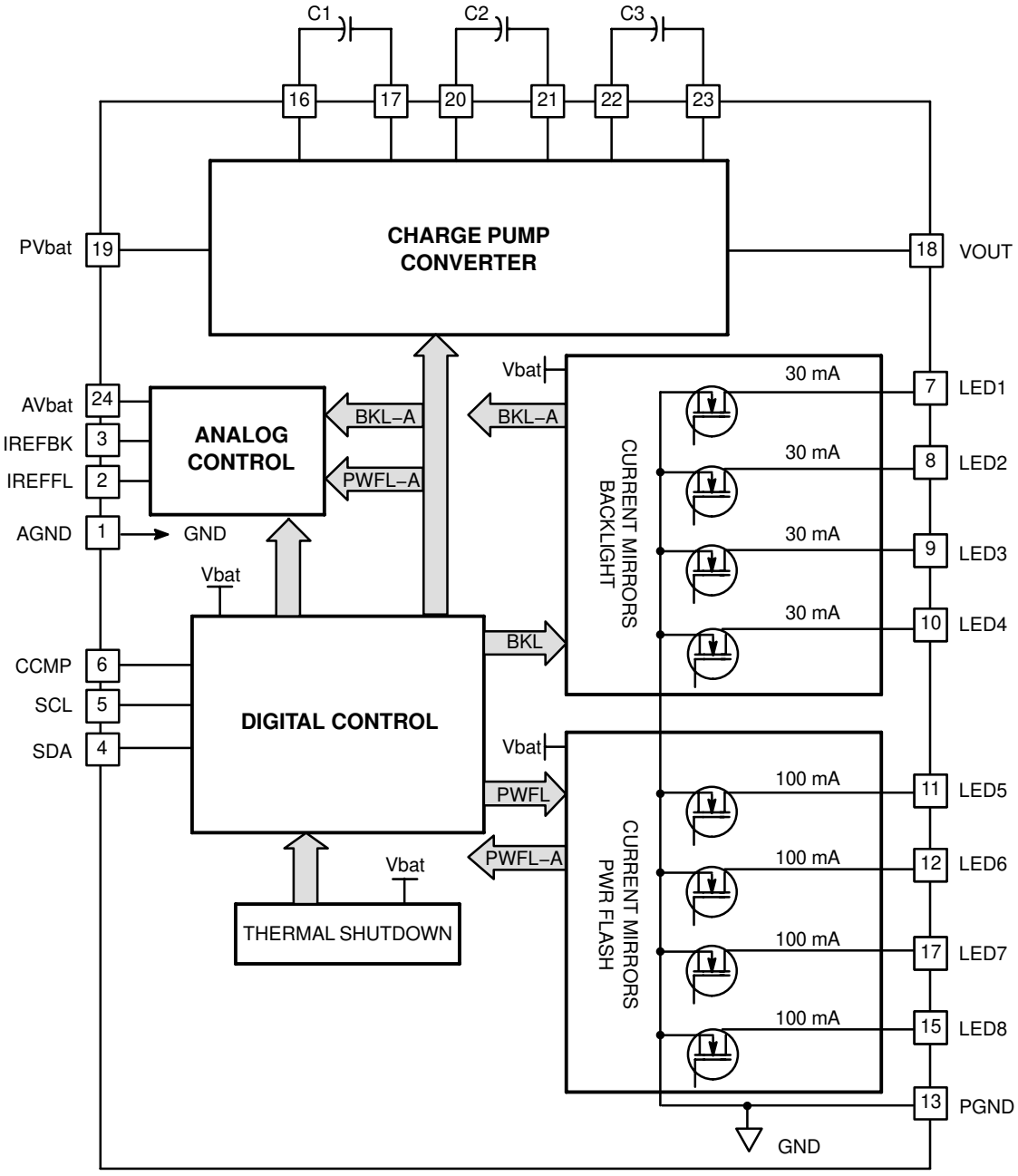


Figure 2. NCP5608 Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Description
1	AGND	GROUND	This pin is the NCP5608 analog ground and shall be connected to the system ground. Care must be observed to minimize the total parasitic inductance between the pin and the ground plane.
2	IREFFL	OUTPUT, ANALOG	This pin is used to set up the current reference for the FLASH output currents (LED5 to LED8). The reference current is derived from the internal bandgap voltage to ground by means of an external resistor. (Note 1)
3	IREFBK	OUTPUT, ANALOG	This pin is used to set up the current reference for the BACK LIGHT output currents (LED1 to LED4). The reference current is derived from the internal bandgap voltage to ground by means of an external resistor. (Note 1)
4	SDA	INPUT, DIGITAL	This pin, associated with the SCL signal, carries the DATA signal to set up the selected output LED current. The DATA signal is built with a single SDA line to support the I2C protocol.
5	SCL	INPUT, DIGITAL	This is the clock signal associated with the SDA pins. The pin carries the standard CLOCK signal to operate the I2C protocol.
6	CCMP	ANALOG, INPUT	This pin is connected to the internal I2C bias network and must be either left open, or bypassed to ground by a 10 nF ceramic capacitor when the I2C voltage drops below 1.8 V. Such a capacitor compensate the voltage drop during normal operation, keeping in mind it is not mandatory when the I2C voltage is 1.8 V and above.
7	LED1	INPUT, POWER	This pin sinks to ground the current flowing into the first LED, and is intended to be used in backlight application. The current is limited to 30 mA max. (Note 2)
8	LED2	INPUT, POWER	This pin sinks to ground the current flowing into the second LED, and is intended to be used in backlight application. The current is limited to 30 mA max. (Note 2)
9	LED3	INPUT, POWER	This pin sinks to ground the current flowing into the third LED, and is intended to be used in backlight application. The current is limited to 30 mA max. (Note 2)
10	LED4	INPUT, POWER	This pin sinks to ground the current flowing into the fourth LED, and is intended to be used in backlight application. The current is limited to 30 mA max. (Note 2) On the other hand, LED4 can be disconnected when only three LEDs are used in the backlight application. (Table 1)
11	LED5	INPUT, POWER	This pin sinks to ground the current flowing into the fifth LED (100 mA max), and is intended to be used in Flash application. (Note 2)
12	LED6	INPUT, POWER	This pin sinks to ground the current flowing into the sixth LED (100 mA max), and is intended to be used in Flash or high power application. (Note 2)
13	PWRGND	POWER	This pin provides the ground reference for the power elements and must be connected to the system ground by a heavy track. Using the ground plane technique is strongly recommended. Care must be observed to minimize the total parasitic inductance between the pin and the ground plane.
14	LED7	INPUT, POWER	This pin sinks to ground the current flowing into the seventh LED (100 mA max), and is intended to be used in flash or high power application. (Note 2)
15	LED8	INPUT, POWER	This pin sinks to ground the current flowing into the eighth LED (100 mA max), and is intended to be used in flash or high power application. (Note 2)
16	C1N	POWER	This pin is the second side of the C1 fly capacitor.
17	C1P	POWER	This pin is the first side of the C1 fly capacitor.
18	VOUT	OUTPUT, POWER	This pin provides the output power to the external LED. Since the regulation is based on a current loop, the voltage will varies as the output current varies in the application. The Vout pin must be bypassed to GND by a 4.7 μF ceramic capacitor. (Note 3)
19	PVBAT	INPUT, POWER	This pin provides the supply voltage to the charge pump converter. The pin must be connected to the AVbat supply source and bypassed to GND by a 10 μF/16 V ceramic capacitor. (Note 3) Using a power plane is recommended.
20	C2N	POWER	This pin is the second side of the C2 fly capacitor.
21	C2P	POWER	This pin is the first side of the C2 fly capacitor.
22	C3P	POWER	This pin is the second side of the C3 fly capacitor.
23	C3N	POWER	This pin is the first side of the C3 fly capacitor.
24	AVbat	INPUT, POWER	This pin provides the supply voltage to the analog and digitals blocks. The pin must be connected to the PVbat supply source and bypassed to GND by a 1 μF/16 V ceramic capacitor. (Note 3) Using a power plane is recommended.

1. To achieve a good accuracy of the LED current, 1% tolerance resistor, with 100 ppm stability, or better, shall be used. The reference current is internally mirrored and sized according to the programmed value for a given external LED.
2. Total DC−DC output current is limited to 500 mA.
3. Ceramic X7R, ESR < 50 mΩ ESL < 0.5 nH, SMD types capacitors are mandatory to achieve the Iout specifications. On the other hand, care must be observed to take into account the DC bias impact on the capacitance value; see ceramic capacitor manufacturer data sheets.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply	V_{bat}	7.0	V
Digital Input Voltage Digital Input Current	SDA, SCL –	$-0.3 \le V_{in} \le V_{BAT} + 0.3$ 1.0	V mA
ESD Capability (Note 4) Human Body Model (HBM) Machine Model (MM)	V_{ESD}	 2.0 200	 kV V
QFN24 Package Power Dissipation @ T_A = +85°C (Note 5) Thermal Resistance, Junction–to–Air (according to JEDEC/EIA JESD51–12)	 P_D $R_{\theta JA}$	 250 160	 mW °C/W
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Latchup Current Maximum Rating (per JEDEC standard: JESD78) Class II	–	± 100	mA
Moisture Sensitivity Level (Note 6)	MSL	1	–

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM): JESD22–A114.
   Machine Model (MM): JESD22–A115.
5. The maximum package power dissipation limit must not be exceeded.
6. Moisture Sensitivity Level (MSL): per IPC/JEDEC standard: J–STD–020A.

POWER SUPPLY SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced –40°C to +85°C ambient temperature, unless otherwise noted.)

Pin	Symbol	Rating	Min	Typ	Max	Unit
19, 24	PV_{bat}, AV_{bat}	Power Supply	2.7	–	5.5	V
18	I_{out}	Continuous DC Current in the Load @ V_{out} = 8xLED, V_{bat} = 3.4 V	500	–	–	mA
18	Isch	Continuous Output Short Circuit Current	–	60	120	mA
18	Vout	Output Voltage Compliance (OVP)	4.8	–	5.5	V
24	I_{stdb}	Standby Current, @ I_{out} = 0 mA, @ 2.7 V < Vbat < 4.2 V	–	–	5.0	μA
19	I_{op}	Operating Current, @ I_{out} > 0 mA PV_{bat} = 3.6 V PV_{bat} = 4.2 V	 – –	 0.5 0.8	 – –	mA
	Fpwr	Charge Pump Operating Frequency (Any C_{FLY} Capacitor Pins)	–	1.3	–	MHz
7, 8, 9, 10	I_{MAT}	Output LED to LED Current Matching, @ V_{bat} = 3.6 V, I_{LED} = 20 mA, LED1 to LED4 are Identical	 2.0	 ±0.5	 2.0	%
7, 8, 9, 10	I_{TOL}	Output Current Tolerance, LED1 to LED4 @ V_{bat} = 3.6 V, I_{LED} = 20 mA	 –	 ±2.0	 –	%
11, 12, 14, 15	I_{MAT}	Output LED to LED Current Matching, @ V_{bat} = 3.6 V, I_{LED} = 80 mA, LED5 to LED8 are Identical	 2.0	 ±0.5	 2.0	%
11, 12, 14, 15	I_{TOL}	Output Current Tolerance, LED5 to LED8 @ V_{bat} = 3.6 V, I_{LED} = 80 mA	 –	 ±2.0	 –	%
18	t_{start}	DC–DC Start Time (C_{out} = 4.7 μF) – from Vbat Operating to Full Load Operation	 –	 150	 –	μs
	T_{SD}	Thermal Shutdown Protection	–	160	–	°C
	T_{SDH}	Thermal Shutdown Protection Hysteresis	–	30	–	°C

ANALOG SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced –25°C to +85°C ambient temperature, unless otherwise noted.)

Pin	Symbol	Rating	Min	Typ	Max	Unit
3	I_{REFBK}	Backlight Reference Current @ Vref = 600 mV (Notes 7, 8)	1.0	–	100	μA
3		Reference Current (I_{REF}) to Backlight Ratio	–	40	–	–
2	I_{REFFL}	Flash Reference Current @ Vref = 600 mV (Notes 7, 8)	1.0	–	100	μA
2		Reference Current (I_{REF}) to Flash Ratio	–	40	–	–
4, 5	C_{in}	Input Capacitance (Parameter not tested, guaranteed by design)	–	–	10	pF

7. The overall output current tolerance depends upon the accuracy of the external resistor. Using 1% or better resistor is recommended.
8. The external circuit must not force the I_{REF} pin voltage either higher or lower than the 600 mV specified.

DIGITAL PARAMETERS SECTION @ 2.70 V ≤ V_{CC} ≤ 5.5 V (T_A = –25°C to +85°C unless otherwise noted.)
Note: Digital inputs undershoot ≤ –0.30 V to ground. Digital inputs overshoot ≤ 0.30 V to V_{CC}.

Pin	Symbol	Rating	Min	Typ	Max	Unit
5	F_{CLK}	Input I2C Clock, Duty Cycle = 50%	–	–	400	kHz
4, 5	V_{IH}	Positive–Going Input High Voltage Threshold (SDA, SCL)	0.7 × V_{CC}	–	V_{cc} + 0.5 V	V
4, 5	V_{IL}	Negative–Going Input High Voltage Threshold (SDA, SCL)	0	–	0.4	V

9. The V_{CC} Bias pins can be either left open, or biased by the same voltage as the external MCU power supply source. An external 10 nF capacitor might be necessary to improve the I2C function when operating with SDA and SCL signal amplitude below 1.8 V.
10. Expernal pullup resistors shall be connected to properly bias the SDA and SCL logic levels according to the I2C specifications.

APPLICATIONS INFORMATION

DC−DC OPERATION

The converter is based on a charge pump technique to generate a DC voltage capable to supply the white LED load. The system regulates the current flowing into each LED by means of internal current mirrors associated with the white diodes. Consequently, the output voltage will be equal to the Vf of the LED, plus the 300 mV (typical) developed across the internal NMOS mirror. Typically, assuming a standard white LED forward biased at 10 mA, the output voltage will be 3.2 V.

The third external capacitor makes possible the 1.33X extra mode of operation, with a significant efficiency improvement of the converter over the normal battery voltage span. The threshold levels have been defined to optimize this range of operating voltages, assuming a high efficiency is not relevant when the system is connected to a battery charger (i.e. Vbat > 4.5 V).

The built−in OVP circuit continuously monitors each output and stops the converter when the voltage is above 5.0 V. The converter resumes normal operation when the voltage drops below 5.0 V (no latch−up mechanism). Consequently, the chip can operate with no load during any test procedures, but in the case of special applications, it is recommended to connect the unused LED driver either to the V_{OUT} supply to avoid any uncontrolled operation.

The structure is built with power MOS devices to accommodate the modes selected by the analog functions.

The current flowing into each LED is continuously regulated according to the value defined by the programming message. The total current is limited to 500 mA DC.

The system runs with two cycles:

– Cycle#1

Fly capacitors are charged from the battery.

– Cycle#2

Energy accumulated into the fly capacitors is transferred to the load.

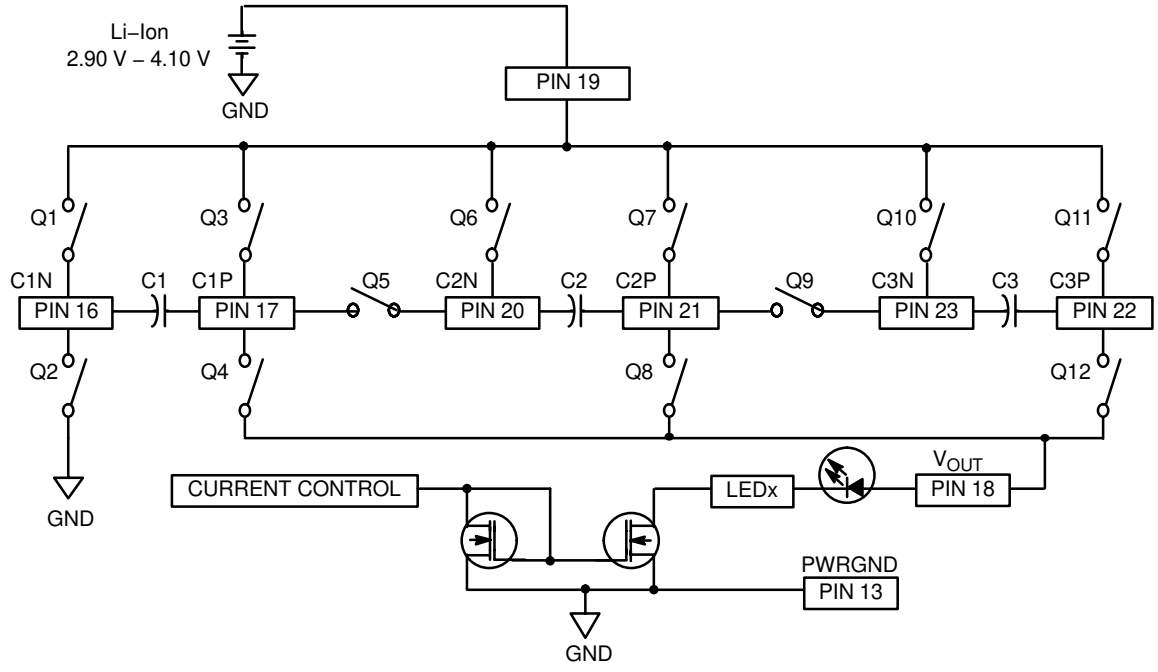


Figure 3. Basic DC−DC NCP5608 Converter Structure

LOAD CURRENT CALCULATION

The load current is derived from the 600 mV reference voltage provided by the internal band gap associated to the external resistor connected across the I_{REFBK} and I_{REFFL} pins and GND (see Figure 4). In any case, no voltage shall be forced at I_{REFBK} or I_{REFFL} pins, either downward or upward. The backlight block, LED1 − LED4, is powered by the current reference defined at the I_{REFBK} pin. The output current can be dimmed by means of a dynamic modulation of the I_{REFBK} pin.

The I_{REFBK} reference current is multiplied by the constant ka to yield the output backlight LED load current. Since the reference voltage is based on a temperature compensated bandgap, a tight tolerance resistor will provide a very accurate load current.

The ka parameter is derived from the constant 40 multiplied by the binary defined in the PWRLED_BK register. Consequently, ka varies from 40 (1.0 mA output/LED) to 1200 to support the full output current range. The resistor is calculated from the Ohm's law ($R = Vref/I_{REF}$) and a more practical equation can be arranged to define the resistor value for a given output current:

Let $Iout = 4*I_{LED}$, then:

$$R_{BK} = (Vref * ka * 30)/I_{out}$$
$$R_{BK} = (0.6 * 1200)/I_{out} \quad \text{(eq. 1)}$$
$$R_{BK} = 720/I_{out}$$

Consequently, the resistor value will range between
$R_{BK} = 720/(30\ mA*4) = 6000\ \Omega$ and
$R_{BK} = 720/(0.5\ mA*4) = 360\ k\Omega$ for the low power block.

Similarly, the PowerFlash block, LED5−LED8, is powered by the current reference defined at the I_{REFFL} pin. The same calculation as before applies, assuming kb = 40, the maximum output current being 100 mA/LED:

Let $Iout = 4*I_{LED}$, then:

$$R_{FL} = (Vref * kb * 100)/I_{out}$$
$$R_{FL} = (0.6 * 4000)/I_{out} \quad \text{(eq. 2)}$$
$$R_{FL} = 2400/I_{out}$$

Finally, the resistor value will range between
$R_{FL} = 2400/(100\ mA*4) = 6000\ \Omega$ and
$R_{FL} = 2400/(1\ mA*4) = 600\ k\Omega$ for the High Power Flash block.

On the other hand, the output currents can be dimmed by means of a dynamic modulation of their respective I_{REFBK}/I_{REFFL} pins current references. Obviously, the tolerance of such resistors must be 1% or better, with a 100 ppm thermal coefficient, to get the expected overall tolerance.

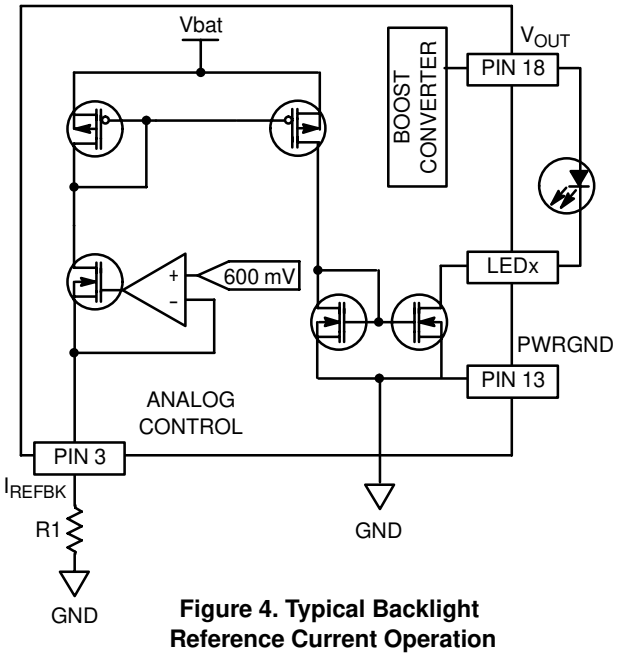


Figure 4. Typical Backlight Reference Current Operation
(Similar Circuit Applies for Power Flash Section)

Note: Due to relative high impedance connected at the reference current pins, cares must be observed to minimize the noise pick−up and stray current present at PCB level. Multi layer layout, with dedicated ground screen, is mandatory.

SERIAL LINK I2C PROTOCOL

The chip is remotely controlled by means of a byte transferred along a serial link between the MCU and the NCP5608. The industrial standard I2C protocol is used, although one can drive the SCL and SDA signal from standard MCU I/O pins . Two dedicated internal registers are used to decode the SDA content and to store the output currents.

The I2C message carries three bytes within the same frame:

Byte #1:
The content of this byte is the physical address of the NCP5608 in the I2C bus.

Byte #2:
The content of this byte contains the address of the selected block.

Byte #3:
This byte contains the output current value to set up the selected block.

In order to improve the efficiency of the back light block when three LED only are used, one can disconnect the fourth LED by setting B6 = Low simultaneously with the third byte (see Table 1).

Table 1. Programming Table

Byte	B7	B6	B5	B4	B3	B2	B1	B0	Comments
Byte #1	0	1	1	1	0	0	1	0	This is the I2C address
Byte #2	0	0	0	0	0	0	0	1	$01 = Select the Back Light internal register
Byte #2	0	0	0	0	0	0	1	0	$02 = Select the Power Flash internal register
Byte #3	1	0	0	X	X	X	X	X	Assuming Byte #2 = $01, then: Bits[0..4] = Back Light output current Bit[5..6] = shall be Low Bit[7] = control the fourth LED in the Back Light Block: B7 = 0 → LED 4th disconnect B7 = 1→ LED 4th connected
Byte #3	0	X	X	X	X	X	X	X	Assuming Byte #2 = $02, then: Bits[0..6] = Power Flash output current Bit[7] = shall be Low

LED CURRENT CONTROL REGISTERS

The eight LED are split in two blocks:

Back Light Block:
LED1 to LED4, current limited to 30 mA per LED

Flash or High Power Block:
LED5 to LED8, current limited to 100 mA per LED

The programmed value of a given bank of LED is memorized into the appropriate registers. There is one register for each set of LED:

PWRLED_BK[0..4]
Stores the Back Light output current.

PWRLED_FL[0..6]
Stores the Power Flash output current.

The total output current is limited to 500 mA, whatever be the configuration.

Table 2. Internal LED Current Control Register

Internal LEDs registers	Bit								Unit
	B7	B6	B5	B4	B3	B2	B1	B0	
PWRLED_BK[7..0]	BLED4 (Note 12)	RFU (Note 11)	RFU (Note 11)	16	8.0	4.0	2.0	1.0	mA
PWRLED_FL[7..0]	RFU (Note 11)	64	32	16	8.0	4.0	2.0	1.0	mA

11. Reserved for future use.
12. Activates/deactivates LED4.

OUTPUT LED PROGRAMMING SEQUENCE

Once the maximum output current has been set up by the external resistor (see Load Current Calculation paragraph above), the I2C protocol can be used to dynamically adjust the brightness of the selected block.

At this point, the dimming of each block depends upon the content of the appropriate register (PWRLD_BK[4..0] or PWRLED_FL[6..0]). The LED current can be calculated according to the digital value stored into the registers.

The LED can be programmed in four steps:

1. Define the maximum ILEDBK−MAX and ILEDFL−MAX currents requested by the Back Light and Flash applications (set by external resistors). This is the maximum current that will be reached when the registers will be at their respective full range (PWRLD_BK[4..0] = $1F = 31 Decimal, PWRLED_FL[6..0] = $7F= 127 decimal).
2. Calculate the reference current (Irefbk and Ireffl):
   Irefbk = ILED−BK/1200 and
   Ireffl = ILED−FL/4000
3. Calculate the external resistor value
   RBK = 0.6/Irefbk
   RFL = 0.6/Ireffl
4. The dimming of flash and backlight LED will be now achieved by changing the PWRLD_BK[4..0] and PWRLED_FL[6..0] registers content to get the operating LED current along the curves 0 mA to ILED−BK−MAX mA and 0 mA to ILED−FL mA:
   BK−NSteps = number of steps stored into the PWRLD_BK register (value, in decimal, of the PWRLD_BK[4..0] register)
   FL−NSteps = number of steps stored into the PWRLED_FL register (value, in decimal, of the PWRLD_FL[6..0] register)
   ILEDBK = (ILEDBK−MAX/31) * BK−NSteps
   ILEDFL = (ILEDFL−MAX/127) * FL−NSteps

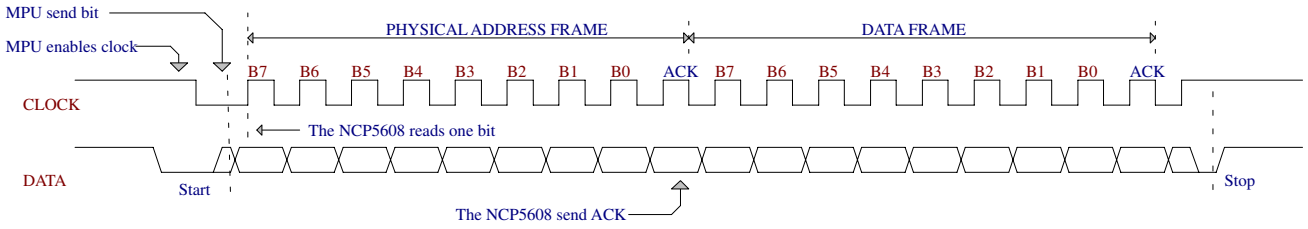
PHYSICAL ADDRESS

The physical I2C address dedicated to the NCP5608 to support the I2C protocol is: 0111 001X → $72. The external controller must fulfill the I2C protocol to drive the chip: see I2C−BUS SPECIFICATION, Version 2.1. The NCP5608 operates as a Slave only and never takes over the I2C control.

Table 3. NCP5608 Operation Truth Table

PWRLED_BK (0−7)	PWRLED_FL (0−7)	Output Voltage	Comments
$00	$00	Forced to zero	DC−DC = OFF
>$80	X	Vfbk + Vsense	DC−DC = ON, LED1 to LED4 active
>$00	X	Vfbk + Vsense	DC−DC = ON, LED1 to LED3 active LED4 deactivated
X	>$00	Vffl + Vsense	DC−DC = ON

The I2C protocol is based on the standard format defined in the industry. Basically, the DATA is transferred from the MCU to the NCP5608 registers by means of the SDA message associated to the SCL clock. The MCU presents the 8 bits during the low state of the SCK signal and the peripheral device (in our case, the NCP5608) shall reads the bits during the high state of the same clock. The transfer is MSB first as depicted in Figure 5.



NOTE: See I2C−BUS SPECIFICATION, Version 2.1, January 2000, for further timing details.

Figure 5. Basic I2C Timings

The three bytes, defined to program the chip, must be sent during the same transaction as depicted in Figure 6 and Figure 7. Leaving aside the ACK signal, the NCP5608 does not provide any digital feedback. The selected PWRLED−BK or PWRLED−FL register described above will be updated according to the content of the third byte serially sent to the chip. Finally, the selected bank of LED will be updated on the last I2C clock positive going slope of the third byte, the DATA being transferred to the appropriate latchup register as defined by the content of the second byte.

The DC−DC charge pump is deactivated when both registers are set to zero as depicted in Table 3.

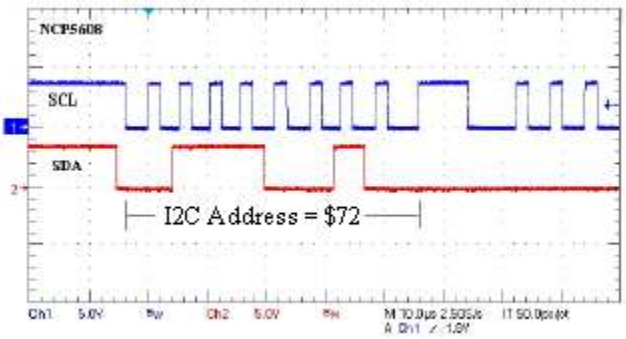


Figure 6. Typical Transaction I2C Sequence: I2C Address

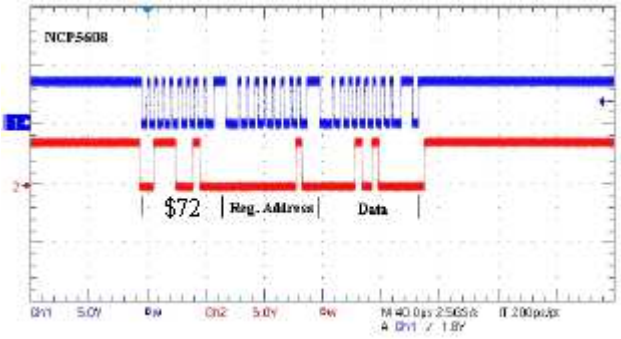


Figure 7. Typical Full I2C Data Transfer

TYPICAL OPERATING CHARACTERISTICS

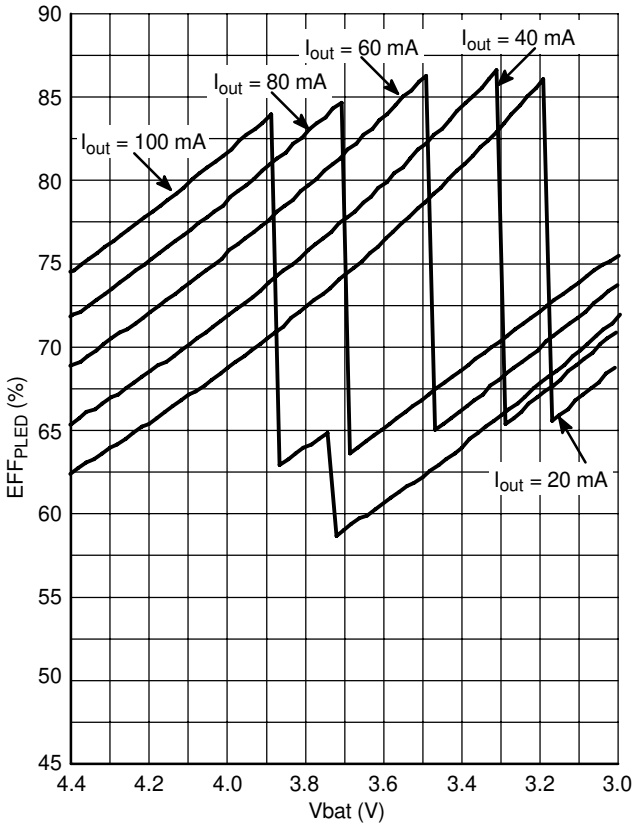


Figure 8. Back Light Efficiency vs. Battery Voltage (LED1 to LED4)

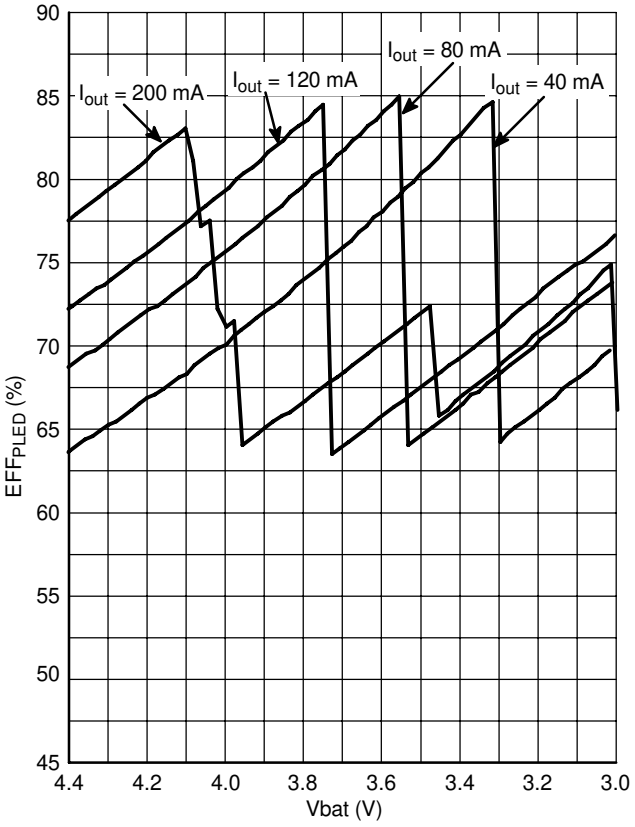


Figure 9. Power Flash Efficiency vs. Battery Voltage (LED5 to LED8)

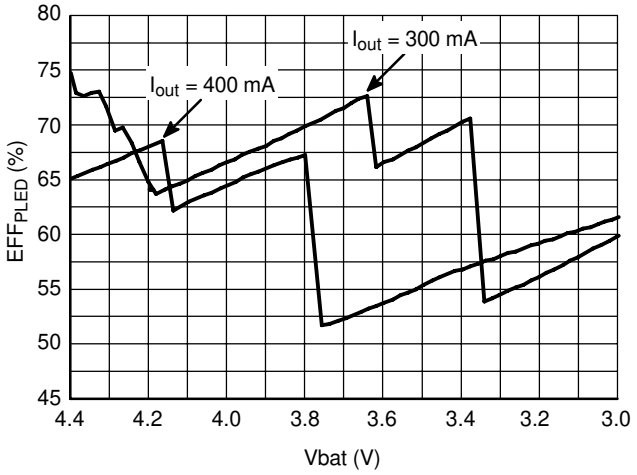


Figure 10. Power Flash Efficiency vs. Battery Voltage (LED5 to LED8) at Full Power

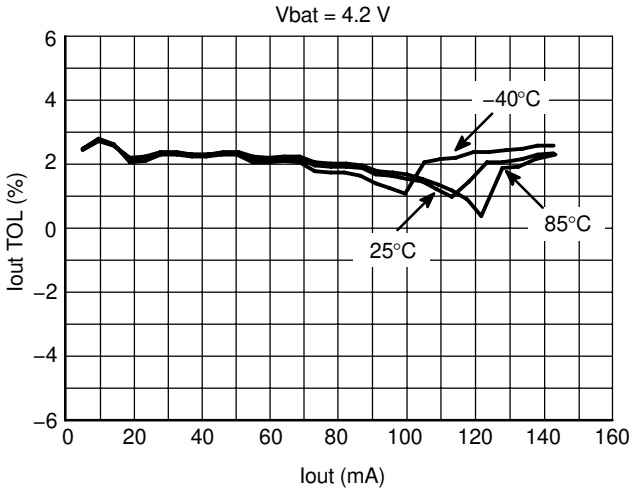


Figure 11. Back Light Output Current Tolerance (LED1 to LED4)

TYPICAL OPERATING WAVEFORMS

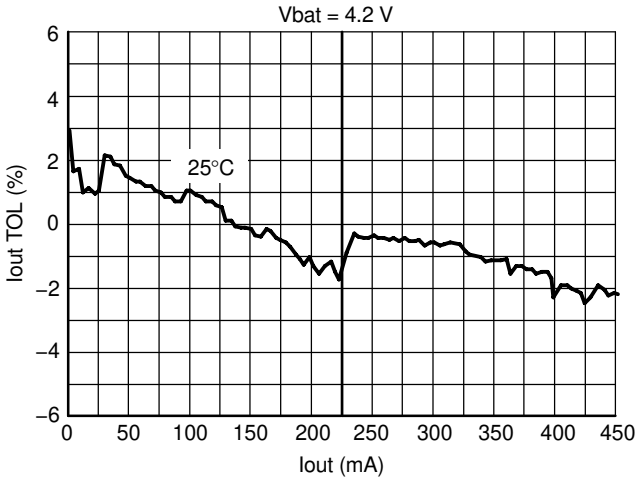


Figure 12. Power Flash Output Current Tolerance (LED5 to LED8)

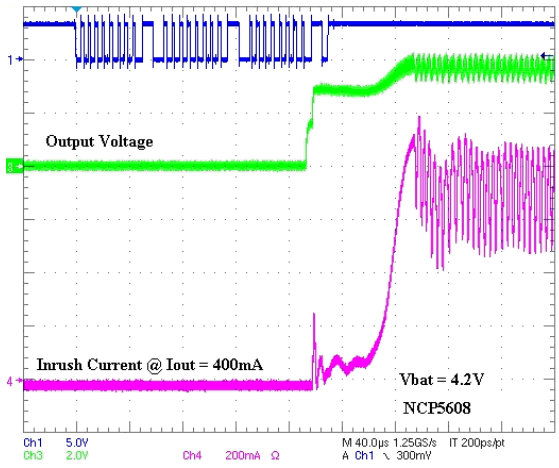


Figure 13. Typical Powerup Response

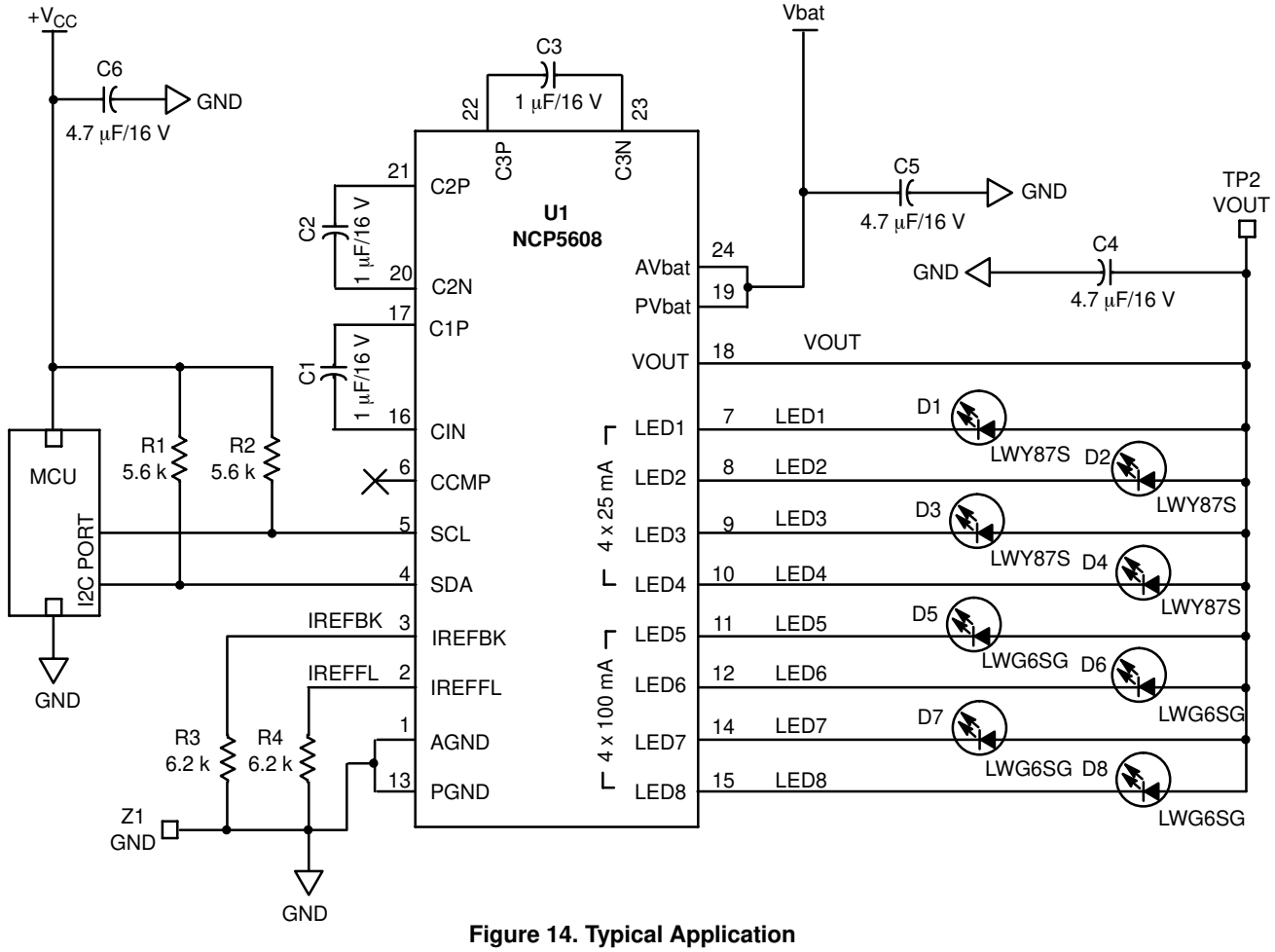


Figure 14. Typical Application

Table 4. Recommended Passive Parts

Part	Manufacturer	Description	Part Number
Ceramic Cap. 1 μF/16 V	TDK	Footprint 0805	C2012X5R1C105MT
Ceramic Cap. 4.7 μF/6.3 V	TDK	Footprint 1206	C3216X5R1C475MT
Ceramic Cap. 10 μF/6.3 V	TDK	Footprint 1206	C3216X5R1C106MT

TYPICAL LEDS LOAD MAPPING

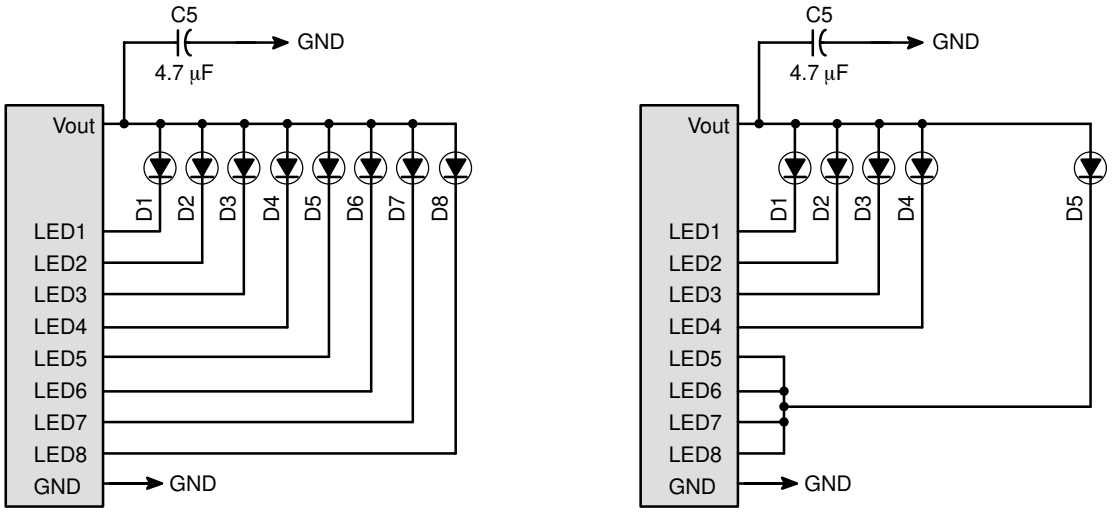


Figure 15. Examples of Possible LED Connections

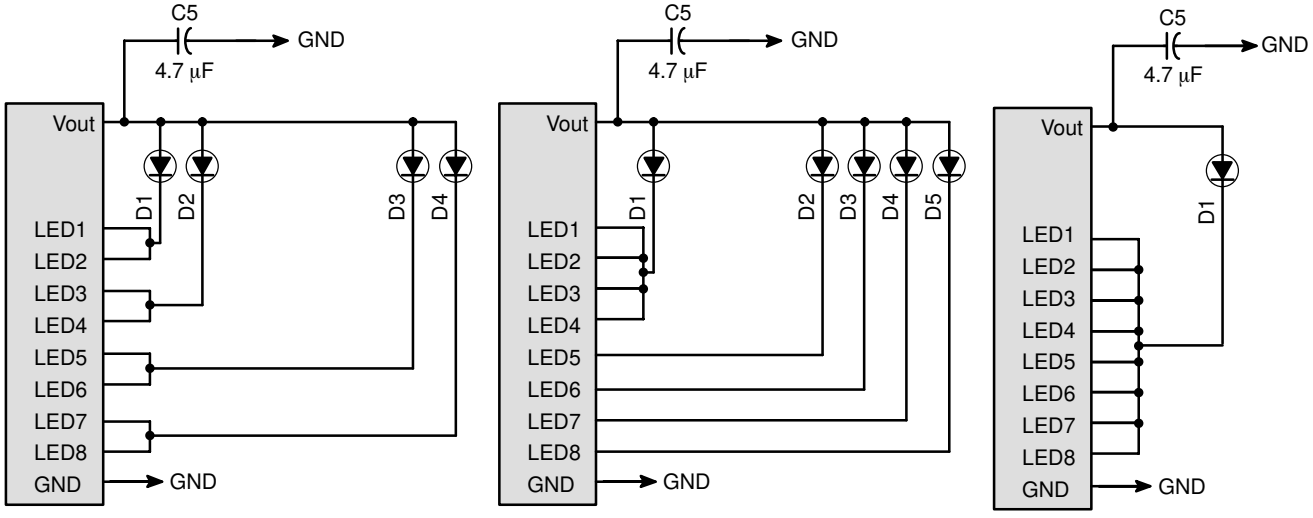


Figure 16. Examples of Possible LED Arrangements

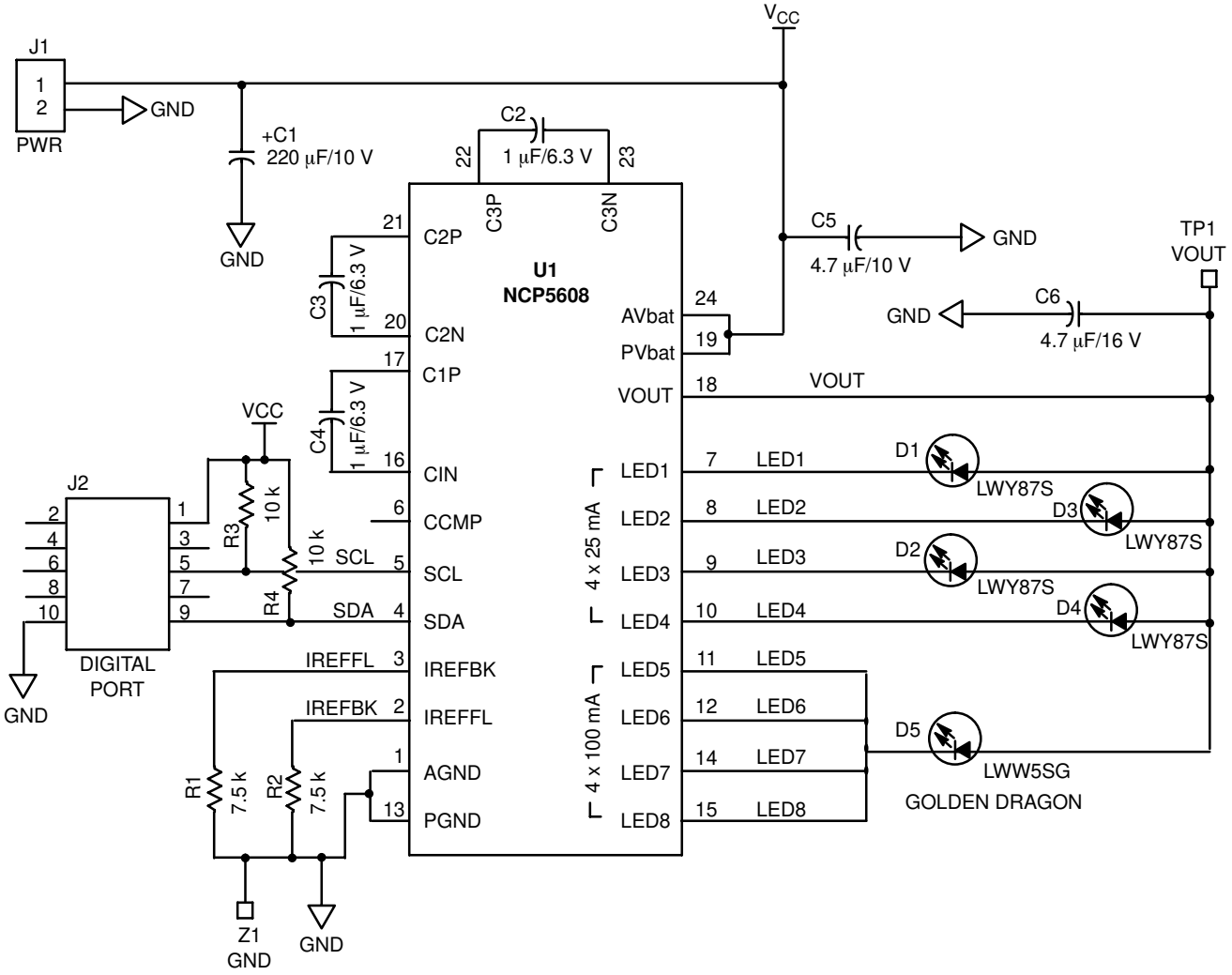


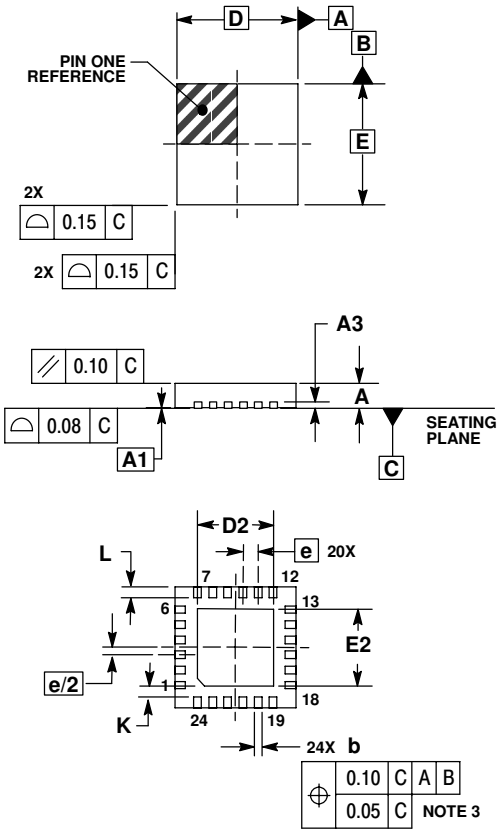
Figure 17. Demo Board Schematic Diagram

ABBREVIATIONS

FB	FeedBack
POR	Power On Reset: internal pulse to reset the chip when the power supply is applied
I2C	Inter Integrated Chip Communication
SDA	Serial DATA, Bidirectional line, associated to the I2C protocol
SCL	Serial Clock, associated to the I2C protocol
REGBL	Register Back Light
REGFL	Register Flash

PACKAGE DIMENSIONS

24 PIN TQFN, 4X4
CASE 511AA–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.40	2.50	2.60
E		4.00 BSC	
E2	2.40	2.50	2.60
e		0.50 BSC	
K	0.20	---	---
L	0.30	0.40	0.50

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