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NCP81022

Dual Output 4 Phase Plus 1 Phase Digital Controller with SVI2 Interface for Desktop and Notebook CPU Applications

ON Semiconductor®

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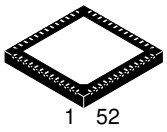


QFN52
CASE 485BE

MARKING DIAGRAM

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 40 of this data sheet.

The NCP81022 dual output four plus one phase buck solution is optimized for AMD® SVI2 CPUs. The controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed−forward, and adaptive voltage positioning to provide accurately regulated power for both desktop and notebook applications.

The control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing providing an ultra fast initial response to dynamic load events and reduced system cost. The NCP81022 provides the mechanism to shed to single phase during light load operation and can auto frequency scale in light load conditions while maintaining excellent transient performance.

Dual high performance operational error amplifiers are provided to simplify compensation of the system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed−loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate current monitoring for droop and digital current monitoring.

Features

- Meets AMD'S SVI2 Specifications
- Four phase CPU Voltage Regulator
- One phase North Bridge Voltage Regulator
- Current Mode Dual Edge Modulation for Fast Initial Response to Transient Loading
- Dual High Performance Operational Error Amplifier
- One Digital Soft Start Ramp for Both Rails
- Dynamic Reference Injection
- Accurate Total Summing Current Amplifier
- DAC with Droop Feed−forward Injection
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase−to−Phase Dynamic Current Balancing
- "Lossless" DCR Current Sensing for Current Balancing
- Summed Compensated Inductor Current Sensing for Droop
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 240 kHz – 1.0 MHz
- Startup into Pre−Charged Loads while avoiding False OVP
- Power Saving Phase Shedding
- Vin Feed Forward Ramp Slope
- Pin Programming for Internal SVI2 Parameters
- Over Voltage Protection (OVP) and Under Voltage Protection (UVP)
- Over Current Protection (OCP)
- Dual Power Good Output with Internal Delays
- These Devices are Pb−Free and Halogen Free

Applications

- Desktop and Notebook Processors
- Gaming

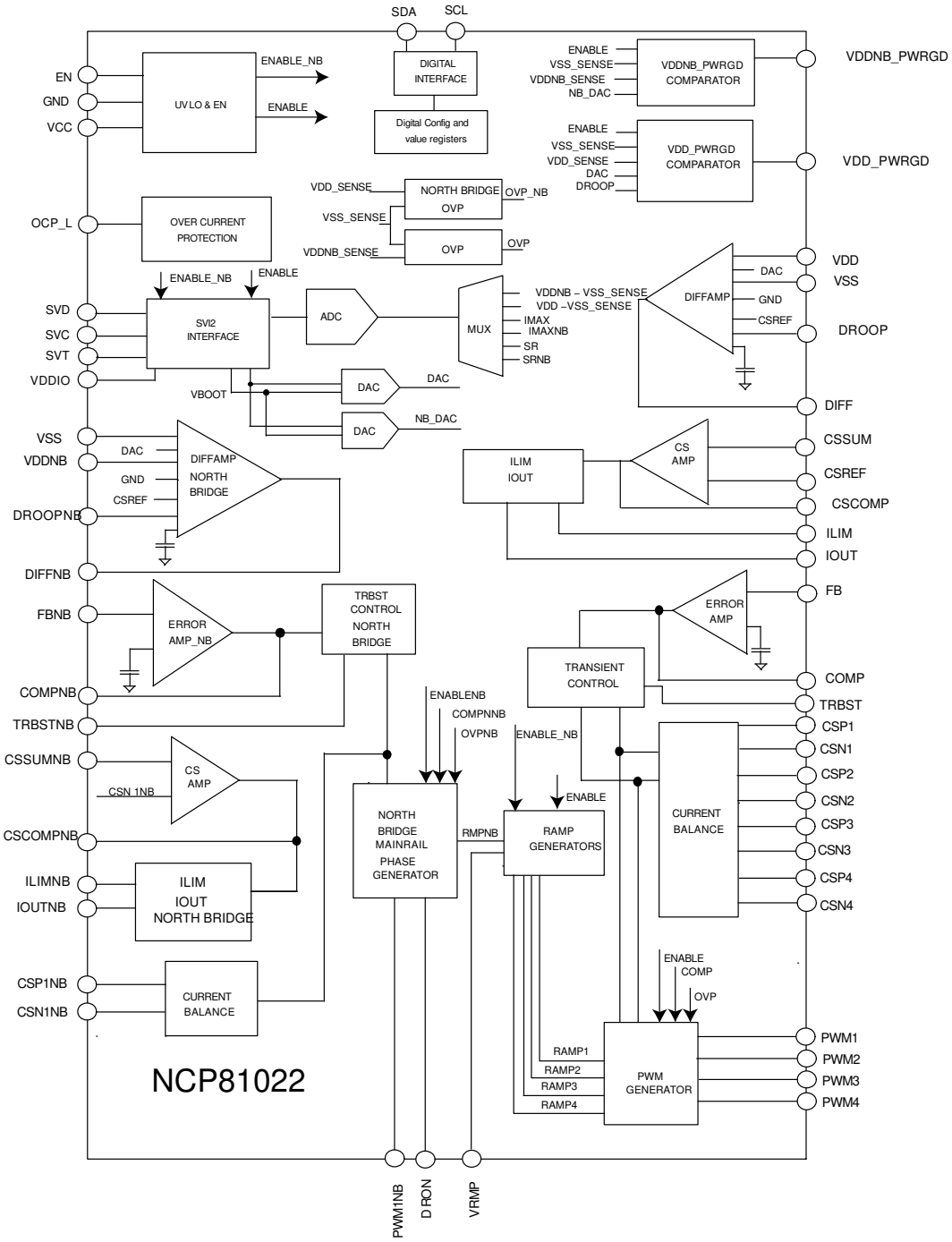


Figure 1. Block Diagram

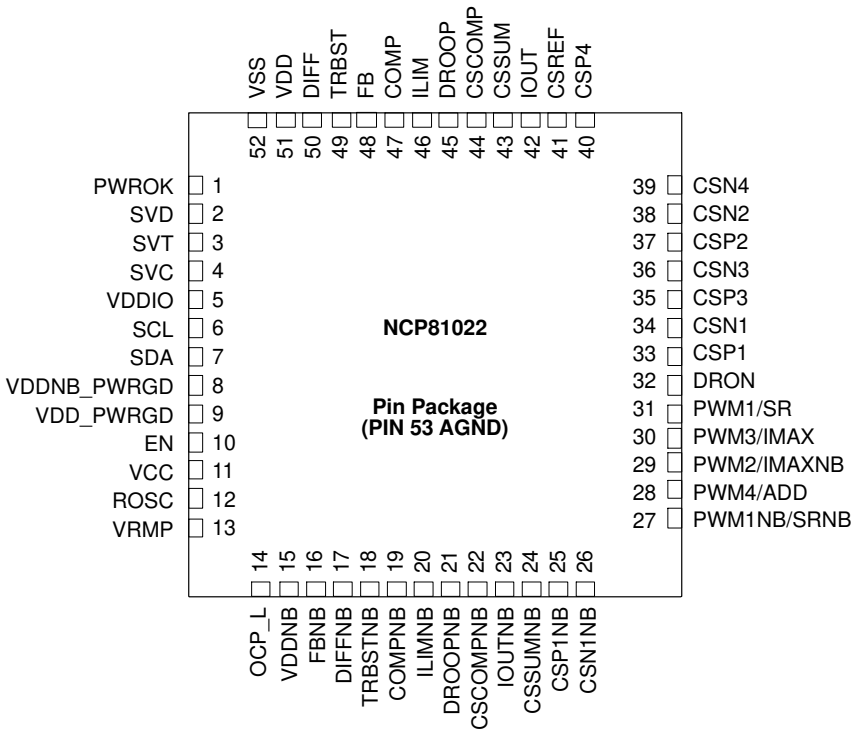


Figure 2. NCP81022 Pinout

QFN52 PIN LIST DESCRIPTION

Pin No.	Symbol	Description
1	PWROK	Active high system wide power ok signal
2	SVD	Serial VID data line
3	SVT	Serial VID telemetry line
4	SVC	Serial VID clock line
5	VDDIO	VDDIO is an interface power rail that serves as a reference for SVI2 interface
6	SCL	serial clock line, Open drain, requires pullup resistor
7	SDA	Bi directional serial data line. Open drain, requires pullup resistor.
8	VDDNB_PWRGD	Open drain output. High output on this pin indicates that the North Bridge Rail output is regulating.
9	VDD_PWRGD	Open drain output. High output on this pin indicates that the Main Rail output is regulating.
10	EN	Logic input. Logic high enables Main and North Bridge Rail output and logic low disables main rail output.
11	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground.
12	ROSC	A resistor to ground on this pin will set the oscillator frequency
13	VRMP	Feed−forward input of Vin for the ramp slope compensation. The current fed into this pin is used to control of the ramp of PWM slope
14	OCP_L	Open drain output. Signals an over current event has occurred
15	VDDNB	Non−inverting input to the North Bridge Rail differential remote sense amplifier.
16	FBNB	Error amplifier voltage feedback for North Bridge Rail output
17	DIFFNB	Output of the North Bridge Rail differential remote sense amplifier.
18	TRBSTNB	Compensation pin for the load transient boost for North Bridge Rail
19	COMPNB	Output of the error amplifier and the inverting inputs of the PWM comparators for the North Bridge Rail output.

QFN52 PIN LIST DESCRIPTION

Pin No.	Symbol	Description
20	ILIMNB	Over current shutdown threshold setting for North Bridge Rail output. Resistor to CSCOMP to set threshold.
21	DROOPNB	Used to program DACFF function for North Bridge Rail output. It's connected to the resistor divider placed between CSCOMPNB and CSREFNB summing node.
22	CSCOMPNB	Output of total current sense amplifier for North Bridge Rail output.
23	IOUTNB	Total output current monitor for North Bridge Rail.
24	CSSUMNB	Inverting input of total current sense amplifier for North Bridge Rail output.
25	CSP1NB	Non−inverting input to current balance sense amplifier for phase 1NB
26	CSN1NB	Inverting input to current balance sense amplifier for phase1NB
27	PWM1NB/SRNB	North Bridge Phase1 PWM output. A resistor from this pin to ground programs SR North Bridge rail
28	PWM4/ADD	Main Rail Phase 4PWM output. A resistor from this pin to ground programs the SMBus address.
29	PWM2/IMAXNB	Main Rail Phase 2PWM output. During start up it is used to program ICC_MAX for the North Bridge Rail with a resistor to ground
30	PWM3/IMAX	Main Rail Phase 3PWM output. During start up it is used to program ICC_MAX for the Main Rail with a resistor to ground
31	PWM1/SR	Main Rail Phase 1PWM output. A resistor to ground on this pin programs SR Main rail.
32	DRON	Bidirectional gate driver enable for external drivers for both Main and North Bridge Rails. It should be left floating if unused.
33	CSP1	Non−inverting input to current balance sense amplifier for Main Rail phase 1
34	CSN1	Non−inverting input to current balance sense amplifier for Main Rail phase 1
35	CSP3	Non−inverting input to current balance sense amplifier for Main Rail phase 3
36	CSN3	Inverting input to current balance sense amplifier for Main Rail phase3
37	CSP2	Non−inverting input to current balance sense amplifier for Main Rail phase 2
38	CSN2	Inverting input to current balance sense amplifier for Main Rail phase2
39	CSN4	Inverting input to current balance sense amplifier for Main Rail phase4
40	CSP4	Non−inverting input to current balance sense amplifier for Main Rail phase 4
41	CSREF	Total output current sense amplifier reference voltage input for Main Rail and inverting input to Main Rail current balance sense amplifier for phase 1 and 2
42	IOUT	Total output current monitor for Main Rail.
43	CSSUM	Inverting input of total current sense amplifier for Main Rail output
44	CSCOMP	Output of total current sense amplifier for Main Rail output
45	DROOP	Used to program DACFF function for Main Rail output. It's connected to the resistor divider placed between CSCOMP and CSREF.
46	ILM	Over current shutdown threshold setting for Main Rail output. Resistor to CSCOMP to set threshold.
47	COMP	Output of the Main Rail error amplifier and the inverting input of the PWM comparator for Main Rail output
48	FB	Error amplifier voltage feedback for Main Rail output
49	TRBST	Compensation pin for the load transient boost for Main Rail
50	DIFF	Output of the Main Rail differential remote sense amplifier.
51	VDD	Non−inverting input to the Main Rail differential remote sense amplifier
52	VSS	Inverting input to the Main Rail differential remote sense amplifier.
53	AGND	

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL INFORMATION

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP, COMPNB	VCC + 0.3 V	–0.3 V	2 mA	2 mA
CSCOMP, CSCOMPNB	VCC + 0.3 V	–0.3 V	2 mA	2 mA
VSS,	GND + 300 mV	GND – 300 mV	1 mA	1 mA
VDD_PWRGD, VDDNB_PWRGD	VCC + 0.3 V	–0.3 V	N/A	2 mA
VCC	6.5 V	–0.3 V	N/A	N/A
VRMP	+25 V	–0.3 V		
All Other Pins	VCC + 0.3 V	–0.3 V		

*All signals referenced to GND unless noted otherwise.

THERMAL INFORMATION

Description	Symbol	Typ	Unit
Thermal Characteristic – QFN Package (Note 1)	R_{JA}	68	°C/W
Operating Junction Temperature Range (Note 2)	T_J	–10 to 125	°C
Operating Ambient Temperature Range		–10 to 100	°C
Maximum Storage Temperature Range	T_{STG}	–40 to +150	°C
Moisture Sensitivity Level – QFN Package	MSL	1	

*The maximum package power dissipation must be observed.
1. JESD 51–5 (1S2P Direct–Attach Method) with 0 LFM
2. JESD 51–7 (1S2P Direct–Attach Method) with 0 LFM

NCP81022 (4+1) ELECTRICAL CHARACTERISTICS

Unless otherwise stated: –10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	MIN	TYP	MAX	Unit
ERROR AMPLIFIER					
Input Bias Current		–400		400	nA
Open Loop DC Gain	C_L = 20 pF to GND, R_L = 10 KΩ to GND		80		dB
Open Loop Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND		55		MHz
Slew Rate	ΔVin = 100 mV, G = –10 V/V, ΔVout = 1.5 V – 2.5 V, CL = 20 pF to GND, DC Load = 10k to GND		20		mV/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.5	–	–	V
Minimum Output Voltage	I_{SINK} = 2.0 mA	–	–	1	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current		–400	–	400	nA
VDD Input Voltage Range		–0.3	–	3.0	V
VSS Input Voltage Range		–0.3	–	0.3	V
–3dB Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND		12		MHz
Closed Loop DC gain VS to DIFF	VS+ to VS– = 0.5 to 1.3 V		1.0		V/V
Droop Accuracy	CSREF–DROOP = 80 mV DAC = 0.8 V to 1.2 V	–1.5		+1.5	mV

NCP81022 (4+1) ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	MIN	TYP	MAX	Unit
DIFFERENTIAL SUMMING AMPLIFIER					
Maximum Output Voltage	I_{SOURCE} = 2 mA	3.0	–	–	V
Minimum Output Voltage	I_{SINK} = 2 mA	–	–	0.5	V
CURRENT SUMMING AMPLIFIER					
Offset Voltage (Vos)	1.2 V	−300		300	μV
Input Bias Current	CSSUM = CSREF= 0.5 – 1.5 V	−1		1	μA
Open Loop Gain			80		dB
Current Sense Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND		10		MHz
Maximum CSCOMP (NB) Output Voltage	Isource = 2mA	3.5	–	–	V
Minimum CSCOMP(NB) Output Voltage	Isink = 500uA	–	–	0.15	V
CURRENT BALANCE AMPLIFIER					
Input Bias Current	CSP1−4NB = CSN1−4NB = 1.2 V CSP = CSN = 1.2 V	−200	–	200	nA
Common Mode Input Voltage Range	CSPx = CSREF	0	–	2.0	V
Differential Mode Input Voltage Range	CSNx = 1.2 V	−100	–	100	mV
Closed loop Input Offset Voltage Matching	CSPx = CSNx =1.2 V, Measured from the average	−1.5	–	1.5	mV
Current Sense Amplifier Gain	0V < CSPx−CSNx < 0.1 V,	5.7	6.0	6.3	V/V
Multiphase Current Sense Gain Matching	CSN = CSP = 10 mV to 30 mV	−3.8		3.8	%
−3dB Bandwidth			8		MHz
BIAS SUPPLY					
Supply Voltage Range		4.75		5.25	
VCC Quiescent Current				48	mA
UVLO Threshold	VCC rising			4.5	V
	VCC falling	3.9			V
VCC UVLO Hysteresis			200		mV
VRMP					
Supply range		4.5		20	V
UVLO Threshold	VCC rising	4.2			V
	VCC falling			3	V
Hysteresis			800		mV
DAC SLEW RATE					
Soft Start Slew Rate			2.5		mv/μs
Slew Rate Slow			5		mv/μs
Slew Rate Fast			20		mv/μs
NORTH BRIDGE Soft Start Slew Rate			2.5		mv/μs
NORTH BRIDGE Slew Rate Slow			2.5		mv/μs
NORTH BRIDGE Slew Rate Fast			10		mv/μs
ENABLE INPUT					
Enable High Input Leakage Current	External 1k pull−up to 3.3 V	–		1.0	μA
Upper Threshold	V_{UPPER}	2			V

NCP81022 (4+1) ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	MIN	TYP	MAX	Unit
ENABLE INPUT					
Lower Threshold	V_{LOWER}			0.8	V
Enable delay time	Measure time from Enable transitioning HI , VBOOT is not 0 V			15	μs
DRON					
Output High Voltage	Sourcing 500 μA	3.0	–	–	V
Output Low Voltage	Sinking 500 μA	–	–	0.1	V
Pull Up Resistances			2.0		kΩ
Rise/Fall Time	CL (PCB) = 20 pF, ΔVo = 10% to 90%		160		ns
Internal Pull Down Resistance	EN = Low		70		kΩ
IOUT OUTPUT /IOUTNB					
Input Referred Offset Voltage	Ilimit to CSREF	−3		+3	mV
Output current max	Ilim Sink current 80 μA	–	–	800	μA
Current Gain	$(IOUT_{CURRENT})$ / $(ILIMIT_{CURRENT})$, R_{LIM} = 20k, R_{IOUT} = 5.0k, DAC = 0.8 V, 1.25 V, 1.52 V	9.5	10	10.5	
OSCILLATOR					
Switching Frequency Range		240	–	1000	kHz
Switching Frequency Accuracy	200 kHz < Fsw < 1 MHz	−10	–	10	%
4 Phase Operation		360	400	440	kHz
OUTPUT OVER VOLTAGE AND UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold During Soft−Start	VDD rising	270	325	380	mV
Over Voltage Delay	VDD rising to PWMx low		50		ns
Under Voltage Threshold Below DAC−DROOP	VDD falling	170	325	380	mV
Under−voltage Hysteresis	VDD rising		25		mV
Under−voltage Delay			5		μs
SVI2 DAC					
System Voltage Accuracy	1.2 V ≤ DAC < 1.55 V 0.8 V< DAC < 1.2 V 0.0 V DAC < 0.800 V	−2 −10 −2		2 10 2	LSB mV LSB
Feed−Forward Current	Measure on DROOP, DROOPNB pin	59	66	71	μA
Droop Falling current	Measure on DROOP, DROOPNB pin	23		29	μA
Droop Feed−Forward Pulse On−Time			0.16		μs
OVERCURRENT PROTECTION					
ILIM Threshold Current (OCP shutdown after 50 μs delay)	Main Rail, RLIM = 20 kΩ	8	10	11.0	μA
ILIM Threshold Current (immediate OCP shut-down)	Main Rail, RLIM = 20 kΩ	13	15	16.5	μA
ILIM Threshold Current (OCP shutdown after 50 μs delay)	Main Rail, (PSI0, PSI1) RLIM = 20 kΩ		10		μA
ILIM Threshold Current (immediate OCP shut-down)	Main Rail, (PSI0, PSI1) RLIM = 20 kΩ		15		μA

NCP81022 (4+1) ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	MIN	TYP	MAX	Unit
OVERCURRENT PROTECTION					
ILIM Threshold Current (OCP shutdown after 50 μs delay)	North Bridge Rail, RLIM = 20 kΩ	8	10	11.0	μA
ILIM Threshold Current (immediate OCP shutdown)	North Bridge Rail, RLIM = 20 kΩ	13	15	16.5	μA
ILIM Threshold Current (OCP shutdown after 50 μs delay)	North Bridge Rail RLIM = 20 kΩ		10		μA
ILIM Threshold Current (immediate OCP shutdown)	North Bridge Rail, RLIM = 20 kΩ		15		μA
MODULATORS (PWM COMPARATORS) FOR MAIN RAIL AND NORTH BRIDGE					
Minimum Pulse Width	Fsw = 360 kHz		60		ns
0% Duty Cycle	COMP voltage when the PWM outputs remain LO		1.3	–	V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI VRMP = 12.0 V	–	2.5	–	V
PWM Ramp Duty Cycle Matching	COMP = 2 V, PWM Ton matching		1		%
PWM Phase Angle Error	Between adjacent phases		±5		Deg
Ramp Feed−forward Voltage range		5		22	V
TRBST#					
Output Low Voltage	I_{Sink} = 500 μA		100		mV
OCP_L#					
Output Low Voltage				0.3	V
Output Leakage Current	High Impedance State	−1.0	–	1.0	μA
ADC					
Voltage Range		0		2	V
Total Unadjusted Error (TUE)		−1.25		1.25	%
Differential Nonlinearity (DNL)	8−bit, No Missing codes			1	LSB
Power Supply Sensitivity			±1		%
Conversion Time			30		μs
Round Robin			90		μs
VDD_PWRGD, VDDNB_PWRGD OUTPUT					
Output Low Saturation Voltage	$I_{VDD(NB)\_PWRGD}$= 4 mA,	–	–	0.3	V
Rise Time	External pull−up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%	–	100		ns
Fall Time	External pull−up of 1 kΩ to 3.3V, C_{TOT} = 45 pF, ΔVo = 90% to 10%		10		ns
Output Voltage at Power−up	VDD_PWRGD, VDDNB_PWRGD pulled up to 5V via 2 kΩ	–	–	1.2	V
Output Leakage Current When High	VDD_ PWRGD& VDDNB_PWRGD = 5.0 V	−1.0	–	1.0	μA
VDD_PWRGD Delay (rising)	DAC=TARGET to VDD_PWRGD		5		μs
VDD_PWRGD Delay (falling)	From OCP or OVP	–	5	–	μs
PWM, PWMNB OUTPUTS					
Output High Voltage	Sourcing 500 μA	VCC − 0.2	–	–	V

NCP81022 (4+1) ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	MIN	TYP	MAX	Unit
PWM, PWMNB OUTPUTS					
Output Mid Voltage	No Load	1.9	2.0	2.1	V
Output Low Voltage	Sinking 500 μA	–	–	0.7	V
Rise and Fall Time	CL (PCB) = 50 pF, ΔVo = GND to VCC	–	10		ns
Tri−State Output Leakage	Gx = 2.0 V, x = 1−4, EN = Low	−1.0	–	1.0	μA
2/3/4 PHASE DETECTION FOR MAIN BRIDGE					
CSN2, CSN3, CSN4 Pin Threshold Voltage		4.7			V
Phase Detect Timer			2.3		ms
SVC, SVD, SVT, PWROK					
VDDIO	Nominal Bus voltage	1.14		1.95	V
VIL	Input Low Voltage			35	%
VDDIO Current	VDDIO = 1.95			100	μA
VIH	Input High Voltage	70			%
VHYS	Hysteresis Voltage	10			%
VOH	Output High Voltage	VDDIO − 0.2		VDDIO	V
VOL	Output Low Voltage	0		0.2	V
Leakage Current		−100		100	μA
Pad Capacitance				4.0	pF
clock to data delay (Tco)		4		8.3	ns
Setup time (Tsu)		5		10	ns
Hold time (Thold)		5		10	ns
SMBus INTERFACE, SDA, SCL					
Logic High Input Voltage	$V_{IH(SDA, SCL)}$	2.1			V
Logic Low Input Voltage	$V_{IL(SDA, SCL)}$			0.8	V
Hysteresis			500		mV
SDA Output low voltage, V_{OL}	I_{SDA} = −6 mA			0.4	V
Input Current		−1		1	μA
Input Capacitance			5.0		pF
Clock Frequency				400	kHz
SCL Falling Edge to SDA Valid Time				1.0	μs

Table 1. SVI2 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	1.55000	00
0	0	0	0	0	0	0	1	1.54375	01
0	0	0	0	0	0	1	0	1.53750	02
0	0	0	0	0	0	1	1	1.53125	03
0	0	0	0	0	1	0	0	1.52500	04
0	0	0	0	0	1	0	1	1.51875	05
0	0	0	0	0	1	1	0	1.51250	06
0	0	0	0	0	1	1	1	1.50625	07
0	0	0	0	1	0	0	0	1.50000	08
0	0	0	0	1	0	0	1	1.49375	09
0	0	0	0	1	0	1	0	1.48750	0A
0	0	0	0	1	0	1	1	1.48125	0B
0	0	0	0	1	1	0	0	1.47500	0C
0	0	0	0	1	1	0	1	1.46875	0D
0	0	0	0	1	1	1	0	1.46250	0E
0	0	0	0	1	1	1	1	1.45625	0F
0	0	0	1	0	0	0	0	1.45000	10
0	0	0	1	0	0	0	1	1.44375	11
0	0	0	1	0	0	1	0	1.43750	12
0	0	0	1	0	0	1	1	1.43125	13
0	0	0	1	0	1	0	0	1.42500	14
0	0	0	1	0	1	0	1	1.41875	15
0	0	0	1	0	1	1	0	1.41250	16
0	0	0	1	0	1	1	1	1.40625	17
0	0	0	1	1	0	0	0	1.40000	18
0	0	0	1	1	0	0	1	1.39375	19
0	0	0	1	1	0	1	0	1.38750	1A
0	0	0	1	1	0	1	1	1.38125	1B
0	0	0	1	1	1	0	0	1.37500	1C
0	0	0	1	1	1	0	1	1.36875	1D
0	0	0	1	1	1	1	0	1.36250	1E
0	0	0	1	1	1	1	1	1.35625	1F
0	0	1	0	0	0	0	0	1.35000	20
0	0	1	0	0	0	0	1	1.34375	21
0	0	1	0	0	0	1	0	1.33750	22
0	0	1	0	0	0	1	1	1.33125	23
0	0	1	0	0	1	0	0	1.32500	24
0	0	1	0	0	1	0	1	1.31875	25
0	0	1	0	0	1	1	0	1.31250	26
0	0	1	0	0	1	1	1	1.30625	27
0	0	1	0	1	0	0	0	1.30000	28
0	0	1	0	1	0	0	1	1.29375	29

Table 1. SVI2 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	1	0	1	0	1	0	1.28750	2A
0	0	1	0	1	0	1	1	1.28125	2B
0	0	1	0	1	1	0	0	1.27500	2C
0	0	1	0	1	1	0	1	1.26875	2D
0	0	1	0	1	1	1	0	1.26250	2E
0	0	1	0	1	1	1	1	1.25625	2F
0	0	1	1	0	0	0	0	1.25000	30
0	0	1	1	0	0	0	1	1.24375	31
0	0	1	1	0	0	1	0	1.23750	32
0	0	1	1	0	0	1	1	1.23125	33
0	0	1	1	0	1	0	0	1.22500	34
0	0	1	1	0	1	0	1	1.21875	35
0	0	1	1	0	1	1	0	1.21250	36
0	0	1	1	0	1	1	1	1.20625	37
0	0	1	1	1	0	0	0	1.20000	38
0	0	1	1	1	0	0	1	1.19375	39
0	0	1	1	1	0	1	0	1.18750	3A
0	0	1	1	1	0	1	1	1.18125	3B
0	0	1	1	1	1	0	0	1.17500	3C
0	0	1	1	1	1	0	1	1.16875	3D
0	0	1	1	1	1	1	0	1.16250	3E
0	0	1	1	1	1	1	1	1.15625	3F
0	1	0	0	0	0	0	0	1.15000	40
0	1	0	0	0	0	0	1	1.14375	41
0	1	0	0	0	0	1	0	1.13750	42
0	1	0	0	0	0	1	1	1.13125	43
0	1	0	0	0	1	0	0	1.12500	44
0	1	0	0	0	1	0	1	1.11875	45
0	1	0	0	0	1	1	0	1.11250	46
0	1	0	0	0	1	1	1	1.10625	47
0	1	0	0	1	0	0	0	1.10000	48
0	1	0	0	1	0	0	1	1.09375	49
0	1	0	0	1	0	1	0	1.08750	4A
0	1	0	0	1	0	1	1	1.08125	4B
0	1	0	0	1	1	0	0	1.07500	4C
0	1	0	0	1	1	0	1	1.06875	4D
0	1	0	0	1	1	1	0	1.06250	4E
0	1	0	0	1	1	1	1	1.05625	4F
0	1	0	1	0	0	0	0	1.05000	50
0	1	0	1	0	0	0	1	1.04375	51
0	1	0	1	0	0	1	0	1.03750	52
0	1	0	1	0	0	1	1	1.03125	53

Table 1. SVI2 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	0	1	0	1	0	0	1.02500	54
0	1	0	1	0	1	0	1	1.01875	55
0	1	0	1	0	1	1	0	1.01250	56
0	1	0	1	0	1	1	1	1.00625	57
0	1	0	1	1	0	0	0	1.00000	58
0	1	0	1	1	0	0	1	0.99375	59
0	1	0	1	1	0	1	0	0.98750	5A
0	1	0	1	1	0	1	1	0.98125	5B
0	1	0	1	1	1	0	0	0.97500	5C
0	1	0	1	1	1	0	1	0.96875	5D
0	1	0	1	1	1	1	0	0.96250	5E
0	1	0	1	1	1	1	1	0.95625	5F
0	1	1	0	0	0	0	0	0.95000	60
0	1	1	0	0	0	0	1	0.94375	61
0	1	1	0	0	0	1	0	0.93750	62
0	1	1	0	0	0	1	1	0.93125	63
0	1	1	0	0	1	0	0	0.92500	64
0	1	1	0	0	1	0	1	0.91875	65
0	1	1	0	0	1	1	0	0.91250	66
0	1	1	0	0	1	1	1	0.90625	67
0	1	1	0	1	0	0	0	0.90000	68
0	1	1	0	1	0	0	1	0.89375	69
0	1	1	0	1	0	1	0	0.88750	6A
0	1	1	0	1	0	1	1	0.88125	6B
0	1	1	0	1	1	0	0	0.87500	6C
0	1	1	0	1	1	0	1	0.86875	6D
0	1	1	0	1	1	1	0	0.86250	6E
0	1	1	0	1	1	1	1	0.85625	6F
0	1	1	1	0	0	0	0	0.85000	70
0	1	1	1	0	0	0	1	0.84375	71
0	1	1	1	0	0	1	0	0.83750	72
0	1	1	1	0	0	1	1	0.83125	73
0	1	1	1	0	1	0	0	0.82500	74
0	1	1	1	0	1	0	1	0.81875	75
0	1	1	1	0	1	1	0	0.81250	76
0	1	1	1	0	1	1	1	0.80625	77
0	1	1	1	1	0	0	0	0.80000	78
0	1	1	1	1	0	0	1	0.79375	79
0	1	1	1	1	0	1	0	0.78750	7A
0	1	1	1	1	0	1	1	0.78125	7B
0	1	1	1	1	1	0	0	0.77500	7C
0	1	1	1	1	1	0	1	0.76875	7D

Table 1. SVI2 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	1	1	1	1	1	0	0.76250	7E
0	1	1	1	1	1	1	1	0.75625	7F
1	0	0	0	0	0	0	0	0.75000	80
1	0	0	0	0	0	0	1	0.74375	81
1	0	0	0	0	0	1	0	0.73750	82
1	0	0	0	0	0	1	1	0.73125	83
1	0	0	0	0	1	0	0	0.72500	84
1	0	0	0	0	1	0	1	0.71875	85
1	0	0	0	0	1	1	0	0.71250	86
1	0	0	0	0	1	1	1	0.70625	87
1	0	0	0	1	0	0	0	0.70000	88
1	0	0	0	1	0	0	1	0.69375	89
1	0	0	0	1	0	1	0	0.68750	8A
1	0	0	0	1	0	1	1	0.68125	8B
1	0	0	0	1	1	0	0	0.67500	8C
1	0	0	0	1	1	0	1	0.66875	8D
1	0	0	0	1	1	1	0	0.66250	8E
1	0	0	0	1	1	1	1	0.65625	8F
1	0	0	1	0	0	0	0	0.65000	90
1	0	0	1	0	0	0	1	0.64375	91
1	0	0	1	0	0	1	0	0.63750	92
1	0	0	1	0	0	1	1	0.63125	93
1	0	0	1	0	1	0	0	0.62500	94
1	0	0	1	0	1	0	1	0.61875	95
1	0	0	1	0	1	1	0	0.61250	96
1	0	0	1	0	1	1	1	0.60625	97
1	0	0	1	1	0	0	0	0.60000	98
1	0	0	1	1	0	0	1	0.59375	99
1	0	0	1	1	0	1	0	0.58750	9A
1	0	0	1	1	0	1	1	0.58125	9B
1	0	0	1	1	1	0	0	0.57500	9C
1	0	0	1	1	1	0	1	0.56875	9D
1	0	0	1	1	1	1	0	0.56250	9E
1	0	0	1	1	1	1	1	0.55625	9F
1	0	1	0	0	0	0	0	0.55000	A0
1	0	1	0	0	0	0	1	0.54375	A1
1	0	1	0	0	0	1	0	0.53750	A2
1	0	1	0	0	0	1	1	0.53125	A3
1	0	1	0	0	1	0	0	0.52500	A4
1	0	1	0	0	1	0	1	0.51875	A5
1	0	1	0	0	1	1	0	0.51250	A6
1	0	1	0	0	1	1	1	0.50625	A7

Table 1. SVI2 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	1	0	1	0	0	0	0.50000	A8
1	0	1	0	1	0	0	1	0.49375	A9
1	0	1	0	1	0	1	0	0.48750	AA
1	0	1	0	1	0	1	1	0.48125	AB
1	0	1	0	1	1	0	0	0.47500	AC
1	0	1	0	1	1	0	1	0.46875	AD
1	0	1	0	1	1	1	0	0.46250	AE
1	0	1	0	1	1	1	1	0.45625	AF
1	0	1	1	0	0	0	0	0.45000	B0
1	0	1	1	0	0	0	1	0.44375	B1
1	0	1	1	0	0	1	0	0.43750	B2
1	0	1	1	0	0	1	1	0.43125	B3
1	0	1	1	0	1	0	0	0.42500	B4
1	0	1	1	0	1	0	1	0.41875	B5
1	0	1	1	0	1	1	0	0.41250	B6
1	0	1	1	0	1	1	1	0.40625	B7
1	0	1	1	1	0	0	0	0.40000	B8
1	0	1	1	1	0	0	1	0.39375	B9
1	0	1	1	1	0	1	0	0.38750	BA
1	0	1	1	1	0	1	1	0.38125	BB
1	0	1	1	1	1	0	0	0.37500	BC
1	0	1	1	1	1	0	1	0.36875	BD
1	0	1	1	1	1	1	0	0.36250	BE
1	0	1	1	1	1	1	1	0.35625	BF
1	1	0	0	0	0	0	0	0.35000	C0
1	1	0	0	0	0	0	1	0.34375	C1
1	1	0	0	0	0	1	0	0.33750	C2
1	1	0	0	0	0	1	1	0.33125	C3
1	1	0	0	0	1	0	0	0.32500	C4
1	1	0	0	0	1	0	1	0.312875	C5
1	1	0	0	0	1	1	0	0.31250	C6
1	1	0	0	0	1	1	1	0.30625	C7
1	1	0	0	1	0	0	0	0.30000	C8
1	1	0	0	1	0	0	1	0.29375	C9
1	1	0	0	1	0	1	0	0.28750	CA
1	1	0	0	1	0	1	1	0.28125	CB
1	1	0	0	1	1	0	0	0.27500	CC
1	1	0	0	1	1	0	1	0.26875	CD
1	1	0	0	1	1	1	0	0.26250	CE
1	1	0	0	1	1	1	1	0.25625	CF
1	1	0	1	0	0	0	0	0.25000	D0
1	1	0	1	0	0	0	1	0.24375	D1

Table 1. SVI2 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	0	1	0	0	1	0	0.23750	D2
1	1	0	1	0	0	1	1	0.23125	D3
1	1	0	1	0	1	0	0	0.22500	D4
1	1	0	1	0	1	0	1	0.21875	D5
1	1	0	1	0	1	1	0	0.21250	D6
1	1	0	1	0	1	1	1	0.20625	D7
1	1	0	1	1	0	0	0	0.20000	D8
1	1	0	1	1	0	0	1	0.19375	D9
1	1	0	1	1	0	1	0	0.18750	DA
1	1	0	1	1	0	1	1	0.18125	DB
1	1	0	1	1	1	0	0	0.17500	DC
1	1	0	1	1	1	0	1	0.16875	DD
1	1	0	1	1	1	1	0	0.16250	DE
1	1	0	1	1	1	1	1	0.15625	DF
1	1	1	0	0	0	0	0	0.15000	E0
1	1	1	0	0	0	0	1	0.14375	E1
1	1	1	0	0	0	1	0	0.13750	E2
1	1	1	0	0	0	1	1	0.13125	E3
1	1	1	0	0	1	0	0	0.12500	E4
1	1	1	0	0	1	0	1	0.11875	E5
1	1	1	0	0	1	1	0	0.11250	E6
1	1	1	0	0	1	1	1	0.10625	E7
1	1	1	0	1	0	0	0	0.10000	E8
1	1	1	0	1	0	0	1	0.09375	E9
1	1	1	0	1	0	1	0	0.08750	EA
1	1	1	0	1	0	1	1	0.08125	EB
1	1	1	0	1	1	0	0	0.07500	EC
1	1	1	0	1	1	0	1	0.06875	ED
1	1	1	0	1	1	1	0	0.06250	EE
1	1	1	0	1	1	1	1	0.05625	EF
1	1	1	1	0	0	0	0	0.05000	F0
1	1	1	1	0	0	0	1	0.04375	F1
1	1	1	1	0	0	1	0	0.03750	F2
1	1	1	1	0	0	1	1	0.03125	F3
1	1	1	1	0	1	0	0	0.02500	F4
1	1	1	1	0	1	0	1	0.01875	F5
1	1	1	1	0	1	1	0	0.01250	F6
1	1	1	1	0	1	1	1	0.00625	F7
1	1	1	1	1	0	0	0	OFF	F8
1	1	1	1	1	0	0	1	OFF	F9
1	1	1	1	1	0	1	0	OFF	FA
1	1	1	1	1	0	1	1	OFF	FB

Table 1. SVI2 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	1	1	1	1	0	0	OFF	FC
1	1	1	1	1	1	0	1	OFF	FD
1	1	1	1	1	1	1	0	OFF	FE
1	1	1	1	1	1	1	1	OFF	FF

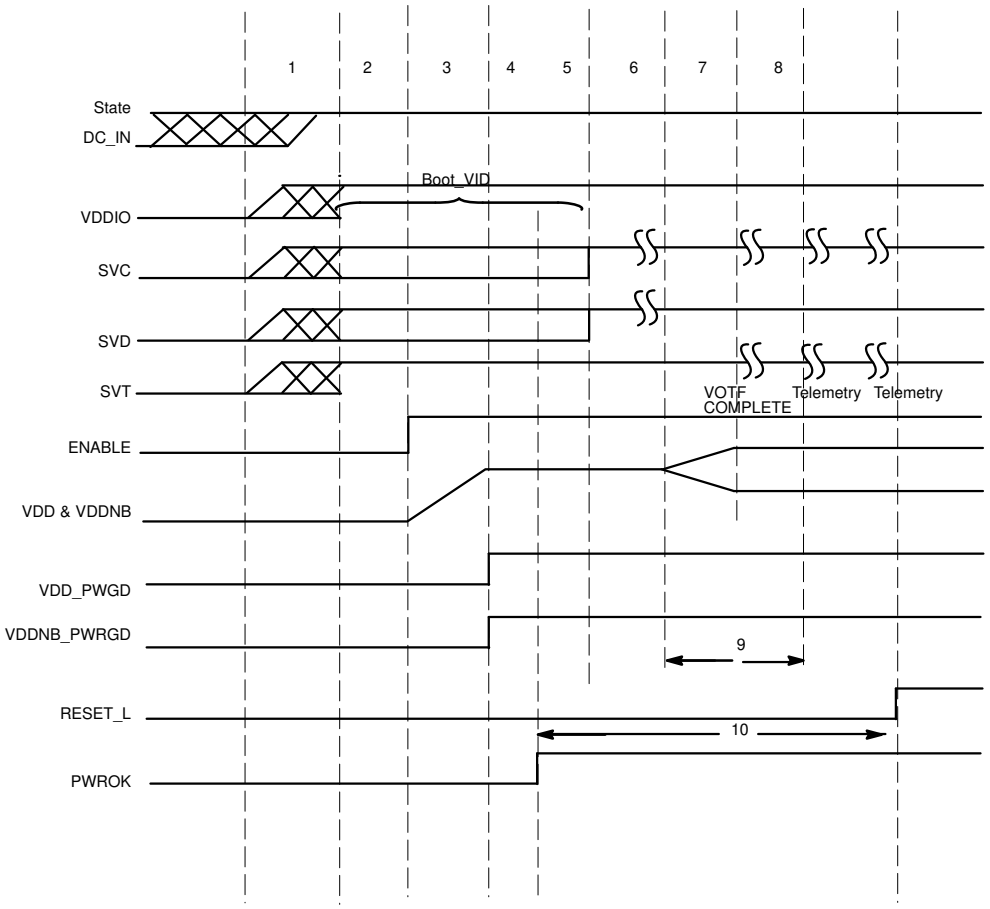


Figure 3. Start Up Timing Diagram

SVI2 INTERFACE

SVD SERIAL PACKET BIT DESCRIPTION

Bit	Default	Description
1:5	11000	Start code
6	1	VDD domain selector bit, if set then the following two data bytes contain the VID for VDD, the PSI state for VDD and the loadline slope trim and offset
7	0	VDDNB domain selector bit, if set then the following two data bytes contain the VID for VDD, the PSI state for VDDNB and the loadline slope trim and offset
8	0	
9	0	ACK
10	0	PSI0 power state indicator level 0. when this signal is asserted the NCP81022 is in a lower power state, and phase shedding is initialized.
11:17	XXXXXXX	VID code [7:1] see table 2
18	0	ACK
19	X	VID code LSB [0] see table 2
20		PSI1, when this bit is asserted the NCP81022 is in a low power state and operated in diode mode emulation mode
21	1	TFN, this is an active high signal that allows the processor to control the telemetry functionality of the NCP81022.
22:24	011	Loadline slope Trim [2:0]
25:26	10	Offset Trim [1:0]
27	0	ACK

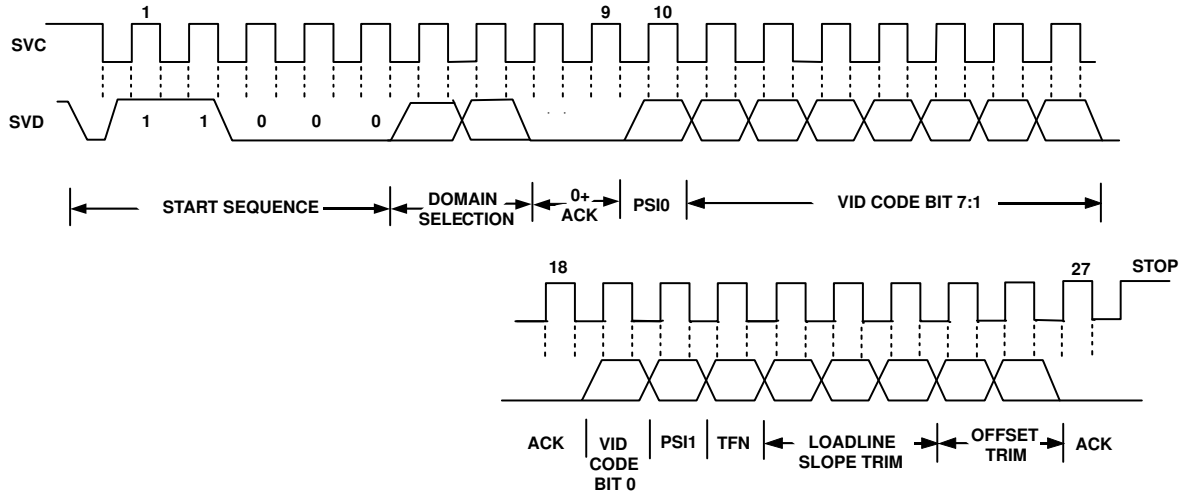


Figure 4. SVD Packet Structure

SVI2 Interface

The NCP81022 is design to accept commands over AMD's SVI2 bus. The communication is accomplished using three lines, a data line SVD, a clock line SVC and a telemetry line SVT. The SVD line can be used not only to set the voltage level of the Main rail and North bridge rail, but can also set the load line slope, programmed offset and also the PSI (power state indicator bits). The SVT line from the NCP81022 communicates voltage, current and status updates back to the processor.

Power State Indicator (PSI)

The SVI2 protocol defines two PSI levels, PSI0 and PSI1. These are active low signals which indicate when the NCP81022 can enter low power states to improve system efficiency and performance. Increasing levels of PSI state indicates low current consumption of the processor.

It is possible for the processor to assert PSI0 and PSI1 out of order i.e. to enter PSI1 prior to PSI0 however; PSI0 always takes priority over PSI1.

With increasing load current demand the number of active phases increase instantaneous. The NCP81022 can potentially change from single−phase to user−configured multiphase operation in a single step, depending on PSI state.

PSI0 is activated once the system power is in the region of 20−30 A, in this mode the NCP81022 controller reduces the number of phases in operation thus reducing switching losses of the system. If the current continues to drop to 1−3 A PSI1 is asserted and the NCP81022 enters diode emulation mode, operating in single phase mode. See below table for PSI mode operation.

PSI0#	PSI1#	Phase
0	0	1−Phase DCM
0	1	1−Phase CCM
1	0	Full phase mode
1	1	Full phase mode

Telemetry

The TFN bit along with the VDD and VDDNB domain selectors are used to change the functionality of the telemetry. See table below for description.

TFN = 1		Description
VDD	VDDNB	
0	1	Telemetry is in voltage and current mode. V&I is sent back for both VDD and VDDNB rails
0	0	Telemetry is in voltage only mode. Voltage information is sent back for both VDD and VDDNB rails
1	0	Telemetry is disabled
1	1	Reserved for future use

Loadline Slope

Within the SVI2 protocol the NCP81022 controller has the ability to manipulate the loadline slope of both the VDD and VDDNB rails independently of each other, when Enable and PWROK are asserted. Loadline slope trim information is transmitted in 3 bits , 22:24, over the SVD packet. Please see table below for description.

Loadline Slope Trim [0:2]	Description
000	Remove all LL droop from output
001	LL slope 12.9%
010	LL slope 25.8%
011	LL slope (Default 38.7%)
100	LL slope 51.6%
101	LL slope 64.8%
110	LL slope 77.4%
111	LL slope 90.2%

Offset Trim

Within the SVI2 protocol the NCP81022 controller has the ability to manipulate the offset of both the VDD and VDDNB rails independently of each other, when Enable and PWROK are asserted. Descriptions of offset codes are described below.

Offset Trim [1:0]	Description
00	0 offset
01	Initial offset −25 mV
10	Use initial offset (default)
11	Initial offset +25 mV

SVT Serial Packet

The NCP81022 has the ability to sample and report voltage and current for both the VDD and VDDNB domain. This information is reported serially over the SVT line which is clocked using the processor driven SVC line. When the PWROK is deasserted, the NCP81022 is not collecting or reporting telemetry information. When PWROK is asserted, the telemetry information reported back is as described below. If the NCP81022 is configured in voltage only telemetry then the sampled voltage for VDD and the sampled voltage for the VDDNB are sent together in every SVT telemetry packet.

Parameter	Value	Unit
Number of voltage Bits	9	Bits
Maximum reporting Voltage	3.15	V
Minimum reported Voltage	0.00	V
Voltage resolution	6.25	mV
Voltage accuracy from 1.2 V to 800 mV	±1	LSB
Voltage accuracy for voltages greater than 1.2 V and less than 800 mV	±2	LSB
Recommended voltage moving average window size	50	μs
Minimum voltage only telemetry reporting rate	20	kHz
Number of bits in current data	8	Bits
Max reported current (FFh = OCP)	100	% of IDD spike _ocp
Max reported current (00h)	0	% of IDD spike _ocp

If the NCP81022 is configured in voltage and current mode then the samples voltage and current information for VDD is sent out in one SVT telemetry packet while the voltage and current information for the VDDNB domain is sent out in the next SVT telemetry packet. The telemetry report rate while the NCP81022 is in current and voltage mode, is double that which is observed in voltage only mode. The reported voltage and current are moving average representations.

Bit	Description		Bit	
0	SVT0	See table below for description	10	Voltage Bit 0
1	SVT1		11	Voltage Bit 8 ‘0’ in V and I mode
2	Voltage Bit 8		12	Voltage or current Bit 7
3	Voltage Bit 7		13	Voltage or current Bit 6
4	Voltage Bit 6		14	Voltage or current Bit 5
5	Voltage Bit 5		15	Voltage or current Bit 4
6	Voltage Bit 4		16	Voltage or current Bit 3
7	Voltage Bit 3		17	Voltage or current Bit 2
8	Voltage Bit 2		18	Voltage or current Bit 1
9	Voltage Bit 1		19	Voltage or current Bit 0

SVT0, SVT1	Description
0,0	Telemetry packet belongs to the VDD domain and in V&I mode.
0,1	Telemetry packet belongs to the VDDNB domain and in V&I mode.
1,0	VOTF Complete, a stop immediately follows these two bits during the next SVC high period. Telemetry data does not follow this bit configuration
1,1	Telemetry package in voltage representation only. (default)

SVI2 VR to Processor Data Communication

As described previously the NCP81022 has the ability to send digitally encoded voltage and current values for the VDD and VDDNB domains to the processor, it also has the capability to send VID On The Fly (VOTF) complete mechanism. The processor uses this information as an indicator for when the VDD, VDDNB are independently, or collectively, at the requested stepped−up VID voltage. The VOTF complete mechanism is not used for VID changes to lower or for repeated VID codes.

VOTF Complete is transmitted as an SVT packet. Since a VOTF request could apply to one or two voltage domains, rules are suggested below to handle these cases.

VID Change	Offset Change	Loadline Change	VOFT Timing	Force or Decay Change
UP	Unchanged	Unchanged	After slewing	Force voltage change
Down	Unchanged	Unchanged	NO VOTF	Voltage Decay
X	UP	Unchanged	After slewing	Force voltage change
X	Down	Unchanged	After slewing	Force voltage change
X	Unchanged	Up	After slewing	Force voltage change
X	Unchanged	Down	After slewing	Force voltage change

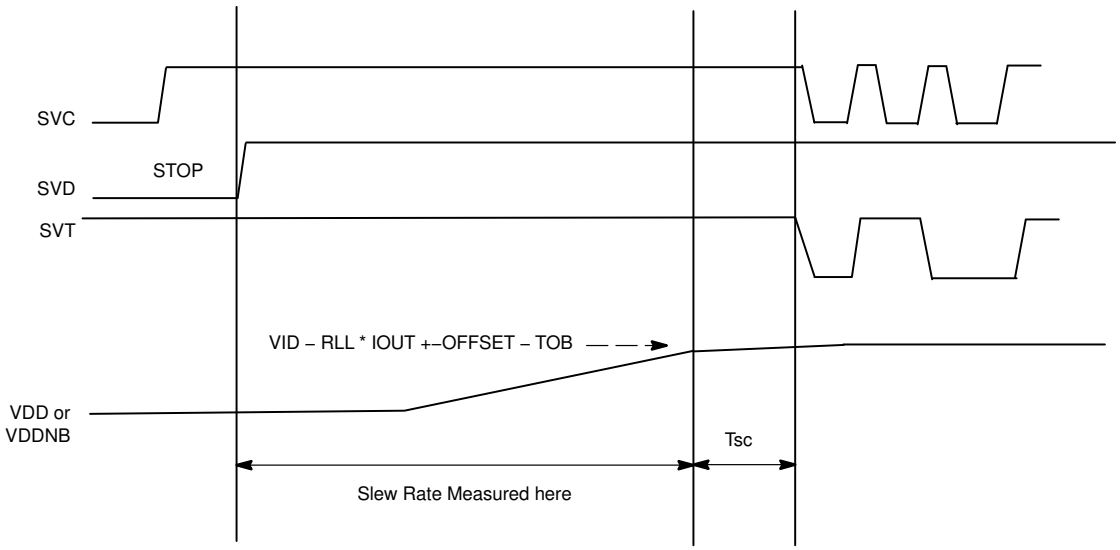


Figure 5. Slew Rate Timing

*Max Tsc =5 μs

- Telemetry takes priority over VOTF Complete signals
- VOTF complete can be sent if the net voltage change is 0 or negative
- VOTF Complete is only used to indicate that a rail(s) has finish slewing to a higher voltage.
- If a VOTF request for a higher voltage is sent for both VDD and VDDNB rails, but only domain will go up in voltage then the returned VOTF Complete will indicate that the increasing domain has finished slewing
- If the processor starts a VOTF request but the VOTF is incomplete then the NCP81022 will not sent the VOTF Complete sequence until after the new VOTF request.

- If the processor is sending a SVD packet when the NCP81022 is sending telemetry packet to send, then the NCP81022 waits to send the telemetry until after the SVD packet has stopped transmitting.
- If the processor stops sending the SVD packet while the NCP81022 is sending telemetry then no action has to be taken, the NCP81022 shifts in the new SVD packet and finishes sending the telemetry while the processor is sending the SVD packet.
- SVT packets are not sent while PWROK is deasserted
- The NCP81022 will not collect or send telemetry data when telemetry functionality is disabled by the TFN bits

The following timing diagrams cover the SVC, SVD and SVT timing when PWROK is asserted and data is being transmitted, the table that follows defines the min and max value for each timing specification.

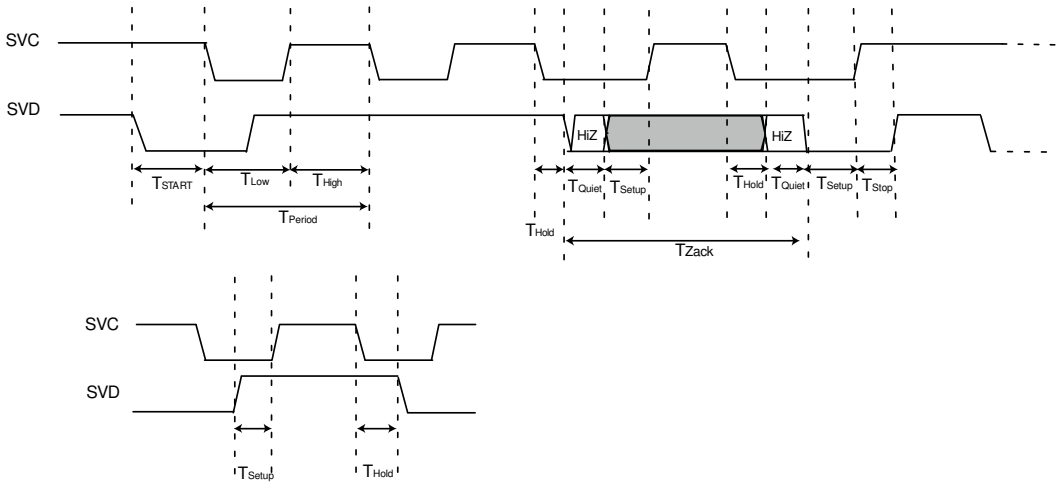


Figure 6. SDV SVC Timing

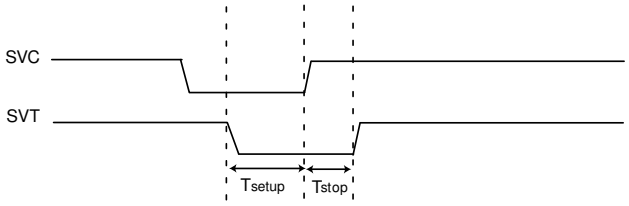


Figure 7. SVT Stop Timing

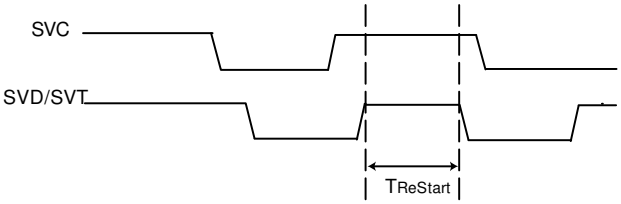


Figure 8. SVD or SVT Re−Start Timing

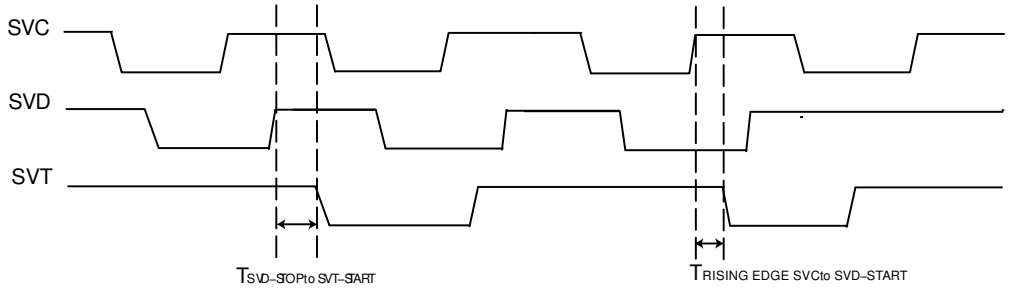


Figure 9. SVT start and Stop timing

Table 2. SVI2 BUS TIMING PARAMETERS FOR 3.33 MHz OR 20 MHz OPERATION

Parameter	Min	Max	Unit
T_{PERIOD}	50	TDC	ns
SVC Frequency	TDC	20	MHz
T_{HIGH} SVC High Time	20		ns
T_{Low} SVC Low Time	30		ns
T_{setup} (SVD, SVT Setup time to SVC rise edge)	5	10	ns
T_{Hold} (SVD, SVT Hold time from SVC falling edge)	5	10	ns
T_{Quiet} (Time neither processor nor VR is driving the SVD line)	10		ns
T_{ZACK} (total time processor tristates SVD)	50		ns
T_{START}	20		ns
T_{STOP}	10		ns
$T_{ReSTART}$ (Time Between Stop and Start on SVD)	50		ns
$T_{ReSTART}$ (Time Between Stop and Start on SVD)	50		ns
$T_{SVD-STOP\ to\ SVT-START}$ (Time Between SVD stop and SVT Start)	80		ns
$T_{Rising\ Edge\ SVC\ to\ SVTD-Start}$ (Time between Rising Edge of SVC after last SVT bit to SVD start)	20		ns
SVC, SVD, SVT Fall Time VOH_DC to VOL_DC		1	ns
SVC, SVD, SVT Rise Time VOH_DC to VOL_DC		1	ns
$T_{Skew-SVC-SVD}$ The skew between SVC, SVD as seen at the NCP81022; dictated by layout and tested by simulation		1	ns
$T_{Skew-SVC-SVD}$ The skew between SVC, SVD as seen at the Processor; dictated by layout and tested by measurement		2	ns
$T_{Propagation}$ The propagation delay of SVC, SVD, SVT; measured from the transmitter to the receiver		2	ns
SVC glitches filter width. NCP81022's glitch filter will reject any SVC transition that persists for shorter periods than this	3	5	ns

Slew Rate

Slew rate is programmable on power up; a resistor from the SR pin to ground sets the slew rate. Each rail can be programmed independently between 10 mV/μs, see table below for resistor values.

Slew Rate	Resistance (Ω)
10 mv/μs	10k
20 mv/μs	25k
30 mv/μs	45k

BOOT VOLTAGE PROGRAMMING

The NCP81022 has a VBOOT voltage register that can be externally programmed for both Main Rail and North Bridge boot−up output voltage. The VBOOT voltage can be programmed when PWROK is deasserted, through the logic levels present on SVC and SVD. The table below defines the Boot−VID codes

BOOT VOLTAGE TABLE:

SVC	SVD	Boot Voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

ADDRESSING PROGRAMMING

The NCP81102 supports eight possible SMBus Addresses. Pin 28 (PWM4) is used to set the SMBus Address. On power up a 10 μA current is sourced from this pin through a resistor connected to this pin and the resulting voltage is measured. The Table below provides the resistor values for each corresponding SMBus Address. The address value is latched at startup.

Table 3. SMBus ADDRESS

Resistor Value	SMBus (Hex)
10k	20
25k	21
45k	22
70k	23
95k	24
125k	25
165k	26
220k	27

Programming the ICC_Max

A resistor to ground on the IMAX pin program the ICC_Max value at the time the NCP81022 in enabled. 10 μA is sourced from this pin to generate a voltage on the program resistor. The resistor value should be no less than 10k.

$$R_{ICC\_MAX} = \frac{(2 * ICC\_MAX)}{(10\mu * 256)}$$

Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to:

$$V_{DIFF} = \left(V_{VSP} - V_{VSN}\right) + \left(1.3\ V - V_{DAC}\right) + \left(V_{DROOP} - V_{CSREF}\right)$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non−inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

High Performance Voltage Error Amplifier

A high performance error amplifier is provided for high bandwidth transient performance. A standard type 3 compensation circuit is normally used to compensate the system.

Differential Current Feedback Amplifiers

Each phase has a low offset differential amplifier to sense that phase current for current balance and per phase OCP protection during soft−start. The inputs to the CSREF and CSPx pins are high impedance inputs. It is recommended that any external filter resistor RCSN not exceed 10 kΩ to avoid offset issues with leakage current. It is also recommended that the voltage sense

element be no less than 0.5 mΩ for accurate current balance, user care should be taken in board design if lower DCR inductor are used as this may affect the current balance in light load conditions. Fine tuning of this time constant is generally not required.

$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} * DCR}$$

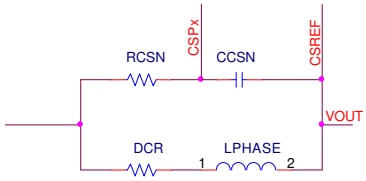


Figure 10. Differential Current Feedback

The individual phase current is summed into to the PWM comparator feedback in this way current is balanced is via a current mode control approach.

Total Current Sense Amplifier

The NCP81022 uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref (n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.

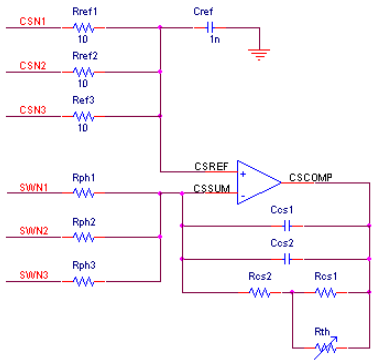


Figure 11. Current Sense Amplifier

The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = -\frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{Total} * DCR\right)$$

Set the gain by adjusting the value of the Rph resistors. The DC gain should set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100mV then it is recommended to increase the gain of the CSCOMP amp and add a resister divider to the Droop pin filter. This is required to provide a good current signal to offset voltage ratio for the ILIM pin. When no droop is needed, the gain of the amplifier should be set to provide ~100 mV across the current limit programming resistor at full load. The values of Rcs1 and Rcs2 are set based on the 220k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. Ccs1 and Ccs2 are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_Z = \frac{DCR@25°C}{2 * PI * L_{Phase}}$$

$$F_P = \frac{1}{2 * PI * \left(Rcs2 + \frac{Rcs1*Rth@25°C}{Rcs1+Rth@25°C}\right) * (Ccs1 + Ccs2)}$$

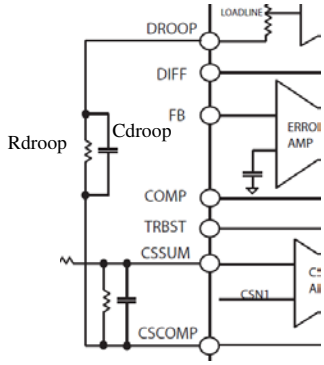
Programming the Current Limit

The current−limit thresholds are programmed with a resistor between the ILIM and CSCOMP pins. The ILIM pin mirrors the voltage at the CSREF pin and the current limit comparators. Set the value of the current limit through CSREF− CSCOMP voltage at $Iout_{LIMIT}$ condition as shown below:

$$R_{ILIM} = \frac{\frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{LIMIT} * DCR\right)}{10\ \mu A} \text{ or } R_{ILIM} = \frac{V_{CSREF-CSCOMP@ILIMIT}}{10\ \mu A}$$

Programming DROOP and DAC feedforward

Programming Rdroop sets the gain of the DAC feed−forward and Cdroop provides the time constant to cancel the time constant of the system per the equations below. Cout_total is the total output capacitance of the system design.



Rdroop = (Cout_total)*loadline*453.6*10^6
Cdroop = (loadline*(Cout_total))/Rdroop

Figure 12. Droop RC

Programming IOUT

The IOUT pin sources a current equal to the ILIM sink current gained by the IOUT Current Gain. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.0\ V * R_{LIMIT}}{10 * \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{ICC\_MAX} * DCR\right)}$$

Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator can also be programmed over the SMBus interface through register 0xF7. The oscillator frequency range is between 200 kHz/phase to 1 MHz/phase in 32 steps. The ROSC pin provides approximately 2 V out and the source current is mirrored into the internal ramp oscillator.