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NCP81105, NCP81105H

DrMOS Supporting, 1/2/3 Phase Power Controller with SVID Interface for Desktop and Notebook VR12.5 & VR12.6 CPU Applications

The NCP81105 is a DrMOS supporting controller optimized for Intel® VR12.5 & VR12.6 compatible CPUs. The controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed−forward, and adaptive voltage positioning to provide accurately regulated power for both Desktop and Notebook CPU applications. The control system is based on Dual−Edge pulse−width modulation (PWM), to provide the fastest initial response to dynamic load events plus reduced system cost. The NCP81105 is compatible with DrMOS type power stages such as NCP5367, NCP5368, NCP5369 and NCP5338.

The NCP81105's output can be configured to operate in single phase during light load operation − improving overall system efficiency. A high performance operational error amplifier is provided to simplify compensation of the system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed−loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate current monitoring for droop and digital current monitoring.

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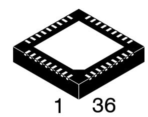
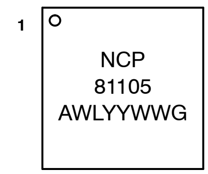
MARKING DIAGRAM



QFN36
CASE 485CC



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 35 of this data sheet.

Features

- Meets Intel's VR12.5 Specifications
- Implements VR12.6 PS4 State and SVID Reporting
- Mixed Voltage/Current Mode, Dual Edge Modulation for Fastest Initial Response to Transient Loading
- High Impedance Differential Voltage Amplifier
- High Performance Operational Error Amplifier
- High Impedance Total Current Sense Amplifier
- True Differential Current Sense Amplifiers for Balancing Current in Each Phase
- Digital Soft Start Ramp
- Dynamic Reference Injection
- Accurate Total Summing Current Amplifier
- "Lossless" Inductor DCR Current Sensing
- Summed, Thermally Compensated Inductor Current Sensing for Adaptive Voltage Positioning (AVP)
- 48 mV/μs Fast Output Slew Rate (NCP81105)
- 10 mV/μs Fast Output Slew Rate (NCP81105H)
- Programmable Slow Slew Rates as a Fraction of Fast Slew Rate
- Reduced Enable to First SVID Command Latency
- Phase−to−Phase Dynamic Current Balancing
- Switching Frequency Range of 280 kHz to 1.5 MHz
- Starts up into Pre−Charged Loads while Avoiding False OVP
- Compatible with DrMOS Power Stages
- Power−saving Phase Shedding
- Vin Feed−forward Ramp Slope Compensation
- Pin Programming for Internal SVID parameters
- Output Over Voltage Protection (OVP) & Under Voltage Protection (UVP)
- Over Current Protection (OCP)
- Power Good Output with Internal Delays
- This is a Pb−Free Device

Applications

- Desktop and Notebook Microprocessors

October, 2013 − Rev. 2
Publication Order Number:
NCP81105/D

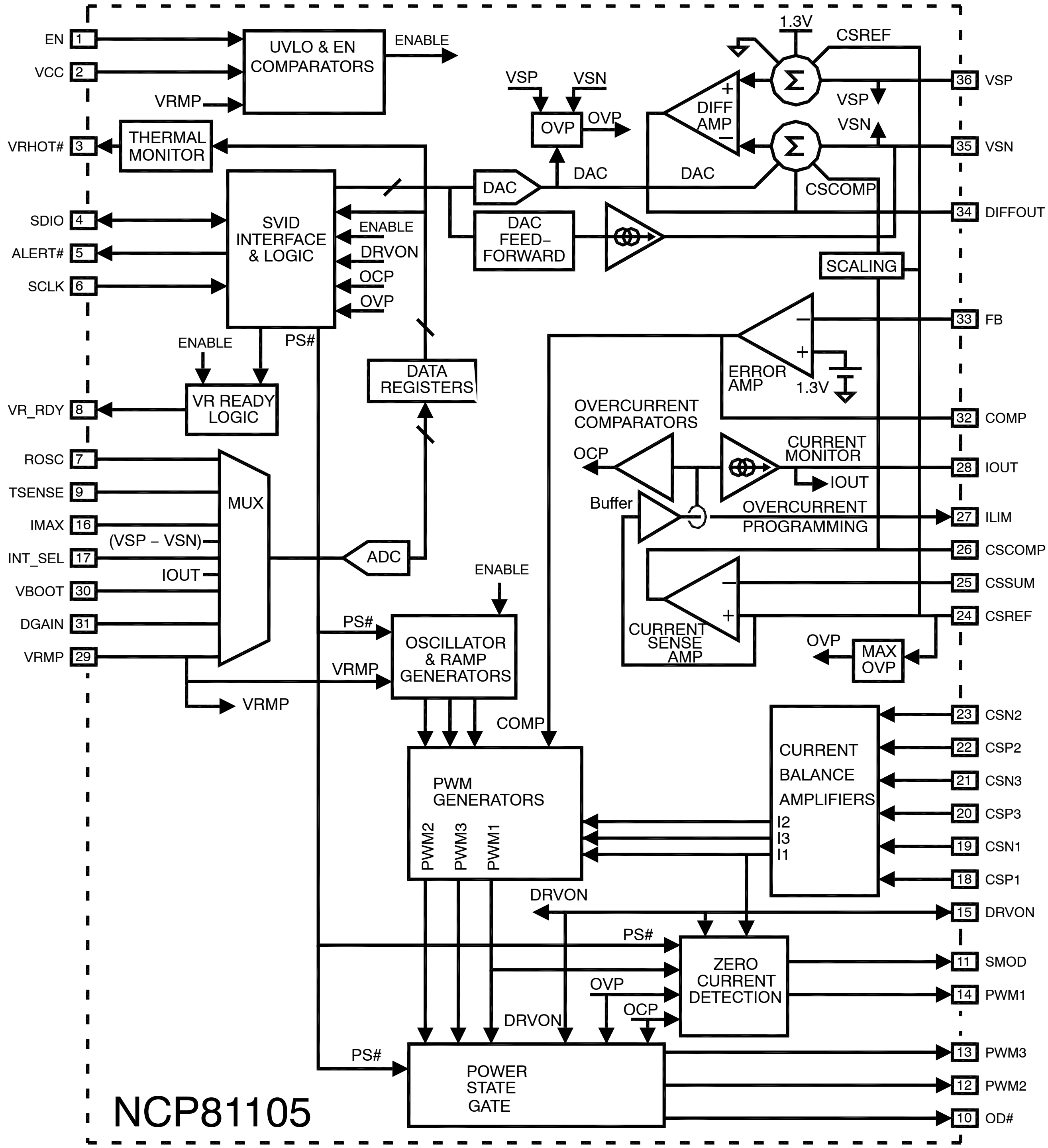


Figure 1. Block Diagram

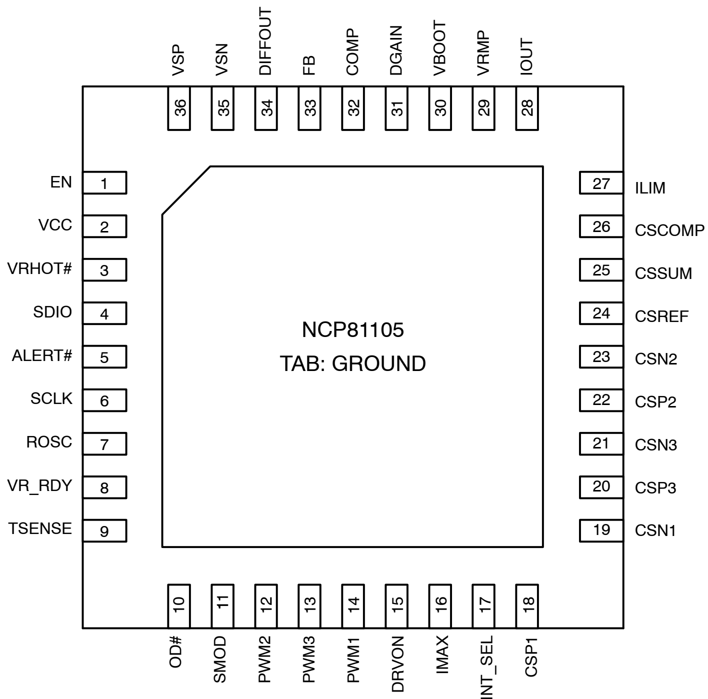


Figure 2. Pin Connections
(Top View)

PIN LIST AND DESCRIPTION

Pin No.	Symbol	Description
1	EN	Logic input. Logic high enables the NCP81105 and logic low disables it.
2	VCC	Power for the internal control circuits. A decoupling capacitor must be connected from this pin to ground.
3	VR_HOT#	Open drain (logic level) output for over−temperature reporting. Low indicates high temp.
4	SDIO	Bidirectional Serial VID data interface.
5	ALERT#	Open drain Serial VID ALERT# output.
6	SCLK	Serial VID clock input.
7	ROSC	This pin outputs a constant current. A resistance from this pin to ground programs the switching frequency.
8	VR_RDY	Open drain output. High indicates that the NCP81105 is regulating the output.
9	TSENSE	Temperature sense input.
10	OD#	Phase Disabling Output, tied to the Enable, SMOD or ZCD_EN# pin of phases 2 and 3 DrMOS. Except in PS0 mode, this output pulls low to disable the DrMOS if connected to an enable input. If connected to a DrMOS SMOD or ZCD_EN# input, both HS & LS FETs are held off since PWM2 & PWM3 are also low. Actively pulls high in PS0 mode.
11	SMOD	Phase 1 Zero Cross Detection (ZCD) disable output. In PS2 & PS3, SMOD pulls LOW when phase 1 inductor current is negative to perform (or allow the DrMOS ZCD function to perform) diode emulation, and pulls HIGH when phase 1 inductor current is positive. In PS0 & PS1, SMOD stays high to force the phase 1 DrMOS into Continuous Conduction.
12	PWM2	PWM output to Phase 2 DrMOS
13	PWM3	PWM output to Phase 3 DrMOS
14	PWM1	PWM output to Phase 1 DrMOS
15	DRVON	Enable output for DrMOS
16	IMAX	During startup, a resistor from this pin to ground programs ICC_MAX.
17	INT_SEL	During startup, a resistor from this pin to ground programs the low frequency compensator pole of the NCP81105 voltage control feedback loop.
18	CSP1	Positive input to phase 1 current sense amplifier for balancing phase currents
19	CSN1	Negative input to phase 1 current sense amplifier
20	CSP3	Positive input to phase 3 current sense amplifier for balancing phase currents
21	CSN3	Negative input to phase 3 current sense amplifier
22	CSP2	Positive input to phase 2 current sense amplifier for balancing phase currents
23	CSN2	Negative input to phase 2 current balance sense amplifier
24	CSREF	Non−inverting input for the total output current sense amplifier. Also, the absolute OVP input.
25	CSSUM	Inverting input of total output current sense amplifier.
26	CSCOMP	Output of total output current sense amplifier.
27	ILIM	Input to program the over−current shutdown threshold.
28	IOUT	Total current monitor output. A resistor from this pin to ground calibrates SVID output current reporting.
29	VRMP	VDC applied to this pin provides feed−forward compensation for the pulsewidth modulator. The current into this pin controls the slope of PWM ramp. A low voltage on this pin will inhibit NCP81105 startup.
30	VBOOT	During startup, a resistor from this pin to ground programs the BOOT voltage
31	DGAIN	During startup, a resistor from this pin to ground programs the scaling of the output Droop with respect to the total output current signal produced between CSCOMP and CSREF.
32	COMP	Output of the error amplifier.
33	FB	Error amplifier voltage feedback input.
34	DIFFOUT	Output of the differential remote sense amplifier.
35	VSN	Inverting input to the differential remote sense amplifier (VSS sense).
36	VSP	Non−inverting input to the differential remote sense amplifier (VCC sense).
37	GND	Power supply return (QFN Flag)

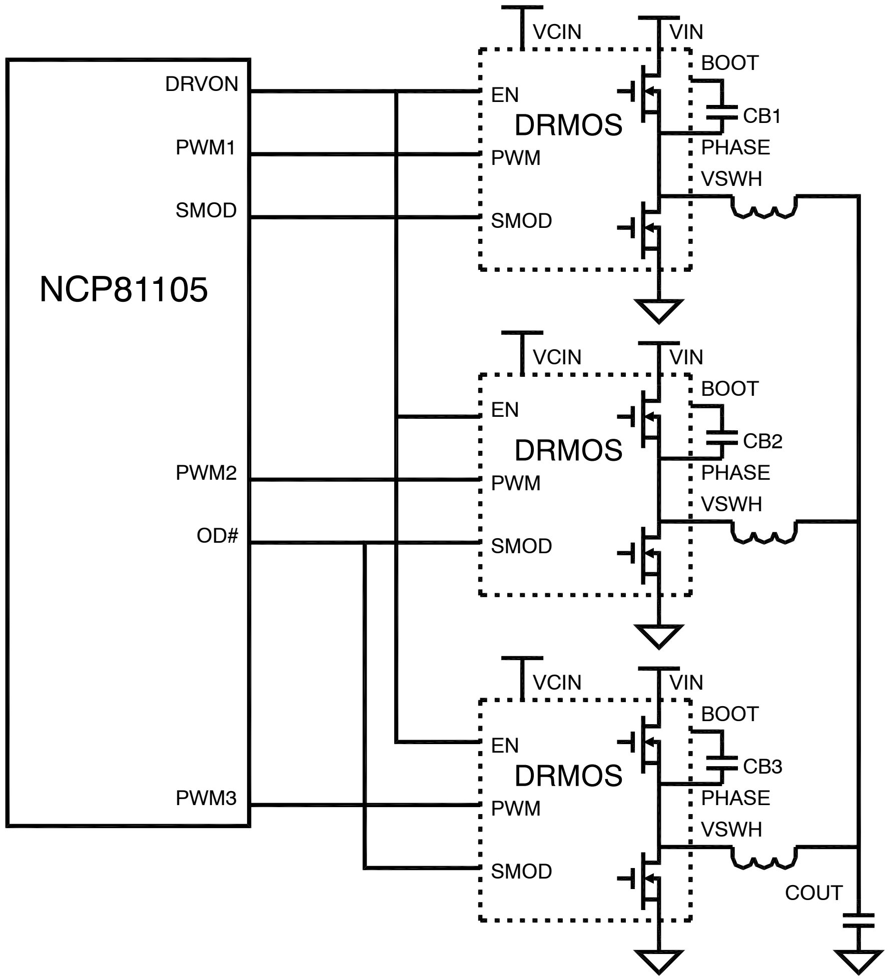


Figure 3. Three Phase Application Diagram

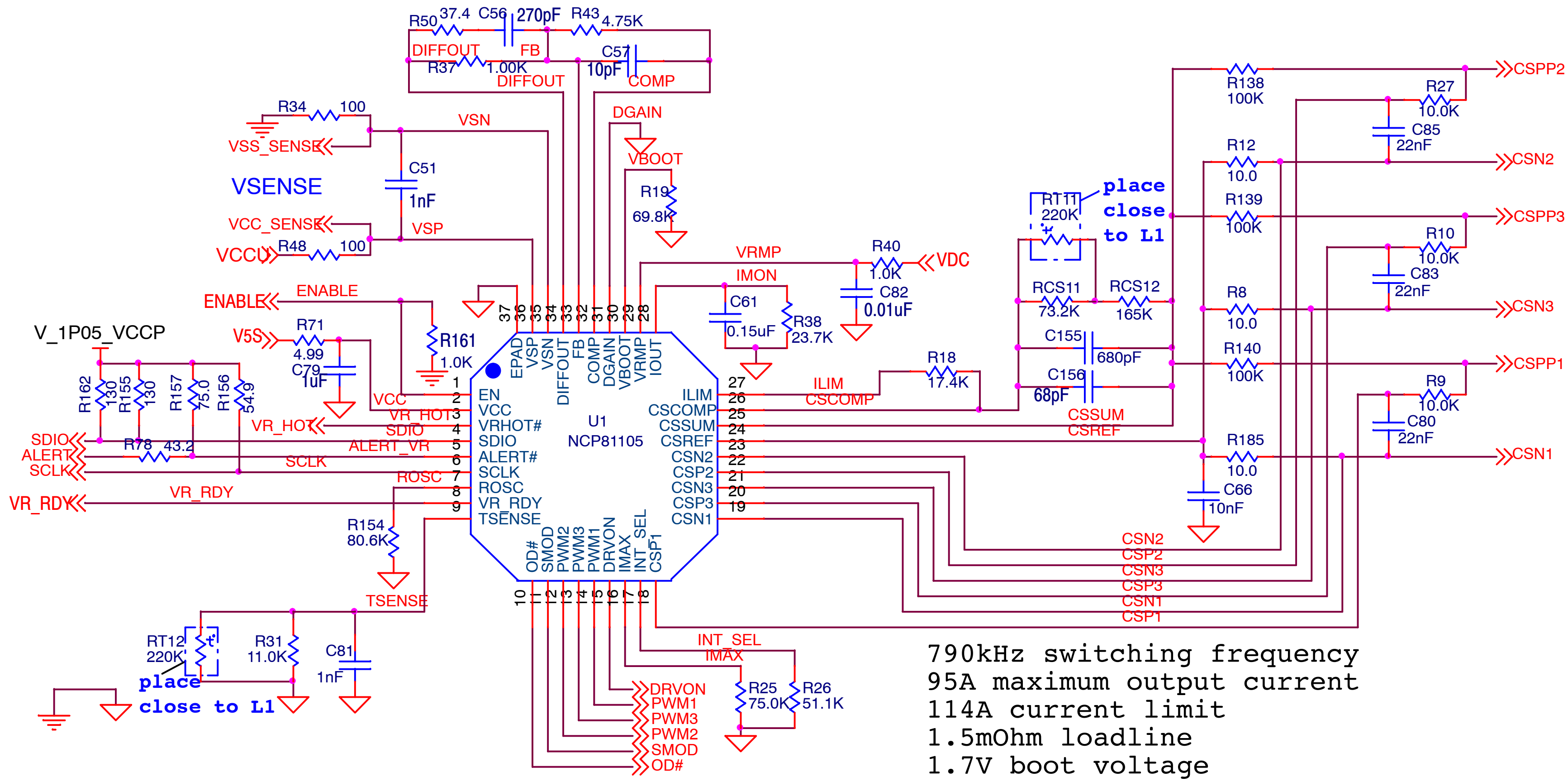


Figure 4. Three Phase Control Circuit Application

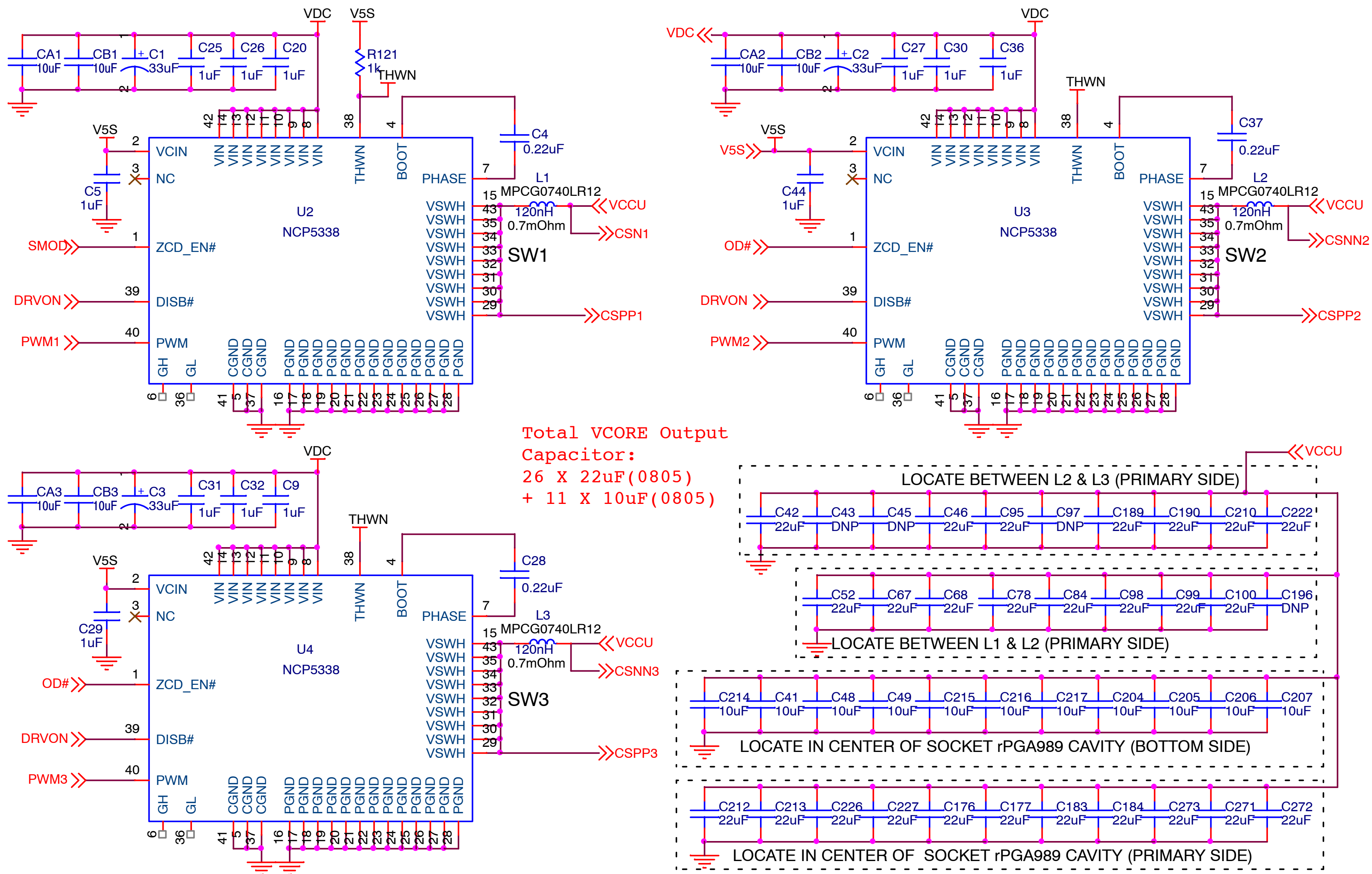


Figure 5. Three Phase Power Stage Circuit

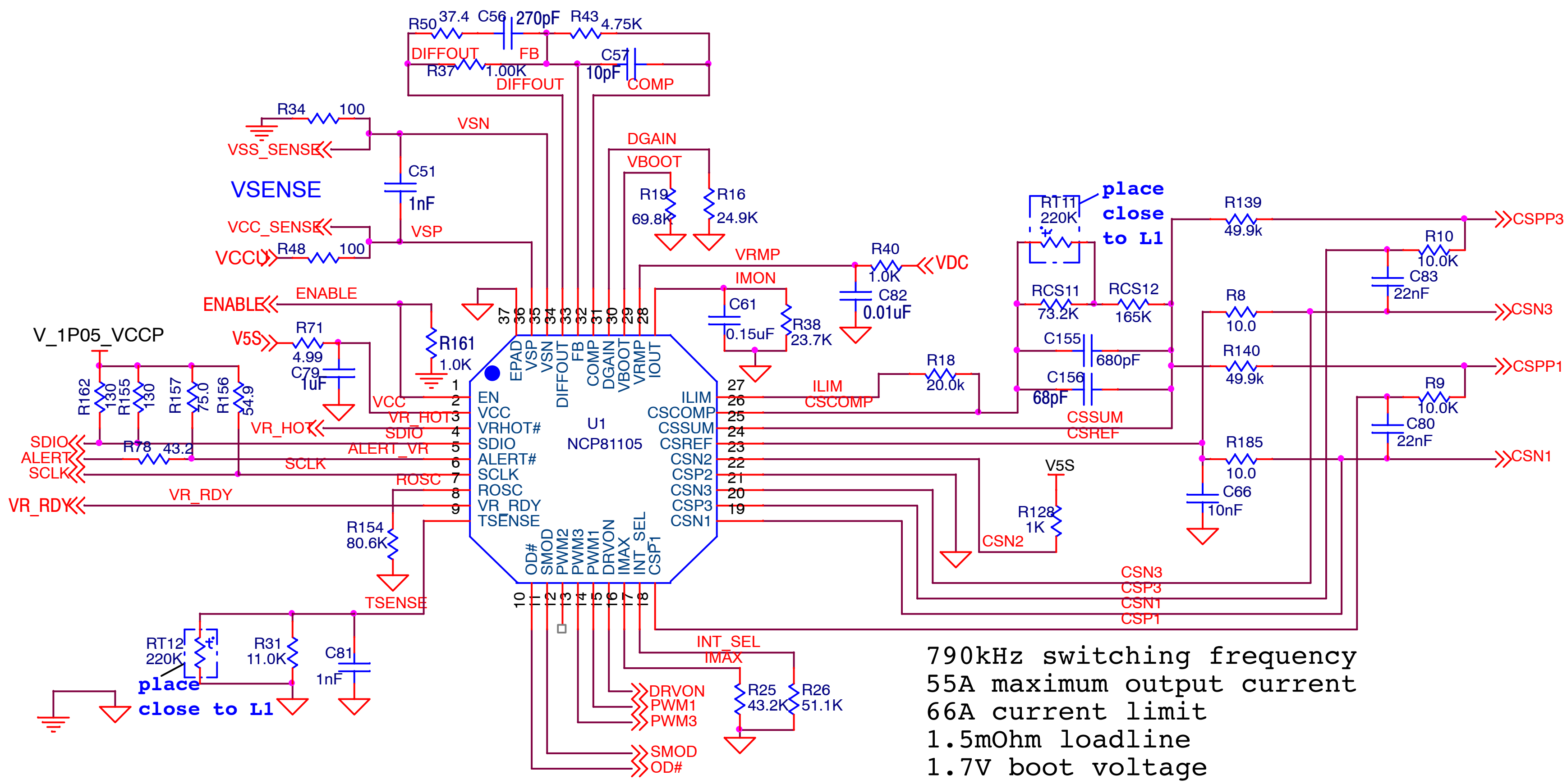


Figure 6. Two Phase Control Circuit Application

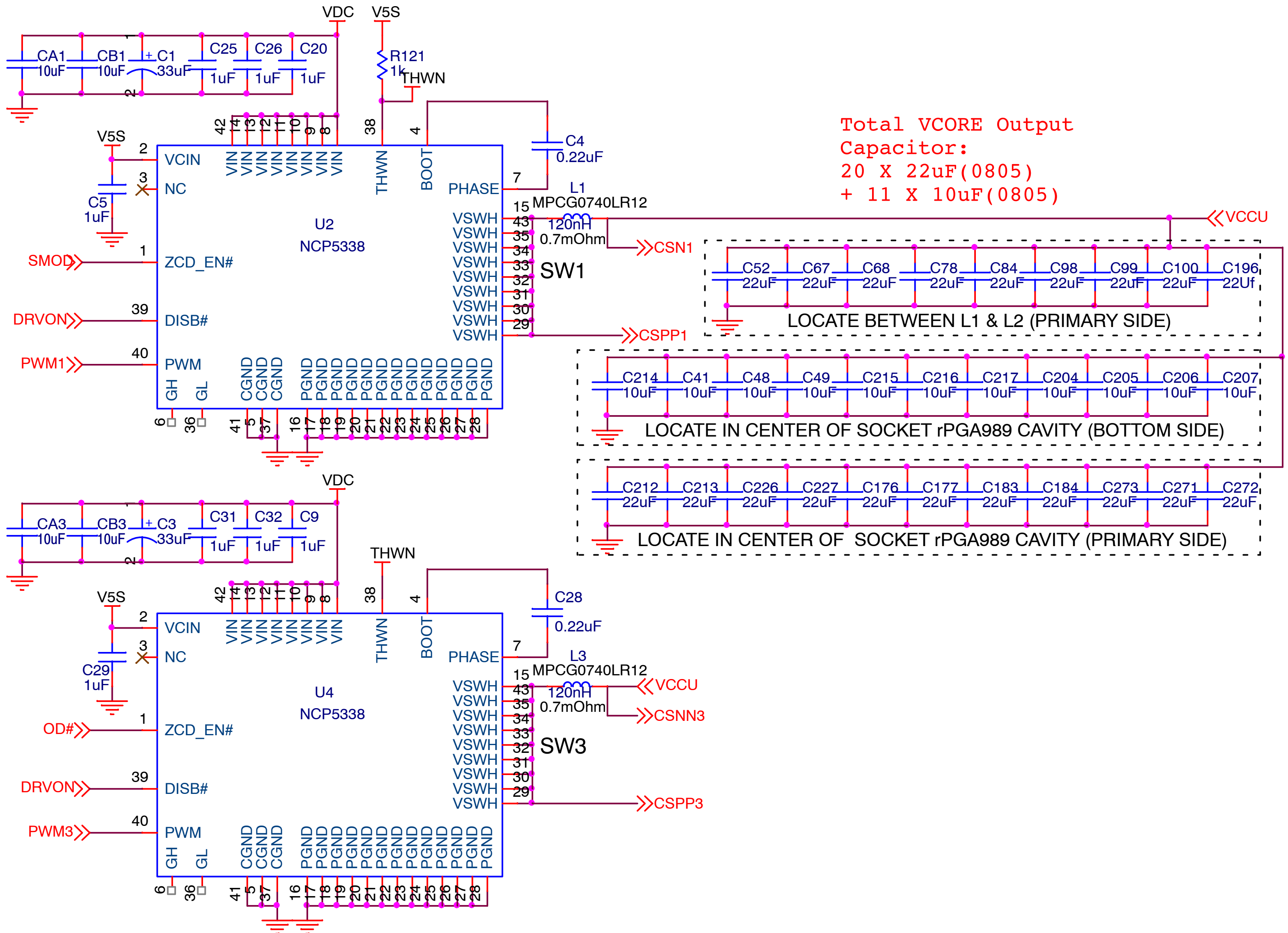


Figure 7. Two Phase Power Stage Circuit

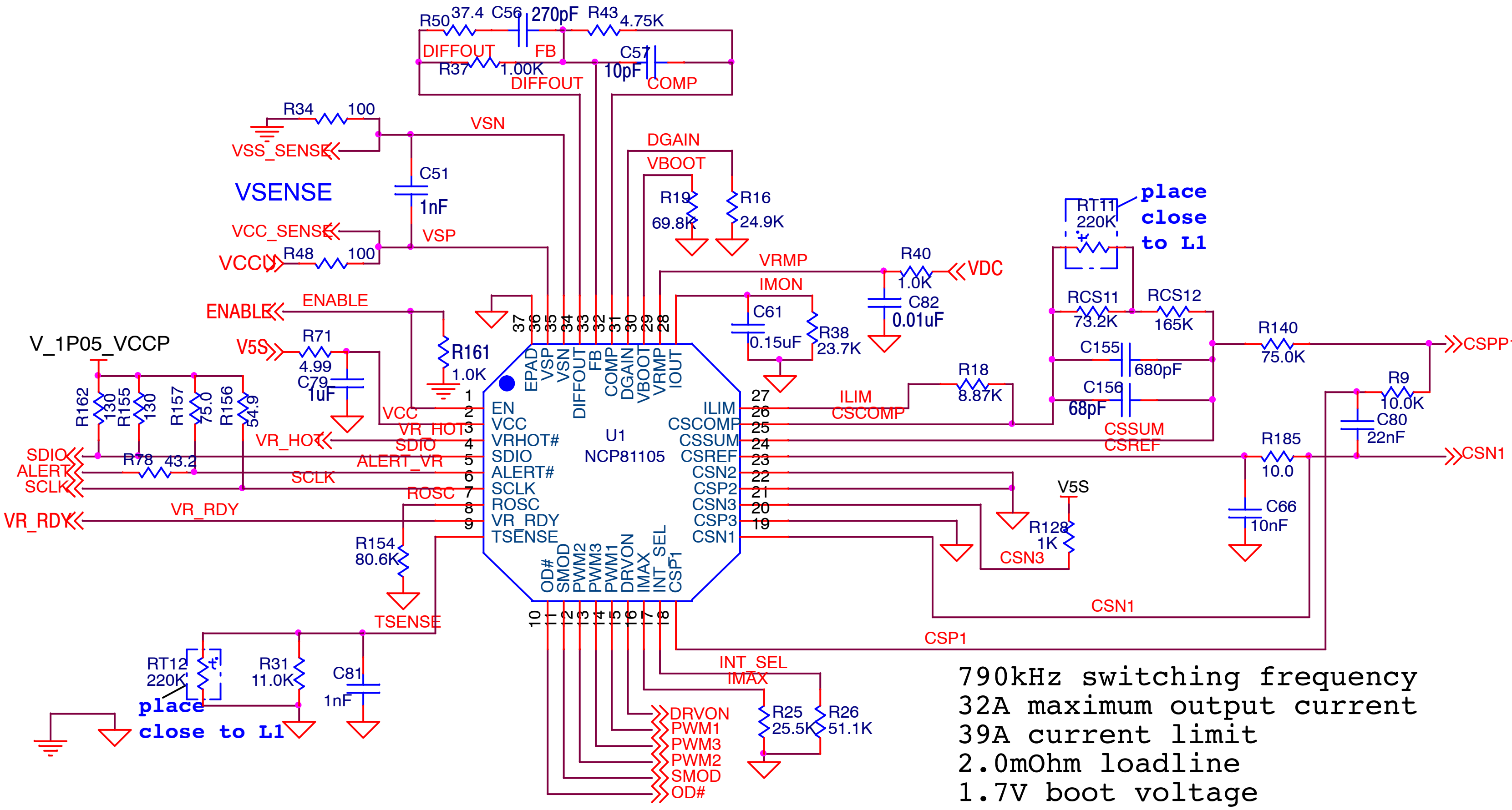


Figure 8. Single Phase Control Circuit Application

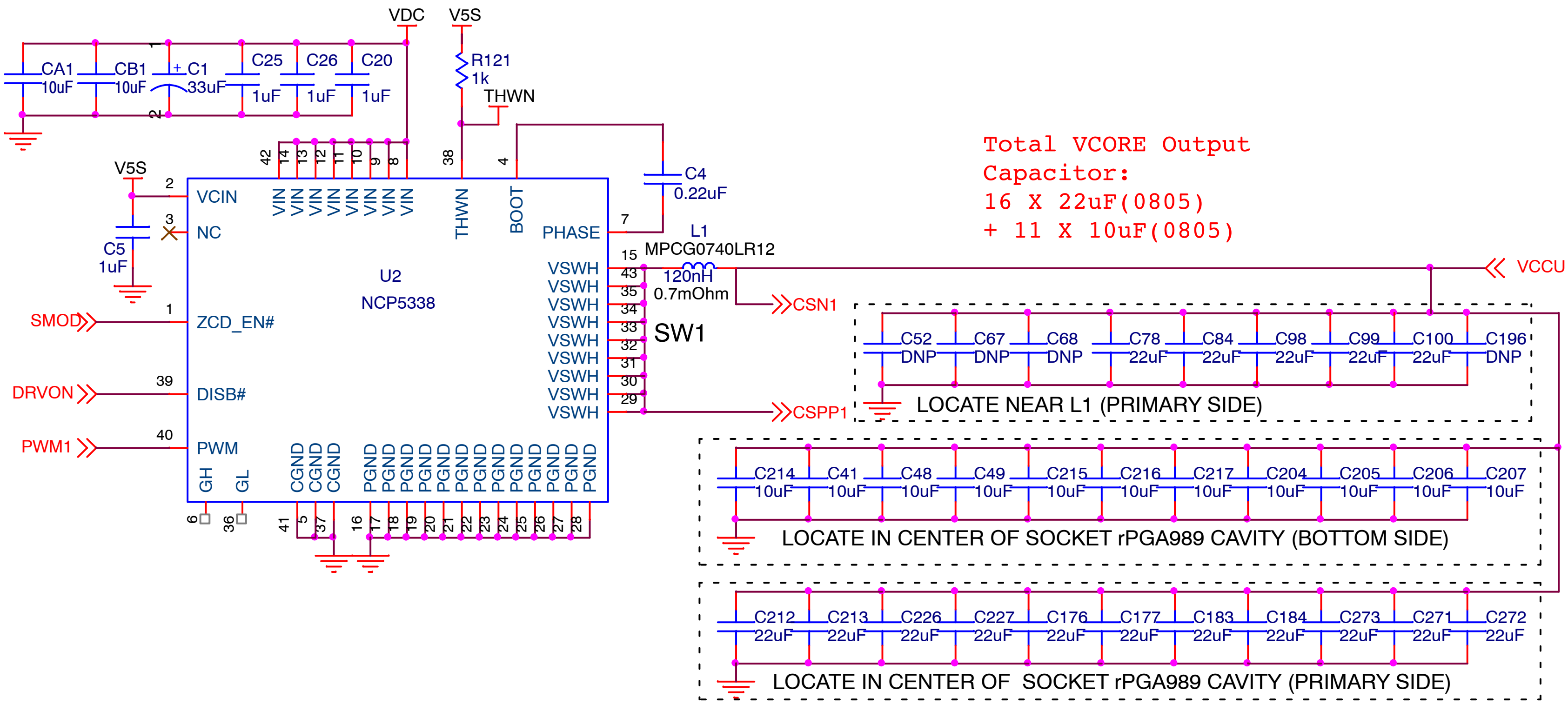


Figure 9. Single Phase Power Stage Circuit

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL INFORMATION − all signals referenced to GND unless noted otherwise.

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP, CSCOMP, DIFFOUT	VCC + 0.3 V	−0.3 V	3 mA	3 mA
VSN	GND + 300 mV	GND − 300 mV		
VR_RDY	VCC + 0.3 V	−0.3 V	N/A	5 mA
VCC	6.5 V	−0.3 V	N/A	N/A
VRMP	+25 V	−0.3 V		
VR_HOT#, SDIO & ALERT#	VCC + 0.3 V	−0.3 V	0 mA	30 mA
OD#, SMOD, PWM1, PWM2, PWM3 & DRVON	VCC + 0.3 V	−0.3 V	5 mA	5 mA
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL INFORMATION

Description	Symbol	Typ	Unit
Thermal Characteristic QFN36 Package (Notes 1 and 2)	$R_{\theta JA}$	68	°C/W
Operating Junction Temperature Range*	T_J	−10 to 125	°C
Operating Ambient Temperature Range		−10 to 100	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Moisture Sensitivity Level	MSL	1	

*The maximum package power dissipation must be observed.
1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 µF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC INPUT						
Supply Voltage Range			4.75		5.25	V
Quiescent Current		EN = high; PS0, 1, 2 modes		23	29	mA
		EN = high; PS3 Mode		14	17.5	mA
		EN = low			30	µA
UVLO Threshold		VCC rising			4.5	V
		VCC falling	4.0			V
UVLO Hysteresis				160		mV
VRMP (VIN monitor)						
UVLO Threshold		VRMP falling	3.0	3.2	3.4	V
UVLO Hysteresis			600	800		mV
Leakage current		PS0, PS1, PS2, PS3; V_{VRMP} = 3.2 V			70	µA
Leakage current		PS4, V_{VRMP} = 20 V			500	nA
Leakage current		V_{EN} = 0 V, V_{VRMP} = 20 V			500	nA
ENABLE INPUT						
Enable High Input Leakage Current		External 1k pull−up to 3.3 V			1.0	µA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ENABLE INPUT						
Upper Threshold	V_{UPPER}				0.8	V
Lower Threshold	V_{LOWER}		0.3			V
Total Hysteresis		V_{UPPER} − V_{LOWER}		300		mV
Enable Delay Time		Time from Enable transitioning HI to when DRVON goes high.			2.4	ms
SCLK, SDIO, ALERT#						
SCLK Input Low Voltage	V_{ILSCLK}				0.45	V
SCLK Input High Voltage	V_{IHSCLK}		0.66			V
SDIO Input Low Voltage	V_{ILSDIO}				0.42	V
SDIO Input High Voltage	V_{IHSDIO}		0.72			V
Hysteresis Voltage (SCLK, SDIO)	V_{HYS}			100		mV
Output High Voltage (SDIO, ALERT#)	V_{OH}	External resistive pullup to 1.05 V		1.05		V
Output Low Voltage (SDIO, ALERT#)	V_{OL}	Sinking 20 mA		100		mV
Buffer On Resistance (SDIO, ALERT#)	R_{ON}	Measured sinking 4 mA		5	13	Ω
Leakage Current		Pin voltage between 0 and 1.05 V	−100		100	μA
Pin Capacitance					4.0	pF
VR clock to data delay	T_{CO}	Time between SCLK rising edge and valid SDIO level	4		8.3	ns
Setup time	T_{SU}	Time before SCLK falling (sampling) edge that SDIO level must be valid	7			ns
Hold time	T_{HLD}	Time after SCLK falling edge that the SDIO level remains valid	14			ns
VR12.5 & VR12.6 DAC						
System Voltage Accuracy		1.5 V ≤ DAC < 2.3 V, −10°C ≤ T_A ≤ 85°C	−0.5		0.5	%
		1.0 V ≤ DAC < 1.49 V, −10°C ≤ T_A ≤ 85°C	−8		8	mV
		0.5 V ≤ DAC < 0.99 V, −10°C ≤ T_A ≤ 85°C	−10		10	mV
DAC SLEW RATES (NCP81105)						
Soft Start Slew Rate		SVID Register 2Ah = default		12		mV/μs
Slew Rate Slow		Selectable Fraction of Fast Slew		3 – 24		mV/μs
Slew Rate Fast				48		mV/μs
DAC SLEW RATES (NCP81105H)						
Soft Start Slew Rate		SVID Register 2Ah = default		2.5		mV/μs
Slew Rate Slow		Selectable Fraction of Fast Slew		1 – 5		mV/μs
Slew Rate Fast				10		mV/μs
DIFFERENTIAL SUMMING AMPLIFIER						
VSP Input Leakage Current		V_{VSP} = 1.3 V	0		15	μA
VSN Bias Current		−0.3 V ≤ V_{VSN} ≤ 0.3 V	−1		1	μA
DVID UP Feedforward Charge		−0.3 V ≤ V_{VSN} ≤ 0.5 V Charge per 5 mV DAC increment		6.8		pC
VSP Input Voltage Range			−0.3		3.0	V
VSN Input Voltage Range			−0.3		0.3	V
−3dB Bandwidth		C_L = 20 pF to GND, R_L = 10 kΩ to GND		10		MHz
DC gain − VSx to DIFFOUT		VSP − VSN = 0.5 V to 2.3 V		1.0		V/V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 µF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL SUMMING AMPLIFIER						
Maximum Output Voltage		I_{SOURCE} = 2 mA	3.0			V
Minimum Output Voltage		I_{SINK} = 2 mA			0.5	V
ERROR AMPLIFIER						
Input Bias Current		V_{FB} = 1.3 V; Internal integrator active	−25		25	µA
Open Loop DC Gain		CL = 20 pF to GND, RL = 10 kΩ to GND		80		dB
Open Loop Unity Gain Bandwidth		CL = 20 pF to GND, RL = 10 kΩ to GND		20		MHz
Slew Rate		ΔVin = 100 mV, G = −10 V/V, ΔVout = 1.5 V − 2.5 V, Load = 20 pF to GND + 10 kΩ to GND		20		V/µs
Maximum Output Voltage		I_{SOURCE} = 2.0 mA	3.5			V
Minimum Output Voltage		I_{SINK} = 2.0 mA			1	V
VR_RDY (Power Good) OUTPUT						
Output Low Saturation Voltage		I_{VR_RDY} = 4 mA			0.3	V
Rise Time		1 kΩ external pull−up to 3.3 V, C_{TOT} = 45 pF		100		ns
Fall Time		1 kΩ external pull−up to 3.3 V, C_{TOT} = 45 pF		10		ns
Output Voltage at Power−up		VR_RDY pulled up to 5 V via 2 kΩ			1.0	V
Output Leakage Current When High		VR_RDY = 5.0 V	−1.0		1.0	µA
VR_RDY Delay (rising)		DAC = TARGET to VR_RDY high		5.5	6	µs
VR_RDY Delay (falling)		From OCP or OVP to VR_RDY low		5		µs
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)						
Absolute Over Voltage Threshold During Soft−Start			2.8	2.9	3.0	V
Over Voltage Threshold Above DAC		VSP rising	350	400	425	mV
Over Voltage Delay		VSP rising to PWMx low		50		ns
Under Voltage Threshold Below DAC		VSP falling		300		mV
Under−voltage Delay				5		µs
CURRENT BALANCE AMPLIFIERS						
Input Bias Current (after phase detection)		CSPx = CSNx = 1.7 V	−50		50	nA
Common Mode Input Voltage Range		CSPx = CSNx	0		2.3	V
Differential Mode Input Voltage Range		CSNx = 1.7 V	−100		100	mV
Closed loop Input Offset Voltage Matching		CSPx = CSNx = 1.7 V, Measured from the average offset	−1.5		1.5	mV
Amplifier Gain		0 V < CSPx−CSNx ≤ 0.1 V	5.7	6.0	6.3	V/V
Gain Matching		10 mV ≤ CSPx−CSNx ≤ 30 mV	−3		3	%
−3 dB Bandwidth				8		MHz
1 & 2 PHASE DETECTION						
CSN Pin Resistance to Ground		During phase detection only		50		kΩ
CSN Pin Threshold Voltage				4.5		V
Phase Detect Timer		Time from Enable transitioning HI to removal of phase detect resistance			3.5	ms

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT SUMMING AMPLIFIER						
Offset Voltage	Vos	V_{CSREF} = 1.0 V	−300		300	μV
CSSUM Input Bias Current		CSSUM = CSREF = 1 V	−7.5		7.5	nA
CSREF Input Bias Current		CSSUM = CSREF = 1 V	0		4.25	μA
Open Loop Gain				80		dB
Current Sense Unity Gain Bandwidth		C_L = 20 pF to GND, R_L = 10 kΩ to GND		10		MHz
Max CSCOMP Output Voltage		Isource = 2 mA	3.5			V
Minimum CSCOMP Output Voltage		Isink = 500 μA			100	mV
		Isink = 25 μA		7.0	30	mV
IOUT OUTPUT						
Maximum Output Voltage		R_{IOUT} = 5 kΩ	2.0			V
Input Referred Offset Voltage		ILIM minus CSREF	−1.9		1.9	mV
Output Source Current		ILIM sink current = 80 μA	700			μA
Current Gain	AI_{IOUT}	$(IOUT_{CURRENT}) / (ILIM_{CURRENT})$; R_{ILIM} = 20 kΩ; R_{IOUT} = 5.0 kΩ; V_{CSREF} = 1.7 V	9.5	10	10.5	A/A
DIMON Full Scale Voltage	V_{DIFS}			2.0		V
OVERCURRENT PROTECTION (ILIM pin)						
3 & 2−phase PS0 Threshold Current, 1−phase all−PS Threshold Current Delayed shutdown Immediate shutdown	 I_{DS} I_{IS}		 9.0 13.5	 10 15	 11.0 16.5	μA
3−phase, non−PS0 Threshold Current Delayed shutdown Immediate shutdown	 I_{DS} I_{IS}	 PS1, 2 or 3 mode (1−phase active) PS1, 2 or 3 mode (1−phase active)		 4 6		μA
2−phase, non−PS0 Threshold Current Delayed shutdown Immediate shutdown	 I_{DS} I_{IS}	 PS1, 2 or 3 mode (1−phase active) PS1, 2 or 3 mode (1−phase active)		 6.7 10		μA
Time for Delayed Shutdown				55		μs
OSCILLATOR						
Maximum Switching Frequency		See Precision Oscillator description	1425			kHz
Minimum Switching Frequency		See Precision Oscillator description			275	kHz
Switching Frequency Tolerance		PS0 mode; RROSC = 110 kΩ	925	1025	1125	kHz
ROSC Pin Output Current		V_{ROSC} = GND	9.5	10	10.5	μA
MODULATORS (PWM Comparators)						
Minimum Pulse Width				20		ns
0% Duty Cycle		COMP voltage when the PWM outputs remain Lo (Dual−edge modulation only)		1.3		V
100% Duty Cycle		COMP voltage when the PWM outputs remain HI, VRMP = 12.0 V; (Dual−edge modulation only)		2.5		V
PWM Phase Angle Error		Between adjacent phases, 3−phase operation	−20		20	deg
Ramp Feed−forward Voltage range		VRMP pin voltage	5		20	V
PWM OUTPUTS (PWM1/2/3)						
Output High Voltage		Sourcing 500 μA	V_{CC} − 0.2			V
Output Low Voltage		Sinking 500 μA			0.7	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PWM OUTPUTS (PWM1/2/3)						
Rise and Fall Times		CL (PCB) = 50 pF, measured between 10% & 90% of V_{CC}		10		ns
DRVON OUTPUT						
Output High Voltage		Sourcing 500 μA	3.0			V
Output Low Voltage		Sinking 500 μA			0.1	V
Rise Time		CL (PCB) = 20 pF, ΔVo = 10% to 90%		150		ns
Fall Time		CL (PCB) = 20 pF, ΔVo = 90% to 10%		5		ns
PWM delay time		Time from DRVON high to first PWM	110	120		μs
Internal Pull Down Resistance		EN = Low		70		kΩ
OD# OUTPUT						
Output High Voltage		Sourcing 500 μA	3.0			V
Output Low Voltage		Sinking 500 μA			0.1	V
PS0 Delay		Entering PS0; from fall of the earlier of PWM2 or PWM3 to OD# rising			15	ns
Rise/Fall Time		C_L (PCB) = 20 pF, ΔVo = 10% to 90%		10		ns
Internal Pull Down Resistance		EN = Low		70		kΩ
SMOD OUTPUT						
Output High Voltage		Sourcing 500 μA	3.0			V
Output Low Voltage		Sinking 500 μA			0.1	V
PS2/3 Delay		PS2&3; PWM1 rising to SMOD rising	10		50	ns
Rise/Fall Time		C_L (PCB) = 20 pF, ΔVo = 10% to 90%		10		ns
Internal Pull Down Resistance		EN = Low		70		kΩ
VR_HOT# OUTPUT						
Output Low Voltage		$I_{\_VRHOT\#}$ = −4 mA			0.3	V
Output Leakage Current		High Impedance State, $V_{VRHOT\#}$ = 3.3 V	−1.0		1.0	μA
TSENSE INPUT						
Alert# Assert Threshold		T_A = 85°C		458		mV
Alert# De−assert Threshold		T_A = 85°C		476		mV
VRHOT# Assert Threshold		T_A = 85°C		437		mV
VRHOT# De−assert Threshold		T_A = 85°C		457		mV
TSENSE Bias Current		V_{TSENSE} = 0.4 V, T_A = 85°C	57.7	60	62.7	μA
VBOOT PIN						
Sensing Current		V_{VBOOT} = GND		10		μA
IMAX PIN						
Sensing Current	I_{IMAX}	V_{IMAX} = GND	9.5	10	10.5	μA
IMAX Full Scale Voltage	V_{IMAXFS}			2.0		V
INT_SEL PIN						
Sensing Current		V_{INT_SEL} = GND		10		μA
DGAIN PIN						
Sensing Current		V_{DGAIN} = GND		10		μA
ADC						
Input Voltage Range			0		2	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EN} = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −10°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ADC						
Total Unadjusted Error (TUE)			−1		+1	%
Differential Nonlinearity (DNL)		8−bit			1	LSB
Power Supply Sensitivity				±1		%
Conversion Time				10		μs
Time to cycle through all inputs					250	μs

VR12.5 & VR12.6 VID TABLE

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	OFF	00	0	0	1	1	1	1	1	0	1.11	3E
0	0	0	0	0	0	0	1	0.50	01	0	0	1	1	1	1	1	1	1.12	3F
0	0	0	0	0	0	1	0	0.51	02	0	1	0	0	0	0	0	0	1.13	40
0	0	0	0	0	0	1	1	0.52	03	0	1	0	0	0	0	0	1	1.14	41
0	0	0	0	0	1	0	0	0.53	04	0	1	0	0	0	0	1	0	1.15	42
0	0	0	0	0	1	0	1	0.54	05	0	1	0	0	0	0	1	1	1.16	43
0	0	0	0	0	1	1	0	0.55	06	0	1	0	0	0	1	0	0	1.17	44
0	0	0	0	0	1	1	1	0.56	07	0	1	0	0	0	1	0	1	1.18	45
0	0	0	0	1	0	0	0	0.57	08	0	1	0	0	0	1	1	0	1.19	46
0	0	0	0	1	0	0	1	0.58	09	0	1	0	0	0	1	1	1	1.20	47
0	0	0	0	1	0	1	0	0.59	0A	0	1	0	0	1	0	0	0	1.21	48
0	0	0	0	1	0	1	1	0.60	0B	0	1	0	0	1	0	0	1	1.22	49
0	0	0	0	1	1	0	0	0.61	0C	0	1	0	0	1	0	1	0	1.23	4A
0	0	0	0	1	1	0	1	0.62	0D	0	1	0	0	1	0	1	1	1.24	4B
0	0	0	0	1	1	1	0	0.63	0E	0	1	0	0	1	1	0	0	1.25	4C
0	0	0	0	1	1	1	1	0.64	0F	0	1	0	0	1	1	0	1	1.26	4D
0	0	0	1	0	0	0	0	0.65	10	0	1	0	0	1	1	1	0	1.27	4E
0	0	0	1	0	0	0	1	0.66	11	0	1	0	0	1	1	1	1	1.28	4F
0	0	0	1	0	0	1	0	0.67	12	0	1	0	1	0	0	0	0	1.29	50
0	0	0	1	0	0	1	1	0.68	13	0	1	0	1	0	0	0	1	1.30	51
0	0	0	1	0	1	0	0	0.69	14	0	1	0	1	0	0	1	0	1.31	52
0	0	0	1	0	1	0	1	0.70	15	0	1	0	1	0	0	1	1	1.32	53
0	0	0	1	0	1	1	0	0.71	16	0	1	0	1	0	1	0	0	1.33	54
0	0	0	1	0	1	1	1	0.72	17	0	1	0	1	0	1	0	1	1.34	55
0	0	0	1	1	0	0	0	0.73	18	0	1	0	1	0	1	1	0	1.35	56
0	0	0	1	1	0	0	1	0.74	19	0	1	0	1	0	1	1	1	1.36	57
0	0	0	1	1	0	1	0	0.75	1A	0	1	0	1	1	0	0	0	1.37	58
0	0	0	1	1	0	1	1	0.76	1B	0	1	0	1	1	0	0	1	1.38	59
0	0	0	1	1	1	0	0	0.77	1C	0	1	0	1	1	0	1	0	1.39	5A
0	0	0	1	1	1	0	1	0.78	1D	0	1	0	1	1	0	1	1	1.40	5B
0	0	0	1	1	1	1	0	0.79	1E	0	1	0	1	1	1	0	0	1.41	5C
0	0	0	1	1	1	1	1	0.80	1F	0	1	0	1	1	1	0	1	1.42	5D
0	0	1	0	0	0	0	0	0.81	20	0	1	0	1	1	1	1	0	1.43	5E
0	0	1	0	0	0	0	1	0.82	21	0	1	0	1	1	1	1	1	1.44	5F
0	0	1	0	0	0	1	0	0.83	22	0	1	1	0	0	0	0	0	1.45	60
0	0	1	0	0	0	1	1	0.84	23	0	1	1	0	0	0	0	1	1.46	61
0	0	1	0	0	1	0	0	0.85	24	0	1	1	0	0	0	1	0	1.47	62
0	0	1	0	0	1	0	1	0.86	25	0	1	1	0	0	0	1	1	1.48	63
0	0	1	0	0	1	1	0	0.87	26	0	1	1	0	0	1	0	0	1.49	64
0	0	1	0	0	1	1	1	0.88	27	0	1	1	0	0	1	0	1	1.50	65
0	0	1	0	1	0	0	0	0.89	28	0	1	1	0	0	1	1	0	1.51	66
0	0	1	0	1	0	0	1	0.90	29	0	1	1	0	0	1	1	1	1.52	67
0	0	1	0	1	0	1	0	0.91	2A	0	1	1	0	1	0	0	0	1.53	68
0	0	1	0	1	0	1	1	0.92	2B	0	1	1	0	1	0	0	1	1.54	69
0	0	1	0	1	1	0	0	0.93	2C	0	1	1	0	1	0	1	0	1.55	6A
0	0	1	0	1	1	0	1	0.94	2D	0	1	1	0	1	0	1	1	1.56	6B
0	0	1	0	1	1	1	0	0.95	2E	0	1	1	0	1	1	0	0	1.57	6C
0	0	1	0	1	1	1	1	0.96	2F	0	1	1	0	1	1	0	1	1.58	6D
0	0	1	1	0	0	0	0	0.97	30	0	1	1	0	1	1	1	0	1.59	6E
0	0	1	1	0	0	0	1	0.98	31	0	1	1	0	1	1	1	1	1.60	6F
0	0	1	1	0	0	1	0	0.99	32	0	1	1	1	0	0	0	0	1.61	70
0	0	1	1	0	0	1	1	1.00	33	0	1	1	1	0	0	0	1	1.62	71
0	0	1	1	0	1	0	0	1.01	34	0	1	1	1	0	0	1	0	1.63	72
0	0	1	1	0	1	0	1	1.02	35	0	1	1	1	0	0	1	1	1.64	73
0	0	1	1	0	1	1	0	1.03	36	0	1	1	1	0	1	0	0	1.65	74
0	0	1	1	0	1	1	1	1.04	37	0	1	1	1	0	1	0	1	1.66	75
0	0	1	1	1	0	0	0	1.05	38	0	1	1	1	0	1	1	0	1.67	76
0	0	1	1	1	0	0	1	1.06	39	0	1	1	1	0	1	1	1	1.68	77
0	0	1	1	1	0	1	0	1.07	3A	0	1	1	1	1	0	0	0	1.69	78
0	0	1	1	1	0	1	1	1.08	3B	0	1	1	1	1	0	0	1	1.70	79
0	0	1	1	1	1	0	0	1.09	3C	0	1	1	1	1	0	1	0	1.71	7A
0	0	1	1	1	1	0	1	1.10	3D	0	1	1	1	1	0	1	1	1.72	7B

VR12.5 & VR12.6 VID TABLE

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	1	1	1	1	0	0	1.73	7C	1	0	0	1	1	0	0	1	2.02	99
0	1	1	1	1	1	0	1	1.74	7D	1	0	0	1	1	0	1	0	2.03	9A
0	1	1	1	1	1	1	0	1.75	7E	1	0	0	1	1	0	1	1	2.04	9B
0	1	1	1	1	1	1	1	1.76	7F	1	0	0	1	1	1	0	0	2.05	9C
1	0	0	0	0	0	0	0	1.77	80	1	0	0	1	1	1	0	1	2.06	9D
1	0	0	0	0	0	0	1	1.78	81	1	0	0	1	1	1	1	0	2.07	9E
1	0	0	0	0	0	1	0	1.79	82	1	0	0	1	1	1	1	1	2.08	9F
1	0	0	0	0	0	1	1	1.80	83	1	0	1	0	0	0	0	0	2.09	A0
1	0	0	0	0	1	0	0	1.81	84	1	0	1	0	0	0	0	1	2.10	A1
1	0	0	0	0	1	0	1	1.82	85	1	0	1	0	0	0	1	0	2.11	A2
1	0	0	0	0	1	1	0	1.83	86	1	0	1	0	0	0	1	1	2.12	A3
1	0	0	0	0	1	1	1	1.84	87	1	0	1	0	0	1	0	0	2.13	A4
1	0	0	0	1	0	0	0	1.85	88	1	0	1	0	0	1	0	1	2.14	A5
1	0	0	0	1	0	0	1	1.86	89	1	0	1	0	0	1	1	0	2.15	A6
1	0	0	0	1	0	1	0	1.87	8A	1	0	1	0	0	1	1	1	2.16	A7
1	0	0	0	1	0	1	1	1.88	8B	1	0	1	0	1	0	0	0	2.17	A8
1	0	0	0	1	1	0	0	1.89	8C	1	0	1	0	1	0	0	1	2.18	A9
1	0	0	0	1	1	0	1	1.90	8D	1	0	1	0	1	0	1	0	2.19	AA
1	0	0	0	1	1	1	0	1.91	8E	1	0	1	0	1	0	1	1	2.20	AB
1	0	0	0	1	1	1	1	1.92	8F	1	0	1	0	1	1	0	0	2.21	AC
1	0	0	1	0	0	0	0	1.93	90	1	0	1	0	1	1	0	1	2.22	AD
1	0	0	1	0	0	0	1	1.94	91	1	0	1	0	1	1	1	0	2.23	AE
1	0	0	1	0	0	1	0	1.95	92	1	0	1	0	1	1	1	1	2.24	AF
1	0	0	1	0	0	1	1	1.96	93	1	0	1	1	0	0	0	0	2.25	B0
1	0	0	1	0	1	0	0	1.97	94	1	0	1	1	0	0	0	1	2.26	B1
1	0	0	1	0	1	0	1	1.98	95	1	0	1	1	0	0	1	0	2.27	B2
1	0	0	1	0	1	1	0	1.99	96	1	0	1	1	0	0	1	1	2.28	B3
1	0	0	1	0	1	1	1	2.00	97	1	0	1	1	0	1	0	0	2.29	B4
1	0	0	1	1	0	0	0	2.01	98	1	0	1	1	0	1	0	1	2.30	B5

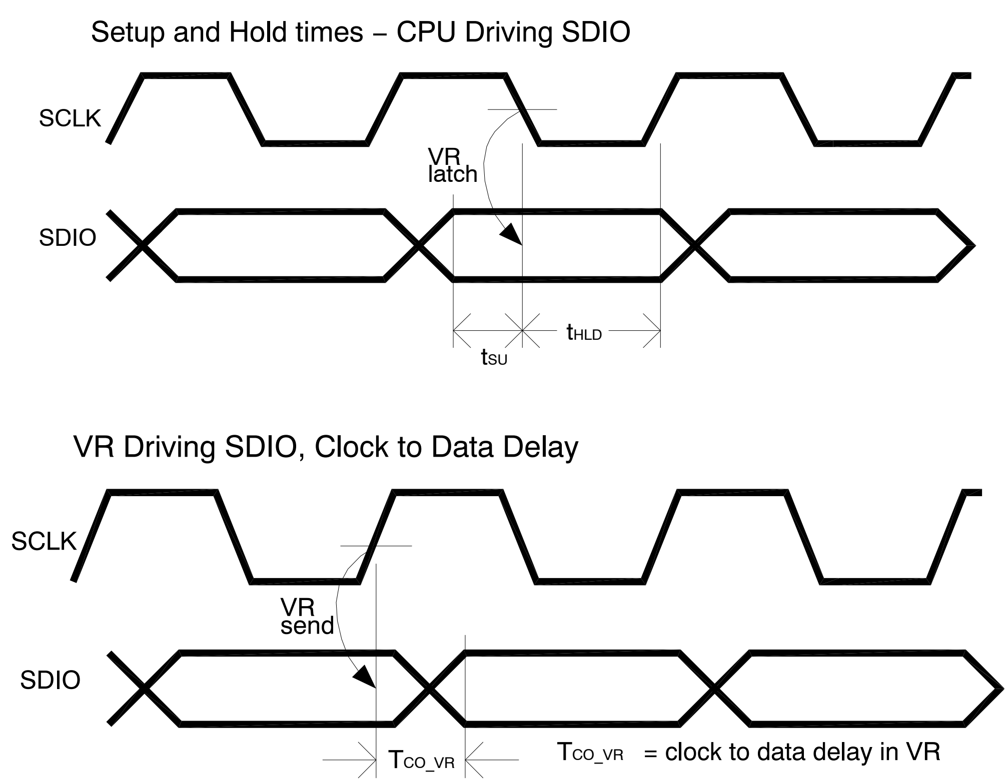


Figure 10. SVID Timing Diagrams

STATE TRUTH TABLE

State	VR_RDY Pin	Error AMP Comp Pin	OVP & UVP	DRVON Pin	SMOD Pin	OD# Pin	Method of Reset
VCC UVLO 0 < VCC < threshold VRMP > threshold	N/A	N/A	N/A	Resistive pull down	Resistive pull down	Resistive pull down	
VRMP UVLO VCC > threshold 0 < VRMP < threshold	N/A	N/A	N/A	Resistive pull down	Resistive pull down	Resistive pull down	
Disabled EN < threshold VCC > threshold VRMP > threshold	Low	Low	Disabled	Low	Low	Low	
Start up Delay & Calibration EN > threshold VCC > threshold VRMP > threshold	Low	Low	Disabled	Low	Low	Low	
Soft Start EN > threshold VCC > threshold VRMP > threshold	Low	Operational	Active	High	Low until first PWM1 pulse	Low until first PWM2 or PWM3 pulse	
Normal Operation EN > threshold VCC > threshold VRMP > threshold	High	Operational	Active	High	High in PS0 & PS1; High or may toggle in PS2 & PS3	High in PS0; Low in PS1, PS2, & PS3	N/A
Over Voltage	Low	Low	DAC + 400 mV	High	High/ Toggles during output rampdown	High/ Toggles during output rampdown	EN low or cycle power
Under Voltage	Low	Operational	DAC−Droop −300 mV	High	High	High	Output voltage > DAC−Droop −300 mV
Over Current	Low	Operational	Last DAC Code + 400 mV	Low	Low	Low	EN low or cycle power
VID Code = 00h	Low	Low	Disabled	High (PWM outputs low)	Low	Low	Set Valid VID Code

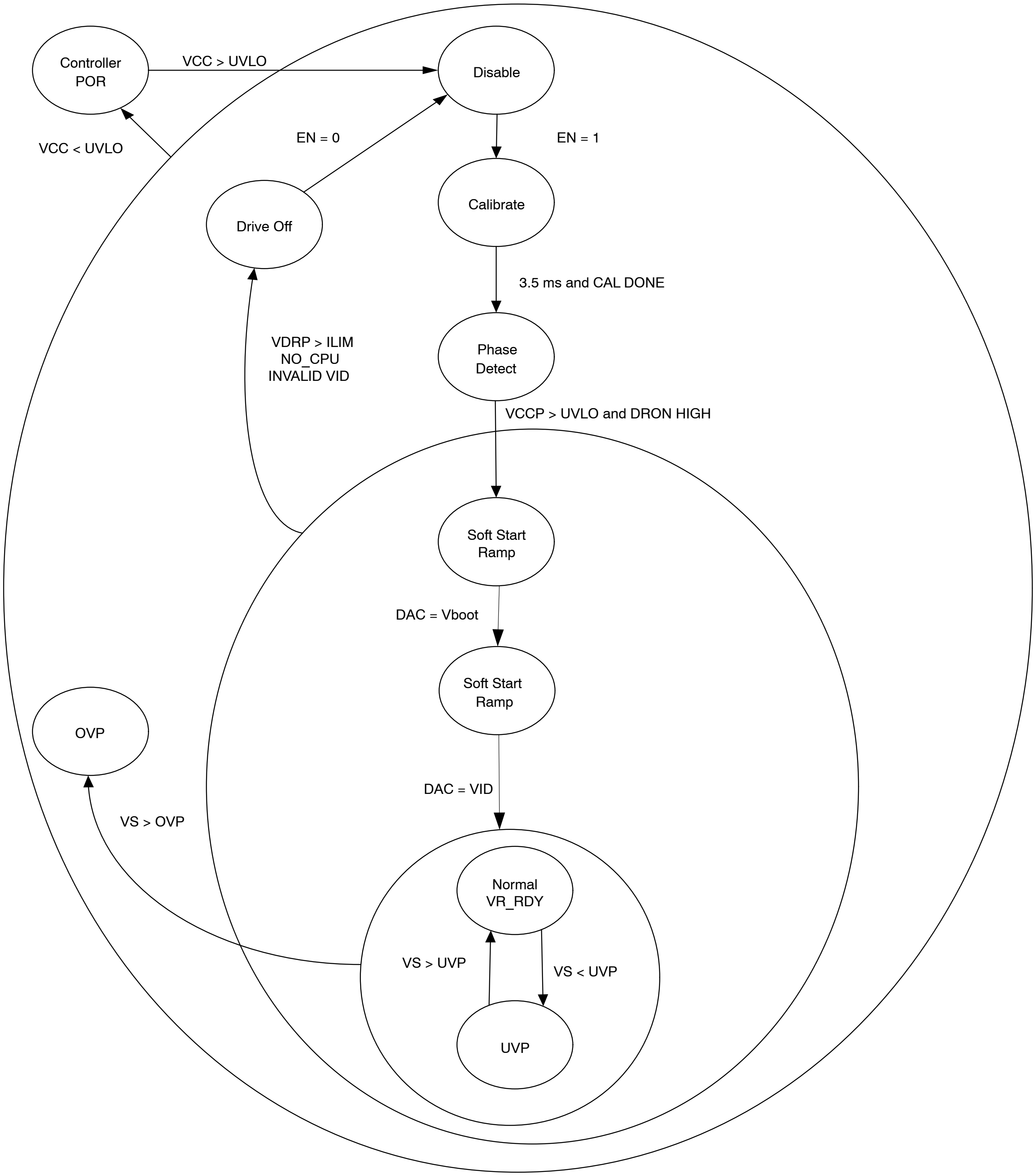


Figure 11. State Diagram

General

The NCP81105 is a single output, one−to−three phase, dual−edge modulated PWM controller with a serial VID control interface designed to meet the Intel VR12.5 & VR12.6 specifications. The NCP81105 implements PS0, PS1, PS2, PS3 and PS4 power states. It is designed to work in notebook and desktop CPU power supply applications.

Power Status	PWM Output Operating Mode
PS0	Multi−phase, fixed frequency, dual edge modulation (RPM modulation when optioned for single phase), interleaved PWM outputs (CCM mode)
PS1	Single−phase (PWM1) COT (CCM mode; Phases 2 & 3 disabled by OD#)
PS2	Single−phase (PWM1) RPM (DCM mode by SMOD; Phases 2 & 3 disabled by OD#)
PS3	Single−phase (PWM1) RPM (DCM mode by SMOD; Phases 2 & 3 disabled by OD#)
PS4	No switching; Memory retained; SVID active

For 81105, the VID code change rate is controlled with the SVID interface with three options as below:

DVID Option	SVID Command Code	Feature	Register Address (Contains the slew rate of VID code change)
SetVID_Fast	01h	48 mV/μs VID code change slew rate	24h
SetVID_Slow	02h	12 mV/μs VID code change slew rate**	25h
SetVID_Decay	03h	No control, VID code down	N/A

**The Slow VID code change slew rate can be modified by writing to the 2Ah register with the SVID bus.

For 81105H, the VID code change rate is controlled with the SVID interface with three options as below:

DVID Option	SVID Command Code	Feature	Register Address (Contains the slew rate of VID code change)
SetVID_Fast	01h	10 mV/μs VID code change slew rate	24h
SetVID_Slow	02h	2.5 mV/μs VID code change slew rate**	25h
SetVID_Decay	03h	No control, VID code down	N/A

**The Slow VID code change slew rate can be modified by writing to the 2Ah register with the SVID bus.

Serial VID

The NCP81105 supports the Intel serial VID (SVID) interface. It communicates with the microprocessor through three wires (SCLK, SDIO, ALERT#). The table of supported registers is shown below.

Index	Name	Description	Access	Default
00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah	R	1Ah
01h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number.	R	15h
02h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.	R	04h
03h	Product date code ID		R	00
05h	Protocol ID	Identifies the SVID Protocol the NCP81105 supports	R	03h
06h	Capability	Informs the Master of the NCP81105’s Capabilities, 1 for supported, 0 for not supported Bit 7: Iout_format; Reg 15 FFh = Icc_Max (=1) Bit 6: ADC Measurement of Temp; Supported (= 1) Bit 5: ADC Measurement of Pin; Not supported (= 0) Bit 4: ADC Measurement of Vin; Supported (= 1) Bit 3: ADC Measurement of Iin; Not supported (= 0) Bit 2: ADC Measurement of Pout; Supported (= 1) Bit 1: ADC Measurement of Vout; Supported (= 1) Bit 0: ADC Measurement of Iout; Supported (= 1)	R	D7h
10h	Status_1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR.	R	00h

Index	Name	Description	Access	Default
11h	Status_2	Data register showing optional status_2 data.	R	00h
12h	Temp zone	Data register showing temperature zones the system is operating in (thermometer format with 3 degree resolution).	R	00h
15h	I_out	8 bit binary word ADC of current. This register reads 0xFF when the output current is at ICC_Max	R	01h
16h	V_out	8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 8 mV	R	01h
17h	VR_Temp	8 bit binary word ADC of temperature. Binary format in deg C, IE 100C = 64h.	R	01h
18h	P_out	8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register.	R	01h
1Ah	V_in	8 bit binary word ADC of input voltage, measured at VRMP pin. LSB size is 112 mV	R	00h
1Ch	Status 2 Last read	When the status 2 register is read, its contents are copied into this register. The format is the same as the Status 2 Register.	R	00h
21h	ICC_Max	Data register containing the ICC_Max supported by the platform. The value is measured at the IMAX pin upon power up and placed in this register. From that point on, the register is read only.	R	00h
22h	Temp_Max	Data register containing the max temperature the platform supports and the level VR_hot asserts. This value defaults to 100°C and is programmable over the SVID Interface	R/W	64h
24h	SR_fast	Slew Rate for SetVID_fast commands. Binary format in mV/μs. NCP81105 NCP81105H	 R R	 32h 0Ah
25h	SR_slow	Slew Rate for SetVID_slow commands. A fraction of the SR_fast rate (register 24h) determined by register 2Ah. Binary format in mV/μs NCP81105 NCP81105H	 R R	 0Ch 03h
26h	Vboot	The Boot voltage is programmed using a resistor on the VBOOT pin which is sensed on power up. The NCP81105 will ramp to Vboot and hold at Vboot until it receives a new SVID SetVID command to move to a different voltage.	R	00h
2Ah	SR_Slow selector	0001 = Fast_SR/2 0010 = Fast_SR/4: default 0100 = Fast_SR/8 1000 = Fast_SR/16	R/W	02h
2Bh	PS4 exit latency	Reflects the latency of exiting the PS4 state. The exit latency is defined as the time duration, in us, from the ACK of the SETVID Slow/Fast command to the beginning of the output voltage ramp.	R	8Ch
2Ch	PS3 exit latency	Reflects the latency of exiting the PS3 state. The exit latency is defined as the time duration, in us, from the ACK of the SETVID Slow/Fast command until the NCP81105 is capable of supplying max current of the commanded PS state.	R	55h
2Dh	Enable to ready for SVID time	Reflects the latency from Enable assertion to the VR controller being ready to accept an SVID command. The latency is defined as the time duration, in μs: $(x/16)*2^{Y}$. X = bits [3:0]: 4 bit value 0000 to 1111 Y = bits [7:4]: 4 bit value 0000 to 1111	R	CAh
30h	Vout_Max	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR will respond with a “not supported” acknowledgement. VR12.5 & VR12.6 VID format, e.g., B5h = 2.3 V (see VID Table)	RW	B5h
31h	VID setting	Data register containing currently programmed VID voltage. VID data format. VR12.5 & VR12.6 VID format, e.g., 97h = 2.0 V	RW	00h
32h	Pwr State	Register containing the current programmed power state.	RW	00h

Index	Name	Description	Access	Default

33h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0 = positive margin, 1 = negative margin. Remaining 7 BITS are # VID steps for margin 2s complement.
		00h=no margin
		01h=+1 VID step
		02h=+2 VID steps
		FFh=−1 VID step
		FEh=−2 VID steps.
			RW	00h

34h	MultiVR Config	Bit 0 set to 1 causes VR_RDY to respond to a SetVID (0.0 V) command as a valid VID voltage setting instead of a disable command (only after ramping to a non−zero VID after startup). Bit 1 set to 1 locks the current VID and Power State settings until such time as the VR is issued a SetPS(00h) command.	RW	00h

Phase Detection Sequence

During start−up, the number of operational phases is determined by the internal circuitry monitoring the CSN inputs. Normally, NCP81105 operates as a 3−phase PWM controller. Connecting the CSN2 pin to V_{CC} programs 2−phase operation using phases 1 and 3. Connecting the CSN3 pin to V_{CC} programs 1−phase operation using phase 1.

Prior to soft start, while ENABLE is high, the CSN2 and CSN3 pins have approximately 50 kΩ to ground. An internal comparator checks the voltage of the CSN pins and compares them to a reference voltage. If either pin is tied to V_{CC}, its voltage is above the reference voltage and the controller is configured for reduced−phase operation. Otherwise, the resistance pulls the pin voltages to ground, which is below the reference, and the part operates in 3 phase mode.

PHASE COUNT TABLE

Number of Phases	Programming Pins (CSNx)	What to do with Unused Pins
3	All CSN pins connected normally	No unused pins
2	Tie CSN2 to VCC through 2 kΩ; CSN3, CSN1 connected normally	Tie CSP2 to ground; Float PWM2
1	Tie CSN3 to VCC through 2 kΩ; CSN1 connected normally	Tie CSN2, CSP2 & CSP3 to ground; Float PWM2, PWM3 & OD#

BOOT Voltage Programming

The NCP81105 has a VBOOT voltage register that can be externally programmed. The Boot voltage for the NCP81105 is set using the VBOOT pin on power up. A 10 μA current is sourced from the VBOOT pin into an external resistance connected to ground, and the resulting voltage is measured. This is compared with the thresholds in the table below and the corresponding value is placed in the VBOOT register (26h). This value is set on power up and cannot be changed after the initial power up sequence is complete.

BOOT VOLTAGE TABLE

Resistance	Boot Voltage
≤30.1k	0 V
49.9k	1.65 V
69.8k	1.70 V
Open	1.75 V

Addressing the NCP81105

The NCP81105 has fixed SVID device address 0000.

Remote Sense Amplifier

A high performance, high input impedance, differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage and a voltage to bias the output above ground.

$$V_{DIFFOUT} = \left(V_{VSP} - V_{VSN}\right) + \left(1.3\text{ V} - V_{DAC}\right) - \left(V_{DROOP} - V_{CSREF}\right)$$

$$V_{DROOP} = V_{CSCOMP} \times \text{Droop Gain Scaling (see the Droop Gain Table)}$$