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NCP81233

Product Preview
Multi-Phase Controller with I²C Interface for DrMOS

The NCP81233, a multi-phase synchronous buck controller with an I²C interface, provides power management solutions for applications supported by DrMOS. It supports 1-, 2-, 3-, 4-, or 6-phase operation and provides differential voltage and current sense, flexible programming, and comprehensive protections.

Features
- Selectable 1-, 2-, 3-, 4-, or 6-Phase Operation
- Support up to 12-Phase Operation with Phase Doublers
- I²C Interface with 8 Programmable Addresses
- Vin = 4.5 V ~ 20 V with Input Feedforward
- Integrated 5.35 V LDO and 3.3 V LDO
- Fsw = 200 k ~ 1.2 MHz
- Vout = 0.6 V ~ 5.3 V with 0.25 V~1.52 V DAC (5 mV/step)
- Programmable Vboot Voltage 0.6V ~ 1.23V (10mV/step) with Restore Function
- DVID Slew Rate Options (0.125 mV/us, 0.25 mV/us, 0.5 mV/us, 1 mV/us, 2 mV/us, 4 mV/us, 8 mV/us, 16 mV/us)
- Programmable External Reference Input
- PWM Output Compatible to 3.3 V and 5 V DrMOS
- Differential Output Voltage Sense
- Differential Current Sense Compatible for both Inductor DCR Sense and DrMOS Iout Signal
- Programmable Load Line
- Report of Vout and Iout
- Enable with Programmable Input UVLO
- DrMOS Power Ready Detection (DRVON)
- Externally Programmable Soft Start
- Power Saving Interface
- Power Good Indicator
- Programmable Over Current Protection
- Programmable Over/Under Voltage Protection
- Hiccup Over Temperature Protection
- Thermal Shutdown Protection
- This is a Pb-Free Device

Typical Applications
- Telecom Applications
- Server and Storage System
- Graphics Card Applications
- Multiphase DC-DC Power Management

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1   52

GFN52 6x6, O.4P
CASE 485BE

PINOUT
52 PIN, QFN
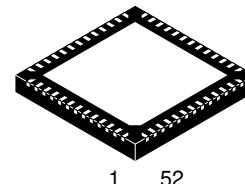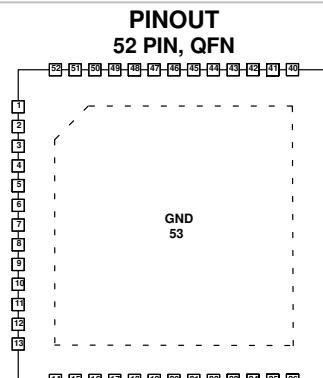
For more details see Figure 1.

MARKING DIAGRAM*

NCP81233
AWLYYWWG
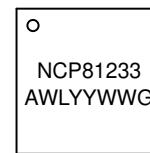
A   = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G   = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ▪", may or may not be present.

ORDERING INFORMATION

Device	Package	Shipping†
NCP81233MNTXG	QFN52 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](BRD8011/D).

March, 2017 – Rev. P1

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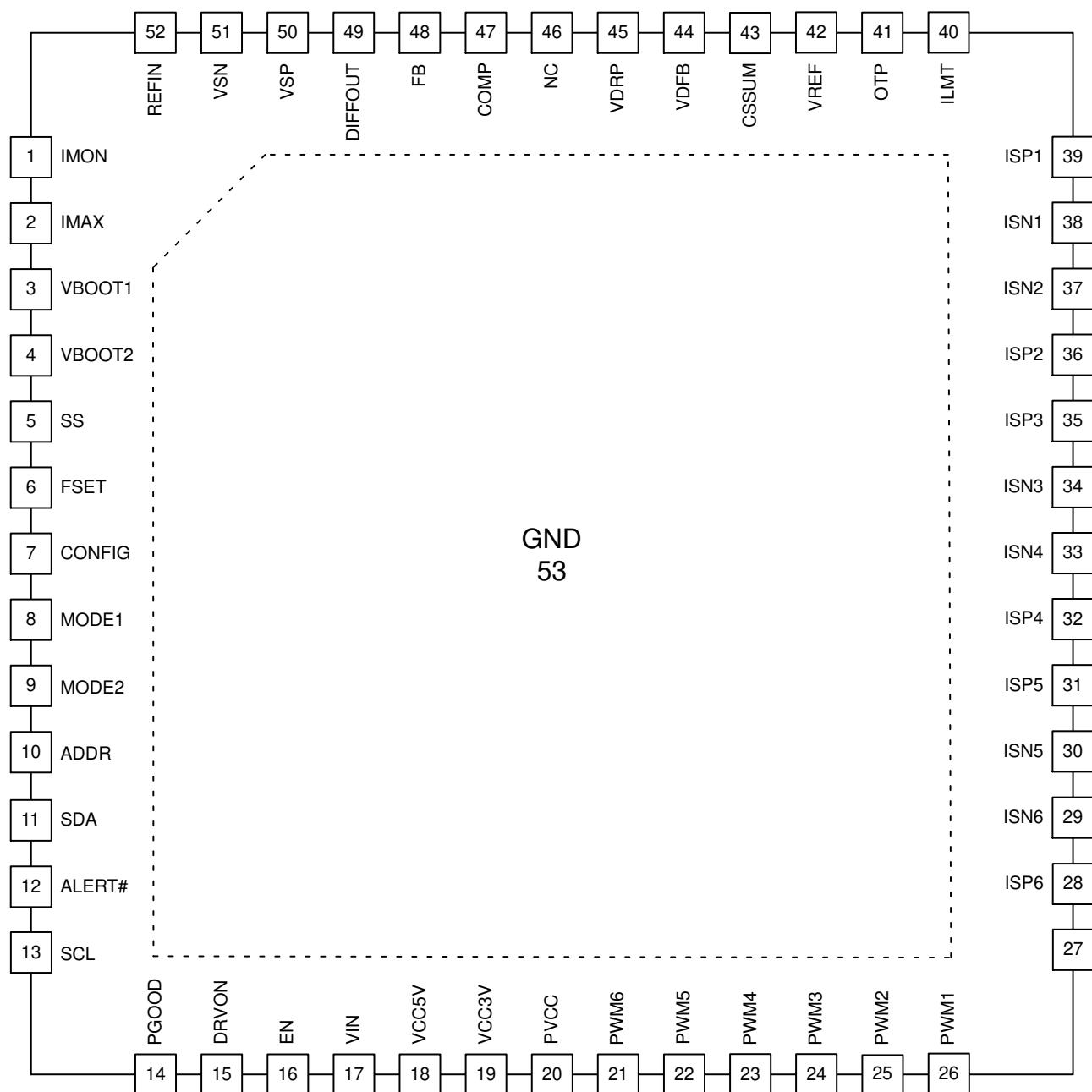
Figure 1. Pin Configuration

ORDERING INFORMATION

TABLE 1. PIN DESCRIPTION

| Pin	Name	Type	Description
1	IMON	Analog Output	OUT Current Monitor. Provides output signal representing output current by connecting a capacitor from this pin to ground.
2	IMAX	Analog Input	Current Maximum. A resistor from this pin to ground programs IMAX.
3	VBOOT1	Analog Input	Boot-Up Voltage 1. A resistor from this pin to ground programs boot voltage
4	VBOOT2	Analog Input	Boot-Up Voltage 2. A resistor from this pin to ground programs boot voltage.
5	SS	Analog Input	Soft-Start Slew Rate. A resistor from this pin to ground programs soft-start slew rate.
6	FSET	Analog Input	Frequency Selection. A resistor from this pin to ground programs switching frequency per phase.
7	CONFIG	Analog Input	Configuration. A resistor from this pin to ground programs configuration of power stages.
8	MODE1	Analog Input	Mode Programming 1. A resistor from this pin to ground programs configuration of operation functions.
9	MODE2	Analog Input	Mode Programming 2. A resistor from this pin to ground programs configuration of operation functions.
10	ADDR	Analog Input	Address. A resistor from this pin to ground programs address of I^{2}C interface.
11	SDA	Logic Bidirectional	Serial Data I/O Port. Data port of I^{2}C interface.
12	ALERT#	Logic Output	ALERT. Open-drain output. Provides a logic low valid alert signal.
13	SCL	Logic Input	Serial Clock. Clock input of I^{2}C interface.
14	PGOOD	Logic Output	Power GOOD. Open-drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window.
15	DRVON	Analog Input	Driver On. High input voltage means power supply of DrMOS's driver is ready.
16	EN	Analog Input	Enable. Logic high enables controller while logic low disables controller. Input supply UVLO can be programmed at this pin.
17	VIN	Power Input	Power Supply Input. Power supply input pin of the device, which is connected to the integrated 5.35 V LDO and 3.3 V LDO. 4.7 µF or more ceramic capacitors must bypass this input to power ground. The capacitors should be placed as close as possible to this pin.
18	VCC5V	Analog Power	Voltage Supply of Controller. Output of integrated 5.35 V LDO and power input pin of analog circuits. A 4.7 µF ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
19	VCC3V	Analog Power	3.3 V Voltage Supply. Output of integrated 3.3 V LDO. A 4.7 µF ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
20	PVCC	Analog Power	Voltage Supply of PWM Drivers. Power supply input pin of internal PWM drivers and digital circuits, which is connected to VCC5 V via a 4.7 Ω resistor. A 1 µF or larger ceramic capacitor bypasses this input to ground. This capacitor should be placed as close as possible to this pin.
21	PWM6	Analog Output	PWM 6. PWM output of phase 6.
22	PWM5	Analog Output	PWM 5. PWM output of phase 5.
23	PWM4	Analog Output	PWM 4. PWM output of phase 4.
24	PWM3	Analog Output	PWM 3. PWM output of phase 3.
25	PWM2	Analog Output	PWM 2. PWM output of phase 2.
26	PWM1	Analog Output	PWM 1. PWM output of phase 1.
27	VB_RST# / PSI	Logic Input	VBOOT Restore. Logic low restores output to boot voltage. Power Saving Interface. Logic high enables Multi-phase CCM operation, and logic low enables 1-phase CCM operation. Pin function is programmed at MODE2 pin.

TABLE 1. PIN DESCRIPTION (continued)

| Pin	Name	Type	Description
28	ISP6	Analog Input	Current Sense Positive Input 6. Non-inverting input of differential current sense amplifier of phase 6.
29	ISN6	Analog Input	Current Sense Negative Input 6. Inverting input of differential current sense amplifier of phase 6.
30	ISN5	Analog Input	Current Sense Negative Input 5. Inverting input of differential current sense amplifier of phase 5.
31	ISP5	Analog Input	Current Sense Positive Input 5. Non-inverting input of differential current sense amplifier of phase 5.
32	ISP4	Analog Input	Current Sense Positive Input 4. Non-inverting input of differential current sense amplifier of phase 4.
33	ISN4	Analog Input	Current Sense Negative Input 4. Inverting input of differential current sense amplifier of phase 4.
34	ISN3	Analog Input	Current Sense Negative Input 3. Inverting input of differential current sense amplifier of phase 3.
35	ISP3	Analog Input	Current Sense Positive Input 3. Non-inverting input of differential current sense amplifier of phase 3.
36	ISP2	Analog Input	Current Sense Positive Input 2. Non-inverting input of differential current sense amplifier of phase 2.
37	ISN2	Analog Input	Current Sense Negative Input 2. Inverting input of differential current sense amplifier of phase 2.
38	ISN1	Analog Input	Current Sense Negative Input 1. Inverting input of differential current sense amplifier of phase 1.
39	ISP1	Analog Input	Current Sense Positive Input 1. Non-inverting input of differential current sense amplifier of phase 1.
40	ILMT	Analog Input	Limit of Current. Voltage at this pin sets over-current threshold.
41	OTP	Analog Input	Over Temperature Protection. Voltage at this pin sets over-temperature threshold.
42	VREF	Analog Output	Output of Reference. Output of 0.6 V reference. A 10 nF ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
43	CSSUM	Analog Output	Current Sense SUM. Output of current sum amplifier.
44	VDFB	Analog Output	Droop Amplifier Feedback. Inverting input of droop amplifier
45	VDRP	Analog Output	Droop Amplifier Output. Output of droop amplifier.
46	NC	No Connection	
47	COMP	Analog Output	Compensation. Output pin of error amplifier.
48	FB	Analog Input	Feedback. Inverting input of internal error amplifier.
49	DIFFOUT	Analog Output	Differential Amplifier Output. Output pin of differential voltage sense amplifier.
50	VSP	Analog Input	Voltage Sense Positive Input. Non-inverting input of differential voltage sense amplifier.
51	VSN	Analog Input	Voltage Sense Negative Input. Inverting input of differential voltage sense amplifier.
52	REFIN	Analog Input	Reference Voltage Input. External reference voltage input.
53	THERM/GND	Analog Ground	Thermal Pad and Analog Ground. Ground of internal control circuits. Must be connected to the system ground.

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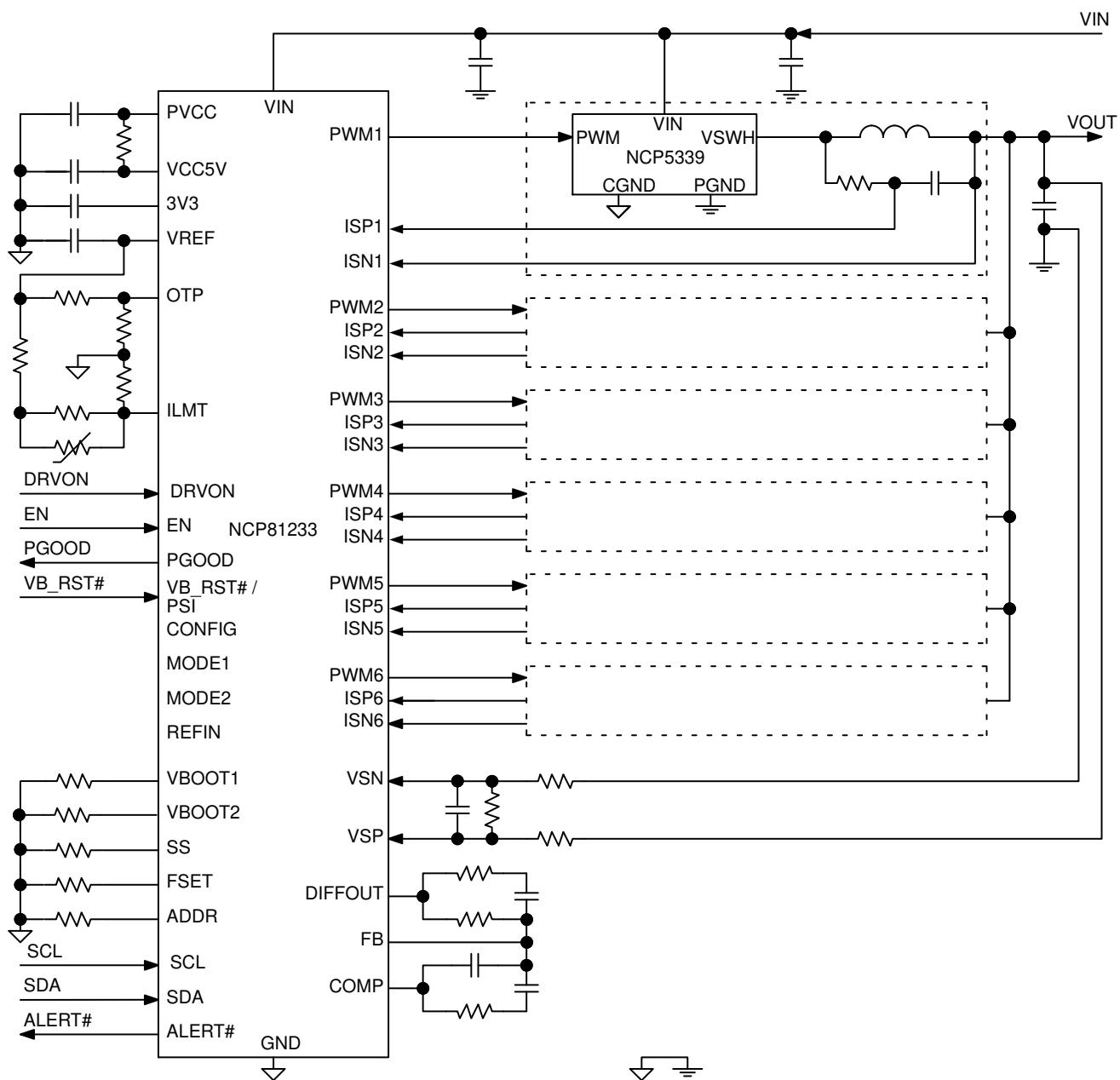
Figure 2. Typical Application Circuit with Programmed Boot Voltage

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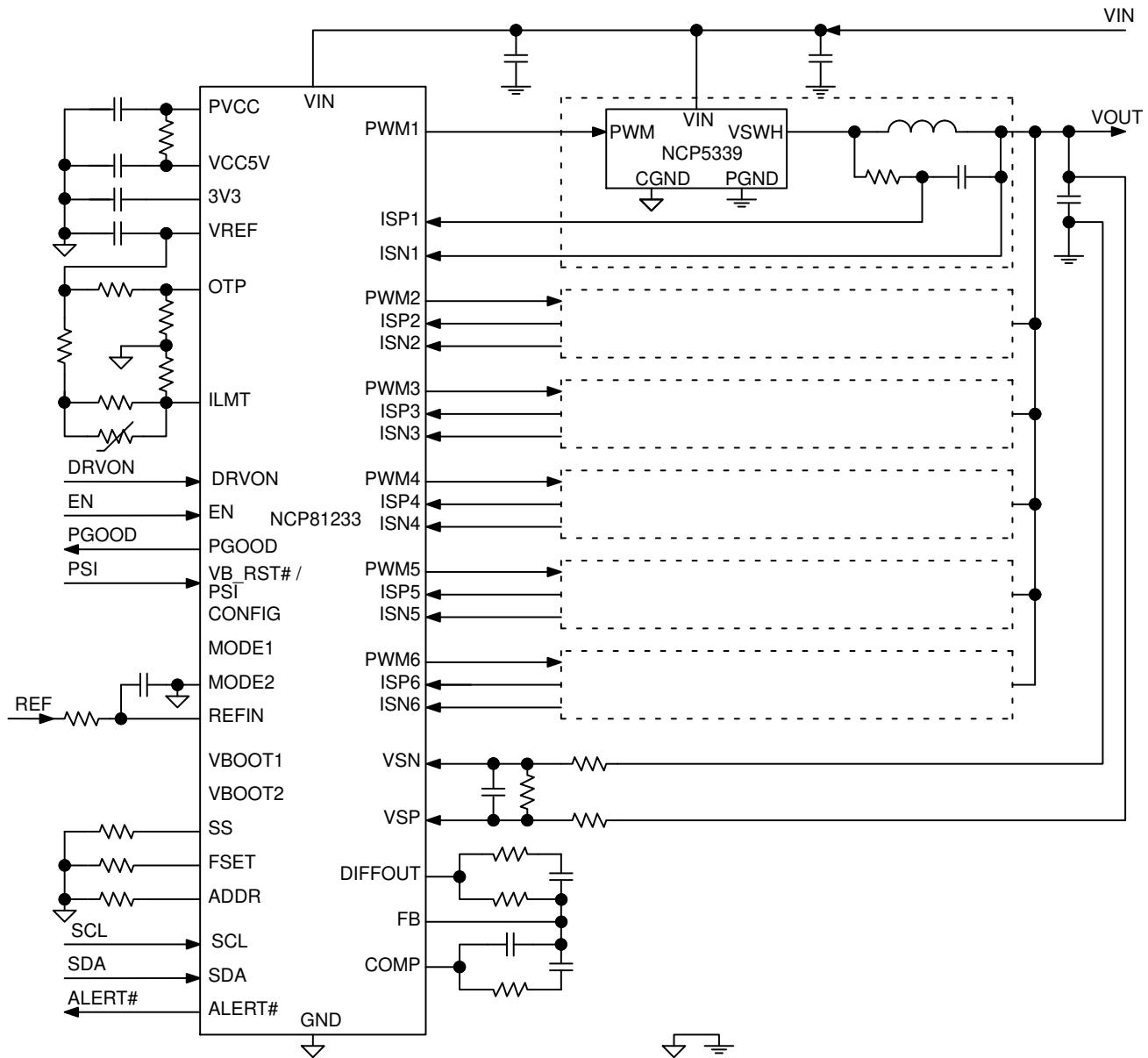
Figure 3. Typical Application Circuit with External Reference Input
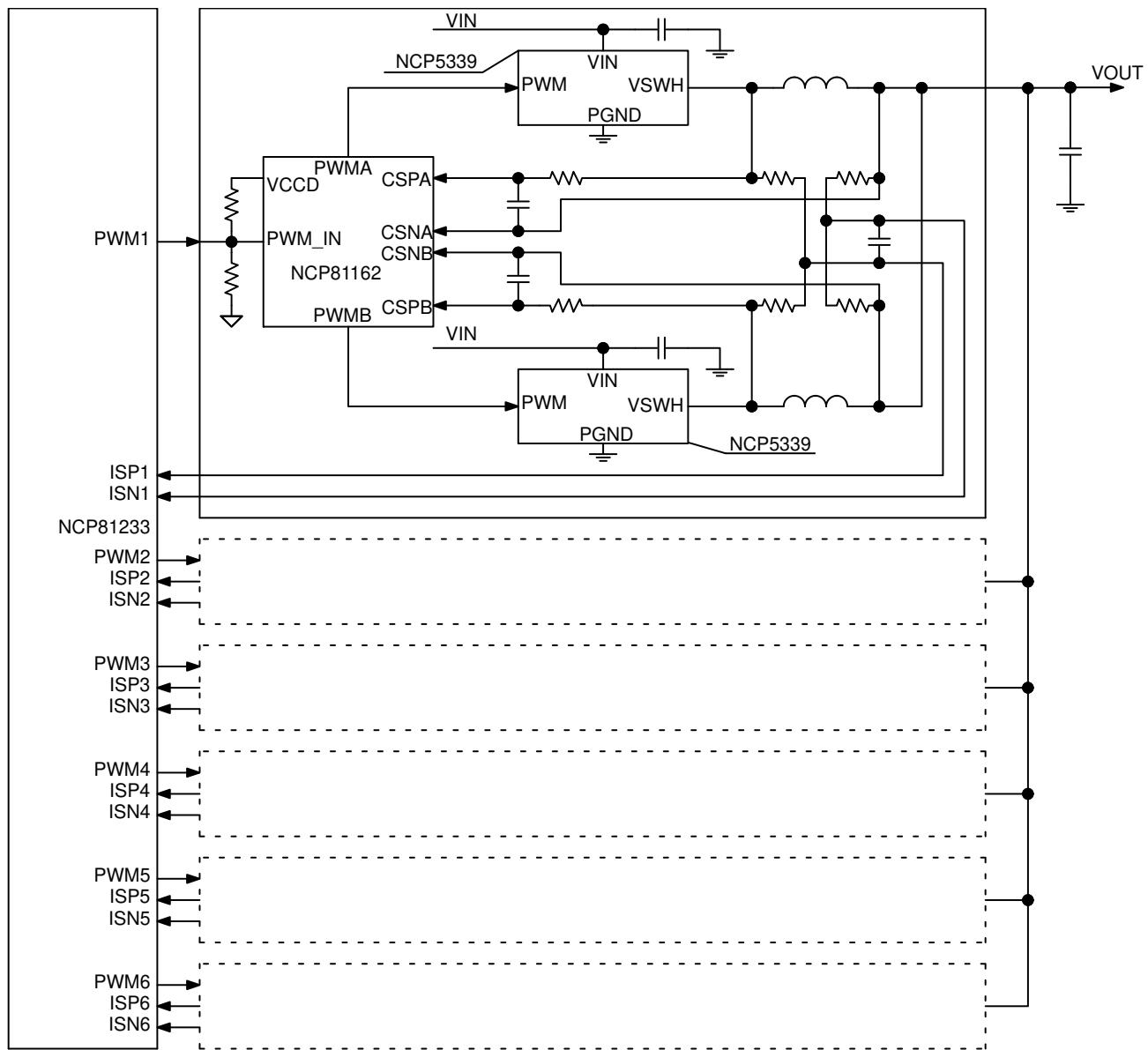
Figure 4. Application Circuit with Phase Doublers

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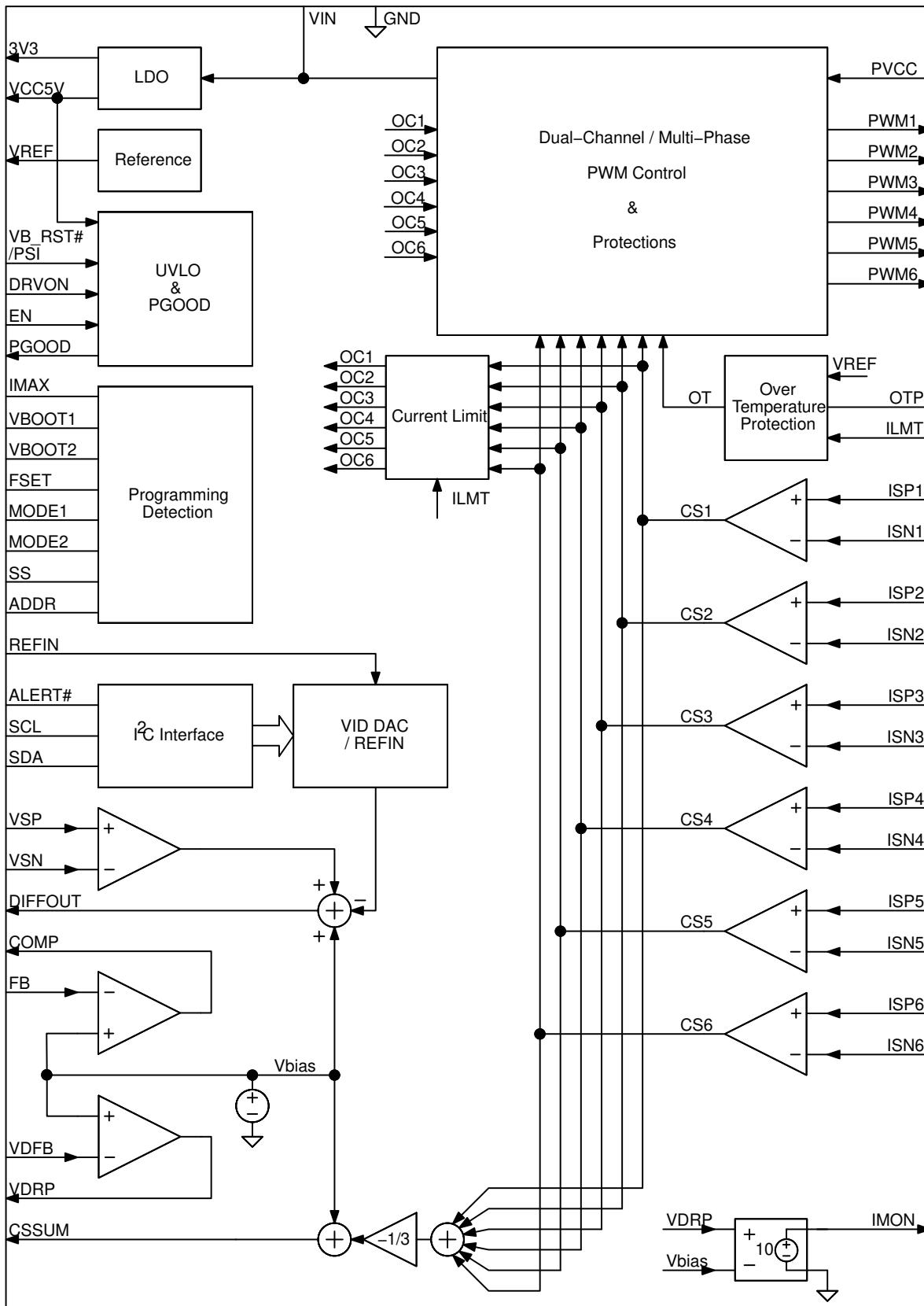
Figure 5. Functional Block Diagram

NCP81233

TABLE 2. MAXIMUM RATINGS

Rating	Symbol	MIN	MAX	Unit
		Value		
Power Supply Voltage to PGND	V_{VIN}		30	V
Supply Voltage VCC5V to GND	V_{VCC5V}	−0.3	6.5	V
VSNx to GND	V_{VSN}	−0.2	0.2	V
Other Pins to GND		−0.3	VCC5 V+0.3	V
Human Body Model (HBM) ESD Rating are (Note 1)	ESD HBM		2500	V
Charge Device Model (CDM) ESD Rating are (Note 1)	ESD CDM		2000	V
Latch up Current: (Note 2)	I_{LU}	−100	100	mA
Operating Junction Temperature Range (Note 3)	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	100	°C
Storage Temperature Range	T_{STG}	−55	150	°C
Thermal Resistance Junction to Top Case(Note 4)	$R_{\Psi JC}$	1.65		°C/W
Thermal Resistance Junction to Board (Note 4)	$R_{\Psi JB}$	3.2		°C/W
Thermal Resistance Junction to Ambient (Note 4)	$R_{\theta JA}$	67.4		°C/W
Power Dissipation (Note 5)	P_D	1.48		W
Moisture Sensitivity Level (Note 6)	MSL	1		–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device is ESD sensitive. Handling precautions are needed to avoid damage or performance degradation.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
4. JEDEC standard JESD 51−7 (1S2P Direct-Attach Method) with 0 LFM. It is for checking junction temperature using external measurement.
5. The maximum power dissipation (PD) is dependent on input voltage, maximum output current and external components selected. Tambient = 25°C, Tjunc_max = 125°C, PD = (Tjunc_max−T_amb)/Theta JA
6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

TABLE 3. ELECTRICAL CHARACTERISTICS
(V_{IN} = 12 V, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J = −40°C to 100°C. unless other noted.)

Characteristics	Test Conditions	Symbol	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
VIN Supply Voltage Range	(Note 7)	V_{IN}	4.5	12	20	V
VCC5V Under-Voltage (UVLO) Threshold	VCC5V falling	V_{CCUV-}	3.7			V
VCC5V OK Threshold	VCC5V rising	V_{CCOK}			4.3	V
VCC5V UVLO Hysteresis		V_{CCHYS}		270		mV
VCC3V Under−Voltage (UVLO) Threshold	VCC3V falling	V_{CC3UV-}	2.6			V
VCC3V OK Threshold	VCC3V rising	V_{CC3OK}			2.9	V
VCC3V UVLO Hysteresis		V_{CC3HYS}		135		mV
VCC5V Regulator						
Output Voltage	6V < VIN < 20V, IVCC5V = 15mA (External),EN = Low	V_{CC}	5.2	5.35	5.5	V
Load Regulation	IVCC5V = 5mA to 25mA (External), EN = Low		−2.0	0.2	2.0	%
Dropout Voltage	VIN = 5V, IVCC5V = 25mA (External), EN = Low	V_{DO_VCC}			200	mV

TABLE 3. ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12 V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = –40°C to 100°C. unless other noted.)

Characteristics	Test Conditions		Symbol	MIN	TYP	MAX	UNITS
VCC3V Regulator							
Output Voltage	IVCC3V = 5 mA (External), EN = Low		V_{3V3}	3.1	3.3	3.5	V
Load Regulation	IVCC3V = 0.5 mA to 10 mA (External), EN = Low			–3.0		3.0	%
SUPPLY CURRENT							
VIN Quiescent Current	EN high, 1–phase only EN high, 6–phase		I_{QVIN}	– –	11 17	20 28	mA mA
VIN Shutdown Current	EN low		I_{sdVIN}	–	5	9	mA
VREF							
VREF Output Voltage	IVREF = 500 µA		V_{VREF}	594	600	606	mV
Load Regulation	IVREF = 0 mA to 2 mA			–1.0		1.0	%
REFIN							
Maximum REFIN Voltage	(Note 7)					1.53	V
REFIN Bias Current	V_{REFIN} = 1.0 V		I_{REFIN}	–100		100	nA
SYSTEM VOLTAG ACCURACY							
System Voltage Accuracy	0.5 V ≤ DAC ≤ 1.52 V Or 0.5 V ≤ REFIN ≤ 1.52 V	–40°C to 85°C		–7		7	mV
		–40°C to 125°C		–10		10	
	0.25 V ≤ DAC ≤ 0.495 V Or 0.25 V ≤ REFIN ≤ 0.495 V	–40°C to 85°C		–8		8	
		–40°C to 125°C		–12		12	
DIFFERENTIAL VOLTAGE-SENSE AMPLIFIER							
VSP Input Voltage Range	(Note 7)			–0.2		1.72	V
VSN Input Voltage Range	(Note 7)			–0.2		0.2	V
DC Gain	VSP–VSN = 0 V to 1.52 V		GAIN_DVA		1.0		V/V
–3dB Gain Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND (Note 7)		BW_DVA		10		MHz
Input Bias Current	VSP = 1.72, VSN = –0.2 V		I_{VS}	–400		400	nA
VOLTAGE ERROR AMPLIFIER							
Open-Loop DC Gain	(Note 7)		$GAIN_{EA}$		80		dB
Unity Gain Bandwidth	(Note 7)		GBW_{EA}		20		MHz
Slew Rate	(Note 7)		SR_{COMP}		20		V/µs
COMP Voltage Swing	I_{COMP}(source) = 2 mA		$V_{maxCOMP}$	3.2	3.4	–	V
	I_{COMP}(sink) = 2 mA	TRBST is Enabled	$V_{minCOMP}$			0.3	V
		TRBST is Disabled		–	1.1		
FB Bias Current	V_{FB} = 1.3V		I_{FB}	–400		400	nA
DIFFERENTIAL CURRENT-SENSE AMPLIFIER							
DC Gain			$GAIN_{CA}$		6		V/V
–3dB Gain Bandwidth	(Note 7)		BW_{CA}		10		MHz
Input Common Mode Voltage Range	(Note 7)			–0.2		Vcc+0.1	V
Differential Input Voltage Range	(Note 7)			–60	–	60	mV
Input Bias Current	ISP, ISN = 1.0 V		I_{CS}	–100		100	nA

TABLE 3. ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12 V, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J = −40°C to 100°C. unless other noted.)

Characteristics	Test Conditions	Symbol	MIN	TYP	MAX	UNITS
CURRENT SUMMING AMPLIFIER						
DC Gain	From (ISPn – ISNn) to (CSSUM – Vbias)	$GAIN_{CSSUM}$		−2		V/V
−3dB Gain Bandwidth	CL = 10 pF to GND, RL = 10 kΩ to GND (Note 7)	BW_{CSSUM}		5		MHz
CSSUM Output Offset	All (ISPn – ISNn) = 0 V (Note 7)	$V_{osCSSUM}$	−7	0	7	mV
Maximum CSSUM Output Voltage	I_{CSSUM}(source) = 1 mA (Note 7)			2.02		V
Minimum CSSUM Output Voltage	I_{CSSUM}(sink) = 1 mA (Note 7)			0.56		V
DROOP AMPLIFIER						
Open-Loop DC Gain	(Note 7)	$GAIN_{DA}$		80		dB
Unity Gain Bandwidth	(Note 7)	GBW_{DA}		10		MHz
Input Offset Voltage	(Note 7)	V_{osDA}	−2.5		2.5	mV
Input Bias Current	V_{DFB} = 1.3V	I_{DFB}	−200		200	nA
Maximum VDRP Output Voltage	I_{VDRP}(source) = 2 mA (Note 7)			3.0		V
Minimum VDRP Output Voltage	I_{VDRP}(sink) = 2 mA (Note 7)			1.0		V
IMON AMPLIFIER						
DC Gain		$GAIN_{IMON}$		10		V/V
−3dB Gain Bandwidth	(Note 7)	BW_{IMON}		2		MHz
Input Offset Voltage	(Note 7)	V_{osIMON}	−2		2	mV
Output Impedance	(Note 7)	R_{IMON}		20		kΩ
IMAX						
SourceCurrent	V_{IMAX} = 1V		47.5	50	52.5	μA
I²C INTERFACE ADDRESS						
Address	Float Short to GND 2.7k 5.1k 8.2k 13k 20k 33k	−	−	1110000 1110001 1110010 1110011 1110100 1110101 1110110 1110111	−	−

TABLE 3. ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12 V, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J = –40°C to 100°C. unless other noted.)

Characteristics	Test Conditions	Symbol	MIN	TYP	MAX	UNITS
VBOOT CODE						
VBOOT1	Float Short to GND 2.7 k 5.1 k 8.2 k 13 k 20 k 33 k	–	–	000XXX 001XXX 010XXX 011XXX 100XXX 101XXX 110XXX 111XXX	–	–
VBOOT2	Float Short to GND 2.7 k 5.1 k 8.2 k 13 k 20 k 33 k	–	–	XXX000 XXX001 XXX010 XXX011 XXX100 XXX101 XXX110 XXX111	–	–
Source Current		I_{VBT}	45	50	55	μA
SWITCHING FREQUENCY						
Switching Frequency	2.7 k 5.1 k Float 8.2 k Short to GND 13 k 20 k 33 k	F_{SW}	180 270 360 450 540 720 900 1080	200 300 400 500 600 800 1000 1200	220 330 440 550 660 880 1100 1320	kHz
Source Current		I_{FS}	45	50	55	μA
SYSTEM RESET TIME						
System Reset Time	Measured from EN to start of soft start.	T_{RST}		2.0		ms
SOFT START						
Soft–Start Slew Rate	Float	SSSR		0.125		mV/us
	33 k			0.25		
	20 k			0.5		
	13 k			1.0		
	8.2 k			2.0		
	5.1 k			4.0		
	2.7 k			8.0		
	Short to GND			16		
Source Current		I_{SS}	45	50	55	μA
DVID						
DVID Slew Rate	000	SR		0.125		mV/us
	001			0.25		
	010			0.5		
	011			1.0		
	100			2.0		
	101			4.0		
	110			8.0		
	111			16		
I^{2}C INTERFACE						
Logic High Input Voltage		$V_{IH(SDA, SCL)}$	1.5			V

TABLE 3. ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12 V, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J = −40°C to 100°C. unless other noted.)

Characteristics	Test Conditions		Symbol	MIN	TYP	MAX	UNITS
I²C INTERFACE							
Logic Low Input Voltage			$V_{IL(SDA, SCL)}$			0.7	V
Hysteresis					350		mV
SDA Output Low Voltage	I_{SDA} = −4 mA		V_{OL}			0.3	V
Input Current			I_{IH}; I_{IL}	−1.0		1.0	μA
Input Capacitance	(Note 7)		$C_{SCL, SDA}$		5.0		pF
Clock Frequency	(Note 7)		f_{SCL}			400	kHz
SCL Falling Edge to SDA Valid Time	(Note 7)					1.0	μs
ALERT# Low Voltage	I_{ALERT}= −4 mA		V_{LALERT}			0.3	V
ALERT# Leakage Current	ALERT# = 5 V		$I_{lkgALERT}$			1.0	μA
PGOOD							
PGOOD Startup Delay	Measured from end of Soft Start to PGOOD assertion (Note 7)		T_{d_PGOOD}		100		μs
PGOOD Shutdown Delay	Measured from EN to PGOOD de-assertion				250		ns
PGOOD Low Voltage	I_{PGOOD}= −4 mA		V_{IPGOOD}			0.3	V
PGOOD Leakage Current	PGOOD = 5 V		$I_{lkgPGOOD}$			1.0	μA
PROTECTIONS							
Current Limit Threshold	Measured from ILIMT to GND	ISP–ISN = 50 mV	V_{OCTH}	285	300	315	mV
		ISP–ISN = 2 0 mV		110	120	130	
Over Current Protection (OCP) Debounce Time	(Note 7)				8 Cycles		us
Under Voltage Threshold Below DAC	VSP falling		V_{UVTH}	250	300	350	mV
Under Voltage Protection (UVP) Hysteresis			V_{UVHYS}		25		mV
Under-voltage Debounce Time	(Note 7)				5		μs
Shutdown Time in Hiccup Mode	UVP (Note 7) OCP (Note 7) OTP (Note 7)				30 40 20		ms
Absolute Over Voltage Threshold During Soft-Start	VSP-GND			2.0	2.1	2.2	V
Absolute Over Voltage Threshold Hysteresis					−25		mV
Over Voltage Threshold Above DAC	VSP rising		V_{OVTH}	175	200	225	mV
Over Voltage Protection Hysteresis	VSP falling		V_{OVHYS}		−25		mV
Over Voltage Debounce Time	VSP rising to GH low				1.0		us
Offset Voltage of OTP Comparator	VILMT = 200 mV		V_{OS_OTP}	−2		2	mV
OTP Source Current			I_{OTP}	9	10	11	μA
OTP Debounce Time	(Note 7)				140		ns
Thermal Shutdown (TSD) Threshold	(Note 7)		T_{sd}	140	150		°C
Recovery Temperature Threshold	(Note 7)		T_{rec}		125		°C
Thermal Shutdown (TSD) Debounce Time	(Note 7)				120		ns

TABLE 3. ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12 V, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J = −40°C to 100°C. unless other noted.)

Characteristics	Test Conditions	Symbol	MIN	TYP	MAX	UNITS
ENABLE						
EN Operation Voltage Range			0		3.5	V
EN ON Threshold		V_{EN_TH}	0.7	0.8	0.85	V
Hysteresis Source Current	VCC5V is OK	I_{EN_HYS}	25	30	35	μA
DRVON						
DRVON Operation Voltage Range			0		2.0	V
DRVON ON Threshold		V_{DRVON_TH}	0.75	0.8	0.85	V
Hysteresis Source Current	VCC5V is OK	I_{DRVON_HYS}	25	30	35	μA
VB_RST# and PSI						
High Threshold		$V_{highRST}$	1.5	–	–	V
Low Threshold		V_{lowRST}	–	–	0.7	V
Hysteresis		V_{hysRST}		350		mV
Input Bias Current	External 1 K pull−up to 3.3 V	$I_{biasRST}$	–	–	1.0	μA
PWM MODULATION						
Minimum On Time	(Note 7)	T_{on_min}			50	ns
Minimum Off Time	(Note 7)	T_{off_min}	160			ns
0% Duty Cycle	COMP voltage when the PWM outputs remain Lo (Note 7)			1.3		V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI, Vin = 12.0 V (Note 7)			2.5		V
Ramp Feed−forward Voltage Range	(Note 7)		4.5		20	V
PWM OUTPUT						
PWM Output High Voltage	Isourse = 0.5 mA	V_{PWM_H}	V_{CC}−0.2			V
PWM Output Low Voltage	Isink = 0.5 mA	V_{PWM_L}			0.2	V
Rise and Fall Times	CL (PCB) = 50 pF, measured between 10% & 90% of V_{CC} (Note 7)			10		ns
Leakage Current in Hi-Z Stage		I_{LK_PWM}	−1.0		1.0	μA

7. Guaranteed by design, not tested in production.

Table 4. RESISTOR OPTIONS FOR FUNCTION PROGRAMMING

Resistance Range (kW)			Resistor Options (kW)				
MIN	TYP	MAX	±5%	±1%			
2.565	2.7	2.835	2.7	2.61	2.67	2.74	2.80
4.845	5.1	5.355	5.1	4.87	4.99	5.11	5.23
7.79	8.2	8.61	8.2	7.87	8.06	8.25	8.45
12.35	13	13.65	13	12.4	12.7	13	13.3
19	20	21	20	19.1	19.6	20	20.5
31.35	33	34.65	33	31.6	32.4	33.2	34

TABLE 5. VBOOT CODES

VBOOT1			VBOOT2			Voltage(V)	HEX		VBOOT1			VBOOT2			Voltage(V)	HEX
0	0	0	0	0	0	0.6	00		1	0	0	0	0	0	0.92	20
0	0	0	0	0	1	0.61	01		1	0	0	0	0	1	0.93	21
0	0	0	0	1	0	0.62	02		1	0	0	0	1	0	0.94	22
0	0	0	0	1	1	0.63	03		1	0	0	0	1	1	0.95	23
0	0	0	1	0	0	0.64	04		1	0	0	1	0	0	0.96	24
0	0	0	1	0	1	0.65	05		1	0	0	1	0	1	0.97	25
0	0	0	1	1	0	0.66	06		1	0	0	1	1	0	0.98	26
0	0	0	1	1	1	0.67	07		1	0	0	1	1	1	0.99	27
0	0	1	0	0	0	0.68	08		1	0	1	0	0	0	1	28
0	0	1	0	0	1	0.69	09		1	0	1	0	0	1	1.01	29
0	0	1	0	1	0	0.7	0A		1	0	1	0	1	0	1.02	2A
0	0	1	0	1	1	0.71	0B		1	0	1	0	1	1	1.03	2B
0	0	1	1	0	0	0.72	0C		1	0	1	1	0	0	1.04	2C
0	0	1	1	0	1	0.73	0D		1	0	1	1	0	1	1.05	2D
0	0	1	1	1	0	0.74	0E		1	0	1	1	1	0	1.06	2E
0	0	1	1	1	1	0.75	0F		1	0	1	1	1	1	1.07	2F
0	1	0	0	0	0	0.76	10		1	1	0	0	0	0	1.08	30
0	1	0	0	0	1	0.77	11		1	1	0	0	0	1	1.09	31
0	1	0	0	1	0	0.78	12		1	1	0	0	1	0	1.1	32
0	1	0	0	1	1	0.79	13		1	1	0	0	1	1	1.11	33
0	1	0	1	0	0	0.8	14		1	1	0	1	0	0	1.12	34
0	1	0	1	0	1	0.81	15		1	1	0	1	0	1	1.13	35
0	1	0	1	1	0	0.82	16		1	1	0	1	1	0	1.14	36
0	1	0	1	1	1	0.83	17		1	1	0	1	1	1	1.15	37
0	1	1	0	0	0	0.84	18		1	1	1	0	0	0	1.16	38
0	1	1	0	0	1	0.85	19		1	1	1	0	0	1	1.17	39
0	1	1	0	1	0	0.86	1A		1	1	1	0	1	0	1.18	3A
0	1	1	0	1	1	0.87	1B		1	1	1	0	1	1	1.19	3B
0	1	1	1	0	0	0.88	1C		1	1	1	1	0	0	1.2	3C
0	1	1	1	0	1	0.89	1D		1	1	1	1	0	1	1.21	3D
0	1	1	1	1	0	0.9	1E		1	1	1	1	1	0	1.22	3E
0	1	1	1	1	1	0.91	1F		1	1	1	1	1	1	1.23	3F

TABLE 6. VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	OFF	00
0	0	0	0	0	0	0	1	0.25000	01
0	0	0	0	0	0	1	0	0.25500	02
0	0	0	0	0	0	1	1	0.26000	03
0	0	0	0	0	1	0	0	0.26500	04
0	0	0	0	0	1	0	1	0.27000	05
0	0	0	0	0	1	1	0	0.27500	06
0	0	0	0	0	1	1	1	0.28000	07
0	0	0	0	1	0	0	0	0.28500	08
0	0	0	0	1	0	0	1	0.29000	09
0	0	0	0	1	0	1	0	0.29500	0A
0	0	0	0	1	0	1	1	0.30000	0B
0	0	0	0	1	1	0	0	0.30500	0C
0	0	0	0	1	1	0	1	0.31000	0D
0	0	0	0	1	1	1	0	0.31500	0E
0	0	0	0	1	1	1	1	0.32000	0F
0	0	0	1	0	0	0	0	0.32500	10
0	0	0	1	0	0	0	1	0.33000	11
0	0	0	1	0	0	1	0	0.33500	12
0	0	0	1	0	0	1	1	0.34000	13
0	0	0	1	0	1	0	0	0.34500	14
0	0	0	1	0	1	0	1	0.35000	15
0	0	0	1	0	1	1	0	0.35500	16
0	0	0	1	0	1	1	1	0.36000	17
0	0	0	1	1	0	0	0	0.36500	18
0	0	0	1	1	0	0	1	0.37000	19
0	0	0	1	1	0	1	0	0.37500	1A
0	0	0	1	1	0	1	1	0.38000	1B
0	0	0	1	1	1	0	0	0.38500	1C
0	0	0	1	1	1	0	1	0.39000	1D
0	0	0	1	1	1	1	0	0.39500	1E
0	0	0	1	1	1	1	1	0.40000	1F
0	0	1	0	0	0	0	0	0.40500	20
0	0	1	0	0	0	0	1	0.41000	21

TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	1	0	0	0	1	0	0.41500	22
0	0	1	0	0	0	1	1	0.42000	23
0	0	1	0	0	1	0	0	0.42500	24
0	0	1	0	0	1	0	1	0.43000	25
0	0	1	0	0	1	1	0	0.43500	26
0	0	1	0	0	1	1	1	0.44000	27
0	0	1	0	1	0	0	0	0.44500	28
0	0	1	0	1	0	0	1	0.45000	29
0	0	1	0	1	0	1	0	0.45500	2A
0	0	1	0	1	0	1	1	0.46000	2B
0	0	1	0	1	1	0	0	0.46500	2C
0	0	1	0	1	1	0	1	0.47000	2D
0	0	1	0	1	1	1	0	0.47500	2E
0	0	1	0	1	1	1	1	0.48000	2F
0	0	1	1	0	0	0	0	0.48500	30
0	0	1	1	0	0	0	1	0.49000	31
0	0	1	1	0	0	1	0	0.49500	32
0	0	1	1	0	0	1	1	0.50000	33
0	0	1	1	0	1	0	0	0.50500	34
0	0	1	1	0	1	0	1	0.51000	35
0	0	1	1	0	1	1	0	0.51500	36
0	0	1	1	0	1	1	1	0.52000	37
0	0	1	1	1	0	0	0	0.52500	38
0	0	1	1	1	0	0	1	0.53000	39
0	0	1	1	1	0	1	0	0.53500	3A
0	0	1	1	1	0	1	1	0.54000	3B
0	0	1	1	1	1	0	0	0.54500	3C
0	0	1	1	1	1	0	1	0.55000	3D
0	0	1	1	1	1	1	0	0.55500	3E
0	0	1	1	1	1	1	1	0.56000	3F
0	1	0	0	0	0	0	0	0.56500	40
0	1	0	0	0	0	0	1	0.57000	41
0	1	0	0	0	0	1	0	0.57500	42
0	1	0	0	0	0	1	1	0.58000	43

TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	0	0	0	1	0	0	0.58500	44
0	1	0	0	0	1	0	1	0.59000	45
0	1	0	0	0	1	1	0	0.59500	46
0	1	0	0	0	1	1	1	0.60000	47
0	1	0	0	1	0	0	0	0.60500	48
0	1	0	0	1	0	0	1	0.61000	49
0	1	0	0	1	0	1	0	0.61500	4A
0	1	0	0	1	0	1	1	0.62000	4B
0	1	0	0	1	1	0	0	0.62500	4C
0	1	0	0	1	1	0	1	0.63000	4D
0	1	0	0	1	1	1	0	0.63500	4E
0	1	0	0	1	1	1	1	0.64000	4F
0	1	0	1	0	0	0	0	0.64500	50
0	1	0	1	0	0	0	1	0.65000	51
0	1	0	1	0	0	1	0	0.65500	52
0	1	0	1	0	0	1	1	0.66000	53
0	1	0	1	0	1	0	0	0.66500	54
0	1	0	1	0	1	0	1	0.67000	55
0	1	0	1	0	1	1	0	0.67500	56
0	1	0	1	0	1	1	1	0.68000	57
0	1	0	1	1	0	0	0	0.68500	58
0	1	0	1	1	0	0	1	0.69000	59
0	1	0	1	1	0	1	0	0.69500	5A
0	1	0	1	1	0	1	1	0.70000	5B
0	1	0	1	1	1	0	0	0.70500	5C
0	1	0	1	1	1	0	1	0.71000	5D
0	1	0	1	1	1	1	0	0.71500	5E
0	1	0	1	1	1	1	1	0.72000	5F
0	1	1	0	0	0	0	0	0.72500	60
0	1	1	0	0	0	0	1	0.73000	61
0	1	1	0	0	0	1	0	0.73500	62
0	1	1	0	0	0	1	1	0.74000	63
0	1	1	0	0	1	0	0	0.74500	64
0	1	1	0	0	1	0	1	0.75000	65

TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	1	0	0	1	1	0	0.75500	66
0	1	1	0	0	1	1	1	0.76000	67
0	1	1	0	1	0	0	0	0.76500	68
0	1	1	0	1	0	0	1	0.77000	69
0	1	1	0	1	0	1	0	0.77500	6A
0	1	1	0	1	0	1	1	0.78000	6B
0	1	1	0	1	1	0	0	0.78500	6C
0	1	1	0	1	1	0	1	0.79000	6D
0	1	1	0	1	1	1	0	0.79500	6E
0	1	1	0	1	1	1	1	0.80000	6F
0	1	1	1	0	0	0	0	0.80500	70
0	1	1	1	0	0	0	1	0.81000	71
0	1	1	1	0	0	1	0	0.81500	72
0	1	1	1	0	0	1	1	0.82000	73
0	1	1	1	0	1	0	0	0.82500	74
0	1	1	1	0	1	0	1	0.83000	75
0	1	1	1	0	1	1	0	0.83500	76
0	1	1	1	0	1	1	1	0.84000	77
0	1	1	1	1	0	0	0	0.84500	78
0	1	1	1	1	0	0	1	0.85000	79
0	1	1	1	1	0	1	0	0.85500	7A
0	1	1	1	1	0	1	1	0.86000	7B
0	1	1	1	1	1	0	0	0.86500	7C
0	1	1	1	1	1	0	1	0.87000	7D
0	1	1	1	1	1	1	0	0.87500	7E
0	1	1	1	1	1	1	1	0.88000	7F
1	0	0	0	0	0	0	0	0.88500	80
1	0	0	0	0	0	0	1	0.89000	81
1	0	0	0	0	0	1	0	0.89500	82
1	0	0	0	0	0	1	1	0.90000	83
1	0	0	0	0	1	0	0	0.90500	84
1	0	0	0	0	1	0	1	0.91000	85
1	0	0	0	0	1	1	0	0.91500	86
1	0	0	0	0	1	1	1	0.92000	87

TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	0	0	1	0	0	0	0.92500	88
1	0	0	0	1	0	0	1	0.93000	89
1	0	0	0	1	0	1	0	0.93500	8A
1	0	0	0	1	0	1	1	0.94000	8B
1	0	0	0	1	1	0	0	0.94500	8C
1	0	0	0	1	1	0	1	0.95000	8D
1	0	0	0	1	1	1	0	0.95500	8E
1	0	0	0	1	1	1	1	0.96000	8F
1	0	0	1	0	0	0	0	0.96500	90
1	0	0	1	0	0	0	1	0.97000	91
1	0	0	1	0	0	1	0	0.97500	92
1	0	0	1	0	0	1	1	0.98000	93
1	0	0	1	0	1	0	0	0.98500	94
1	0	0	1	0	1	0	1	0.99000	95
1	0	0	1	0	1	1	0	0.99500	96
1	0	0	1	0	1	1	1	1.00000	97
1	0	0	1	1	0	0	0	1.00500	98
1	0	0	1	1	0	0	1	1.01000	99
1	0	0	1	1	0	1	0	1.01500	9A
1	0	0	1	1	0	1	1	1.02000	9B
1	0	0	1	1	1	0	0	1.02500	9C
1	0	0	1	1	1	0	1	1.03000	9D
1	0	0	1	1	1	1	0	1.03500	9E
1	0	0	1	1	1	1	1	1.04000	9F
1	0	1	0	0	0	0	0	1.04500	A0
1	0	1	0	0	0	0	1	1.05000	A1
1	0	1	0	0	0	1	0	1.05500	A2
1	0	1	0	0	0	1	1	1.06000	A3
1	0	1	0	0	1	0	0	1.06500	A4
1	0	1	0	0	1	0	1	1.07000	A5
1	0	1	0	0	1	1	0	1.07500	A6
1	0	1	0	0	1	1	1	1.08000	A7
1	0	1	0	1	0	0	0	1.08500	A8
1	0	1	0	1	0	0	1	1.09000	A9

TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	1	0	1	0	1	0	1.09500	AA
1	0	1	0	1	0	1	1	1.10000	AB
1	0	1	0	1	1	0	0	1.10500	AC
1	0	1	0	1	1	0	1	1.11000	AD
1	0	1	0	1	1	1	0	1.11500	AE
1	0	1	0	1	1	1	1	1.12000	AF
1	0	1	1	0	0	0	0	1.12500	B0
1	0	1	1	0	0	0	1	1.13000	B1
1	0	1	1	0	0	1	0	1.13500	B2
1	0	1	1	0	0	1	1	1.14000	B3
1	0	1	1	0	1	0	0	1.14500	B4
1	0	1	1	0	1	0	1	1.15000	B5
1	0	1	1	0	1	1	0	1.15500	B6
1	0	1	1	0	1	1	1	1.16000	B7
1	0	1	1	1	0	0	0	1.16500	B8
1	0	1	1	1	0	0	1	1.17000	B9
1	0	1	1	1	0	1	0	1.17500	BA
1	0	1	1	1	0	1	1	1.18000	BB
1	0	1	1	1	1	0	0	1.18500	BC
1	0	1	1	1	1	0	1	1.19000	BD
1	0	1	1	1	1	1	0	1.19500	BE
1	0	1	1	1	1	1	1	1.20000	BF
1	1	0	0	0	0	0	0	1.20500	C0
1	1	0	0	0	0	0	1	1.21000	C1
1	1	0	0	0	0	1	0	1.21500	C2
1	1	0	0	0	0	1	1	1.22000	C3
1	1	0	0	0	1	0	0	1.22500	C4
1	1	0	0	0	1	0	1	1.23000	C5
1	1	0	0	0	1	1	0	1.23500	C6
1	1	0	0	0	1	1	1	1.24000	C7
1	1	0	0	1	0	0	0	1.24500	C8
1	1	0	0	1	0	0	1	1.25000	C9
1	1	0	0	1	0	1	0	1.25500	CA
1	1	0	0	1	0	1	1	1.26000	CB

TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	0	0	1	1	0	0	1.26500	CC
1	1	0	0	1	1	0	1	1.27000	CD
1	1	0	0	1	1	1	0	1.27500	CE
1	1	0	0	1	1	1	1	1.28000	CF
1	1	0	1	0	0	0	0	1.28500	D0
1	1	0	1	0	0	0	1	1.29000	D1
1	1	0	1	0	0	1	0	1.29500	D2
1	1	0	1	0	0	1	1	1.30000	D3
1	1	0	1	0	1	0	0	1.30500	D4
1	1	0	1	0	1	0	1	1.31000	D5
1	1	0	1	0	1	1	0	1.31500	D6
1	1	0	1	0	1	1	1	1.32000	D7
1	1	0	1	1	0	0	0	1.32500	D8
1	1	0	1	1	0	0	1	1.33000	D9
1	1	0	1	1	0	1	0	1.33500	DA
1	1	0	1	1	0	1	1	1.34000	DB
1	1	0	1	1	1	0	0	1.34500	DC
1	1	0	1	1	1	0	1	1.35000	DD
1	1	0	1	1	1	1	0	1.35500	DE
1	1	0	1	1	1	1	1	1.36000	DF
1	1	1	0	0	0	0	0	1.36500	E0
1	1	1	0	0	0	0	1	1.37000	E1
1	1	1	0	0	0	1	0	1.37500	E2
1	1	1	0	0	0	1	1	1.38000	E3
1	1	1	0	0	1	0	0	1.38500	E4
1	1	1	0	0	1	0	1	1.39000	E5
1	1	1	0	0	1	1	0	1.39500	E6
1	1	1	0	0	1	1	1	1.40000	E7
1	1	1	0	1	0	0	0	1.40500	E8
1	1	1	0	1	0	0	1	1.41000	E9
1	1	1	0	1	0	1	0	1.41500	EA
1	1	1	0	1	0	1	1	1.42000	EB
1	1	1	0	1	1	0	0	1.42500	EC
1	1	1	0	1	1	0	1	1.43000	ED

TABLE 6. VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	1	0	1	1	1	0	1.43500	EE
1	1	1	0	1	1	1	1	1.44000	EF
1	1	1	1	0	0	0	0	1.44500	F0
1	1	1	1	0	0	0	1	1.45000	F1
1	1	1	1	0	0	1	0	1.45500	F2
1	1	1	1	0	0	1	1	1.46000	F3
1	1	1	1	0	1	0	0	1.46500	F4
1	1	1	1	0	1	0	1	1.47000	F5
1	1	1	1	0	1	1	0	1.47500	F6
1	1	1	1	0	1	1	1	1.48000	F7
1	1	1	1	1	0	0	0	1.48500	F8
1	1	1	1	1	0	0	1	1.49000	F9
1	1	1	1	1	0	1	0	1.49500	FA
1	1	1	1	1	0	1	1	1.50000	FB
1	1	1	1	1	1	0	0	1.50500	FC
1	1	1	1	1	1	0	1	1.51000	FD
1	1	1	1	1	1	1	0	1.51500	FE
1	1	1	1	1	1	1	1	1.52000	FF

TABLE 7. STANDARD COMMAND CODES (PART 1)

Command Code	R/W	Default	Description	# Bytes	Comment			
0x01	R/W	0x80	Operation	1	Operation command turns the device on or off in conjunction with EN signal.			
					Bit	**Default**	**R/W**	**Comment**
					7	1	R/W	0: Immediate Off; 1: On (slew rate set by soft-start) Default
					6	0	R	(Reserved for future use.)
					5:2	0000	R	Margin Operation. (Reserved for future use.)
					1:0	00	R	(Reserved for future use.)
0x02	R/W	0x17	ON_OFF_Config	1	Configures how the controller is turned on and off.			
					Bit	**Default**	**R/W**	**Comment**
					7:5	000	R	(Reserved for future use.)
					4	1	R	Switching starts when commanded by the EN Pin and the Operation Command, as set in Bits 3:0
					3	0	R/W	0: Unit ignores OPERATION commands over the I^{2}C Interface 1: Unit responds to OPERATION command, power up may also depend upon EN input, as described in Bit 2
					2	1	R	0: Unit ignores EN pin 1: Unit responds EN pin, power up may also depend upon the Operation Register, as described for Bit 3
					1	1	R	EN Pin polarity 0 = Active Low 1 = Active High
					0	1	R	1: When the controller is disabled it will immediately turn off (as set in the Operation Command)
0x03	W	NA	Clear_Faults	0	Writing any value to this command code will clear all Status Bits immediately. The ALERT# is deasserted on this command. If the fault is still present the fault bit shall immediately be asserted again. This command is write only. There is no data byte for this command.			
0x19	R	0xB0	Capability	1	This command allows the host to get some information on the I^{2}C device.			
					Bit	**Default**	**R/W**	**Comment**
					7	1	R	PEC (Packet Error Checking is supported)
					6:5	01	R	Supported maximum bus speed is 400 kHz
					4	1	R	NCP81233 has an ALERT# pin and Alert Response Address (ARA) protocol is supported
					3:0	0000	R	(Reserved for future use.)

TABLE 7. STANDARD COMMAND CODES (PART 1) (continued)

Command Code	R/W	Default	Description	# Bytes	Comment
0x20	R	0x20	Vout_Mode	1	The NCP81233 supports VID mode for programming the output voltage.
0x21	R/W	0x0000	Vout_Command	2	Sets the output voltage using VID in low byte.
0x24	R/W	0x00FF	Vout_Max	2	Sets maximum output voltage (VID data format). (Reserved for future use.)
0xA4	R/W	0x0000	Vout_Min	2	Sets minimum output voltage (VID data format). (Reserved for future use.)
0x60	R/W	0x0000	TON_DELAY	2	Sets the delay time, in ms, from the end of system reset until the output voltage starts to rise. The lowest 4 bits of the high byte is valid, i.e. 0x0000 = 0ms 0x0100 = 1ms 0x0200 = 2ms … 0x0F00 = 15ms

Command Code	R/W	Default	Description	# Bytes			
0x78	R	0x00	STATUS BYTE	1	**Bit**	**Name**	**Description**
					7	BUSY	A fault was declared because the NCP81233 was busy and unable to respond
					6	OFF	This bit is set whenever the NCP81233 is not switching
					5	VOUT_OV	This bit gets set whenever the NCP81233 goes into OVP (Abs OVP and/or Normal OVP) mode.
					4	IOUT_OC	This bit gets set whenever the NCP81233 turns off due to an over current event.
					3	VIN_UV	Not supported.
					2	OT	This bit gets set whenever the NCP81233 turns off due to an over temperature event.
					1	CML	This bit gets set whenever a communications or logic fault has occurred.
					0	None of the Above	A fault has occurred which is not one of the above.