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Nuvoton
SMBus GPIO Controller

NCT5605Y

Revision: 1.0 Date: Nov, 2009

NCT5605Y Datasheet Revision History

| | PAGES | DATES | VERSION | WEB VERSION | MAIN CONTENTS |
|---|-------|---------|---------|-------------|------------------------------|
| 1 | N.A. | Nov./09 | 1.0 | | Initial Version for customer |
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1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

NCT5605Y SMBus™ Address is:

| | | | | | | | |
|---|---|---|---|----|----|----|-----|
| 0 | 0 | 1 | 1 | A2 | A1 | A0 | R/W |
|---|---|---|---|----|----|----|-----|

NCT5605Y also provides an interrupt to inform system that a transition occurs on general purpose input pins. By NCT5605Y, flashing LED output and beep function are also supported.

2. FEATURES

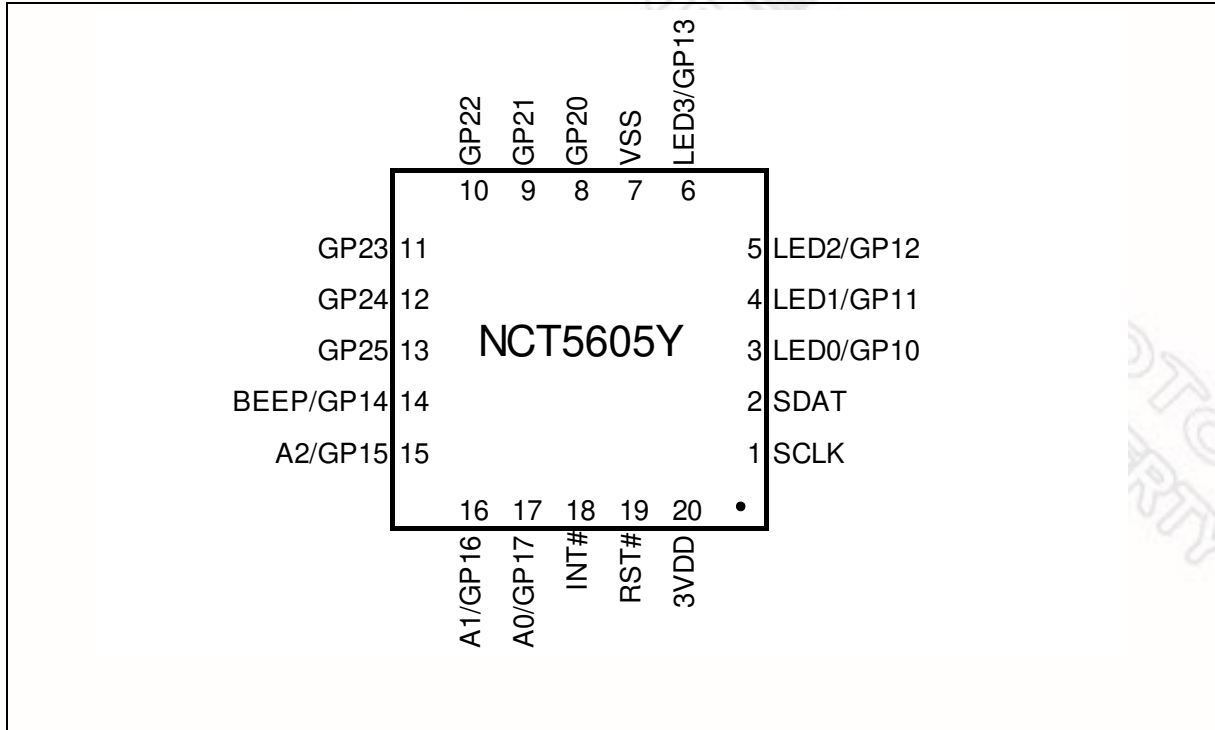
2.1 General Features

- SMBus™ Compliance with 3.3V Voltage Levels
- 14pins Flexible GPIO Support
- Interrupt Notification Support for System Event Occurs
- Support General Purpose Output Setting for Level or Pulse Mode
- Support Interrupt Output Setting for Level or Pulse mode
- Support Internal Power-on Reset or External RST# Pin Reset.
- Support Flashing LED Output
- Support PC Beep Output
- Chip Power down mode support
- 20-QFN Halogen free package (RoHS Compliant)

2.2 Key Specifications

- Supply Voltage is 3.3V
- Operating Supply Current is 150 uA typ.
- Operating Temperature is from 0 °C to 70 °C

3. PIN CONFIGURATION



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4. PIN DESCRIPTION

| | |
|-----------------------|---|
| IN _{ts} | TTL level Schmitt-trigger input pin |
| I/OD _{12ts} | TTL level bi-directional pin open drain output with 12 mA sink capability and schmitt-trigger level input |
| I/O _{12t} | TTL level bi-directional pin bi-directional output with 12 mA source-sink capability |
| I/O(D) _{16t} | TTL level bi-directional pin bi-directional (or open drain) output with 16 mA (source-) sink capability |
| I/O(D) _{12t} | TTL level bi-directional pin bi-directional (or open drain) output with 12 mA (source-) sink capability |
| OD ₁₂ | Open drain output pin with 12 mA sink capability |

| PIN | SYMBOL | I/O | FUNCTION |
|-----|-----------|-----------------------|--|
| 1 | SCL | IN _{ts} | SMBus Clock. |
| 2 | SDA | I/OD _{12ts} | SMBus bi-directional Data. |
| 3 | GP10/LED0 | I/O(D) _{16t} | General Purpose I/O. ; LED output |
| 4 | GP11/LED1 | I/O(D) _{16t} | General Purpose I/O. ; LED output |
| 5 | GP12/LED2 | I/O(D) _{16t} | General Purpose I/O. ; LED output |
| 6 | GP13/LED3 | I/O(D) _{16t} | General Purpose I/O. ; LED output |
| 7 | VSS | PWR | Power Pin. |
| 8 | GP20 | I/O(D) _{12t} | General Purpose I/O. |
| 9 | GP21 | I/O(D) _{12t} | General Purpose I/O. |
| 10 | GP22 | I/O(D) _{12t} | General Purpose I/O. |
| 11 | GP23 | I/O(D) _{12t} | General Purpose I/O. |
| 12 | GP24 | I/O(D) _{12t} | General Purpose I/O. |
| 13 | GP25 | I/O(D) _{12t} | General Purpose I/O. |
| 14 | GP14/BEEP | I/O(D) _{16t} | General Purpose I/O. ; BEEP output |
| 15 | GP15 / A2 | I/O _{12t} | General Purpose I/O.; Strapping pin for SMBus address bit 2, this pin is internal weak pull down during hardware reset. |

| PIN | SYMBOL | I/O | FUNCTION |
|-----|-----------|--------------------|--|
| 16 | GP16 / A1 | I/O _{12t} | General Purpose I/O.; Strapping pin for SMBus address bit 1, this pin is internal weak pull down during hardware reset. |
| 17 | GP17 / A0 | I/O _{12t} | General Purpose I/O.; Strapping pin for SMBus address bit 0, this pin is internal weak pull down during hardware reset. |
| 18 | INT# | OD ₁₂ | Auto-generated Interrupt signal when detecting a transition on GP inputs. |
| 19 | RST# | IN _{ts} | System reset signal input. Low level must be greater than 0.1uS. |
| 20 | 3VDD | PWR | Power Pin. |

5. ARCHITECTURE DESCRIPTION

5.1 Register 00h – GP1 input port register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|----|----|----|
| R/W | RO | RO | RO | RO | RO | RO | RO | RO |

*This register reflects the respective GPI1x pin level.

5.2 Register 01h – GP1 output port register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| R/W | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

5.3 Register 02h – GP1 Polarity Inversion register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| R/W | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

*Refer to Section 6.2.1 for respective GPO1x pin type implementation.

5.4 Register 03h – GP1 input/output configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| R/W | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

*This register configures the respective GPIO1x pin as input mode ("1"; by default) or output mode ("0").

5.5 Register 04h – GP1 output style register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| R/W | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

*This register configures the respective GPO1x pins as level ("0"; by default) or pulse ("1") output style.

*Set output port register (CR01) to "0" before switch the output style to pulse mode.

5.6 Register 05h – GP1 output mode register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|----|----|----|----|----|----|----|
| R/W | RFU | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit4-Bit0: Configures the respective GPO1x output pads function as Open-drain ("0"; by default) or Push-pull ("1") mode.

Bit6-5: GP14 / BEEP multi-function configuration register

=11, BEEP frequency = 4KHz; tone = 250 Hz.

=10, BEEP frequency = 2KHz; tone = 10 Hz.

=01, BEEP frequency = 1KHz / 500 Hz; tone= 1 Hz.

=00, BEEP function is disabled on GP14.

Bit7: Reserved for future use.

5.7 Register 06h – GP1 interrupt control register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| R/W | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

* This register configures the respective GPI1x pin interrupt control as disable ("0"; by default) or enable ("1").

*Clear interrupt status register (CR07) before set to enable.

5.8 Register 07h – GP1 interrupt status register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W | R/clr | R/clr | R/clr | R/clr | R/clr | R/clr | R/clr | R/clr |

*The registers are read clear.

*Refer to Section 6.2.3 for implementation.

5.9 Register 08h – GP11-GP13 / LED multi-function configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| R/W | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit7-6: GP13 / LED multi-function configuration register

=11, GP13 functions LED output of 2Hz clock, 50% duty cycle.

=10, GP13 functions LED output of 1Hz clock, 50% duty cycle.

=01, GP13 functions LED output of 1/2 Hz clock, 50% duty cycle.

=00, LED function is disabled on GP13. (Default)

Bit5-4: GP12 / LED multi-function configuration register

=11, GP12 functions LED output of 2Hz clock, 50% duty cycle.

=10, GP12 functions LED output of 1Hz clock, 50% duty cycle.

=01, GP12 functions LED output of 1/2 Hz clock, 50% duty cycle.

=00, LED function is disabled on GP12. (Default)

Bit3-2: GP11 / LED multi-function configuration register

=11, GP11 functions LED output of 2Hz clock, 50% duty cycle.

=10, GP11 functions LED output of 1Hz clock, 50% duty cycle.

=01, GP11 functions LED output of 1/2 Hz clock, 50% duty cycle.

=00, LED function is disabled on GP11. (Default)

Bit1-0: GP10 / LED multi-function configuration register

=11, GP10 functions LED output of 2Hz clock, 50% duty cycle.

=10, GP10 functions LED output of 1Hz clock, 50% duty cycle.

=01, GP10 functions LED output of 1/2 Hz clock, 50% duty cycle.

=00, LED function is disabled on GP10. (Default)

5.10 Register 09h – GP1 input latch data register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| R/W | RO | RO | RO | RO | RO | RO | RO | RO |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

*This register reflects the latch value of GP1x pins during hardware reset.

5.11 Register 10h – GP2 input port register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|---|----|----|----|----|----|----|
| R/W | NA | | RO | RO | RO | RO | RO | RO |

*This register reflects the respective GPI2x pin level.

5.12 Register 11h – GP2 output port register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|----|----|----|----|----|----|
| R/W | NA | | RW | RW | RW | RW | RW | RW |
| Default | NA | | 0 | 0 | 0 | 0 | 0 | 0 |

5.13 Register 12h – GP2 Polarity Inversion register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|----|----|----|----|----|----|
| R/W | NA | | RW | RW | RW | RW | RW | RW |
| Default | NA | | 0 | 0 | 0 | 0 | 0 | 0 |

*Refer to Section 6.2.1 for respective GPO2x pin type implementation.

5.14 Register 13h – GP2 input/output configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|----|----|----|----|----|----|
| R/W | NA | | RW | RW | RW | RW | RW | RW |
| Default | NA | | 1 | 1 | 1 | 1 | 1 | 1 |

*This register configures the respective GPIO2x pin as input mode ("1"; by default) or output mode ("0").

5.15 Register 14h – GP2 output style register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|----|----|----|----|----|----|
| R/W | NA | | RW | RW | RW | RW | RW | RW |
| Default | NA | | 0 | 0 | 0 | 0 | 0 | 0 |

*This register configures the respective GPO2x pins as level ("0"; by default) or pulse ("1") output style.

*Set output port register (CR11) to "0" before switch the output style to pulse mode.

5.16 Register 15h – GP2 output mode register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|----|----|----|----|----|----|
| R/W | NA | | RW | RW | RW | RW | RW | RW |
| Default | NA | | 0 | 0 | 0 | 0 | 0 | 0 |

*This register configures the respective GPO2x output pads function as **Open-drain** ("0"; by default) or **Push-pull** ("1") mode.

5.17 Register 16h – GP2 interrupt control register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|----|----|----|----|----|----|
| R/W | NA | | RW | RW | RW | RW | RW | RW |
| Default | NA | | 0 | 0 | 0 | 0 | 0 | 0 |

* This register configures the respective GPI2x pin interrupt control as disable ("0"; by default) or enable ("1").

*Clear interrupt status register (CR17) before set to enable.

5.18 Register 17h – GP2 interrupt status register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|---|-------|-------|-------|-------|-------|-------|
| R/W | NA | | R/clr | R/clr | R/clr | R/clr | R/clr | R/clr |

*The registers are read clear.

*Refer to Section 6.2.3 for implementation.

5.19 Register 20h – Chip ID (High byte; 95h)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|-----|-----|
| R/W | RO | RO | RO | RO | RO | RO | RO | RO |
| Default | 1 | 0 | 0 | 1 | 0 | 1 | 0/1 | 1/0 |

5.20 Register 21h – Chip ID (Low byte; 92h)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| R/W | RO | RO | RO | RO | RO | RO | RO | RO |
| Default | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

5.21 Register 22h – Global configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|-----|----|----|----|----|----|----|
| R/W | WO | RFU | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit7: Write "1" to issue a software reset.

Bit6: Reserved for future use.

Bit5: Low power enable bit. The internal clock generator will shutdown while the bit is set. In the low-power mode, the functions of SMBus, LED, BEEP, and all signals configured as the pulse mode will NOT work.

Bit4: Wake-up enable. If the bit is set, low-power enable bit (Bit-5) can be cleared whenever interrupt event is triggered on GPI pin. To enable the interrupt control register (CR06,CR16) is necessary.

Bit3: Interrupt polarity bit. Refer to Section 6.2.2 for INT pin type implementation.

Bit2: This bit configures the INT signal output as level ("0"; by default) or pulse ("1") style.

Bit1: GP2 registers mask enable. Set "1" will mask the RST# signal for all GP2 registers. (10h ~ 17h)

Bit0: GP1 registers mask enable. Set "1" will mask the RST# signal for all GP1 registers. (00h ~ 08h)

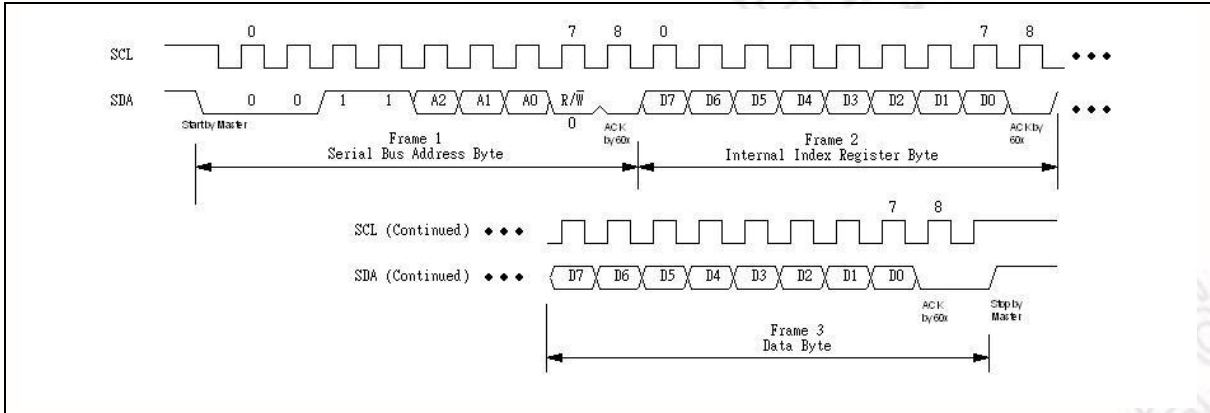
*Bit1 and Bit0 will not be reset by RST#.

6. FUNCTION DESCRIPTIONS

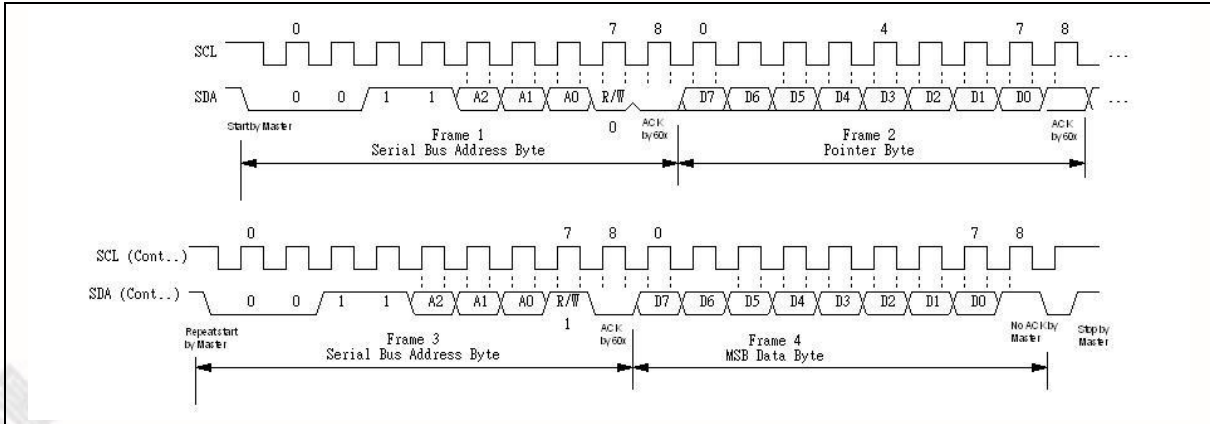
6.1 Access Interface

NCT5605Y provides a two-wired serial interface which is compliant with SMBus™ Write Byte and Read Byte protocol.

6.1.1 Write a data into NCT5605Y register









6.1.2 Read a data from NCT5605Y register



6.2 GPI/O Application Mode:

6.2.1 GPO output

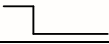
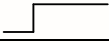


Take Reference Table for GPO Style and Polarity Function.

| GPO OUTPUT STYLE | POLARITY | OUTPUT PORT REGISTER | OUTPUT VALUE AT PIN | WAVE |
|------------------|----------|----------------------|---------------------|---|
| Level | 0 | 0 | 0 |  |
| | | 1 | 1 |  |
| | 1 | 0 | 1 |  |
| | | 1 | 0 |  |
| Pulse | 0 | Write 1 | Active |  |
| | 1 | Write 1 | Active |  |

*The GPO Pulse Mode output waveform width is 0.5uS.

6.2.2 INT output

Take Reference Table for INT Output Mode and Polarity Function.

| INT OUTPUT MODE | POLARITY | OUTPUT | WAVE |
|-----------------|----------|------------|---|
| Level | 0 | 0 |  |
| | 1 | 1 |  |
| Pulse | 0 | Low Pulse |  |
| | 1 | High Pulse |  |

*In Level mode, if INT is activated, it will be de-activated when interrupt status registers are read.

*In Pulse mode, interrupt will be activated again unless all enabled interrupt status registers are read.

*The INT Pulse Mode output waveform width is 0.25uS.

6.2.3 GPI interrupt status

Once a transition occurs at GPI input pins, interrupt status registers (CR07, CR17) will be set. At the mean time, if interrupt function is enable (CR06, CR16), the INT pin will generate an interrupt waveform. Reading these interrupt status registers will self clear and reset interrupt. If an interrupt occurs but never read the interrupt status registers, the interrupt will not be generated again.

7. DC AND AC SPECIFICATION

7.1 Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|-----------------------|----------------|------|
| Power Supply Voltage | $3.3 \pm 10\%$ | V |
| Input Voltage | $3.3 \pm 10\%$ | V |
| Operating Temperature | 0 to +70 | °C |
| Storage Temperature | -55 to +150 | °C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 Power Supply Current Consumption

($T_a = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.3\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

| PARAMETER | TYPICAL | UNIT |
|-----------------|---------|---------------|
| Normal Mode | 150 | μA |
| Power Down Mode | 10 | μA |

Note: The Typical value is measured by whole GPIO pins output without load.

7.3 DC Characteristics

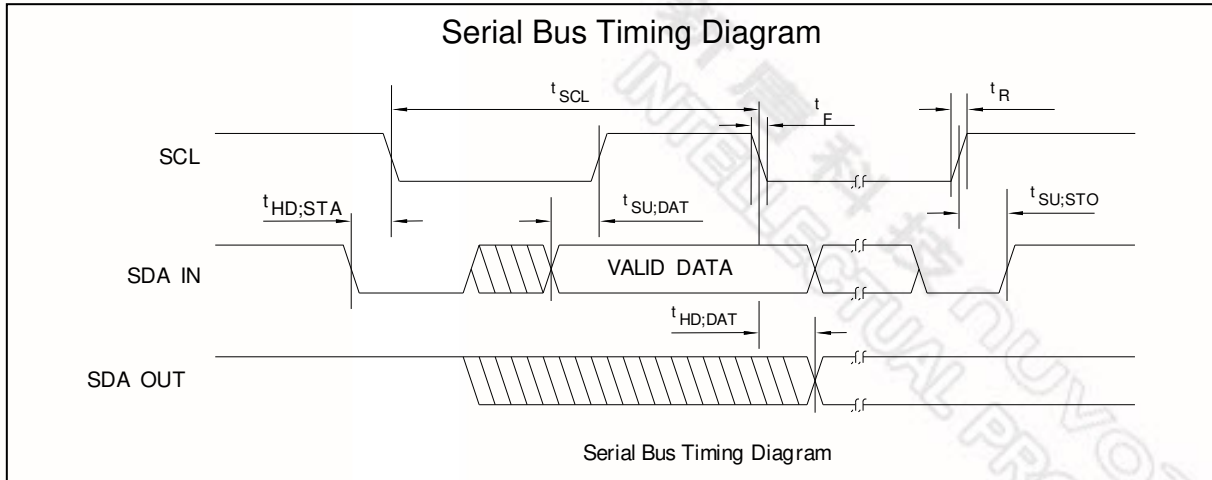
($T_a = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.3\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

| IN _{ts} - TTL level schmitt-trigger input pin | | | | | | |
|---|-----------|------|------|------|---------------|------------------------|
| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
| Input Low Voltage | V_{IL} | | | 0.8 | V | $V_{DD} = 3.3\text{V}$ |
| Input High Voltage | V_{IH} | 2.0 | | | V | $V_{DD} = 3.3\text{V}$ |
| Input High Leakage | I_{LH} | | | +10 | μA | $V_{IN} = V_{DD}$ |
| Input Low Leakage | I_{LIL} | | | -10 | μA | $V_{IN} = 0\text{V}$ |
| I/OD _{12ts} - TTL level bi-direction pin with 12mA sink capability and schmitt-trigger input | | | | | | |
| Input Low Voltage | V_{IL} | | | 0.8 | V | $V_{DD} = 3.3\text{V}$ |
| Input High Voltage | V_{IH} | 2.0 | | | V | $V_{DD} = 3.3\text{V}$ |
| Output Low Voltage | V_{OL} | | | 0.4 | V | $I_{OL} = 12\text{mA}$ |
| Input High Leakage | I_{LH} | | | +10 | μA | $V_{IN} = V_{DD}$ |
| Input Low Leakage | I_{LIL} | | | -10 | μA | $V_{IN} = 0\text{V}$ |

DC Characteristics , continued.

| I/O_{12t} - TTL level bi-direction pin with 12mA source-sink capability | | | | | | |
|---|------------------|-----|--|-----|----|-------------------------|
| Input Low Voltage | V _{IL} | | | 0.8 | V | V _{DD} = 3.3 V |
| Input High Voltage | V _{IH} | 2.0 | | | V | V _{DD} = 3.3 V |
| Output Low Voltage | V _{OL} | | | 0.4 | V | I _{OL} = 12 mA |
| Output High Voltage | V _{OH} | 2.4 | | | V | I _{OH} = 12 mA |
| Input High Leakage | I _{LIH} | | | +15 | μA | V _{IN} = 3.3 V |
| Input Low Leakage | I _{LIL} | | | -15 | μA | V _{IN} = 0 V |
| I/O(D)_{16t} - TTL level bi-direction pin with 16mA source-sink capability | | | | | | |
| Input Low Voltage | V _{IL} | | | 0.8 | V | V _{DD} = 3.3 V |
| Input High Voltage | V _{IH} | 2.0 | | | V | V _{DD} = 3.3 V |
| Output Low Voltage | V _{OL} | | | 0.4 | V | I _{OL} = 16 mA |
| Output High Voltage | V _{OH} | 2.4 | | | V | I _{OH} = 16 mA |
| Input High Leakage | I _{LIH} | | | +10 | μA | V _{IN} = 3.3 V |
| Input Low Leakage | I _{LIL} | | | -10 | μA | V _{IN} = 0 V |
| I/O(D)_{12t} - TTL level bi-direction pin with 12mA source-sink capability | | | | | | |
| Input Low Voltage | V _{IL} | | | 0.8 | V | V _{DD} = 3.3 V |
| Input High Voltage | V _{IH} | 2.0 | | | V | V _{DD} = 3.3 V |
| Output Low Voltage | V _{OL} | | | 0.4 | V | I _{OL} = 12 mA |
| Output High Voltage | V _{OH} | 2.4 | | | V | I _{OH} = 12 mA |
| Input High Leakage | I _{LIH} | | | +10 | μA | V _{IN} = 3.3 V |
| Input Low Leakage | I _{LIL} | | | -10 | μA | V _{IN} = 0 V |
| OD₁₂ - open-drain output pin with 12mA sink capability | | | | | | |
| Output Low Voltage | V _{OL} | | | 0.4 | V | I _{OL} = 12 mA |

7.4 AC Characteristics



Serial Bus Timing

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|------------------------------|--------------|------|------|------|
| SCL clock period | t_{SCL} | 10 | | uS |
| Start condition hold time | $t_{HD;STA}$ | 4.7 | | uS |
| Stop condition setup-up time | $t_{SU;STO}$ | 4.7 | | uS |
| DATA to SCL setup time | $t_{SU;DAT}$ | 120 | | nS |
| DATA to SCL hold time | $t_{HD;DAT}$ | 5 | | nS |
| SCL and SDA rise time | t_R | | 1.0 | uS |
| SCL and SDA fall time | t_F | | 300 | nS |

8. ORDERING INFORMATION

| PART NUMBER | PACKAGE TYPE | PRODUCTION FLOW |
|-------------|--------------|--------------------------|
| NCT5605Y | 20-QFN | Commercial, 0°C to +70°C |

9. TOP MARKING SPECIFICATION



1st line: Nuvoton logo

2nd line: Part number: NCT5605Y

3rd line: Tracking code 938 T B UA

938: packages assembled in Year 09', week 38

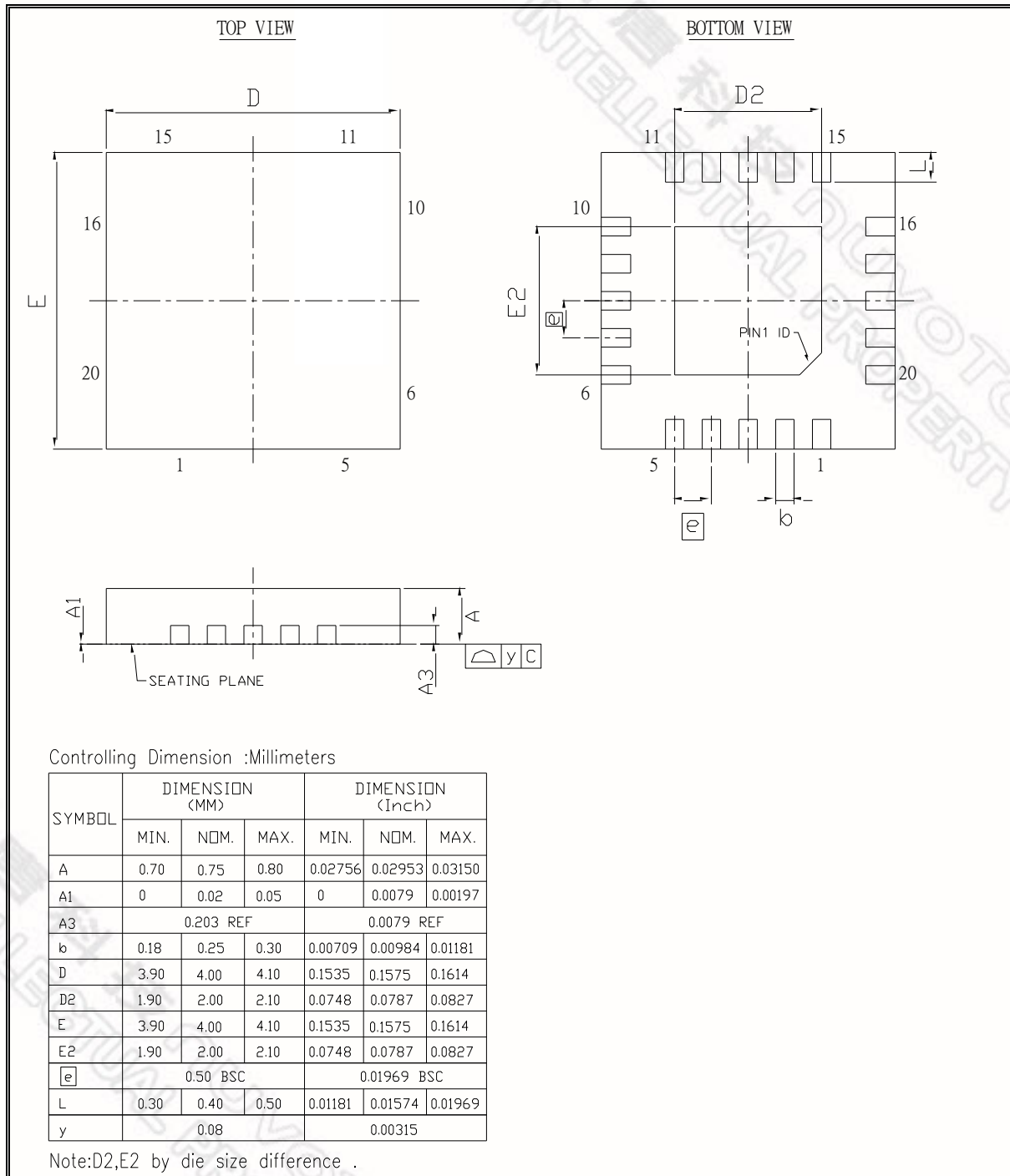
T: assembly house ID

B: the IC version

UA: Internal use code

10. PACKAGE DIMENSION OUTLINE

QFN 20L 4X4 MM², Pitch:0.50 MM



Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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