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# W83627UHG

# NCT6627UD

# NUVOTON LPC I/O

Date: October 26th, 2010 Revision: 1.7

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# 1. GENERAL DESCRIPTION

The W83627UHG is a member of Nuvoton's Super I/O product line. This family features the LPC (Low Pin Count) interface. This interface is more economical than its ISA counterpart because it has approximately forty pins fewer, yet still provides as great performance. In addition, the improvement allows even more efficient operation of software, BIOS and device drivers.

In addition to providing an LPC interface for I/O, the W83627UHG monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the W83627UHG adopts the Current Mode (dual current source) approach. The W83627UHG also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ III, which makes the system more stable and user-friendly.

The W83627UHG supports four – 360K, 720K, 1.2M, 1.44M, or 2.88M – disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s. The disk drive adapter supports the functions of floppy disk drive controller (compatible with the industry standard 82077/ 765), data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. Such a wide range of functions integrated into one W83627UHG greatly reduces the number of required components to interface with floppy disk drives.

The W83627UHG provides six high-speed serial communication ports (UARTs), one of which provides IR functions IrDA 1.0 (SIR for 1.152K bps). Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. All of the UARTs support legacy speeds up to 115.2K bps as well as higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The W83627UHG supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP).

The W83627UHG provides flexible I/O control functions through a set of 45 general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The W83627UHG supports the SST (Simple Serial Transport) interface and Intel® PECI (Platform Environment Control Interface).

The W83627UHG fully complies with the Microsoft© PC98 and PC99 Hardware Design Guide and meets the requirements of ACPI.

The configuration registers inside the W83627UHG support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows 95/98/2000/XP™, making the allocation of the system resources more efficient than ever.

One special characteristic of the Super I/O product line is the separation of the power supply in normal operation from that in standby operation. Please pay attention to the layout of these two power supplies to avoid short circuits. Otherwise, the feature will not function.

There is NCT6627UD, which is exactly the same as W83627UHG, except the package dimension. NCT6627UD is thin package type, LQFP-128, 14mm x 14mm body size; W83627UHG is QFP-128, 14mm x 20mm body size.

## 2. FEATURES

### General

- Meet LPC Spec. 1.0
- Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
- Integrated hardware monitor functions
- Compliant with Microsoft PC2000/PC2001 Hardware Design Guide
- Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
- Programmable configuration settings
- Single 24- or 48-MHz clock input

### FDC

- Variable write pre-compensation with track-selection capability
- Support vertical recording format
- DMA-enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detect all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD-write enable signal (write data signal forced to be inactive)
- Support 3.5-inch or 5.25-inch floppy disk drives
- Compatible with industry standard 82077
- 360K / 720K / 1.2M / 1.44M / 2.88M formats
- 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD and its Windows driver

### UART

- W83627UHG supports Six high-speed, 16550-compatible UARTs with 16-byte send / receive FIFOs
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop-bit generation
- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud rate generator allows division of clock source by any value from 1 to $(2^{16}-1)$
- Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5M bps.
- Support RS485 auto flow control of four UARTs. (UARTA, UARTC, UARTD and UARTE) --- for rev. E only

### Parallel Port

- Compatible with IBM parallel port
- Support PS/2-compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

### Keyboard Controller

- 8042-based keyboard controller
- Support Phoenix MultiKey/42™ firmware
- Asynchronous Access to two data registers and one status register
- Software-compatible with 8042
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8-bit timer / counter
- Support binary and BCD arithmetic
- 12MHz operating frequency

### Hardware Monitor Functions

- Smart Fan control system, supporting the functions of SMART FAN™ I - "Thermal Cruise™" and "Fan Speed Cruise™" modes and SMART FAN™ III functions
- Programmable threshold temperature to speed fan fully while current temperature exceeds this temperature during Thermal Cruise™ mode
- Two thermal inputs from optionally-remote thermistors or thermal diode output
- Support Current Mode (dual current source) temperature sensing method
- Eight voltage inputs (CPUVCORE, VIN[0..2] and 5VCC, AVCC , 5VSB, VBAT)
- Two fan-speed monitoring inputs
- Two fan-speed controls
- Dual mode for fan control (PWM and DC)
- Built-in case open detection circuit
- Programmable hysteresis and setting points for all monitored items
- Over-temperature indicator output
- Issue SMI#, OVT# to activate system protection
- Nuvoton Hardware Doctor™ Support

- Provide $I^2C$ interface to read / write registers

### Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

### General Purpose I/O Ports

- 45 programmable general purpose I/O ports
- GP25, GP26 and GP27 can distinguish whether the input pins have any transitions by reading the registers and all of the 3 GPIOs also can assert PSOUT# or PME# to wake up the system if each them has any transition.

### OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

### Simple Serial Transport™ Interface

- SST temperature and voltage Combination Sensor command support
- Support SST 0.9 Specification

### PECI Interface

- PECI Host
- Support PECI 1.0 Specification
- Support 4 CPU addresses and 2 domains per CPU address

### Package

- W83627UHG 128-pin QFP, 14mm x 20mm x 2.75mm
- NCT6627UD 128-pin LQFP, 14mm x 14mm x 1.4mm
- Green / RoHS

## 3. BLOCK DIAGRAM

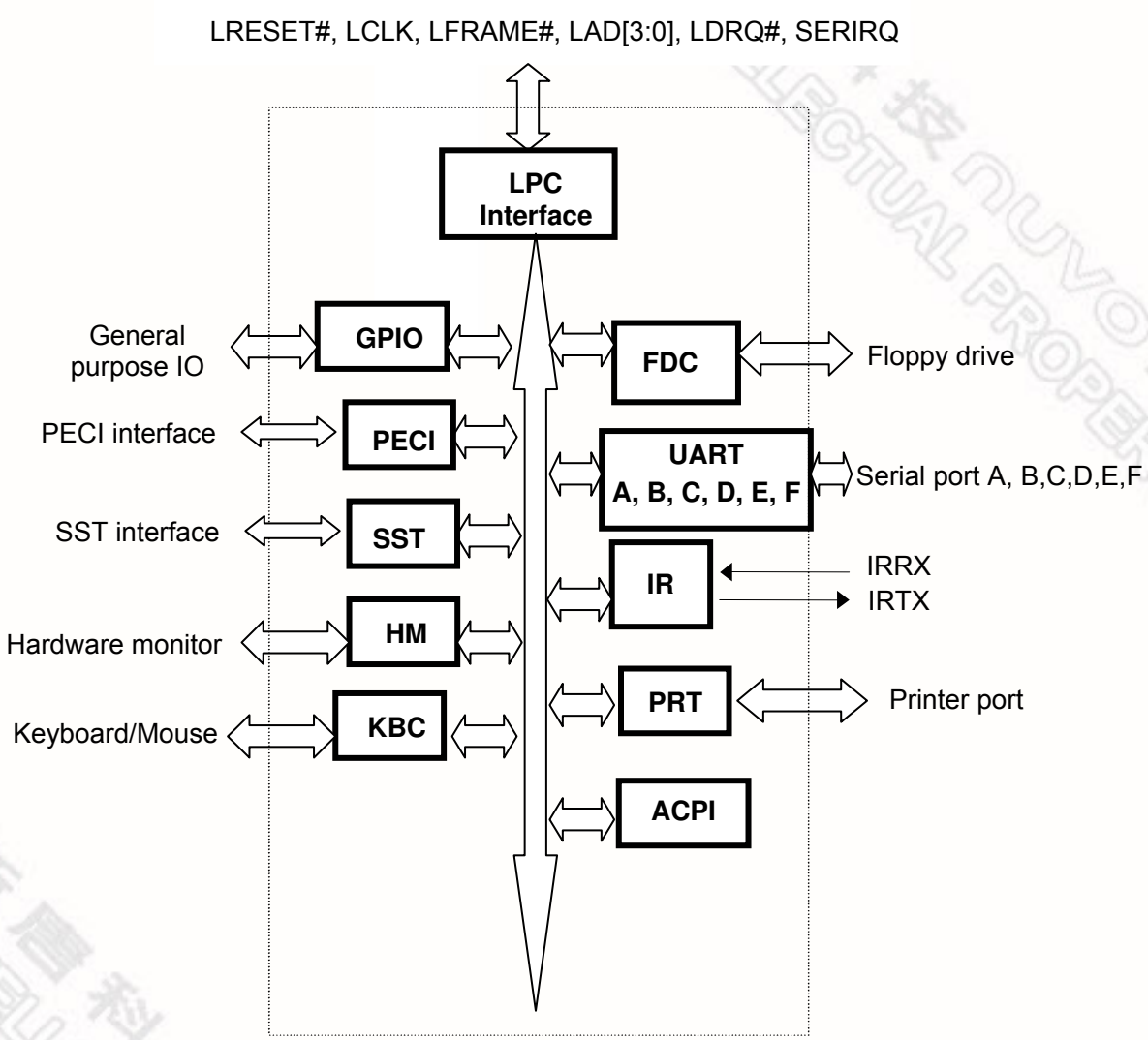


Figure 3-1 W83627UHG and NCT6627UD Block Diagram

## 4. PIN LAYOUT

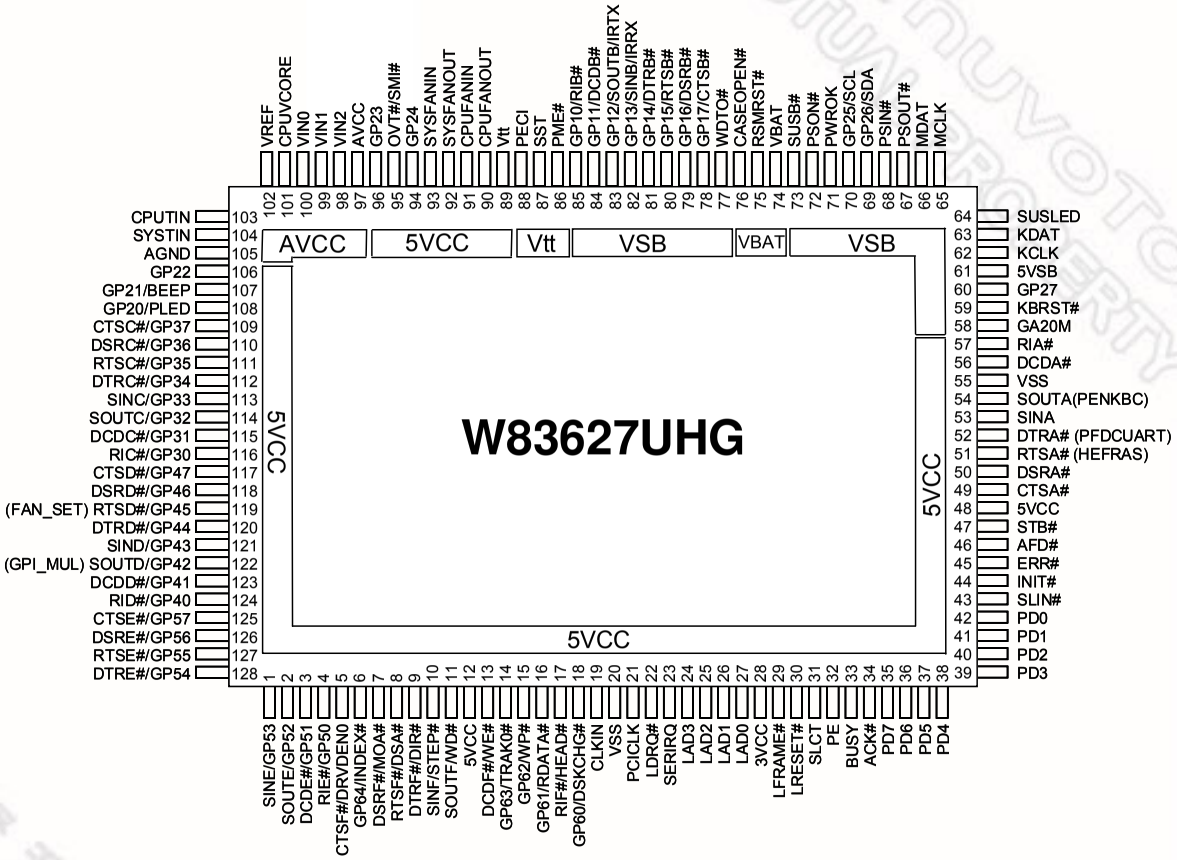


Figure 4-1 W83627UHG Pin Layout

## 5. PIN DESCRIPTION

**Note**: Please refer to 18.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
$I/O_{12tp3}$ - 3.3-V, TTL-level, bi-directional pin with 12mA source-sink capability
$I/O_{12ts}$ - TTL-level Schmitt-trigger bi-directional pin with 12mA source-sink capability
$I/OD_{8}$ - Bi-directional pin. Open-drain output with 8mA sink capability.
$I/OD_{8t}$ - TTL-level, bi-directional pin. Open-drain output with 8mA sink capability.
$I/OD_{12t}$ - TTL-level, bi-directional pin and open-drain output with 12mA sink capability
$I/OD_{16ts}$ - TTL-level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability
$I/OD_{12ts}$ - TTL-level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
$I/OD_{12tsu}$ - TTL-level, bi-directional, Schmitt-trigger pin with internal pull-up resistor
. Open-drain output with 12-mA sink capability.
$I/O_{v3}$ - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
$I/O_{v4}$ - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
$IN_{ts}$ - TTL-level Schmitt-trigger input pin
$IN_{tsu}$ - TTL-level Schmitt-trigger input pin with internal pull-up resistor
$IN_{tsp3}$ - 3.3-V, TTL-level Schmitt-trigger input pin
$IN_{t}$ - TTL-level input pin
$IN_{tu}$ - TTL-level input pin with internal pull-up resistor
$IN_{cd}$ - CMOS-level input pin with internal pull-down resistor
$O_{12p3}$ - 3.3-V, output pin with 12mA source-sink capability
$OD_{12}$ - Open-drain output pin with 12mA sink capability
$OD_{24}$ - Open-drain output pin with 24mA sink capability
$O_{8}$ - Output pin with 8mA source-sink capability
$O_{12}$ - Output pin with 12mA source-sink capability
$O_{24}$ - Output pin with 24mA source-sink capability

## 5.1 LPC Interface

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| CLKIN | 19 | $IN_t$ | System clock input, either 24MHz or 48MHz. The actual frequency must be specified in register. The default value is 48MHz. |
| PME# | 86 | $OD_{12}$ | Generated PME event. |
| PCICLK | 21 | $IN_{tsp3}$ | PCI-clock 33-MHz input. |
| LDRQ# | 22 | $O_{12p3}$ | Encoded DMA Request signal. |
| SERIRQ | 23 | $I/O_{12tp3}$ | Serialized IRQ input / output. |
| LAD[3:0] | 24-27 | $I/O_{12tp3}$ | These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral. |
| LFRAME# | 29 | $IN_{tsp3}$ | Indicates the start of a new cycle or the termination of a broken cycle. |
| LRESET# | 30 | $IN_{tsp3}$ | Reset signal. It can be connected to the PCIRST# signal on the host. |

## 5.2 FDC Interface

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| DRVDEN0 | 5 | $OD_{24}$ | Drive Density Select bit 0. |
| CTSF# | | $IN_t$ | Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register. |
| INDEX# | 6 | $IN_{tsu}$ | This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the beginning of a track marked by an index hole. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility. |
| GP64 | | $I/OD_{12ts}$ | General purpose I/O port 6 bit 4. |
| MOA# | 7 | $OD_{24}$ | Motor A On. When set to 0, this pin enables disk drive A. This is an open-drain output. |
| DSRF# | | $IN_t$ | Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| DSA# | 8 | $OD_{24}$ | Drive Select A. When set to 0, this pin enables disk drive A. This is an open-drain output. |
| RTSF# | | $O_{24}$ | UART F Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. |

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| DIR# | 9 | $OD_{24}$ | Direction of the head step motor. An open-drain output.<br>Logic 1 = outward motion<br>Logic 0 = inward motion |
| DTRF# | | $O_{24}$ | UART F Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. |
| STEP# | 10 | $OD_{24}$ | Step output pulses. This active-low open-drain output produces a pulse to move the head to another track. |
| SINF | | $IN_t$ | Serial Input. This pin is used to receive serial data through the communication link. |
| WD# | 11 | $OD_{24}$ | Write data. This logic-low open-drain writes pre-compensation serial data to the selected FDD. An open-drain output. |
| SOUTF | | $O_{24}$ | UART F Serial Output. This pin is used to transmit serial data out to the communication link. |
| WE# | 13 | $OD_{24}$ | Write enable. An open-drain output. |
| DCDF# | | $IN_t$ | Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier. |
| TRAK0# | 14 | $IN_{tsu}$ | Track 0. This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the outermost track. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility. |
| GP63 | | $I/OD_{12ts}$ | General purpose I/O port 6 bit 3. |
| WP# | 15 | $IN_{tsu}$ | Write Protected. This active-low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility. |
| GP62 | | $I/OD_{12ts}$ | General purpose I/O port 6 bit 2. |
| RDATA# | 16 | $IN_{tsu}$ | The read-data input signal from the FDD. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility. |
| GP61 | | $I/OD_{12ts}$ | General purpose I/O port 6 bit 1. |
| HEAD# | 17 | $OD_{24}$ | Head Select. This open-drain output determines which disk drive head is active.<br>Logic 1 = side 0<br>Logic 0 = side 1 |
| RIF# | | $IN_t$ | Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. |

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| DSKCHG# | 18 | $IN_{tsu}$ | Diskette Change. This signal is active-low at power-on and whenever the diskette is removed. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility. |
| GP60 | | $I/OD_{12ts}$ | General purpose I/O port 6 bit 0. |

## 5.3 Multi-Mode Parallel Port

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| SLCT | 31 | $IN_{ts}$ | PRINTER MODE:<br>An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| PE | 32 | $IN_{ts}$ | PRINTER MODE:<br>An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| BUSY | 33 | $IN_{ts}$ | PRINTER MODE:<br>An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| ACK# | 34 | $IN_{ts}$ | PRINTER MODE: ACK#<br>An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| ERR# | 45 | $IN_{ts}$ | PRINTER MODE: ERR#<br>An active-low input on this pin indicates that the printer has encountered an error. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| SLIN# | 43 | $OD_{12}$ | PRINTER MODE: SLIN#<br>Output line for detection of printer selection. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| INIT# | 44 | $OD_{12}$ | PRINTER MODE: INIT#<br>Output line for the printer initialization. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| AFD# | 46 | $OD_{12}$ | PRINTER MODE: AFD#<br>An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| STB# | 47 | $OD_{12}$ | PRINTER MODE: STB#<br>An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| PD0 | 42 | $I/O_{12ts}$ | PRINTER MODE: PD0<br>Parallel port data bus bit 0. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| PD1 | 41 | $I/O_{12ts}$ | PRINTER MODE: PD1<br>Parallel port data bus bit 1. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| PD2 | 40 | $I/O_{12ts}$ | PRINTER MODE: PD2<br>Parallel port data bus bit 2. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| PD3 | 39 | $I/O_{12ts}$ | PRINTER MODE: PD3<br>Parallel port data bus bit 3. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| PD4 | 38 | $I/O_{12ts}$ | PRINTER MODE: PD4<br>Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| PD5 | 37 | $I/O_{12ts}$ | PRINTER MODE: PD5<br>Parallel port data bus bit 5. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| PD6 | 36 | $I/O_{12ts}$ | PRINTER MODE: PD6<br>Parallel port data bus bit 6. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |
| PD7 | 35 | $I/O_{12ts}$ | PRINTER MODE: PD7<br>Parallel port data bus bit 7. See the description of the parallel port for the definition of this pin in ECP and EPP modes. |

## 5.4 Serial Port & Infrared Port Interface

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| CTSA# | 49 | $IN_t$ | Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. |
| CTSB# | 78 | $IN_t$ | Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. (This is for W83627UHG only) |
| GP17 | | $I/OD_{12t}$ | General-purpose I/O port 1 bit 7. |

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| CTSC# | 109 | $IN_t$ | Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. |
| GP37 | | $I/OD_{12t}$ | General-purpose I/O port 3 bit 7. |
| CTSD# | 117 | $IN_t$ | Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. |
| GP47 | | $I/OD_{12t}$ | General-purpose I/O port 4 bit 7. |
| CTSE# | 125 | $IN_t$ | Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. |
| GP57 | | $I/OD_{12t}$ | General-purpose I/O port 5 bit 7. |
| CTSF# | 5 | $IN_t$ | Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register. (This is for W83627UHG only) |
| DRVDEN0 | | $OD_{24}$ | Drive Density Select bit 0. |
| DSRA# | 50 | $IN_t$ | Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| DSRB# | 79 | $IN_t$ | Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. (This is for W83627UHG only) |
| GP16 | | $I/OD_{12t}$ | General-purpose I/O port 1 bit 6. |
| DSRC# | 110 | $IN_t$ | Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| GP36 | | $I/OD_{12t}$ | General-purpose I/O port 3 bit 6. |
| DSRD# | 118 | $IN_t$ | Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| GP46 | | $I/OD_{12t}$ | General-purpose I/O port 4 bit 6. |
| DSRE# | 126 | $In_t$ | Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| GP56 | | $I/OD_{12t}$ | General-purpose I/O port 5 bit 6. |
| DSRF# | 7 | $IN_t$ | Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. (This is for W83627UHG only) |
| MOA# | | $OD_{24}$ | Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output. |

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| RTSA# | 51 | $O_8$ | UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. |
| HEFRAS | | $IN_{cd}$ | During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin so as to ensure the selection of I/O port's configuration address to 2EH, and a 1-kΩ resistor is recommended to pull it up if 4EH is selected as I/O port's configuration address. |
| RTSB# | 80 | $O_8$ | UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. (This is for W83627UHG only) |
| GP15 | | $I/OD_8$ | General-purpose I/O port 1 bit 5. |
| RTSC# | 111 | $O_8$ | UART C Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. |
| GP35 | | $I/OD_8$ | General-purpose I/O port 3 bit 5. |
| RTSD# | 119 | $O_8$ | UART D Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. |
| FAN_SET | | $IN_{cd}$ | Determines the initial FAN speed. Power-on configuration for 2 fan speeds, 50% or 100%. During power-on reset, this pin needs a pulled-up or a pull-down resistor to decide whether the fan speed is 50% or 100%. |
| GP45 | | $I/OD_8$ | General-purpose I/O port 4 bit 5. |
| RTSE# | 127 | $O_{12}$ | UART E Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. |
| GP55 | | $I/OD_{12t}$ | General-purpose I/O port 5 bit 5. |
| RTSF | 8 | $O_{24}$ | UART F Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data. (This is for W83627UHG only) |
| DSA# | | $OD_{24}$ | Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output. |
| DTRA# | 52 | $O_8$ | UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. |
| PFDCUART | | $IN_{cd}$ | During power-on reset, this pin is pulled down internally and is defined as FDC enable, which provides the power-on value for CR24 bit 1. A 1 kΩ is reserved to pull down and a 1 kΩ resistor is recommended if intends to pull-up to enable UART F. |
| DTRB# | 81 | $O_8$ | UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. (This is for W83627UHG only) |
| GP14 | | $I/OD_{12t}$ | General-purpose I/O port 1 bit 4. |

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| DTRC# | 112 | $O_8$ | UART C Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. |
| GP34 | | $I/OD_{12t}$ | General-purpose I/O port 3 bit 4. |
| DTRD# | 120 | $O_8$ | UART D Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. |
| GP44 | | $I/OD_{8t}$ | General-purpose I/O port 4 bit 4. |
| DTRE# | 128 | $O_8$ | UART E Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. |
| GP54 | | $I/OD_{12t}$ | General-purpose I/O port 5 bit 4. |
| DTRF# | 9 | $O_{24}$ | UART F Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate. (This is for W83627UHG only) |
| DIR# | | $OD_{24}$ | Direction of the head step motor. An open drain output.<br>Logic 1 = outward motion<br>Logic 0 = inward motion |
| SINA | 53 | $IN_t$ | Serial Input. This pin is used to receive serial data through the communication link. |
| SINB | 82 | $IN_t$ | Serial Input. This pin is used to receive serial data through the communication link. (This is for W83627UHG only) |
| IRRX | | | IR Receiver input. |
| GP13 | | $I/OD_{12t}$ | General-purpose I/O port 1 bit 3. |
| SINC | 113 | $IN_t$ | Serial Input. This pin is used to receive serial data through the communication link. |
| GP33 | | $I/OD_{12t}$ | General-purpose I/O port 3 bit 3. |
| SIND | 121 | $IN_t$ | Serial Input. This pin is used to receive serial data through the communication link. |
| GP43 | | $I/OD_{12t}$ | General-purpose I/O port 4 bit 3. |
| SINE | 1 | $IN_t$ | Serial Input. This pin is used to receive serial data through the communication link. |
| GP53 | | $I/OD_{12t}$ | General-purpose I/O port 5 bit 3. |
| SINF | 10 | $IN_t$ | Serial Input. This pin is used to receive serial data through the communication link. (This is for W83627UHG only) |
| STEP# | | $OD_{24}$ | Step output pulses. This active low open drain output produces a pulse to move the head to another track. |
| SOUTA | 54 | $O_8$ | UART A Serial Output. This pin is used to transmit serial data out to the communication link. |

| SYMBOL | PIN | I/O | DESCRIPTION |
|---|---|---|---|
| PENKBC | | $IN_{cd}$ | During power on reset, this pin is pulled down internally and is defined as PENKBC, and the power-on values are shown at CR24 bit 2. The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure the disabling of KBC, and a 1-kΩ resistor is recommended to pull the pin up If wish to enable KBC. |
| SOUTB | 83 | $O_8$ | UART B Serial Output. This pin is used to transmit serial data out to the communication link. (This is for W83627UHG only) |
| IRTX | | | IR Transmitter output. |
| GP12 | | $I/OD_8$ | General-purpose I/O port 1 bit 2. |
| SOUTC | 114 | $O_8$ | UART C Serial Output. This pin is used to transmit serial data out to the communication link. |
| GP32 | | $I/OD_8$ | General-purpose I/O port 3 bit 2. |
| SOUTD | 122 | $O_8$ | UART D Serial Output. This pin is used to transmit serial data out to the communication link. |
| GPI_MUL | | $IN_{cd}$ | Determines PIN 107 and 108 multi-function select. During power-on reset, this pin is pulled down internally and is defined as BEEP function and power LED enable. A 1 kΩ is reserved to pull down and a 1 kΩ resistor is recommended if intending to pull up to enable GPIO output. |
| GP42 | | $I/OD_8$ | General-purpose I/O port 4 bit 2. |
| SOUTE | 2 | $O_8$ | UART E Serial Output. This pin is used to transmit serial data out to the communication link. |
| GP52 | | $I/OD_8$ | General-purpose I/O port 5 bit 2. |
| SOUTF | 11 | $O_{24}$ | UART F Serial Output. This pin is used to transmit serial data out to the communication link. (This is for W83627UHG only) |
| WD# | | $OD_{24}$ | Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output. |
| DCDA# | 56 | $IN_t$ | Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier. |
| DCDB# | 84 | $IN_t$ | Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier. (This is for W83627UHG only) |
| GP11 | | $I/OD_{12t}$ | General-purpose I/O port 1 bit 1. |
| DCDC# | 115 | $IN_t$ | Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier. |
| GP31 | | $I/OD_{12t}$ | General-purpose I/O port 3 bit 1. |
| DCDD# | 123 | $IN_t$ | Data Carrier Detect. An active-low signal indicates the modem or data set has detected a data carrier. |