



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NCT6776F / NCT6776D
Nuvoton LPC I/O

Date: July 12th, 2011 Revision 1.2

Table of Contents –

1.	GENERAL DESCRIPTION	1
2.	FEATURES	2
3.	BLOCK DIAGRAM	6
4.	PIN LAYOUT	7
5.	PIN DESCRIPTION.....	9
5.1	LPC Interface	10
5.2	FDC Interface	10
5.3	Multi-Mode Parallel Port.....	11
5.4	Serial Port Interface	13
5.5	KBC Interface	14
5.6	CIR Interface	14
5.7	Hardware Monitor Interface.....	15
5.8	VID Input/Output	16
5.9	Intel® PECl Interface	16
5.10	Advanced Configuration & Power Interface	17
5.11	Advanced Sleep State Control Control	17
5.12	Port 80 Message Display & LED Control.....	18
5.13	SMBus Interface.....	18
5.14	Hard Disk Message Display & LED Control.....	19
5.15	Power Pins	19
5.16	AMD Power-On Sequence.....	19
5.17	Intel Serial VID	19
5.18	AMD Serial VID	20
5.19	AMD SB-TSI Interface.....	20
5.20	Dual Voltage Control	20
5.21	DSW	20
5.22	IR.....	21
5.23	General Purpose I/O Port.....	21
5.23.1	GPIO-0 Interface.....	21
5.23.2	GPIO-1 Interface.....	22
5.23.3	GPIO-2 Interface.....	23
5.23.4	GPIO-3 Interface.....	23
5.23.5	GPIO-4 Interface.....	24
5.23.6	GPIO-5 Interface.....	25
5.23.7	GPIO-6 Interface.....	26
5.23.8	GPIO-7 Interface.....	26
5.23.9	GPIO-8 Interface.....	27
5.23.10	GPIO-9 Interface.....	28
5.23.11	GPIO-A Interface	28
5.24	Strapping Pins	29
5.25	Internal pull-up, pull-down pins	30
6.	GLUE LOGIC	31
6.1	ACPI Glue Logic.....	31
6.2	BKFD_CUT & LATCH_BKFD_CUT	34
6.3	3VSBSW#	35

6.4	PSON# Block Diagram.....	36
6.5	PWROK.....	37
6.6	Front Panel LEDs.....	38
6.6.1	Automatic Mode.....	38
6.6.2	Manual Mode	39
6.6.3	S0~S5 LED Blink Block Diagram.....	39
6.6.4	LED Pole (LED_POL)	40
6.6.5	Deeper Sleeping State Detect Function.....	41
6.7	HDD LED.....	43
6.8	Advanced Sleep State Control (ASSC) Function.....	44
6.8.1	When ASSC is disabled.....	44
6.8.2	When ASSC is enabled (Enter into Deeper Sleeping State).....	45
6.8.3	When ASSC is enabled (Exit Deeper Sleeping State)	45
6.8.4	SLP_S5#_LATCH Control Function.....	46
6.9	Intel DSW Function	47
6.9.1	Enter DSW State timing diagram	47
6.9.2	Exit DSW State timing diagram.....	48
6.9.3	Application Circuit.....	48
6.10	AMD Power-On Sequence.....	49
7.	CONFIGURATION REGISTER ACCESS PROTOCOL	52
7.1	Configuration Sequence.....	54
7.1.1	Enter the Extended Function Mode	54
7.1.2	Configure the Configuration Registers	54
7.1.3	Exit the Extended Function Mode	55
7.1.4	Software Programming Example	55
8.	HARDWARE MONITOR	56
8.1	General Description	56
8.2	Access Interfaces.....	56
8.3	LPC Interface	56
8.4	I ² C interface.....	58
8.5	Analog Inputs	59
8.5.1	Voltages Over 2.048 V or Less Than 0 V	60
8.5.2	Voltage Data Format.....	60
8.5.2.1.	Voltage Reading	60
8.5.3	Temperature Data Format	61
8.5.3.1.	Monitor Temperature from Thermistor	61
8.5.3.2.	Monitor Temperature from Thermal Diode (Voltage Mode)	61
8.5.3.3.	Monitor Temperature from Thermal Diode (Current Mode)	62
8.5.3.4.	Temperature Reading.....	62
8.6	PECI	63
8.7	Fan Speed Measurement and Control.....	65
8.7.1	Fan Speed Reading.....	65
8.7.2	Fan Speed Calculation by Fan Count Reading.....	65
8.7.3	Fan Speed Calculation by Fan RPM Reading	65
8.7.4	Fan Speed Control.....	65
8.7.5	SMART FAN TM Control	66
8.7.6	Temperature Source & Reading for Fan Control	67
8.8	SMART FAN TM I	68

8.8.1	Thermal Cruise Mode	68
8.8.2	Speed Cruise Mode	69
8.9	SMART FAN™ IV & Close Loop Fan Control Mode	71
8.9.1	Step Up Time / Step Down Time	74
8.9.2	Fan Output Start-up Value	74
8.9.3	Fan Output Stop Value	74
8.9.4	Fan Output Stop Time	75
8.9.5	Fan Output Step	75
8.9.6	Revolution Pulse Selection	75
8.9.7	Weight Value Control	76
8.10	Alert and Interrupt	78
8.10.1	SMI# Interrupt Mode	78
8.10.2	Voltage SMI# Mode	78
8.10.3	Fan SMI# Mode	79
8.10.4	Temperature SMI# Mode	79
8.10.4.1.	Temperature Sensor 1 SMI# Interrupt (Default: SYSTIN)	79
8.10.4.2.	SMI# Interrupt of Temperature Sensor 2 (Default: CPUTIN) and Temperature Sensor 3 (Default: AUXTIN) and Temperature Sensor 4 (Default: SYSTIN) and Temperature Sensor 5 (Default: SYSTIN) and Temperature Sensor 6 (Default: SYSTIN)	81
8.10.5	OVT# Interrupt Mode	84
8.10.6	Caseopen Detection	85
8.11	Power Measurement	86
9.	HARDWARE MONITOR REGISTER SET	87
9.1	Address Port (Port x5h)	87
9.2	Data Port (Port x6h)	87
9.3	SYSFANOUT PWM Output Frequency Configuration Register – Index 00h (Bank 0)	87
9.4	SYSFANOUT Output Value Select Register – Index 01h (Bank 0)	88
9.5	CPUFANOUT PWM Output Frequency Configuration Register – Index 02h (Bank 0)	89
9.6	CPUFANOUT Output Value Select Register – Index 03h (Bank 0)	90
9.7	SYSFANOUT Configuration Register I – Index 04h (Bank 0)	90
9.8	Reserved Register – Index 05h ~ 0Fh (Bank 0)	90
9.9	AUXFANOUT PWM Output Frequency Configuration Register – Index 10h (Bank 0)	91
9.10	AUXFANOUT Output Value Select Register – Index 11h (Bank 0)	91
9.11	Reserved Register – Index 12-17h (Bank 0)	92
9.12	OVT# Configuration Register – Index 18h (Bank 0)	92
9.13	Reserved Registers – Index 19h ~ 1Fh (Bank 0)	92
9.14	Value RAM — Index 20h ~ 3Fh (Bank 0)	92
9.15	Configuration Register – Index 40h (Bank 0)	93
9.16	Interrupt Status Register 1 – Index 41h (Bank 0)	94
9.17	Interrupt Status Register 2 – Index 42h (Bank 0)	94
9.18	SMI# Mask Register 1 – Index 43h (Bank 0)	95
9.19	SMI# Mask Register 2 – Index 44h (Bank 0)	95
9.20	Interrupt Status Register 4 – Index 45h (Bank 0)	96
9.21	SMI# Mask Register 3 – Index 46h (Bank 0)	96
9.22	Reserved Register – Index 47h (Bank 0)	97
9.23	Serial Bus Address Register – Index 48h (Bank 0)	97
9.24	Reserved Register – Index 49h ~ 4Bh (Bank 0)	97
9.25	SMI/OVT Control Register1 – Index 4Ch (Bank 0)	97

9.26	FAN IN/OUT Control Register – Index 4Dh (Bank 0)	98
9.27	Bank Select Register – Index 4Eh (Bank 0).....	99
9.28	Nuvoton Vendor ID Register – Index 4Fh (Bank 0)	99
9.29	Reserved Register – Index 50h ~ 57h (Bank 0).....	99
9.30	Chip ID – Index 58h (Bank 0).....	99
9.31	Reserved Register – Index 59h ~ 5Ch (Bank 0).....	100
9.32	VBAT Monitor Control Register – Index 5Dh (Bank 0)	100
9.33	Current Mode Enable Register – Index 5Eh (Bank 0)	100
9.34	Reserved Register – Index 5F (Bank 0).....	101
9.35	PORT 80 DATA INPUT Register – Index 60 (Bank 0).....	101
9.36	Reserved Register – Index 61F ~ 62F (Bank 0).....	101
9.37	Reserved Register – Index 65 (Bank 0).....	101
9.38	Reserved Register – Index 66 (Bank 0).....	101
9.39	Reserved register – Index 67h ~ 72h (Bank 0).....	101
9.40	MONITOR TEMPERATURE 1 Register (Integer Value)- Index 73h (Bank 0).....	101
9.41	MONITOR TEMPERATURE 1 Register (Fractional Value)- Index 74h (Bank 0)	102
9.42	MONITOR TEMPERATURE 2 Register (Integer Value)- Index 75h (Bank 0).....	102
9.43	MONITOR TEMPERATURE 2 Register (Fractional Value)- Index 76h (Bank 0)	102
9.44	MONITOR TEMPERATURE 3 Register (Integer Value)- Index 77h (Bank 0).....	103
9.45	MONITOR TEMPERATURE 3 Register (Fractional Value)- Index 78h (Bank 0)	103
9.46	Reserved Register – Index 79h~ADh (Bank 0).....	103
9.47	PECI Temperature Reading Enable for SMIOVT and SMART FAN Control Register – Index AEh (Bank 0)	103
9.48	BEEP Control Register 1 – Index B2h (Bank0).....	104
9.49	BEEP Control Register 2 – Index B3h (Bank0).....	104
9.50	BEEP Control Register 3 – Index B4h (Bank0).....	105
9.51	BEEP Control Register 4 – Index B5h (Bank0).....	106
9.52	SYSFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 1)	106
9.53	SYSFAN Target Temperature Register / SYSFANIN Target Speed_L Register – Index 01h (Bank 1).....	107
9.54	SYSFAN MODE Register / SYSFAN TOLERANCE Register – Index 02h (Bank 1)	108
9.55	SYSFANOUT Step Up Time Register – Index 03h (Bank 1)	108
9.56	SYSFANOUT Step Down Time Register – Index 04h (Bank 1)	108
9.57	SYSFANOUT Stop Value Register – Index 05h (Bank 1)	109
9.58	SYSFANOUT Start-up Value Register – Index 06h (Bank 1)	109
9.59	SYSFANOUT Stop Time Register – Index 07h (Bank 1).....	109
9.60	Reserved Register – Index 08h (Bank 1).....	110
9.61	SYSFANOUT Output Value Select Register – Index 09h (Bank 1)	110
9.62	SYSFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 1)	110
9.63	Reserved Register – Index 0Dh (Bank 1)	110
9.64	SMART FAN IV SYSFANOUT STEP Register – Index 20h (Bank 1)	110
9.65	SYSFAN (SMART FAN TM IV) Temperature 1 Register(T1) – Index 21h (Bank 1)	111
9.66	SYSFAN (SMART FAN TM IV) Temperature 2 Register(T2) – Index 22h (Bank 1)	111
9.67	SYSFAN (SMART FAN TM IV) Temperature 3 Register(T3) – Index 23h (Bank 1)	111
9.68	SYSFAN (SMART FAN TM IV) Temperature 4 Register(T4) – Index 24h (Bank 1)	112
9.69	SYSFAN (SMART FAN TM IV) DC/PWM 1 Register – Index 27h (Bank 1)	112

9.70	SYSFAN (SMART FAN TM IV) DC/PWM 2 Register – Index 28h (Bank 1)	112
9.71	SYSFAN (SMART FAN TM IV) DC/PWM 3 Register – Index 29h (Bank 1)	112
9.72	SYSFAN (SMART FAN TM IV) DC/PWM 4 Register – Index 2Ah (Bank 1)	113
9.73	Reserved Register – Index 2Bh~30h (Bank 1)	113
9.74	SYSFAN 3-Wire Enable Register – Index 31h (Bank 1).....	113
9.75	Reserved Register – Index 32h ~ 34h(Bank 1).....	113
9.76	SYSFAN (SMART FAN TM IV) Critical Temperature Register – Index 35h (Bank 1).....	113
9.77	Reserved Register – Index 36h ~ 37h (Bank 1).....	114
9.78	SYSFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 1)	114
9.79	Weight value Configuration Register – Index 39h (Bank 1).....	114
9.80	SYSFANOUT Temperature Step Register – Index 3Ah (Bank 1).....	115
9.81	SYSFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 1)	115
9.82	SYSFANOUT Weight Step Register – Index 3Ch (Bank 1).....	115
9.83	SYSFANOUT Temperature Base Register – Index 3Dh (Bank 1).....	115
9.84	SYSFANOUT Temperature Fan Duty Base Register – index 3Eh (Bank 1)	116
9.85	Reserved Register – Index 3Fh (Bank 1).....	116
9.86	Reserved Register – Index 40h (Bank 1).....	116
9.87	Reserved Register – Index 41h (Bank 1).....	116
9.88	Reserved Register – Index 42h ~ 44h (Bank 1).....	116
9.89	Reserved Register – Index 45h (Bank 1).....	116
9.90	Reserved Register – Index 46h (Bank 1).....	116
9.91	Reserved Register – Index 49h ~ 4Fh (Bank1)	116
9.92	SMIOVT2 Temperature Source (High Byte) Register – Index 50h (Bank 1)	116
9.93	SMIOVT2 Temperature Source (Low Byte) Register – Index 51h (Bank 1).....	117
9.94	SMIOVT2 Temperature Source Configuration Register – Index 52h (Bank 1).....	117
9.95	SMIOVT2 Temperature Source Hysteresis (High Byte) Register – Index 53h (Bank 1)	117
9.96	SMIOVT2 Temperature Source Hysteresis (Low Byte) Register – Index 54h (Bank 1)....	118
9.97	SMIOVT2 Temperature Source Over-temperature (High Byte) Register – Index 55h (Bank1)	118
9.98	SMIOVT2 Temperature Source Over-temperature (Low Byte) Register – Index 56h (Bank 1)	118
9.99	Reserved Register – Index 57h ~ 7Fh (Bank 1)	118
9.100	CPUFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 2).....	119
9.101	CPUFAN Target Temperature Register / CPUFANIN Target Speed_L Register – Index 01h (Bank 2).....	119
9.102	CPUFAN MODE Register / CPUFAN TOLERANCE Register – Index 02h (Bank 2)	120
9.103	CPUFANOUT Step Up Time Register – Index 03h (Bank 2).....	120
9.104	CPUFANOUT Step Down Time Register – Index 04h (Bank 2).....	120
9.105	CPUFANOUT Stop Value Register – Index 05h (Bank 2).....	121
9.106	CPUFANOUT Start-up Value Register – Index 06h (Bank 2).....	121
9.107	CPUFANOUT Stop Time Register – Index 07h (Bank 2)	121
9.108	Reserved Register – Index 08h (Bank 2).....	122
9.109	CPUFANOUT Output Value Select Register – Index 09h (Bank 2).....	122
9.110	CPUFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 2).....	122
9.111	Reserved Register – Index 0Dh (Bank 2)	122
9.112	SMART FAN IV CPUFANOUT STEP Register – Index 20h (Bank 2).....	122

9.113	CPUFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 2).....	123
9.114	CPUFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 2).....	123
9.115	CPUFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 2).....	123
9.116	CPUFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 2).....	123
9.117	CPUFAN (SMART FAN™ IV) DC or DUTY_SMF4 PWM1 Register – Index 27h (Bank 2)	124
9.118	CPUFAN (SMART FAN™ IV) DC or DUTY_SMF4 PWM2 Register – Index 28h (Bank 2)	124
9.119	CPUFAN (SMART FAN™ IV) DC or DUTY_SMF4 PWM3 Register – Index 29h (Bank 2)	124
9.120	CPUFAN (SMART FAN™ IV) DC or DUTY_SMF4 PWM4 Register – Index 2Ah (Bank 2)	124
9.121	Reserved Register – Index 2Dh~ 30h (Bank 2).....	125
9.122	CPUFAN 3-Wire FAN Enable Register – Index 31h (Bank 2)	125
9.123	Reserved Register – Index 32h ~ 34h(Bank 2).....	125
9.124	CPUFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 2)	125
9.125	Reserved Register – Index 36h ~ 37h (Bank 2).....	125
9.126	CPUFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 2)	125
9.127	Weight value Configuration Register – Index 39h (Bank 2).....	126
9.128	CPUFANOUT Temperature Step Register – Index 3Ah (Bank 2)	127
9.129	CPUFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 2)	127
9.130	CPUFANOUT Weight Step Register – Index 3Ch (Bank 2)	127
9.131	CPUFANOUT Temperature Base Register – Index 3Dh (Bank 2)	127
9.132	CPUFANOUT Temperature Fan Duty Base Register – Index 3Eh (Bank 2).....	128
9.133	Reserved Register – Index 3Fh (Bank 2).....	128
9.134	Reserved Register – Index 40h (Bank 2).....	128
9.135	Reserved Register – Index 41h (Bank 2).....	128
9.136	Reserved Register – Index 42h ~ 44h (Bank 2).....	128
9.137	Reserved Register – Index 45h (Bank 2).....	128
9.138	Reserved Register – Index 46h (Bank 2).....	128
9.139	Reserved Register – Index 49h ~ 4Fh (Bank2)	128
9.140	SMIOVT3 Temperature Source (High Byte) Register – Index 50h (Bank 2)	128
9.141	SMIOVT3 Temperature Source (Low Byte) Register – Index 51h (Bank 2).....	128
9.142	SMIOVT3 Temperature Source Configuration Register – Index 52h (Bank 2).....	129
9.143	SMIOVT3 Temperature Source Hysteresis (High Byte) Register – Index 53h (Bank 2)	129
9.144	SMIOVT3 Temperature Source Hysteresis (Low Byte) Register – Index 54h (Bank 2)....	129
9.145	SMIOVT3 Temperature Source Over-temperature (High Byte) Register – Index 55h (Bank 2)	130
9.146	SMIOVT3 Temperature Source Over-temperature (Low Byte) Register – Index 56h (Bank 2)	130
9.147	Reserved Register – Index 57h ~ 7Fh (Bank 2)	130
9.148	AUXFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 3).....	130
9.149	AUXFAN Target Temperature Register / AUXFANIN Target Speed_L Register – Index 01h (Bank 3).....	131
9.150	AUXFAN MODE Register / AUXFAN TOLERRANCE Register – Index 02h (Bank 3).....	132
9.151	AUXFANOUT Step Up Time Register – Index 03h (Bank 3).....	132
9.152	AUXFANOUT Step Down Time Register – Index 04h (Bank 3)	132
9.153	AUXFANOUT Stop Value Register – Index 05h (Bank 3)	133
9.154	AUXFANOUT Start-up Value Register – Index 06h (Bank 3)	133
9.155	AUXFANOUT Stop Time Register – Index 07h (Bank 3)	133

9.156	Reserved Register – Index 08h (Bank 3).....	133
9.157	AUXFANOUT Output Value Select Register – Index 09h (Bank 3).....	134
9.158	AUXFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 3).....	134
9.159	Reserved Register – Index 0Dh (Bank 3)	134
9.160	SMART FAN IV AUXFANOUT STEP Register – Index 20h (Bank 3)	134
9.161	AUXFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 3)	135
9.162	AUXFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 3)	135
9.163	AUXFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 3)	135
9.164	AUXFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 3)	135
9.165	AUXFAN (SMART FAN™ IV) DC/PWM 1 Register – Index 27h (Bank 3)	136
9.166	AUXFAN (SMART FAN™ IV) DC/PWM 2 Register – Index 28h (Bank 3)	136
9.167	AUXFAN (SMART FAN™ IV) DC/PWM 3 Register – Index 29h (Bank 3)	136
9.168	AUXFAN (SMART FAN™ IV) DC/PWM 4 Register – Index 2Ah (Bank 3).....	136
9.169	Reserved Register – Index Index 2Dh~ 30h (Bank 3)	137
9.170	AUXFAN 3-Wire Enable Register – Index 31h (Bank 3).....	137
9.171	Reserved Register – Index 32h ~ 34h(Bank 3).....	137
9.172	AUXFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 3).....	137
9.173	Reserved Register – Index 36h ~ 37h (Bank 3).....	137
9.174	AUXFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 3).....	137
9.175	Weight value Configuration Register – Index 39h (Bank 3).....	138
9.176	AUXFANOUT Temperature Step Register – Index 3Ah (Bank 3)	139
9.177	AUXFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 3)	139
9.178	AUXFANOUT Weight Step Register – Index 3Ch (Bank 3).....	139
9.179	AUXFANOUT Temperature Base Register – Index 3Dh (Bank 3)	139
9.180	AUXFANOUT Temperature Fan Duty Base Register – Index 3Eh (Bank 3).....	140
9.181	Reserved Register – Index 3Fh (Bank 3).....	140
9.182	Reserved Register – Index 40h (Bank 3).....	140
9.183	Reserved Register – Index 41h (Bank 3).....	140
9.184	Reserved Register – Index 42h ~ 44h (Bank 3).....	140
9.185	Reserved Register – Index 45h (Bank 3).....	140
9.186	Reserved Register – Index 46h (Bank 3).....	140
9.187	Reserved Register – Index 47h ~ 7Fh (Bank3)	140
9.188	PCH_CHIP_CPU_MAX_TEMP Register – Index 00h (Bank 4)	140
9.189	PCH_CHIP_TEMP Register – Index 01h (Bank 4)	140
9.190	PCH_CPU_TEMP_H Register – Index 02h (Bank 4)	141
9.191	PCH_CPU_TEMP_L Register – Index 03h (Bank 4)	141
9.192	PCH_MCH_TEMP Register – Index 04h (Bank 4)	141
9.193	PCH_DIM0_TEMP Register – Index 05h (Bank 4)	142
9.194	PCH_DIM1_TEMP Register – Index 06h (Bank 4)	142
9.195	PCH_DIM2_TEMP Register – Index 07h (Bank 4)	142
9.196	PCH_DIM3_TEMP Register – Index 08h (Bank 4)	142
9.197	PCH_TSI0_TEMP_H Register – Index 09h (Bank 4)	143
9.198	PCH_TSI0_TEMP_L Register – Index 0Ah (Bank 4)	143
9.199	PCH_TSI1_TEMP_H Register – Index 0Bh (Bank 4)	143
9.200	PCH_TSI1_TEMP_L Register – Index 0Ch (Bank 4)	143
9.201	PCH_TSI2_TEMP_H Register – Index 0Dh (Bank 4)	144
9.202	PCH_TSI2_TEMP_L Register – Index 0Eh (Bank 4)	144

9.203	PCH_TSI3_TEMP_H Register – Index 0Fh (Bank 4)	144
9.204	PCH_TSI3_TEMP_L Register – Index 10h (Bank 4)	144
9.205	PCH_TSI4_TEMP_H Register – Index 11h (Bank 4)	145
9.206	PCH_TSI4_TEMP_L Register – Index 12h (Bank 4)	145
9.207	PCH_TSI5_TEMP_H Register – Index 13h (Bank 4)	145
9.208	PCH_TSI5_TEMP_L Register – Index 14h (Bank 4)	146
9.209	PCH_TSI6_TEMP_H Register – Index 15h (Bank 4)	146
9.210	PCH_TSI6_TEMP_L Register – Index 16h (Bank 4)	146
9.211	PCH_TSI7_TEMP_H Register – Index 17h (Bank 4)	146
9.212	PCH_TSI7_TEMP_L Register – Index 18h (Bank 4)	147
9.213	ByteTemp_H Register – Index 19h (Bank 4)	147
9.214	ByteTemp_L Register – Index 1Ah (Bank 4)	147
9.215	Reserved Register – Index 1Bh ~ 22h (Bank 4)	147
9.216	VIN0 High Limit Compared Voltage Register – Index 23h (Bank 4)	148
9.217	VIN0 Low Limit Compared Voltage Register – Index 24h (Bank 4)	148
9.218	VIN1 High Limit Compared Voltage Register – Index 25h (Bank 4)	148
9.219	VIN1 Low Limit Compared Voltage Register – Index 26h (Bank 4)	148
9.220	AVCC High Limit Compared Voltage Register – Index 27h (Bank 4)	149
9.221	AVCC Low Limit Compared Voltage Register – Index 28h (Bank 4)	149
9.222	Reserved Register – Index 29h ~ 3Fh (Bank 4)	149
9.223	SMI_TEMP4-6 SMI# Mask Register - Index 40h (Bank 4)	149
9.224	SMI_TEMP4-6 Interrupt Status Register - Index 41h (Bank 4)	150
9.225	Voltage Comparation Interrupt Status Register - Index 42h (Bank 4)	150
9.226	Interrupt Status Register 3 – Index 50h (Bank 4)	151
9.227	SMI# Mask Register 4 – Index 51h (Bank 4)	151
9.228	Reserved Register – Index 52h ~ 53h (Bank 4)	151
9.229	SYSTIN Temperature Sensor Offset Register – Index 54h (Bank 4)	151
9.230	CPUTIN Temperature Sensor Offset Register – Index 55h (Bank 4)	152
9.231	AUXTIN Temperature Sensor Offset Register – Index 56h (Bank 4)	152
9.232	Reserved Register – Index 57h-58h (Bank 4)	152
9.233	Real Time Hardware Status Register I – Index 59h (Bank 4)	152
9.234	Real Time Hardware Status Register II – Index 5Ah (Bank 4)	153
9.235	Real Time Hardware Status Register III – Index 5Bh (Bank 4)	154
9.236	Reserved Register – Index 5Ch ~ 5Fh (Bank 4)	155
9.237	Is<8:1> Current Register – Index 60h (Bank 4)	155
9.238	Is<0> Current Register – Index 61h (Bank 4)	155
9.239	POWER <9:2> Register – Index 62h (Bank 4)	155
9.240	POWER<1:0> Register – Index 63h (Bank 4)	155
9.241	VIN Register – Index 64h (Bank 4)	156
9.242	Rreg Setting Register – Index 65h (Bank 4)	156
9.243	Reg_Ratio_K and POWER_Voltage Enable Register – Index 66h (Bank 4)	156
9.244	POWER_V Register – Index 67h (Bank 4)	157
9.245	Reserved Register – Index 68h ~ 7Fh (Bank 4)	157
9.246	Reserved Register – Index 00h ~ 4Fh (Bank 5)	157
9.247	Value RAM 2 — Index 50h-5Fh (Bank 5)	157
9.248	Reserved Register – Index 60h ~ 7Fh (Bank 5)	157
9.249	Close-Loop Fan Control RPM mode Register – Index 00 (Bank 6)	157

9.250	Close-Loop Fan Control RPM Mode Tolerance Register – Index 01 (Bank 6).....	158
9.251	SMIOVT1 Temperature Source Select Register – Index 21 (Bank 6)	158
9.252	SMIOVT2 Temperature Source Select Register – Index 22 (Bank 6)	159
9.253	SMIOVT3 Temperature Source Select Register – Index 23 (Bank 6)	159
9.254	SMIOVT4 Temperature Source Select Register – Index 24 (Bank 6)	160
9.255	SMIOVT5 Temperature Source Select Register – Index 25 (Bank 6)	161
9.256	SMIOVT6 Temperature Source Select Register – Index 26 (Bank 6)	162
9.257	Reserved Register – Index 27h (Bank 6).....	163
9.258	SMIOVT4 Temperature Source Configuration Register – Index 28h (Bank 6).....	163
9.259	SMIOVT5 Temperature Source Configuration Register – Index 29h (Bank 6).....	163
9.260	SMIOVT6 Temperature Source Configuration Register – Index 2Ah (Bank 6)	163
9.261	SMIOVT4 Temperature Source (High Byte) Register – Index 2Bh (Bank 6).....	164
9.262	SMIOVT5 Temperature Source (High Byte) Register – Index 2Ch (Bank 6)	164
9.263	SMIOVT6 Temperature Source (High Byte) Register – Index 2Dh (Bank 6)	164
9.264	SMIOVT4/SMIOVT5/SMIOVT6 Temperature Source (Low Byte) Register – Index 2Eh (Bank 6)	165
9.265	Reserved Register – Index 2Fh (Bank 6).....	165
9.266	(SYSFANIN) FANIN1 COUNT High-byte Register – Index 30h (Bank 6)	165
9.267	(SYSFANIN) FANIN1 COUNT Low-byte Register – Index 31h (Bank 6)	165
9.268	(CPUFANIN) FANIN2 COUNT High-byte Register – Index 32h (Bank 6)	166
9.269	(CPUFANIN) FANIN2 COUNT Low-byte Register – Index 33h (Bank 6)	166
9.270	(AUXFANIN0) FANIN3 COUNT High-byte Register – Index 34h (Bank 6)	166
9.271	(AUXFANIN0) FANIN3 COUNT Low-byte Register – Index 35h (Bank 6)	166
9.272	(AUXFANIN1) FANIN4 COUNT High-byte Register – Index 36h (Bank 6)	167
9.273	(AUXFANIN1) FANIN4 COUNT Low-byte Register – Index 37h (Bank 6)	167
9.274	(AUXFANIN2) FANIN5 COUNT High-byte Register – Index 38h (Bank 6)	167
9.275	(AUXFANIN2) FANIN5 COUNT Low-byte Register – Index 39h (Bank 6)	167
9.276	(SYSFANIN) Fan Count Limit High-byte Register – Index 3Ah (Bank 6)	168
9.277	(SYSFANIN) Fan Count Limit Low-byte Register – Index 3Bh (Bank 6)	168
9.278	(CPUFANIN) Fan Count Limit High-byte Register – Index 3Ch (Bank 6).....	168
9.279	(CPUFANIN) Fan Count Limit Low-byte Register – Index 3Dh (Bank 6)	169
9.280	(AUXFANIN0) Fan Count Limit High-byte Register – Index 3Eh (Bank 6)	169
9.281	(AUXFANIN0) Fan Count Limit Low-byte Register – Index 3Fh (Bank 6)	169
9.282	(AUXFANIN1) Fan Count Limit High-byte Register – Index 40h (Bank 6)	169
9.283	(AUXFANIN1) Fan Count Limit Low-byte Register – Index 41h (Bank 6)	170
9.284	(AUXFANIN2) Fan Count Limit High-byte Register – Index 42h (Bank 6)	170
9.285	(AUXFANIN2) Fan Count Limit Low-byte Register – Index 43h (Bank 6)	170
9.286	SYSFANIN Revolution Pulses Selection Register – Index 44h (Bank 6)	170
9.287	CPUFANIN Revolution Pulses Selection Register – Index 45h (Bank 6).....	171
9.288	AUXFANIN Revolution Pulses Selection Register – Index 46h (Bank 6)	171
9.289	SMIOVT1 SMI# Shut-down mode High Limit Temperature Register – Index 50h (Bank 6)172	
9.290	SMIOVT1 SMI# Shut-down mode Low Limit Temperature Register – Index 51h (Bank 6)172	
9.291	SMIOVT2 SMI# Shut-down mode High Limit Temperature Register – Index 52h (Bank 6)172	
9.292	SMIOVT2 SMI# Shut-down mode Low Limit Temperature Register – Index 53h (Bank 6)172	
9.293	SMIOVT3 SMI# Shut-down mode High Limit Temperature Register – Index 54h (Bank 6)173	
9.294	SMIOVT3 SMI# Shut-down mode Low Limit Temperature Register – Index 55h (Bank 6)173	
9.295	SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - Index 56h (Bank 6)	173

9.296	SYSFANIN SPEED LOW-BYTE VALUE (RPM) - Index 57h (Bank 6).....	173
9.297	CPUFANIN SPEED HIGH-BYTE VALUE (RPM) – Index 58h (Bank 6).....	174
9.298	CPUFANIN SPEED LOW-BYTE VALUE (RPM) – Index 59h (Bank 6).....	174
9.299	AUXFANIN0 SPEED HIGH-BYTE VALUE (RPM) – Index 5Ah (Bank 6).....	174
9.300	AUXFANIN0 SPEED LOW-BYTE VALUE (RPM) – Index 5Bh (Bank 6)	174
9.301	AUXFANIN1 SPEED HIGH-BYTE VALUE (RPM) – Index 5Ch (Bank 6)	175
9.302	AUXFANIN1 SPEED LOW-BYTE VALUE (RPM) – Index 5Dh (Bank 6)	175
9.303	AUXFANIN2 SPEED HIGH-BYTE VALUE (RPM) – Index 5Eh (Bank 6).....	175
9.304	AUXFANIN2 SPEED LOW-BYTE VALUE (RPM) – Index 5Fh (Bank 6).....	175
9.305	SMIOVT4 SMI# Shut-down mode High Limit Temperature Register – Index 70h (Bank 6)176	
9.306	SMIOVT4 SMI# Shut-down mode Low Limit Temperature Register – Index 71h (Bank 6) 176	
9.307	SMIOVT4 Temperature Source Over-temperature (High Byte) Register – Index 72h (Bank 6) 176	
9.308	SMIOVT4 Temperature Source Hysteresis (High Byte) Register – Index 73h (Bank 6) 177	
9.309	SMIOVT4 Over-temperature and Hysteresis LSB Temperature and DIS_OVT and EN_WS Register – Index 74h (Bank 6)	177
9.310	SMIOVT5 SMI# Shut-down mode High Limit Temperature Register – Index 75h (Bank 6)177	
9.311	SMIOVT5 SMI# Shut-down mode Low Limit Temperature Register – Index 76h (Bank 6) 178	
9.312	SMIOVT5 Temperature Source Over-temperature (High Byte) Register – Index 77h (Bank 6) 178	
9.313	SMIOVT5 Temperature Source Hysteresis (High Byte) Register – Index 78h (Bank 6) 178	
9.314	SMIOVT5 Over-temperature and Hysteresis LSB Temperature and DIS_OVT and EN_WS Register – Index 79h (Bank 6)	178
9.315	SMIOVT6 SMI# Shut-down mode High Limit Temperature Register – Index 7Ah (Bank 6) 179	
9.316	SMIOVT6 SMI# Shut-down mode Low Limit Temperature Register – Index 7Bh (Bank 6)179	
9.317	SMIOVT6 Temperature Source Over-temperature (High Byte) Register – Index 7Ch (Bank 6) 179	
9.318	SMIOVT6 Temperature Source Hysteresis (High Byte) Register – Index 7Dh (Bank 6).... 180	
9.319	SMIOVT6 Over-temperature and Hysteresis LSB Temperature and DIS_OVT and EN_WS Register – Index 7Eh (Bank 6)	180
9.320	Reserved Register – Index 7Fh (Bank 6).....	180
9.321	PECI Function Control Registers – Index 01 ~ 04h (Bank 7)	181
9.322	PECI Enable Function Register – Index 01h (Bank 7).....	181
9.323	PECI Timing Config Register – Index 02h (Bank 7)	181
9.324	PECI Agent Config Register – Index 03h (Bank 7).....	182
9.325	PECI Temperature Config Register – Index 04h (Bank 7).....	182
9.326	PECI Command Write Date Registers – Index 05 ~ 1Eh (Bank 7).....	183
9.327	PECI Command Address Register – Index 05h (Bank 7).....	183
9.328	PECI Command Write Length Register – Index 06h (Bank 7).....	183
9.329	PECI Command Read Length Register – Index 07h (Bank 7)	183
9.330	PECI Command Code Register – Index 08h (Bank 7)	184
9.331	PECI Command Tbase0 Register – Index 09h (Bank 7)	184
9.332	PECI Command Tbase1 Register – Index 0Ah (Bank 7).....	184
9.333	PECI Command Write Data 1 Register – Index 0Bh (Bank 7).....	184
9.334	PECI Command Write Data 2 Register – Index 0Ch (Bank 7)	185
9.335	PECI Command Write Data 3 Register – Index 0Dh (Bank 7)	185
9.336	PECI Command Write Data 4 Register – Index 0Eh (Bank 7).....	185

9.337	PECI Command Write Data 5 Register – Index 0Fh (Bank 7).....	185
9.338	PECI Command Write Data 6 Register – Index 10h (Bank 7).....	186
9.339	PECI Command Write Data 7 Register – Index 11h (Bank 7).....	186
9.340	PECI Command Write Data 8 Register – Index 12h (Bank 7).....	186
9.341	PECI Command Write Data 9 Register – Index 13h (Bank 7).....	187
9.342	PECI Command Write Data 10 Register – Index 14h (Bank 7).....	187
9.343	PECI Command Write Data 11 Register – Index 15h (Bank 7).....	187
9.344	PECI Command Write Data 12 Register – Index 16h (Bank 7).....	187
9.345	PECI Agent Relative Temperature Register (ARTR) – Index 17h-1Eh (Bank 7).....	188
9.346	PECI Command Read Date Registers – Index 1F ~ 32h (Bank 7).....	189
9.347	PECI Alive Agent Register – Index 1Fh (Bank 7)	189
9.348	PECI Temperature Reading Register (Integer) – Index 20h (Bank 7).....	189
9.349	PECI Temperature Reading Register (Fraction) – Index 21h (Bank 7)	190
9.350	PECI Command TN Count Value Register – Index 22h (Bank 7)	190
9.351	PECI Command TN Count Value Register – Index 23h (Bank 7)	190
9.352	PECI Command Warning Flag Register – Index 24h (Bank 7).....	191
9.353	PECI Command FCS Data Register – Index 25h (Bank 7)	191
9.354	PECI Command WFCS Data Register – Index 26h (Bank 7).....	191
9.355	PECI RFCS Data Register – Index 27h (Bank 7)	192
9.356	PECI AWFCs Data Register – Index 28h (Bank 7)	192
9.357	PECI CRC OUT WFCS Data Register – Index 29h (Bank 7)	192
9.358	PECI Command Read Data 1 Register – Index 2Ah (Bank 7)	193
9.359	PECI Command Read Data 2 Register – Index 2Bh (Bank 7)	193
9.360	PECI Command Read Data 3 Register – Index 2Ch (Bank 7)	193
9.361	PECI Command Read Data 4 Register – Index 2Dh (Bank 7)	193
9.362	PECI Command Read Data 5 Register – Index 2Eh (Bank 7)	194
9.363	PECI Command Read Data 6 Register – Index 2Fh (Bank 7).....	194
9.364	PECI Command Read Data 7 Register – Index 30h (Bank 7).....	194
9.365	PECI Command Read Data 8 Register – Index 31h (Bank 7).....	195
9.366	PECI Command Read Data 9 Register – Index 32h (Bank 7).....	195
10.	FLOPPY DISK CONTROLLER.....	198
10.1	FDC Functional Description	198
10.1.1	FIFO (Data).....	198
10.1.2	Data Separator	199
10.1.3	Write Precompensation	199
10.1.4	Perpendicular Recording Mode	199
10.1.5	FDC Core.....	199
10.1.6	FDC Commands	199
10.2	Register Descriptions	207
10.2.1	Status Register A (SA Register) (Read base address + 0)	207
10.2.2	Status Register B (SB Register) (Read base address + 1).....	208
10.2.3	Digital Output Register (DO Register) (Write base address + 2)	209
10.2.4	Tape Drive Register (TD Register) (Read base address + 3).....	209
10.2.5	Main Status Register (MS Register) (Read base address + 4)	210
10.2.6	Data Rate Register (DR Register) (Write base address + 4)	211
10.2.7	FIFO Register (R/W base address + 5)	212
10.2.8	Digital Input Register (DI Register) (Read base address + 7).....	214

10.2.9 Configuration Control Register (CC Register) (Write base address + 7).....	215
11. UART PORT	217
11.1 UART Control Register (UCR) (Read/Write).....	217
11.2 UART Status Register (USR) (Read/Write)	219
11.3 Handshake Control Register (HCR) (Read/Write)	219
11.4 Handshake Status Register (HSR) (Read/Write)	220
11.5 UART FIFO Control Register (UFR) (Write only).....	221
11.6 Interrupt Status Register (ISR) (Read only)	221
11.7 Interrupt Control Register (ICR) (Read/Write).....	222
11.8 Programmable Baud Generator (BLL/BHL) (Read/Write)	223
11.9 User-defined Register (UDR) (Read/Write)	223
11.10 UART RS485 Auto Flow Control.....	224
12. PARALLEL PORT	225
12.1 Printer Interface Logic.....	225
12.2 Enhanced Parallel Port (EPP).....	226
12.2.1 Data Port (Data Swapper)	226
12.2.2 Printer Status Buffer	226
12.2.3 Printer Control Latch and Printer Control Swapper.....	227
12.2.4 EPP Address Port.....	227
12.2.5 EPP Data Port 0-3	228
12.2.6 EPP Pin Descriptions.....	228
12.2.7 EPP Operation.....	228
12.2.8 EPP Version 1.9 Operation.....	229
12.2.9 EPP Version 1.7 Operation.....	229
12.3 Extended Capabilities Parallel (ECP) Port.....	229
12.3.1 ECP Register and Bit Map	230
12.3.2 Data and <i>ecpAFifo</i> Port	231
12.3.3 Device Status Register (DSR)	231
12.3.4 Device Control Register (DCR).....	231
12.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010	232
12.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011	232
12.3.7 TFIFO (Test FIFO Mode) Mode = 110	232
12.3.8 CNFGA (Configuration Register A) Mode = 111.....	232
12.3.9 CNFGB (Configuration Register B) Mode = 111.....	232
12.3.10 ECR (Extended Control Register) Mode = all	233
12.3.11 ECP Pin Descriptions	234
12.3.12 ECP Operation.....	235
12.3.12.1. Mode Switching	235
12.3.12.2. Command/Data	235
12.3.12.3. Data Compression	236
12.3.13 FIFO Operation.....	236
12.3.14 DMA Transfers.....	236
12.3.15 Programmed I/O (NON-DMA) Mode	236
13. KEYBOARD CONTROLLER.....	238
13.1 Output Buffer	238
13.2 Input Buffer.....	238
13.3 Status Register.....	239
13.4 Commands	240

13.5	Hardware GATEA20/Keyboard Reset Control Logic	242
13.5.1	KB Control Register (Logic Device 5, CR-F0).....	242
13.5.2	Port 92 Control Register (Default Value = 0x24).....	243
14.	CONSUMER INFRARED REMOTE (CIR).....	244
14.1	CIR Register Table.....	244
14.1.1	IR Configuration Register – Base Address + 0	244
14.1.2	IR Status Register – Base Address + 1	245
14.1.3	IR Interrupt Configuration Register – Base Address + 2	245
14.1.4	RX FIFO Count– Base Address + 5.....	246
14.1.5	IR TX Carrier Prescalar Configuration Register (CP) – Base Address + 4	246
14.1.6	IR TX Carrier Period Configuration Register (CC) – Base Address + 5	247
14.1.7	IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6	247
14.1.8	IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7.....	247
14.1.9	IR FIFO Configuration Register (FIFOCON) – Base Address + 8.....	247
14.1.10	IR Sample RX FIFO Status Register – Base Address + 9	248
14.1.11	IR Sample RX FIFO Register – Base Address + A.....	249
14.1.12	TX FIFO Count– Base Address + 5	249
14.1.13	IR Sample TX FIFO Register – Base Address + C	249
14.1.14	IR Carrier Count High Byte Register – Base Address + D	250
14.1.15	IR Carrier Count Low Byte Register – Base Address + E	250
14.1.16	IR FSM Status Register (IRFSM) – Base Address + F	250
14.1.17	IR Minimum Length Register – Base Address + F	251
15.	CONSUMER INFRARED REMOTE (CIR) WAKE-UP	252
15.1	CIR WAKE-UP Register Table.....	252
15.1.1	IR Configuration Register – Base Address + 0	252
15.1.2	IR Status Register – Base Address + 1	253
15.1.3	IR Interrupt Configuration Register – Base Address + 2	253
15.1.4	IR TX Configuration Register – Base Address + 3.....	254
15.1.5	IR FIFO Compare Tolerance Configuration Register – Base Address + 4.....	254
15.1.6	RX FIFO Count– Base Address + 5.....	254
15.1.7	IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6	255
15.1.8	IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7.....	255
15.1.9	IR FIFO Configuration Register (FIFOCON) – Base Address + 8.....	255
15.1.10	IR Sample RX FIFO Status Register – Base Address + 9	256
15.1.11	IR Sample RX FIFO Register – Base Address + A.....	256
15.1.12	Write FIFO – Base Address + B	256
15.1.13	Read FIFO Only – Base Address + C.....	257
15.1.14	Read FIFO Index – Base Address + D	257
15.1.15	Reserved – Base Address + E.....	257
15.1.16	IR FSM Status Register (IRFSM) – Base Address + F	258
15.1.17	IR Minimum Length Register – Base Address + F	258
16.	POWER MANAGEMENT EVENT	259
16.1	Power Control Logic.....	259
16.1.1	PSON# Logic	260
16.1.1.1	Normal Operation	260
16.1.2	AC Power Failure Resume	261
16.2	Wake Up the System by Keyboard and Mouse	262
16.2.1	Waken up by Keyboard events	262

16.2.2	Waken up by Mouse events.....	263
16.3	Resume Reset Logic.....	264
17.	SERIALIZED IRQ.....	265
17.1	Start Frame	265
17.2	IRQ/Data Frame.....	266
17.3	Stop Frame.....	266
18.	WATCHDOG TIMER.....	268
19.	GENERAL PURPOSE I/O.....	269
19.1	GPIO ARCHITECTURE	269
19.2	ACCESS CHANNELS.....	275
20.	PARALLEL VID (PVID).....	276
20.1	VID Input Detection.....	277
20.2	VID Output Control.....	277
20.3	VID Reset Source	277
21.	INTEL SERIAL VID (SVID)	279
22.	AMD SERIAL VID (SVID).....	283
23.	SMBUS MASTER INTERFACE.....	287
23.1	General Description	287
23.2	Introduction to the SMBus Master.....	287
23.2.1	Data Transfer Format	287
23.2.2	Arbitration	287
23.2.3	Clock Synchronization	288
23.3	SB-TSI.....	289
23.3.1	SB-TSI Address	289
23.4	PCH.....	289
23.4.1	Command Summary.....	289
23.5	SMBus Master.....	290
23.5.1	Block Diagram	290
23.5.2	Programming Flow.....	291
23.5.3	TSI Routine.....	292
23.5.4	PCH Routine.....	292
23.5.5	BYTE Ruttine	293
23.5.6	Manual Mode interface	293
23.6	Register Type Abbreviations.....	294
23.6.1	Enter the Extended Function Mode	294
23.6.2	Configure the Configuration Registers	295
23.7	SMBus Master Register Set.....	295
23.7.1	SMBus Register Map.....	295
23.7.2	SMBus Data (SMDATA) – Bank 0	295
23.7.3	SMBus Write Data Size (SMWRSIZE) – Bank 0	296
23.7.4	SMBus Command (SMCMD) – Bank 0	296
23.7.5	SMBus INDEX (SMIDX) – Bank 0	297
23.7.6	SMBus Control (SMCTL) – Bank 0	297
23.7.7	SMBus Address (SMADDR) – Bank 0	298
23.7.8	SCL FREQ (SCLFREQ) – Bank 0	298
23.7.9	PCH Address (PCHADDR) – Bank 0	299
23.7.10	SMBus Error Status (Error_status) – Bank 0	299

23.7.11 PCH Command (PCHCMD) – Bank 0	300
23.7.12 TSI Agent Enable Register (TSI_AGENT) – Bank	300
23.7.13 SMBus Control 3 Register (SMCTL3) – Bank 0.....	301
23.7.14 SMBus Control 2 Register (SMCTL2) – Bank 0.....	301
23.7.15 BYTE ADDRESS (BYTE ADDR) – Bank 0	302
23.7.16 BYTE INDEX_H (BYTE_IDX_H) – Bank 0	302
23.7.17 BYTE INDEX_L (BYTE_IDX_L) – Bank 0	303
24. CONFIGURATION REGISTER.....	304
24.1 Chip (Global) Control Register	304
24.2 Logical Device 0 (FDC)	328
24.3 Logical Device 1 (Parallel Port).....	331
24.4 Logical Device 2 (UART A)	334
24.5 Logical Device 3 (UART B, IR).....	336
24.6 Logical Device 5 (Keyboard Controller)	339
24.7 Logical Device 6 (CIR)	341
24.8 Logical Device 7 (GPIO6, GPIO7, GPIO8, GPIO9)	343
24.9 Logical Device 8 (WDT1, GPIO0, GPIO1, GPIOA).....	350
24.10 Logical Device 9 (GPIO2, GPIO3, GPIO4, GPIO5)	356
24.11 Logical Device A (ACPI).....	364
24.12 Logical Device B (Hardware Monitor, Front Panel LED)	374
24.13 Logical Device D (VID).....	380
24.14 Logical Device E (CIR WAKE-UP).....	385
24.15 Logical Device F (GPIO Push-pull or Open-drain selection)	386
24.16 Logical Device 14 (SVID).....	390
24.17 Logical Device 16 (Deep Sleep)	392
24.18 Logical Device 17 (GPIOA).....	394
25. SPECIFICATIONS	396
25.1 Absolute Maximum Ratings	396
25.2 DC CHARACTERISTICS	396
26. AC CHARACTERISTICS	399
26.1 Power On / Off Timing.....	399
26.2 AC Power Failure Resume Timing.....	400
26.3 Clock Input Timing	403
26.4 PECI Timing	404
26.5 SMBus Timing	404
26.6 Floppy Disk Drive Timing	405
26.7 UART/Parallel Port.....	407
26.8 Modem Control Timing	408
26.9 Parallel Port Mode Parameters.....	408
26.9.1 Parallel Port Timing	409
26.9.2 EPP Data or Address Read Cycle Timing Parameters	410
26.9.3 EPP Data or Address Read Cycle (EPP Version 1.9).....	411
26.9.4 EPP Data or Address Read Cycle (EPP Version 1.7).....	411
26.9.5 EPP Data or Address Write Cycle Timing Parameters	413
26.9.6 EPP Data or Address Write Cycle (EPP Version 1.9).....	414
26.9.7 EPP Data or Address Write Cycle (EPP Version 1.7).....	414
26.9.8 Parallel Port FIFO Timing Parameters	415

26.9.9	Parallel FIFO Timing.....	416
26.9.10	ECP Parallel Port Forward Timing Parameters.....	416
26.9.11	ECP Parallel Port Forward Timing	417
26.9.12	ECP Parallel Port Reverse Timing Parameters	417
26.9.13	ECP Parallel Port Reverse Timing.....	418
26.9.14	KBC Timing Parameters	418
26.9.15	Writing Cycle Timing.....	419
26.9.16	Read Cycle Timing	420
26.9.17	Send Data to K/B	420
26.9.18	Receive Data from K/B	420
26.9.19	Input Clock.....	421
26.9.20	Send Data to Mouse	421
26.9.21	Receive Data from Mouse	421
26.10	GPIO Timing Parameters.....	422
26.10.1	GPIO Write Timing.....	422
27.	TOP MARKING SPECIFICATIONS.....	423
28.	ORDERING INFORMATION.....	424
29.	PACKAGE SPECIFICATION	425
30.	REVISION HISTORY	427

LIST OF FIGURE

Figure 3-1 NCT6776F / NCT6776D Block Diagram.....	6
Figure 4-1 NCT6776F Pin Layout	7
Figure 4-2 NCT6776D Pin Layout.....	8
Figure 6-1 RSMRST#.....	31
Figure 6-2 PWROK	32
Figure 6-3 RESETCONI# and PWROK	32
Figure 6-4 RSTOUTX# and LRESET#.....	32
Figure 6-5 BKFD_CUT and LATCH_BKFD_CUT	34
Figure 7-1 Structure of the Configuration Register	52
Figure 7-2 Configuration Register	54
Figure 8-1 LPC Bus' Reads from / Write to Internal Registers	57
Figure 8-2 Serial Bus Write to Internal Address Register Followed by the Data Byte	58
Figure 8-3 Serial Bus Read from Internal Address Register.....	58
Figure 8-4 Analog Inputs and Application Circuit of the NCT6776F / NCT6776D	59
Figure 8-5 Monitoring Temperature from Thermistor.....	61
Figure 8-6 Monitoring Temperature from Thermal Diode (Voltage Mode).....	62
Figure 8-7 Monitoring Temperature from Thermal Diode (Current Mode).....	62
Figure 8-8 PECI Temperature	63
Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets	64
Figure 8-10 Mechanism of Thermal Cruise™ Mode (PWN Duty Cycle).....	68
Figure 8-11 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)	69
Figure 8-12 Mechanism of Fan Speed Cruise™ Mode	69
Figure 8-13 SMART FAN™ IV & Close Loop Fan Control Mechanism	71
Figure 8-14 Fan Control Duty Mode Programming Flow	73
Figure 8-15 Close-Loop Fan Control RPM mode Programming Flow	74
Figure 8-16 SYS TEMP and Weight Value Relations	76
Figure 8-17 Fan Control Weighting Duty Mode Programming Flow	77
Figure 8-18 SMI Mode of Voltage and Fan Inputs	78
Figure 8-19 Shut-down Interrupt Mode	79
Figure 8-20 SMI Mode of SYSTIN I	80
Figure 8-21 SMI Mode of SYSTIN II	80
Figure 8-22 Shut-down Interrupt Mode	81
Figure 8-23 SMI Mode of CPUTIN	82
Figure 8-24 OVT# Modes of Temperature Inputs	84
Figure 8-25 Caseopen Mechanism	85
Figure 8-26 Power measurement architecture.....	86
Figure 13-1 Keyboard and Mouse Interface.....	238
Figure 16-1 Power Control Mechanism.....	260
Figure 16-2 Power Sequence from S5 to S0, then Back to S5.....	261
Figure 16-3 The previous state is "on"	262
Figure 16-4 The previous state is "off"	262
Figure 16-5 Mechanism of Resume Reset Logic.....	264

Figure 17-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1	265
Figure 17-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period.....	267
Figure 23-1 Data Transfer Format	287
Figure 23-2 SMBus Arbitration.....	288
Figure 23-3 Clock synchronization.....	288
Figure 23-4 SMBus Master Block Diagram.....	290
Figure 23-5 Programming Flow.....	291
Figure 23-6 TSI Routine	292
Figure 23-7 PCH Routine	292
Figure 23-8 PCH Routine	293
Figure 23-9 Manual Mode Programming Flow.....	294

LIST OF TABLE

Table 6-1 Pin Description	31
Table 7-1 Devices of I/O Base Address	53
Table 8-1 Temperature Data Format	61
Table 8-2 Relative Registers – at Thermal CruiseTM Mode.....	70
Table 8-3 Relative Registers – at Speed CruiseTM Mode.....	70
Table 8-4 Relative Register-at SMART FANTM IV Control Mode	71
Table 8-5 Relative Register-at Weight Value Control	76
Table 8-6 Relative Register of SMI functions.....	82
Table 8-7 Relative Register of OVT functions.....	83
Table 10-1 The Delays of the FIFO.....	198
Table 11-1 Register Summary for UART	218
Table 12-1 Pin Descriptions for SPP, EPP, and ECP Modes	225
Table 12-2 EPP Register Addresses	226
Table 12-3 Address and Bit Map for SPP and EPP Modes	226
Table 12-4 ECP Mode Description.....	229
Table 12-5 ECP Register Addresses	230
Table 12-6 Bit Map of the ECP Registers	230
Table 13-1 Bit Map of Status Register	239
Table 13-2 KBC Command Sets	240
Table 14-1 CIR Register Table	244
Table 16-1 Bit Map of Logical Device A, CR[E4h], Bits[6:5]	261
Table 16-2 Definitions of Mouse Wake-Up Events	263
Table 16-3 Timing and Voltage Parameters of RSMRST#.....	264
Table 17-1 SERIRQ Sampling Periods	266
Table 19-1 Relative Control Registers of GPIO 41, 46, 92 and 93 that Support Wake-Up Function	269
Table 23-1 SB-TSI Address Encoding	289
Table 23-2 PCH Command Summary	289
Table 23-3 SMBus Master Bank 0 Registers	295

1. GENERAL DESCRIPTION

The NCT6776F / NCT6776D is a member of Nuvoton's Super I/O product line. The NCT6776F / NCT6776D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the NCT6776F / NCT6776D adopts the Current Mode (dual current source) and thermistor sensor approach. The NCT6776F / NCT6776D also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ IV, which makes the system more stable and user-friendly.

The NCT6776F / NCT6776D supports four – 360K, 720K, 1.2M, 1.44M, or 2.88M – disk drive types and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s. The disk drive adapter supports the functions of floppy disk drive controller (compatible with the industry standard 82077/ 765), data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. Such a wide range of functions integrated into one NCT6776F / NCT6776D greatly reduce the number of required components to interface with floppy disk drives.

The NCT6776F / NCT6776D provides two high-speed serial communication port (UART), which includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The NCT6776F / NCT6776D supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP). The NCT6776F / NCT6776D supports keyboard and mouse interface which is 8042-based keyboard controller.

The NCT6776F / NCT6776D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The NCT6776F / NCT6776D supports the Intel® PECL (Platform Environment Control Interface) and AMD® SB-TSI interface. The NCT6776F / NCT6776D supports separated VID input and output pins for Vcore voltage adjustment. It also supports AMD® CPU power on sequence, and it also supports Intel® Deep Sleep Well glue logic to help customers to reduce the external circuits needed while using Deep Sleep Well function.

The NCT6776F / NCT6776D supports to decode port 80 diagnostic messages on the LPC bus. This could help on system power on debugging. It also supports two-color LED control to indicate system power states. The NCT6776F / NCT6776D supports Consumer IR function for remote control purpose. It also supports Advanced Power Saving function to further reduce the power consumption while the system is at S5 state.

The configuration registers inside the NCT6776F / NCT6776D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

2. FEATURES

General

- Meet LPC Specification 1.1
- Support AMD power on sequence
- Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
- Integrated hardware monitor functions
- Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
- Programmable configuration settings
- Single 24-MHz or 48-MHz clock input
- Support selective pins of 5 V tolerance

FDC

- Variable write pre-compensation with track-selection capability
- Support vertical recording format
- DMA-enable logic
- 16-byte data FIFO
- Support floppy disk drives and tape drives
- Detect all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD-write enable signal (write data signal forced to be inactive)
- Support 3.5-inch or 5.25-inch floppy disk drives
- Compatible with industry standard 82077
- 360K / 720K / 1.2M / 1.44M / 2.88M formats
- 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD and its Windows driver

UART

Two high-speed, 16550-compatible UART with 16-byte send / receive FIFO

Support RS485

--- Supports auto flow control

Fully programmable serial-interface characteristics:

--- 5, 6, 7 or 8-bit characters

--- Even, odd or no parity bit generation / detection

--- 1, 1.5 or 2 stop-bit generation

Internal diagnostic capabilities:

--- Loop-back controls for communications link fault isolation

--- Break, parity, overrun, framing error simulation

Programmable baud rate generator allows division of clock source by any value from 1 to $(2^{16}-1)$

Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

Parallel Port

Compatible with IBM® parallel port
Support PS/2-compatible bi-directional parallel port
Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
Enhanced printer port back-drive current protection

Keyboard Controller

8042-based keyboard controller
Asynchronous access to two data registers and one status register
Software-compatible with 8042
Support PS/2 mouse
Support Port 92
Support both interrupt and polling modes
Fast Gate A20 and Hardware Keyboard Reset
12MHz operating frequency

Hardware Monitor Functions

Smart Fan control system
Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode
Support Current Mode (dual current source) temperature sensing method
Nine voltage inputs (CPUVCORE, VIN[0..3], 3VCC, AVCC, 3VSB and VBAT)
Five fan-speed monitoring inputs
Three fan-speed controls
Dual mode for fan control (PWM and DC) for SYSFANOUT
Built-in case-open and CPU socket occupied detection circuit
Programmable hysteresis and setting points for all monitored items
Issue SMI#, OVT# (Over-temperature) to activate system protection
Nuvoton Health Manager support
Provide I²C master / slave interface to read / write registers

CIR and IR (Infrared)

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR, including CIRTX, CIRRX, CIRRXWB, CIR LED, CIR SENSE

VCORE Voltage Adjustment

Support INTEL® VRM11.1 VID input to VID output
Watch Dog Timer for VID over-voltage failure recovery
Support AMD® Parallel VID input to VID output
Support Intel® VR12 SVID
Support AMD® Serial VID input to Serial VID output

General Purpose I/O Ports

GPIO0 ~ GPIOA programmable general purpose I/O ports

Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access.

ACPI Configuration

Support Glue Logic functions

Support general purpose Watch Dog Timer functions

OnNow Functions

Keyboard Wake-Up by programmable keys

Mouse Wake-Up by programmable buttons

OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

Support PECI 1.1, 2.0 and 3.0 specification

Support 2 CPU addresses and 2 domains per CPU address

AMD SB-TSI Interface

Support AMD® SB-TSI specification

SMBus Interface

Support SMBus Slave interface to report Hardware Monitor device data

Support SMBus Master interface to get thermal data from PCH

Support SMBus Master interface to get thermal data from MXM module

Power Measurement

Support Power Consumption measurement

Fading LED driver control for power status and diagnostic indications

Intel Deep Sleep Well (DSW) Glue Logic

Support Deep Sleep Well (DSW) Glue Logic

AMD® CPU Power on Sequence

Support AMD® CPU power on sequence

Advanced Power Saving

Advanced Sleep State Control to save motherboard Stand-by power consumption

Operation voltage

- 3.3 voltage

Package

NCT6776F 128-pin QFP

NCT6776D 128-pin LQFP

Green