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NCT7290

16 Channel ADC, 12 Channel DAC, Internal Temp Sensor with I²C & SPI Interface

The NCT7290 is a serially programmable voltage and temperature monitor. It can monitor its on chip temperature via its local sensor, a remotely connected diode and 16 analog inputs. Two 12 bit DACs allow for voltage control on 12 pins. Eight GPIO pins allow digital control and monitoring. An $\overline{\text{ALERT}}$ output is also available to signal out-of-limit conditions.

Communication with the NCT7290 is accomplished via an I²C interface which is compatible with industry standard protocols or a 4 wire SPI interface. Both interfaces are available on this device. Through these interfaces the NCT7290s internal registers may be accessed. These registers allow the user to read the current temperature and input voltages, change the configuration settings, adjust each channels limits and set set the output DAC voltages on each of the 12 channels available.

The NCT7290 is available in a 56-lead QFN ($8 \times 8 \times 0.5$ mm) package and operates over a supply range of 5.0 V ±10% (digital supply range of 3 V to 3.6 V) and temperature range of –55 to +125°C. This makes the NCT7290 ideal for a wide variety of applications ranging from cellular base stations to servers and industrial controls.

Features

- On-chip Temperature Sensor (±2°C Accuracy)
- Remote Temperature Sensor
- 5.0 V ±10% Supply Range
- 16 Analog Voltage Inputs
- 12 DAC Output Channels
- 8 Digital GPIO Pins
- SPI and I²C Interface
- Package Type: 56 Lead QFN
- These Devices are Pb-Free and are RoHS Compliant

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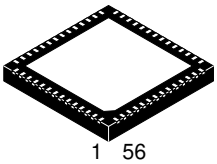
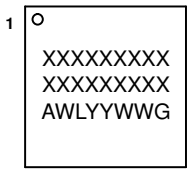


QFN–56
CASE 485BK

MARKING DIAGRAM



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCT7290MNTXG	QFN–56	2000 Tape & Reel with MPQ

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

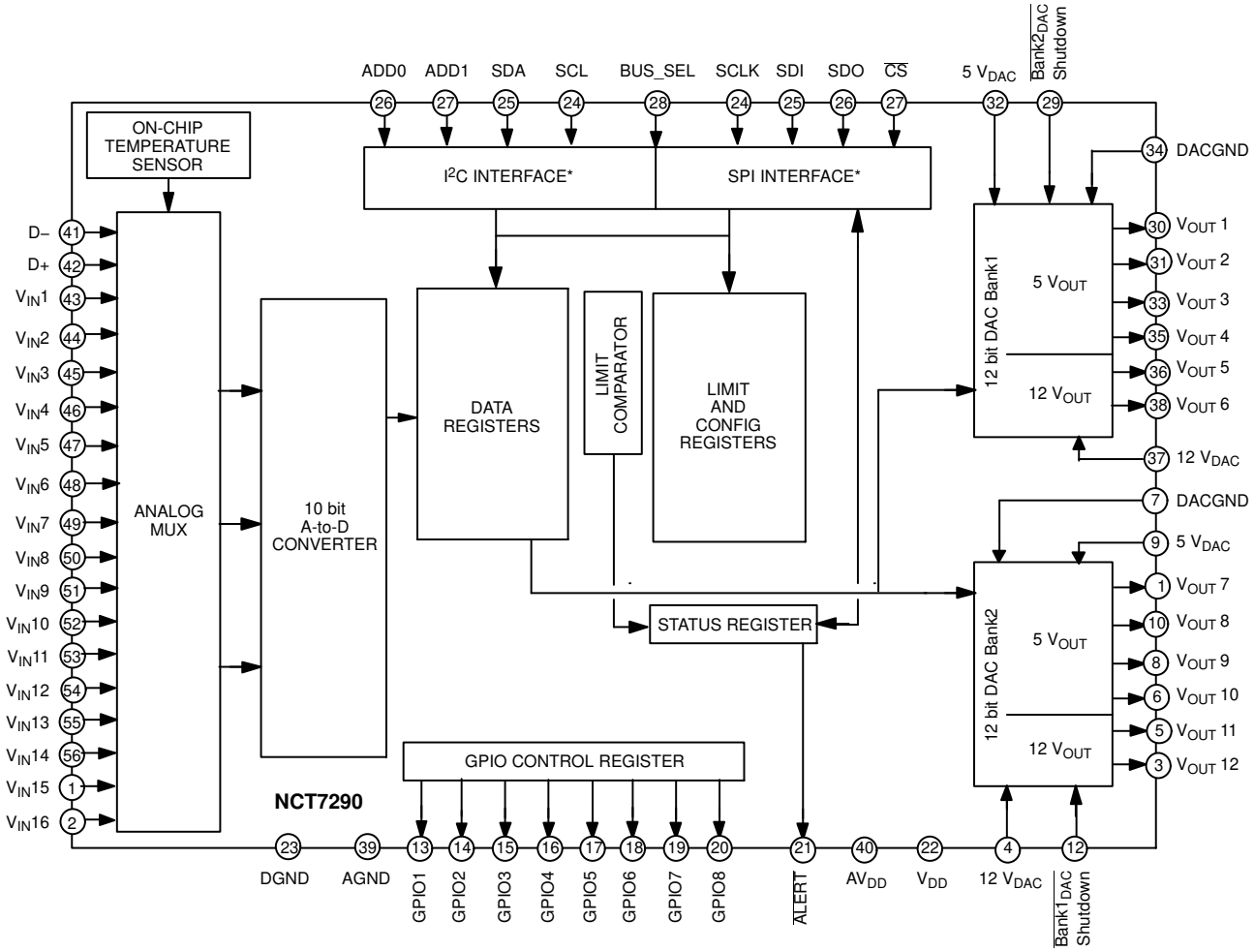


Figure 1. Functional Block Diagram of NCT7290

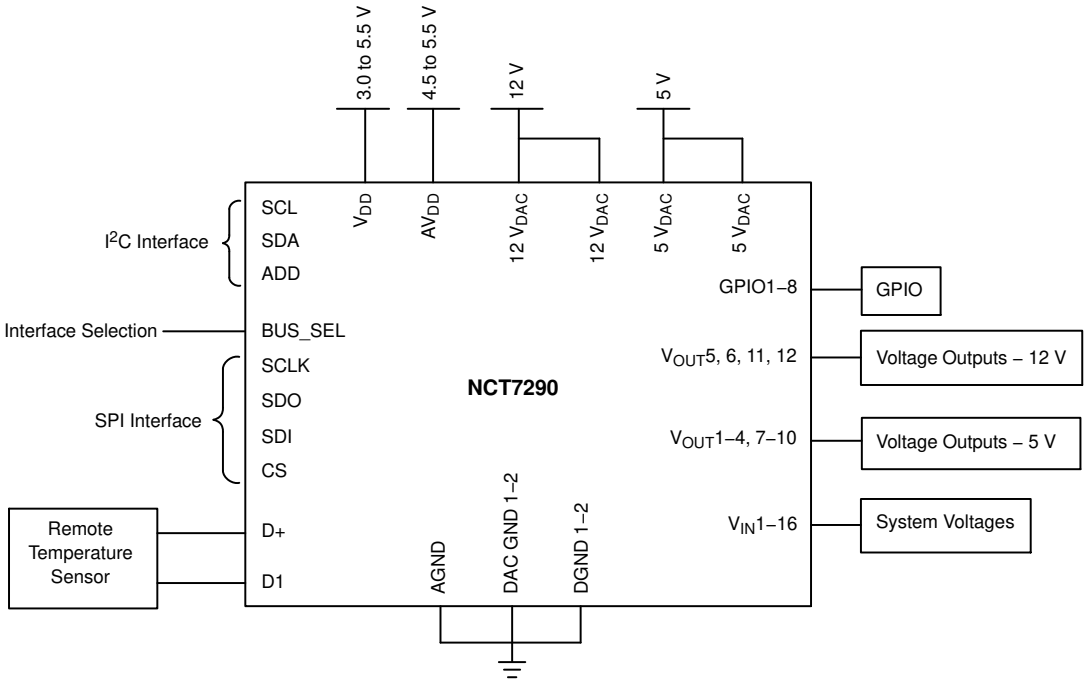
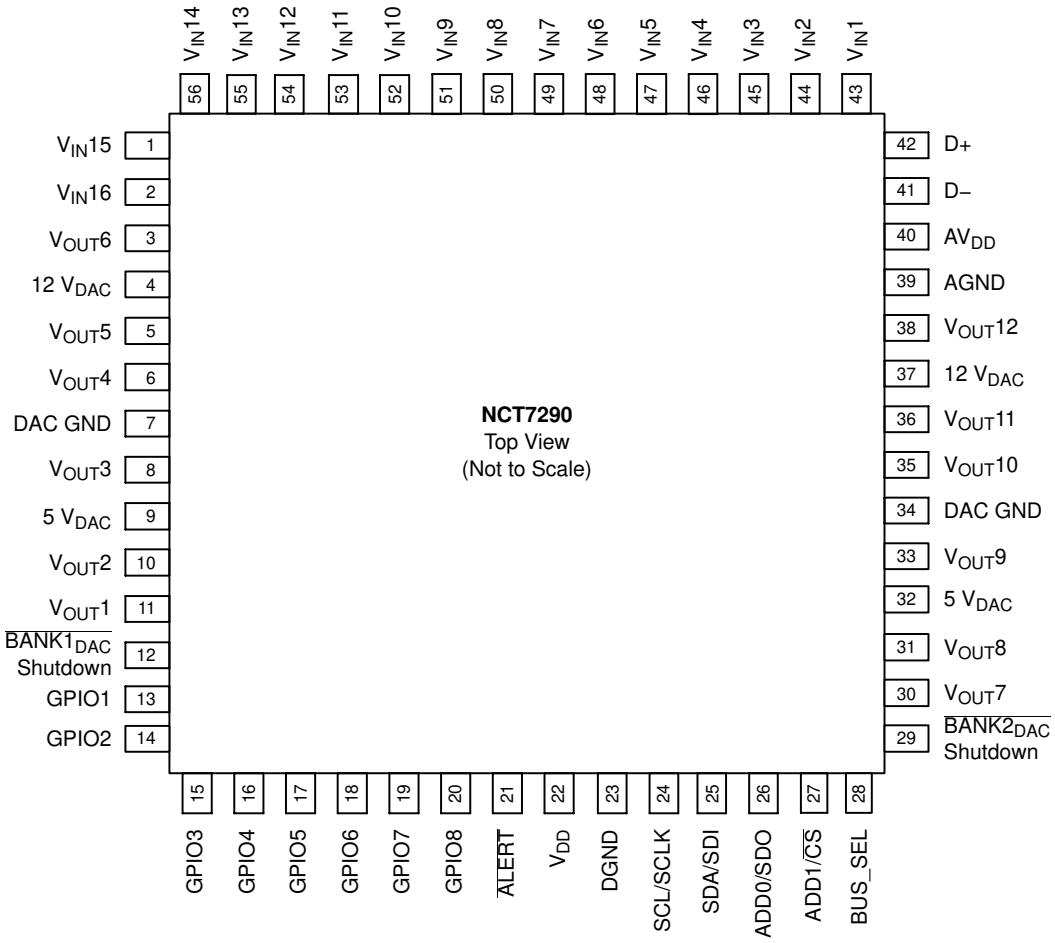


Figure 2. Typical Application Circuit



Note: GND Flag Located Underneath NCT7290

Figure 3. Pin Connections

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	$V_{IN}15$	Analog Input. 0 V to 2.5 V.
2	$V_{IN}16$	Analog Input. 0 V to 2.5 V.
3	$V_{OUT}6$	Analog Output. 0 V to 12 V.
4	$12V_{DAC}$	Analog Supply. Analog supply pins for the DAC output amplifiers on $V_{OUT}5$–6.
5	$V_{OUT}5$	Analog Output. 0 V to 12 V.
6	$V_{OUT}4$	Analog Output. 0 V to 5 V.
7	DACGND	Ground pin for the DAC output amplifiers.
8	$V_{OUT}3$	Analog Output. 0 V to 5 V.
9	$5V_{DAC}$	Analog Supply. Analog supply pin for the DAC output amplifiers on $V_{OUT}1$–4.
10	$V_{OUT}2$	Analog Output. 0 V to 5 V.
11	$V_{OUT}1$	Analog Output. 0 V to 5 V.
12	$\overline{BANK1_{DAC}}$ Shutdown	Shutdown pin for Bank1 DAC outputs ($V_{OUT}1$, $V_{OUT}2$, $V_{OUT}3$, $V_{OUT}4$, $V_{OUT}5$ and $V_{OUT}6$). Active low input (i.e. tie low to shutdown the bank). Active low input. Pin cannot be left floating.
13	GPIO1	Programmable general purpose digital input or output. Default = input.
14	GPIO2	Programmable general purpose digital input or output. Default = input.
15	GPIO3	Programmable general purpose digital input or output. Default = input.
16	GPIO4	Programmable general purpose digital input or output. Default = input.

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Pin Name	Description
17	GPIO5	Programmable general purpose digital input or output. Default = input.
18	GPIO6	Programmable general purpose digital input or output. Default = input.
19	GPIO7	Programmable general purpose digital input or output. Default = input.
20	GPIO8	Programmable general purpose digital input or output. Default = input.
21	$\overline{\text{ALERT}}$	Open-Drain Logic Output Used as Interrupt or SMBus Alert. Active low output.
22	V_{DD}	Power Supply. Can be powered from a supply in the range 3.3 V or 5.0 V ±10%
23	DGND	Digital Ground. This is the ground pin for all the digital circuitry.
24	SCL/SCLK	Serial Clock Input for I^2C and SPI interfaces
25	SDA/SDI	Serial Data Input/Output in I^2C mode. Serial Data Input in SPI mode.
26	ADD0/SDO	Address selection pin for I^2C mode. Can be tied high, low or left floating to give multiple address options. Serial Data Out in SPI mode.
27	ADD1/CS	Address selection pin for I^2C mode. Can be tied high, low or left floating to give multiple address options. Chip Select. Slave transmit enable in SPI mode – active low.
28	BUS_SEL	Selects I^2C or SPI interface. BUS_SEL = DGND selects I^2C; BUS_SEL = V_{DD} selects SPI.
29	$\overline{\text{BANK2}_{\text{DAC}}}$ Shutdown	Shutdown pin for Bank1 DAC outputs ($V_{OUT}7$, $V_{OUT}8$, $V_{OUT}9$, $V_{OUT}10$, $V_{OUT}11$ and $V_{OUT}12$). Active low input (i.e. tie low to shutdown the bank). Active low input. Pin cannot be left floating.
30	$V_{OUT}7$	Analog Output. 0 V to 5 V.
31	$V_{OUT}8$	Analog Output. 0 V to 5 V.
32	$5V_{DAC}$	Analog Supply. Analog supply pin for the DAC output amplifiers on $V_{OUT}7$–10.
33	$V_{OUT}9$	Analog Output. 0 V to 5 V.
34	DACGND	Ground pin for the DAC output amplifiers.
35	$V_{OUT}10$	Analog Output. 0 V to 5 V.
36	$V_{OUT}11$	Analog Output. 0 V to 12 V.
37	$12V_{DAC}$	Analog Supply. Analog supply pins for the DAC output amplifiers on $V_{OUT}11$–12.
38	$V_{OUT}12$	Analog Output. 0 V to 12 V.
39	AGND	Analog ground. This is the ground pin for all the analog circuitry.
40	AV_{DD}	Analog Power Supply. Can be powered from a supply in the range 5.0 V ±10%.
41	D–	Negative Connection to Remote Temperature Sensor.
42	D+	Positive Connection to Remote Temperature Sensor.
43	$V_{IN}1$	Analog Input. 0 V to 2.5 V.
44	$V_{IN}2$	Analog Input. 0 V to 2.5 V.
45	$V_{IN}3$	Analog Input. 0 V to 2.5 V.
46	$V_{IN}4$	Analog Input. 0 V to 2.5 V.
47	$V_{IN}5$	Analog Input. 0 V to 2.5 V.
48	$V_{IN}6$	Analog Input. 0 V to 2.5 V.
49	$V_{IN}7$	Analog Input. 0 V to 2.5 V.
50	$V_{IN}8$	Analog Input. 0 V to 2.5 V.
51	$V_{IN}9$	Analog Input. 0 V to 2.5 V.
52	$V_{IN}10$	Analog Input. 0 V to 2.5 V.
53	$V_{IN}11$	Analog Input. 0 V to 2.5 V.
54	$V_{IN}12$	Analog Input. 0 V to 2.5 V.
55	$V_{IN}13$	Analog Input. 0 V to 2.5 V.
56	$V_{IN}14$	Analog Input. 0 V to 2.5 V.
	GND	QFN GND flag located underneath package.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	AV_{DD}	5.7	V
Supply Voltage	DV_{DD}	5.7	V
Input Voltage on SCL, SDA, A2, A1 and A0		−0.3 V to DV_{DD} + 0.3 V	V
Voltage on All Other Pins Except 12 V_{DAC} Outputs		−0.3 V to AV_{DD} + 0.3 V	V
Input Current on All Other Pins		5	mA
Input Current on SDA, A2, A1 and A0	I_{IN}	−1 mA to +50 mA	mA
Maximum Junction Temperature	$T_{J(max)}$	150.7	°C
Operating Temperature Range	T_{OP}	−55 to 125	°C
Storage Temperature Range	T_{STG}	−65 to 160	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
   ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN-56 (Note 3) Thermal Resistance, Junction-to-Air (Note 4) Thermal Reference, Junction-to-Board (Note 4)	 $R_{\theta JA}$ $R_{\Psi JB}$	 25 4	°C/W

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. As measured using a copper heat spreading area of 650 mm^2 (or 1 in^2), of 1 oz copper thickness.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	V_{DD}	3.0	–	3.6	V
	AV_{DD}	4.5	–	5.5	V
5 V_{DAC} Supply	$5V_{DAC}$	–	5	5.5	V
12 V_{DAC} supply	$12V_{DAC}$	–	12	13.2	V
Operating Ambient Temperature Range	T_A	−55	–	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

ELECTRICAL CHARACTERISTICS

$T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = 5.0 V ±10%. All specifications for −55°C to +125°C, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
TEMPERATURE SENSOR					
Local Sensor Accuracy AV_{DD} = 5.0 V ±10%	T_A = −40°C to +105°C, AV_{DD} = 5 V	–	–	±3	°C
	T_A = −55°C to +125°C, AV_{DD} = 5 V	–	–	±3.5	°C
Local Temperature Resolution		–	0.25	–	°C
Remote Sensor Accuracy AV_{DD} = 5.0 V ±10%	T_A = −40°C to +105°C, AV_{DD} = 5 V	–	–	±2	°C
	T_A = −55°C to +125°C, AV_{DD} = 5 V	–	–	±2.25	°C
Remote Temperature resolution		–	0.25	–	°C

ELECTRICAL CHARACTERISTICS (continued)
$T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = 5.0 V ±10%. All specifications for –55°C to +125°C, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
TEMPERATURE SENSOR					
Remote Sensor Current	High Level 1	–	240	–	μA
	Low Level 1	–	30	–	μA
	High Level 2	–	300	–	μA
	Low Level 2	–	37.5	–	μA
Temperature Conversion Time	Averaging On	–	38	–	ms
	Averaging Off	–	25	–	ms
D– Voltage		–	0.7	–	V
ADC					
ADC Resolution		–	10	–	Bits
Input Voltage Range		0	–	2.5	V
Input Impedance	Converting	–	1	–	MΩ
Input Capacitance		–	15	–	pF
Input Leakage Current		–	±1	–	μA
Integral Linearity		–	–	±1	LSB
Differential Linearity		–	–	±1	LSB
Offset Error		–	±1	±4	LSB
Gain Error		–	–	±5	LSB
Conversion Time	2 × 2.5 μs ADCs in Parallel	–	5	–	μs
DAC					
Output Voltage Range	V_{OUT}1–4, V_{OUT}7–10	0	–	5.25*	V
	V_{OUT}5–6, V_{OUT}11–12	0	–	12.5*	V
Output Current	Fullscale Output	–	±10	–	mA
Resolution		–	12	–	bits
Integral Linearity	200 mV to V_{DD} – 200 mV	–	±1	±2	LSB
Differential Linearity		–	–	±1	LSB
Offset Error	Output: 0–5 V (200 mV to DAC Supply – 200 mV)	–	±1	±10	mV
	Output: 0–12 V (200 mV to DAC Supply – 200mV)	–	±3	±25	mV
Gain Error	Output: 0–5 V (200 mV to DAC Supply – 200 mV)	–	±5	±15	LSB
	Output: 0–12 V (200 mV to DAC Supply – 200 mV)	–	±5	±25	LSB
Gain Error Drift		–	±10	–	ppmFS/°C
Settling Time	Output = 1/4 to 3/4 of Fullscale, 2 kΩ // 200 pF Load	–	3.5	10	μs
Overshoot	Output = 1/4 to 3/4 of Fullscale, 2 kΩ // 200 pF Load	–	200	–	mV
Crosstalk	Midscale Code	–	1	–	LSB
Slew Rate	Measure between 3/8 and 5/8	–	1500	–	mV/μs
POWER REQUIREMENTS					
Supply Voltage (AV_{DD})		4.5	5.0	5.5	V
Supply Current (I_{AVDD})		–	7.5	10	mA
Digital Supply Voltage (V_{DD})		3.0	3.3	3.6	V
Supply Current (I_{VDD})		–	2	5	mA

ELECTRICAL CHARACTERISTICS (continued)
$T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = 5.0 V ±10%. All specifications for –55°C to +125°C, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
OPEN DRAIN DIGITAL OUTPUT (SDA & ALERT)					
Current Sink I_{OL}		–	–	8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = –4.0 mA	–	–	0.6	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{DD}$	–	0.1	20	μA
GPIOs					
Input High Voltage V_{IH}		1.6	–	V_{DD}	V
Input Low Voltage, V_{IL}		0	–	0.8	V
Output Low Voltage, V_{OL}		–	–	0.4	V
Input Capacitance		–	5	–	pF
I²C INTERFACE INPUT (SCL)					
Input High Voltage V_{IH}	V_{DD} = 3.3 V, I_{IH} = 5 μA	2	–	V_{DD} + 0.3	V
Input Low Voltage, V_{IL}	V_{DD} = 3.3 V, I_{IL} = –5 μA	0	–	0.8	V
Input Capacitance		–	5	–	pF
SPI INTERFACE INPUT (SDI, SCLK, CS, BUS_SEL)					
Input High Voltage V_{IH}	V_{DD} = 3.3 V, I_{IH} = 5 μA	2	–	V_{DD} + 0.3	V
Input Low Voltage, V_{IL}	V_{DD} = 3.3 V, I_{IL} = –5 μA	0	–	0.8	V
Input Capacitance		–	5	–	pF
SPI INTERFACE OUTPUT (SDO)					
Output High Voltage, V_{OH}	V_{DD} = 3.3 V, I_{OL} = 3 μA	2.4	–	V_{DD}	V
Output Low Voltage, V_{OL}	V_{DD} = 3.3 V, I_{OL} = –3 μA	0	–	0.4	V
GENERAL INTERFACE INFORMATION					
Bit Rate	SPI	–	–	5	MHz
	I²C FS Mode	–	–	400	kHz

Table 1. I²C TIMING

Parameter (Note 6)	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Clock Frequency	f_{SCLK}	10	–	400	kHz
Clock Period	t_{SCLK}	2.5	–	–	μs
SCL High Time	t_{HIGH}	0.6	–	–	μs
SCL Low Time	t_{LOW}	1.3	–	–	μs
Start Setup Time	$t_{SU;STA}$	0.6	–	–	μs
Start Hold Time (Note 7)	$t_{HD;STA}$	0.6	–	–	μs
Data Setup Time (Note 8)	$t_{SU;DAT}$	100	–	–	ns
Data Hold Time (Note 9)	$t_{HD;DAT}$	0.3	–	0.9	μs
SCL, SDA Rise Time	t_r	–	–	300	ns
SCL, SDA Fall Time	t_f	–	–	300	ns
Stop Setup Time	$t_{SU;STO}$	0.6	–	–	μs
Bus Free Time	t_{BUF}	1.3	–	–	μs
Glitch Immunity	t_{SW}	–	50	–	ns

6. Guaranteed by design, but not production tested
7. Time from 10% of SDA to 90% of SCL
8. Time for 10%or 90% of SDA to 10% of SCL
9. A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

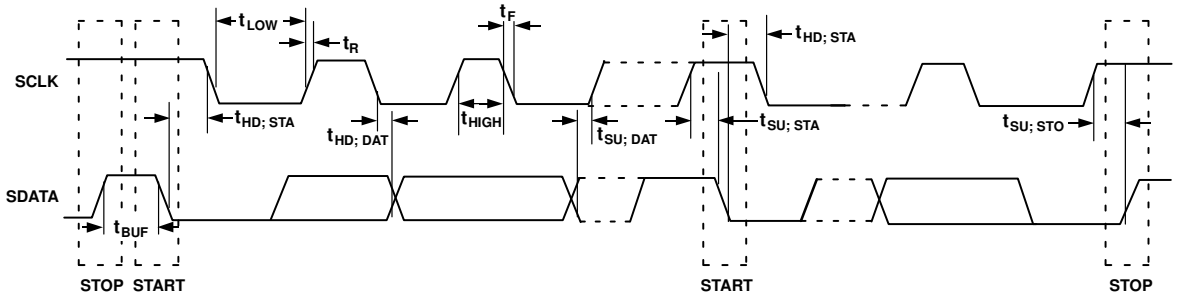


Figure 4. I²C Timing Diagram

Table 2. SPI TIMING

Parameter (Note 10)	**Symbol**	**Min**	**Max**	**Unit**
SPI Clock Freq	f_{SCLK}	–	5	MHz
SPI Clock Period	t_{SCLK}	200	–	ns
$\overline{CS}$ Falling Edge to SCLK Falling Edge	t_{DELAY}	15	–	ns
SCLK Rising Edge to CS Rising Edge	t_{QUIET}	15	–	ns
$\overline{CS}$ Rising Edge to SDO Disabled	t_{DIS}	–	110	ns
$\overline{CS}$ Deassertion between SPI Communications	$t_{CS,DIS}$	250	–	ns
SCLK Low Pulse Width	t_S	$0.4 \times t_{SCLK}$	–	ns
SCLK High Pulse Width	t_M	$0.4 \times t_{SCLK}$	–	ns
SCLK Falling Edge to SDO Transition	t_{SDO}	–	100	ns
SDI Valid before SCLK Rising Edge	t_{SETUP}	15	–	ns
SDI Valid after SCLK Rising Edge	t_{HOLD}	15	–	ns

10. Guaranteed by design, but not production tested

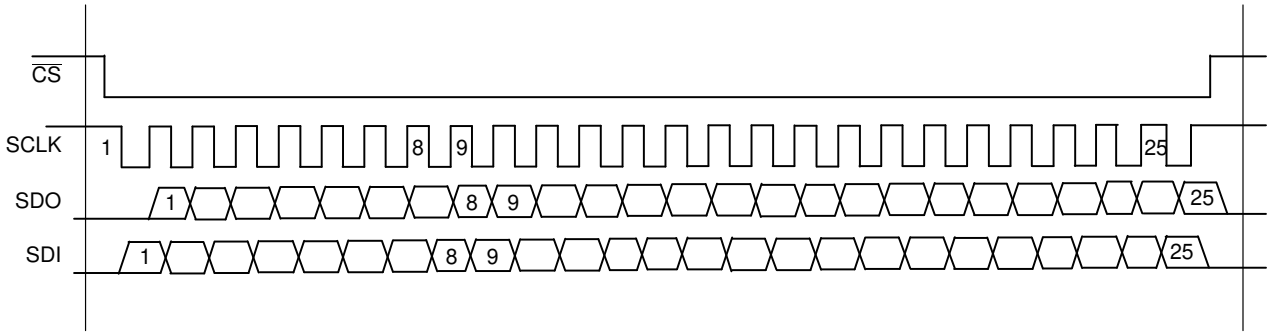


Figure 5. SPI Timing Diagram

TYPICAL CHARACTERISTICS

(T_A = +25°C, V_{DD} = +3.3 V, AV_{DD} = 5 V, unless otherwise stated)

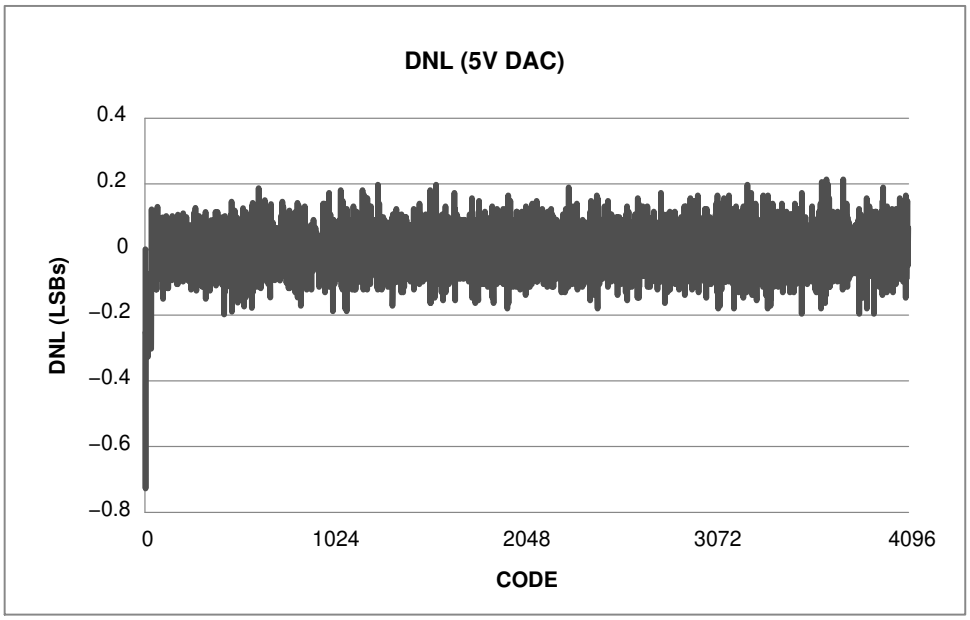


Figure 6. DNL vs Code at 25°C for 5 V DAC OUTPUT

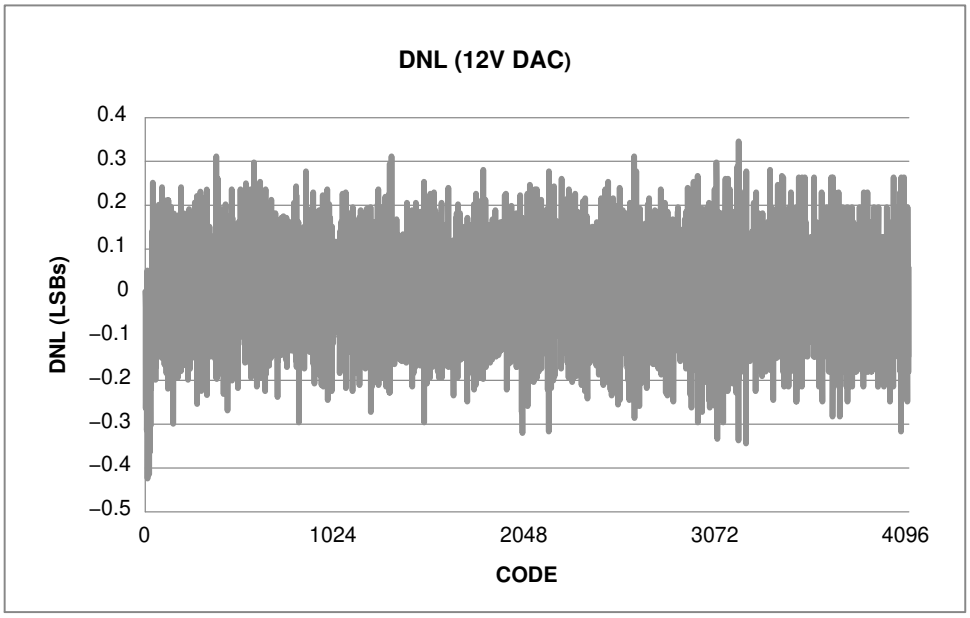


Figure 7. DNL vs Code at 25°C for 12 V DAC OUTPUT

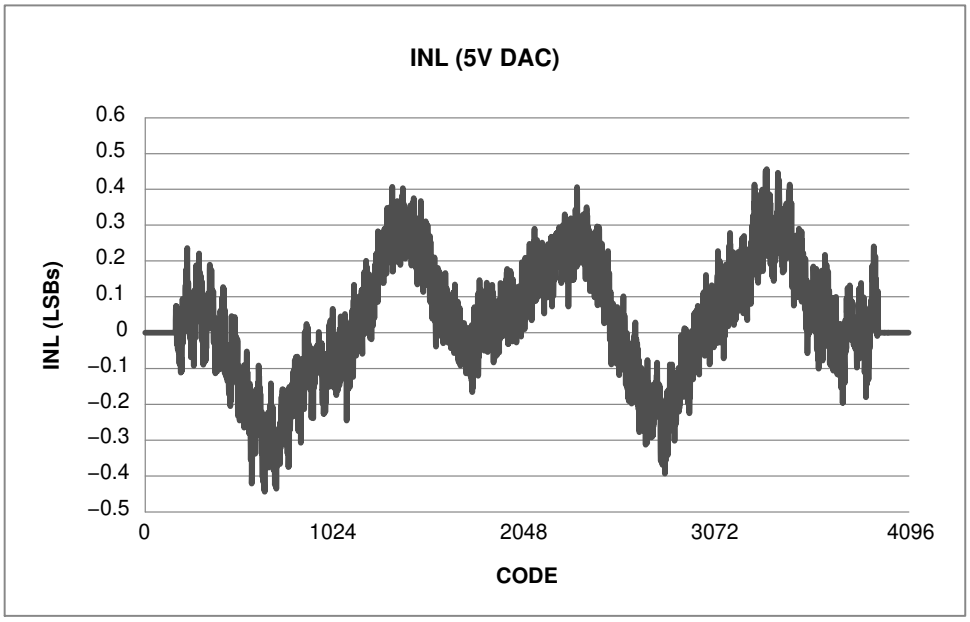


Figure 8. INL vs Code at 25°C for 5 V DAC OUTPUT

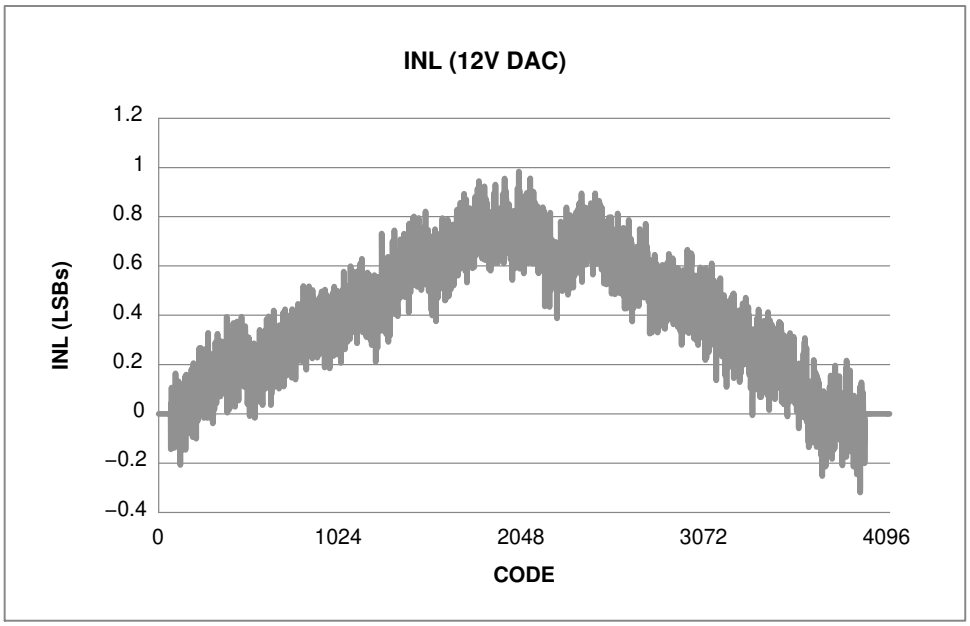


Figure 9. INL vs Code at 25°C for 12 V DAC OUTPUT

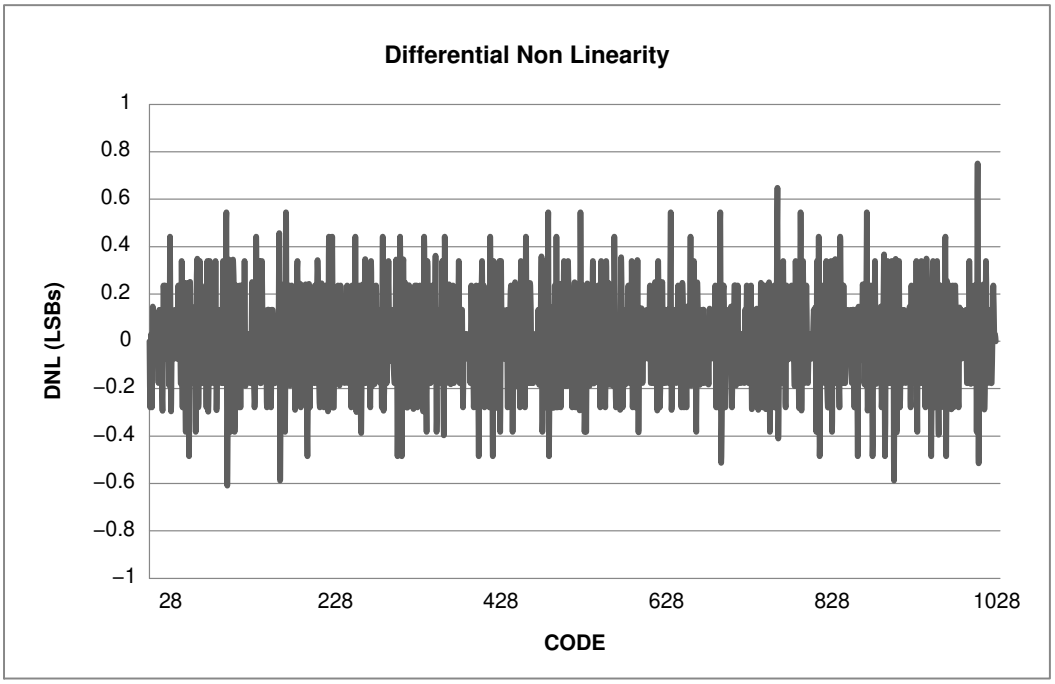


Figure 10. ADC DNL vs Code at 25°C

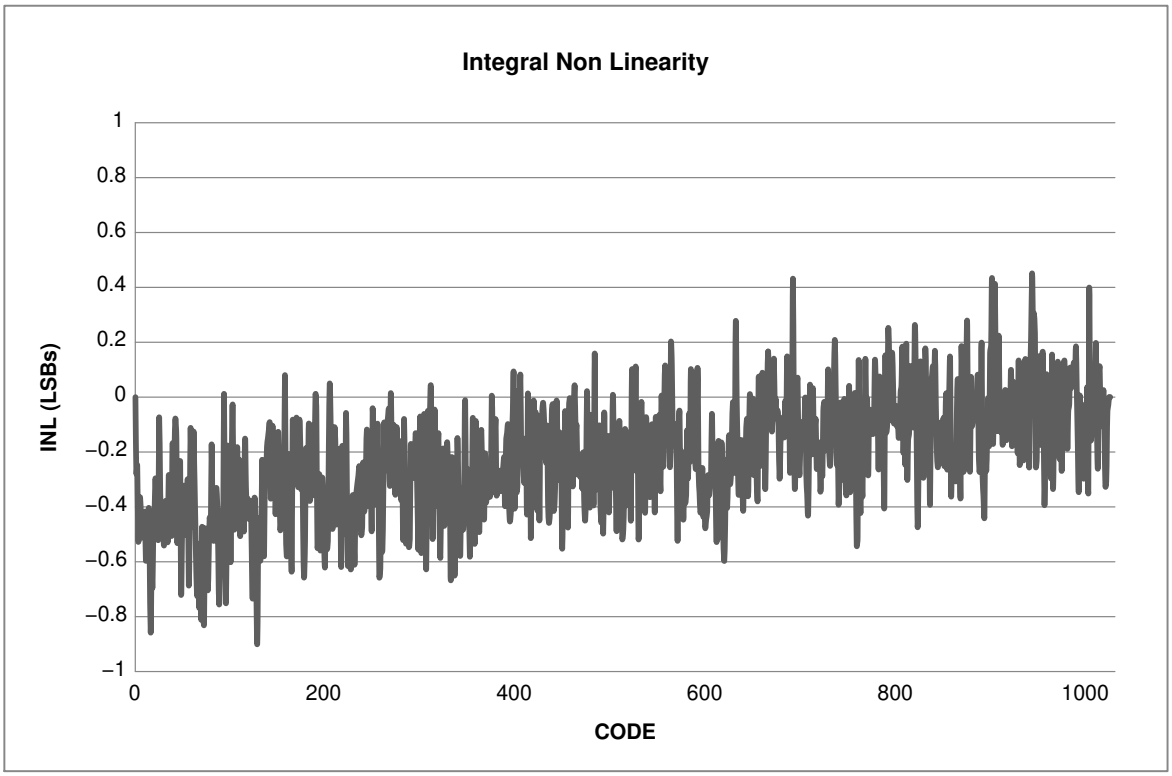


Figure 11. ADC INL vs Code at 25°C

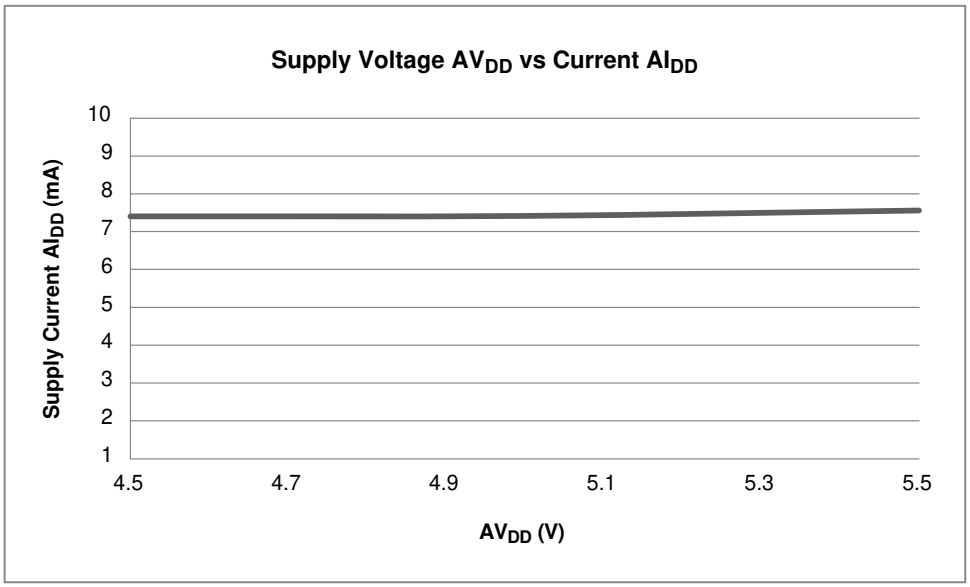


Figure 12. Supply Current vs Supply Voltage

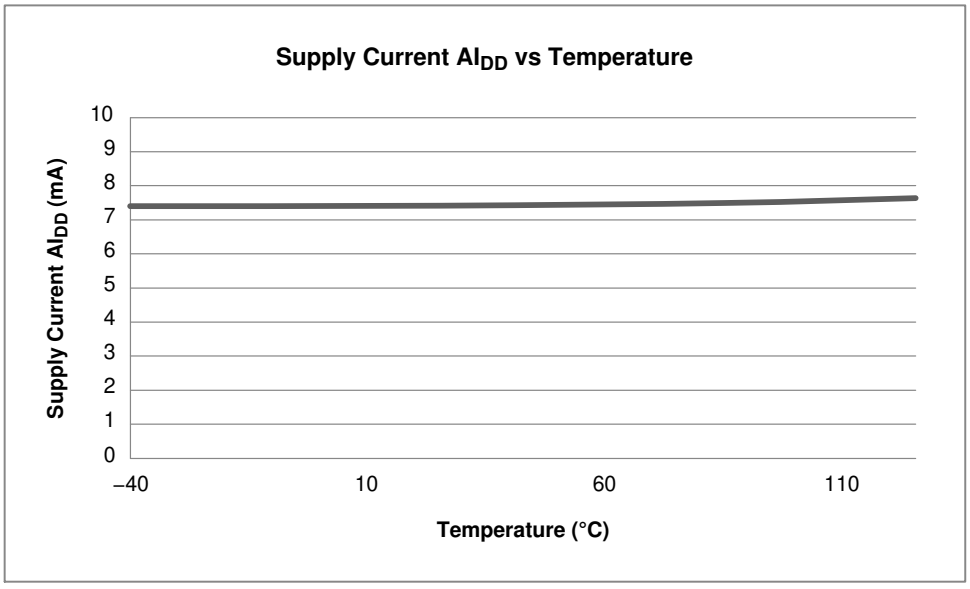


Figure 13. Supply Current vs Temperature

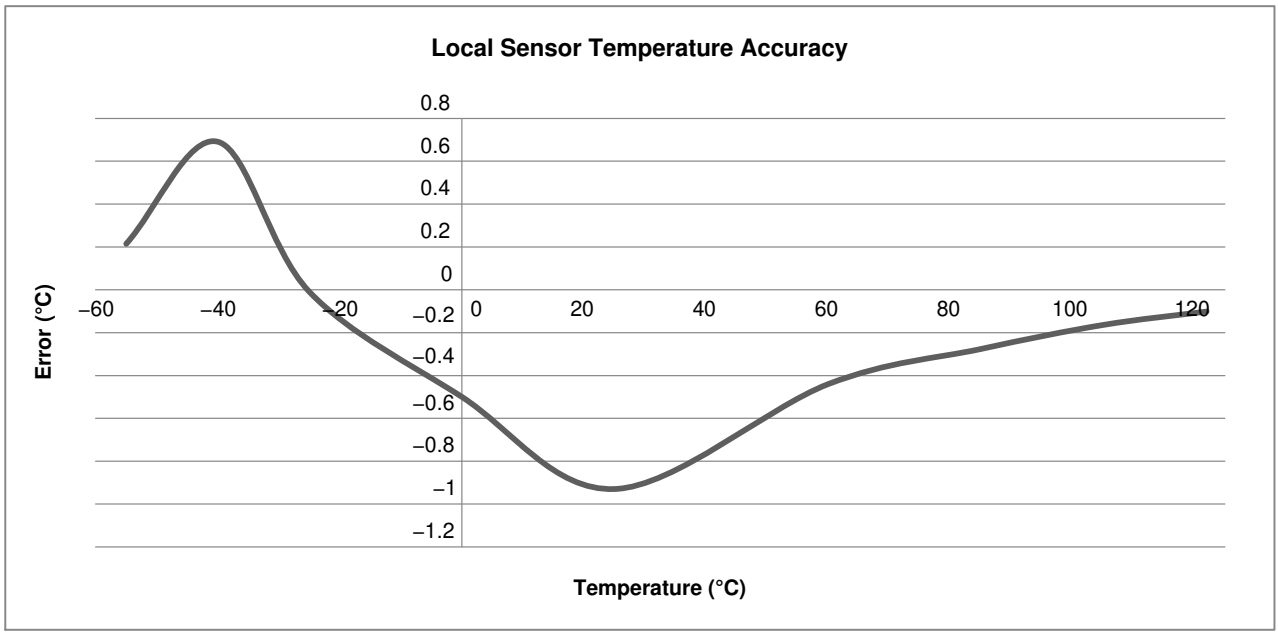


Figure 14. Local Temperature Error vs Temperature

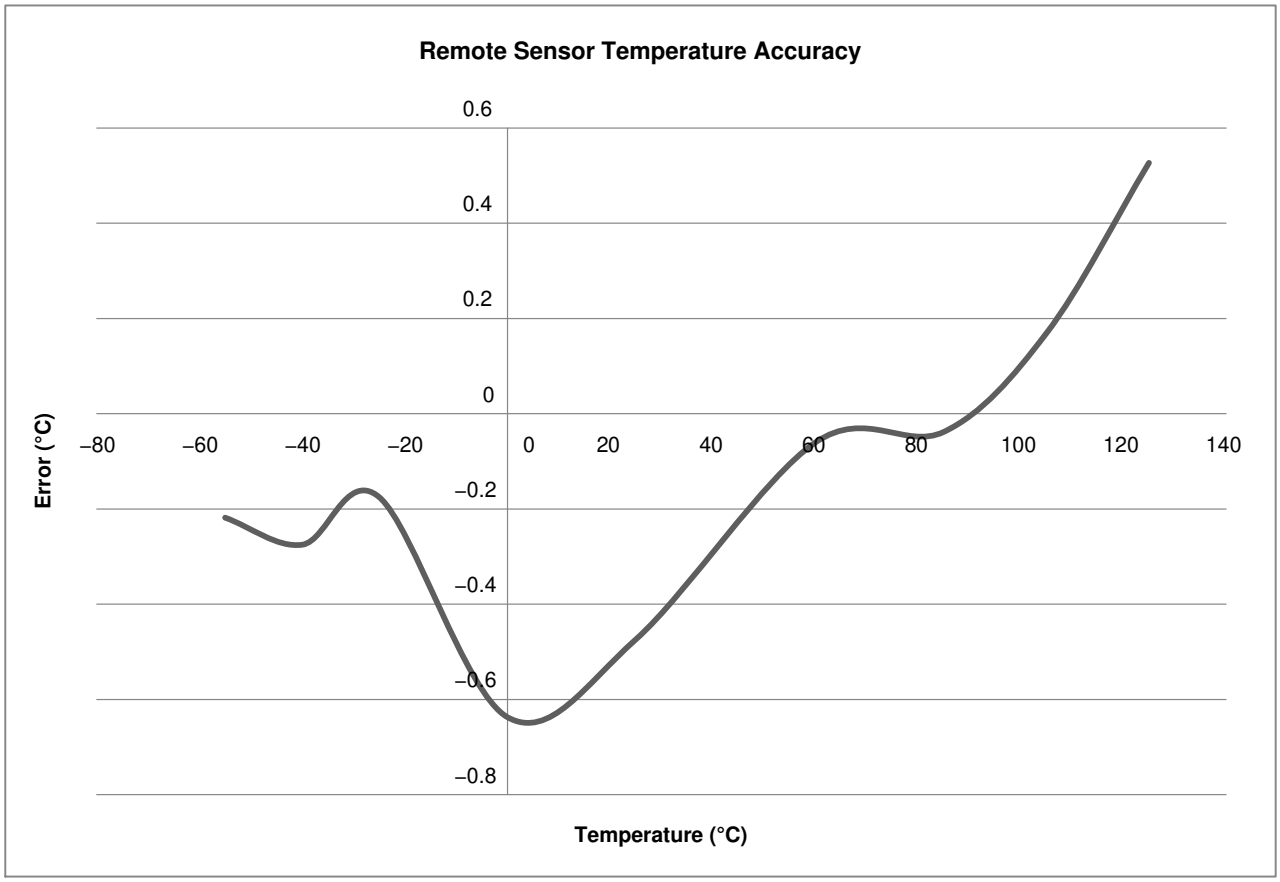


Figure 15. Remote Temperature Error vs Temperature

OVERVIEW

NCT7290 encompasses full analog monitoring, local and remote temperature sensing along with general purpose I/Os. The operational details of these functions are discussed below.

Power On Reset

NCT7290 has a power-on-reset circuitry that resets the device if the voltage level of power supplies goes below the values specified in the datasheet. To avoid reset on the go AV_{DD}, DV_{DD} and DAC supplies must be within their specified range.

ANALOG TO DIGITAL CONVERTERS

The NCT7290 has three ADCs. These are all successive approximation ADCs used for the digitization of analog inputs and temperature information.

SAR ADC

The ADCs are power successive approximation with a built in analog channel multiplexers and 10 bit resolution. The 10 bit resolution assures high noise immunity and fast digitization that makes this device suitable for medium to high speed applications. The device internal circuitry operates at speed higher than the conversion time of the device because of the binary algorithm used. The algorithm is based on approximating the input signal by comparing with successive analog signal generated from the builtin DAC.

The value of each output bit is evaluated on the basis of output of the comparator. The converter requires N conversion periods to give N bit digital output of the input analog signal. The SAR register stores the digital equivalent bits of the input analog signal and can be read by the master device using an I^2C interface. The main building block of the device are:

- Digital to Analog Converter
- Comparator
- Digital Logic

Digital to Analog Converter

A charge scaling DAC is used due to its compatibility with the switch capacitor circuits. The DAC operation consists of two phases called acquisition phase and the conversion phase. The acquisition phase is analogous to sample and hold circuit while the conversion phase is the process of conversion of the internal digital word in to an analog output.

Acquisition phase: The top plates of all the capacitors on the array are connected to the ground and the bottom plates are connected to the applied voltage V_{in}. Thus there is a charge proportional to input voltage on the capacitor array. After acquisition the top and bottom plates are disconnected from their respective connections.

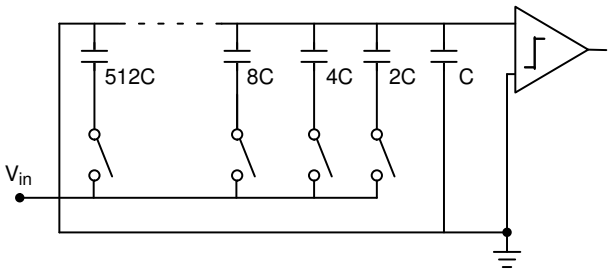


Figure 16. The Acquisition Phase of the Typical ADC

Conversion Phase*:* The conversion phase is administered by a two phase non overlapping clock with phases φ1 and φ2 respectively. During φ1 the bottom plates of all the capacitors are grounded i.e. the top plates of all the capacitors are now V_{in} times higher than the ground. As the conversion process starts the digital control sets all the bits zero except the MSB in the SAR register. During the φ2 the capacitors associated with MSB is connected to V_{REF} while others are connected to ground. In this way the DAC generates analog voltage of magnitude $V_{REF}/2$. The analog output of DAC is compared with the input analog signal. The digital control logic sets the MSB to 1 if comparator output is high and 0 otherwise. Thus the first step of SAR algorithm decides whether the input signal is greater or less than $V_{REF}/2$. The approximation process is then run again with the MSB in its proven value and the next lower bit is set to 1. This gives a general direction path and the remaining approximations will converge the output in this direction.

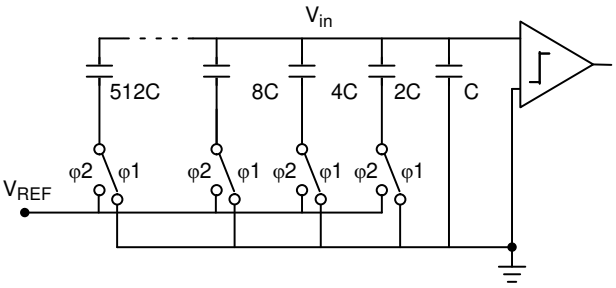


Figure 17. The Conversion Phase of the Typical ADC

Comparator

A switch capacitor comparator is used to alleviate the effects of input offset voltage. The issue of charge injection is controlled by using fully differential topology.

Digital Logic

The function of the digital logic is to generate the binary word to be compared with the input analog signal in each approximation cycle. The result of each approximation cycle is stored in the SAR register. In short the digital logic determines the value of each output bit in a sequential manner base don the output of the comparator.

ANALOG CHANNELS

The analog inputs ($V_{IN}1-V_{IN}16$) are multiplexed into two on-chip successive approximation, analog-digital converters. Analog inputs $V_{IN}1-V_{IN}8$ are multiplexed on a 10 bit ADC1 whereas $V_{IN}9-V_{IN}16$ are multiplexed on a second 10 bit ADC2. The maximum input range of analog inputs is 0–2.5 V. The device generates an internal reference of 2.5 V which is used for the digitization of the analog input channel values.

VOLTAGE & TEMPERATURE MONITORING

The NCT7290 implements a simple round robin for gathering and converting voltage and temperature data. All inputs are divided into groups and then multiplexed into 3 separate ADCs. An internally generated reference of 2.5 V is used.

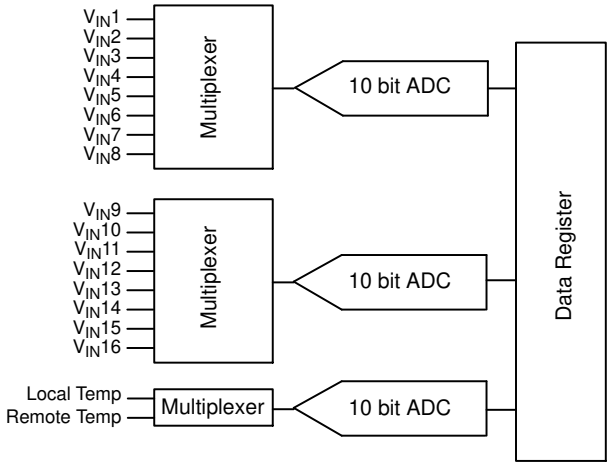


Figure 18. Input Monitoring

$V_{IN}1-8$ are implemented as one round robin sequence and multiplexed into ADC1. $V_{IN}9-16$ are implemented as another separate round robin sequence and multiplexed into ADC2. Both local and remote temperature measurements are then multiplexed into the third ADC. The resulting outputs of each ADC is then stored in the appropriate register.

Remote Sensing Diodes

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base emitter voltage (V_{BE}) of a transistor operated at constant current. However, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from device to device.

The NCT7290 is designed to work with either substrate transistors built into processors or discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter is connected to D–. If a PNP transistor is used, the collector and base are connected to D– and the emitter is connected to D+.

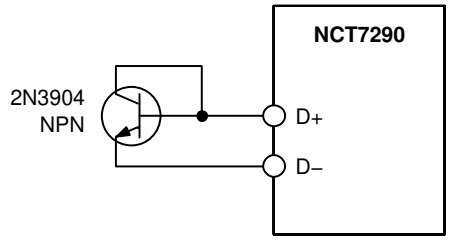


Figure 19. Discrete NPN Transistor as Remote Sensor

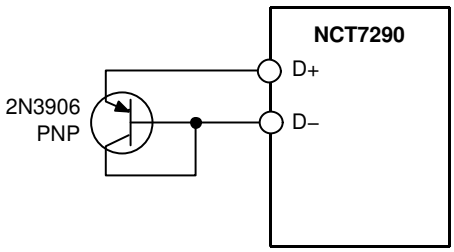


Figure 20. Discrete PNP Transistor as Remote Sensor

If a discrete transistor is used with the NCT7290, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage is greater than 0.25 V at 6 μA with the highest operating temperature
- Base-emitter voltage is less than 0.95 V at 100 μA with the lowest operating temperature

- Base resistance is less than 100 Ω
- There is a small variation in h_{FE} (for example, 50 to 150) that indicates tight control of V_{BE} characteristics

Transistors such as 2N3904, 2N3906, or equivalents in SOT−23 packages are suitable devices to use. If alternative transistor is used the device operates as specified as long as the above condition are met.

Series Resistance Cancellation

Parasitic resistance to the D+ and D− inputs to the NCT7290, seen in series with the remote diode, is caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor temperature measurement. This error typically causes a 0.5°C offset per ohm of parasitic resistance in series with the remote diode.

The NCT7290 automatically cancels out the effect of this series resistance on the temperature reading, providing a more accurate result, without the need for user characterization of this resistance. The NCT7290 is designed to automatically cancel typically up to 130 Ω of resistance per leg. By using an advanced temperature measurement method, this is transparent to the user. This feature allows resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments.

The technique used in the NCT7290 measures the change in V_{BE} when the device operates at four different currents. Previous devices used only two operating currents, but it is the use of a third and fourth current that allows automatic cancellation of resistances in series with the external temperature sensor.

To measure ΔV_{BE}, the operating current through the sensor is switched among four related currents. $N1 \times I$, $N2 \times I$ and $N3 \times I$ are different multiples of the current, I. The currents through the temperature diode are switched between I and $N1 \times I$, giving ΔV_{BE1}; then between I and $N2 \times I$, giving ΔV_{BE2} and then between I and $N3 \times I$, giving ΔV_{BE3}. The temperature is then calculated using the three ΔV_{BE} measurements. This method also cancels the effect of any series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low-pass filter to remove noise and then to a chopper-stabilized amplifier. This amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage producing a temperature measurement.

Reading Temperature

The results of the local and remote temperature measurements are stored in the temperature value registers in two's complement format.

The result in these registers is compared with limits programmed into the high and low limit registers. The high and low limits are also stored in 2's complement format.

The data registers for storing local and remote temperature data are present at address 0x0E and 0x0F respectively. Only 10 bits are used which gives the temperature measurement a resolution of 0.25°C.

Table 3. TWO'S COMPLEMENT TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit)
−55°C	1100 1001 **00**
−40°C	1101 1000 **00**
−10°C	1111 0110 **00**
−1°C	1111 1111 **00**
−0.25°C	1111 1111 **11**
0°C	0000 0000 **00**
10.25°C	0000 1010 **01**
25°C	0001 1001 **00**
125°C	0111 1101 **00**

Table 4. 10-BIT ADC OUTPUT CODE VS V_{IN}

Input Voltage	ADC Output	
2.5 V_{IN}	Decimal	Binary (10-bits)
< 0.002441	0	00000000 00
0.002441 to 0.004883	1	00000000 01
0.004883 to 0.007324	2	00000000 10
0.007324 to 0.009776	3	00000000 11
0.009776 to 0.012207	4	00000001 00
0.012207 to 0.014648	5	00000001 01
–	–	–
0.625000 to 0.627441	256	01000000 00
–	–	–
1.25000 to 1.252441	512	10000000 00
–	–	–
1.875000 to 1.877441	768	11000000 00
–	–	–
2.485352 to 2.487793	1018	11111110 10
2.487793 to 2.490234	1019	11111110 11
2.490234 to 2.492676	1020	11111111 00
2.492676 to 2.495117	1021	11111111 01
2.495117 to 2.497559	1022	11111111 10
2.497559 to 2.5	1023	11111111 11

The temperature measurement channels take longer to present the data to the ADC than voltage channels. This is due to the time it takes to measure the temperature before presenting the corresponding voltage to the ADC. Data is updated on every temperature round robin cycle. If averaging is enabled then 16 round robin cycles are required

before data is updated. Until valid data is available the previous temperature stays in the temperature value register.

Averaging

To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles for low conversion rates. The conversion rates for which averaging can be on are 1/16, 1/8, 1/4, 1/2, 1 and 2 conversions/second. At rates of 4, 8, 16 and 32 conversions/second, no digital averaging occurs.

Signal conditioning and measurement of the internal temperature sensor are performed in the same manner. Switching from Averaging OFF to ON or vice versa requires a procedure. *The user needs to stop monitoring, change the averaging status and re-start monitoring to avoid glitches. Alternatively, the user can discard the first reading after changing the averaging state*.

DAC OPERATION

There are 12 DACs output that can be programmed with 12 bits resolution using an internal reference. This is a decoder type based Resistor String type converter where N bits are used to create 2^N value output.

Resistor String DAC

A resistor string in connected to a switch network. The switch network is connected like a tree. Depending on the switch selection there will be only one low impedance path between the resistor string and the input of the amplifier. Figure 21 shows the block diagram of resistor string DAC architecture.

The resistor string consists of resistors, each with value R. The code loaded in the DAC output registers determines at which node on the string the voltage is tapped off to be fed into the output amplifier. Thus, the selection of switches is controlled by the bit selection in the DAC output registers from 0x2A to 0x35. Table 4 shows the DAC output values that can be achieved depending on the codes in the DAC output registers. Please the the Register Map section for more details

Power Rails for DAC Outputs

Separate power rails of 5 V and 12 V are required to be connected to the device at pin 9 and 37 respectively. See typical application circuit Figure 2 for more details. The DAC powers-up with a default output of 0 V.

Configuration of 12 V DAC Outputs

The device has 12 DAC outputs, 8 of them have 5 V output range while 4 have 12 V output range. The eight 5 V DAC outputs are available as $V_{OUT}1-4$ and $V_{OUT}7-10$. On the other hand four 5 V/12 V DAC outputs are available as $V_{OUT}5-6$ and $V_{OUT}11-12$ respectively.

The 12 V DAC outputs can be configured to operate as 5 V outputs by setting the bit 7 of configuration Register 1 (0x03). By default all DAC outputs are configured to operate as 5 V outputs. See Configuration Register 1 in the Register Map section for more information.

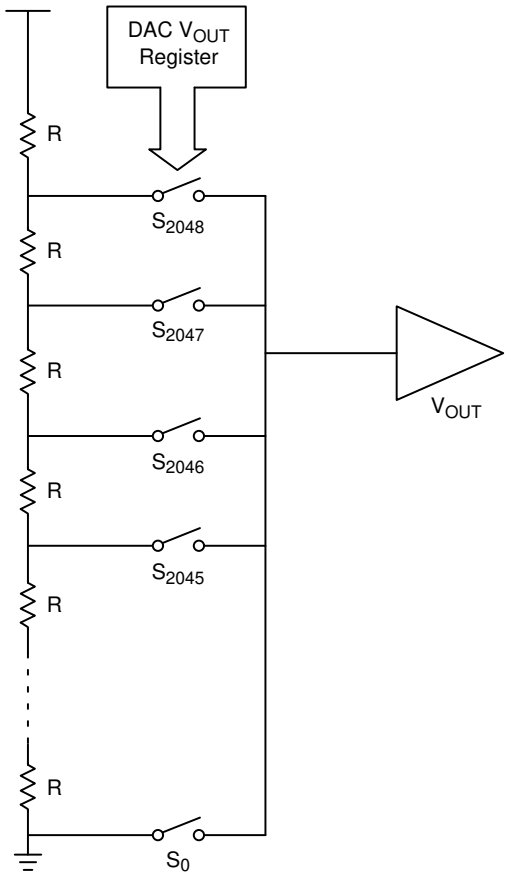


Figure 21. DAC Register String Architecture

Table 5. 12 BIT REGISTER CODE VS DAC OUTPUT

Register Value (12 Bits)		Output Voltage	
Decimal	Binary (12 Bits)	5.0 V_{OUT}	12 V_{OUT}
0	00000000 0000	< 0.00122	< 0.00293
1	00000000 0001	0.00122 to 0.00244	0.00293 to 0.00586
2	00000000 0010	0.00244 to 0.00366	0.00586 to 0.00879
3	00000000 0011	0.00366 to 0.00488	0.00879 to 0.01172
4	00000000 0100	0.00488 to 0.00611	0.01172 to 0.01465
5	00000000 0101	0.00611 to 0.00733	0.01465 to 0.01758
–	–	–	–
256	00010000 0000	0.3126 to 0.3138	0.75018 to 0.75311
–	–	–	–
512	00100000 0000	0.62515 to 0.6264	1.5004 to 1.50329
–	–	–	–
768	00110000 0000	0.9377 to 0.9389	2.25055 to 2.25348
–	–	–	–
1024	01000000 0000	1.2503 to 1.2515	3.0007 to 3.00367
–	–	–	–
2048	10000000 0000	2.5006 to 2.5018	6.0015 to 6.00439
–	–	–	–
4090	111111111010	4.9939 to 4.9951	11.9853 to 11.9883
4091	111111111011	4.9951 to 4.9963	11.9883 to 11.9912
4092	111111111100	4.9963 to 4.9976	11.9912 to 11.9941
4093	111111111101	4.9976 to 4.9988	11.9941 to 11.9971
4094	111111111110	4.9988 to 5	11.9971 to 12
4095	111111111111	5	12

Clearing of DACs

NCT7290 contains two external control lines, $\overline{BANK1_{DAC}}$SHUTDOWN and $\overline{BANK2_{DAC}}$SHUTDOWN pins to shutdown the DAC outputs. When either pin goes low, the corresponding DAC outputs are cleared. Shutdown pins disconnect the DAC output pins and cleared them to ground. However, the outputs registers' values remain intact until they are changed by writing to the corresponding V_{OUT} registers. When the DAC outputs are shutdown the device internally connects the DACs output pins to GND via a 3 kΩ internal resistor

DAC outputs can also be cleared by writing appropriately in the register DAC_CHANNEL_SHUTDOWN register at address 0xC. All the DACs are enabled by default however; individual DACs can be turned OFF by writing 0 to their corresponding bits. The clearing of any DAC output will just pull-down the output pin to ground while the corresponding VOUTx_DATA register retains its value. See Register Map section for more details.

$\overline{ALERT}$

The $\overline{ALERT}$ output goes low whenever an out-of-limit measurement is detected or if the remote temperature sensor is open-circuit. It is an open drain pin and requires a 10 kΩ pull-up to V_{DD}.

Status registers 1−5 (0x10−0x14) contains flags indicating the result of the limit comparisons.

If the local and/or remote temperature measurement is above the corresponding high temperature limit or below the corresponding low temperature limit in the limit registers (0x56−0x59), one or more of these flags will be set in Status register 5.

If the high limit of analog input signal is over the corresponding high limit in the limit registers (0x36−0x45) the corresponding flag in the status register 1−2 will be set.

If the low limit of analog input signal is below the corresponding low limit in the limit registers (0x46−0x55) the corresponding flag in the status register 3−4 will be set.

These flags are NOR'd together, so that if any of them are high, the $\overline{\text{ALERT}}$ interrupt latch is set, and the $\overline{\text{ALERT}}$ output goes low.

Reading the status register clears the flag bits provided the error conditions that caused the flags to be set have gone away. While a limit comparator is tripped due to a value register containing an out-of-limit measurement or the sensor is open-circuit, the corresponding flag bit cannot be reset. A flag bit can be reset only if the corresponding value register contains an in-limit measurement, or the sensor is good.

The $\overline{\text{ALERT}}$ interrupt latch is not reset by reading the status register, but it resets when the $\overline{\text{ALERT}}$ output has been serviced by the master reading the device address, provided the error condition has gone away and the status register flag bits have been reset.

GPIOs HANDLING

The NCT7290 has eight GPIO pins. The GPIO1−8 pins are dedicated general purpose bidirectional, digital I/O signals. These pins can receive an input or produce an output. GPIO Configuration register (0x05) can be used to configure a GPIO as input or output. When GPIO-n is used as an output, it has an open drain configuration and the status is determined by the corresponding GPIO-n-polarity bit in the GPIO Polarity Register (0x06). Note that a pull-up resistor of 10 kΩ is required when using any GPIO pin as an output.

NCT7290 REGISTERS

The NCT7290 16-bit registers that are used for the configuration, monitoring, setting limits and other application related functions. Important registers are described briefly below. In order to get detailed description of each individual register please see the Register Map section.

Configuration Register

Configuration register (0x03) is critical to initialize the device for proper operation. Bit 0 is used to enable the monitoring of analog and temperature channels. Bit 1 is used to enable/disable the SMBUS timeout. Bit 5 is used to reset the device using the software control. Alert output can be enable/disable using the bit 6 of the configuration register.

Remote Temperature Conversion Rate Register

The conversion rate register (0x04) must be programmed with 0x06 on power-up to ensure correct operation. This setting corresponds to 4 conv/sec with averaging ON. For more detailed information please see the Register Map section.

Chanel Selector Registers

There are three different sequencers, one for each ADC. Sequencer 1 starts with $V_{IN}1$ and goes to $V_{IN}8$ before starting again. Sequencer 2 starts at $V_{IN}9$ and goes to $V_{IN}16$ before starting again. The temperature channels have a separate sequencer. All three sequencers run in parallel.

Individual V_{INs} and temperature channels can be disabled to remove them from the round robin sequence of the respected ADCs CHANNEL_SELECTOR_REGISTERs (0x09−0x0B) See Register Map section for more information.

ADC DATA Registers

The digitized data of analog inputs $V_{IN}1-V_{IN}16$ is stored in the ADC data registers (0x1A−0x29). Similarly registers Local_Temp_Data (0xE) and Remote_Temp_data (0xF) store the measured values of local and remote temperatures.

DAC Data Registers

There are 12 DAC output data registers available to set the analog voltage level at the V_{OUT} pins. These are 16 bit registers however, only the 12 LSB bits are available for the setting of corresponding V_{OUT} value. The DAC output registers are available from address 0x2A to 0x35 and are called $V_{OUT}1$_DATA to $V_{OUT}12$_DATA respectively.

The table below outlines what codes must be programmed to the DAC registers in order to obtain a certain output voltage.

Limit Registers

NCT7290 has 36 limit registers to store analog inputs, local and remote, high and low temperature limits. For more detailed information please see the Register Map section. These registers can be written to and read back over the SMBus. The high limit registers perform a > comparison, while the low limit registers perform a < comparison. For example, if the high limit register is programmed as a limit of 90°C, measuring 81°C results in an alert condition.

GPIO Registers

The writable GPIO registers are used to set the direction and polarity of the GPIO pins. There are also two read-only registers that gives the status of datain-out. The GPIO registers can be accessed from address 0x05−0x08 for this purpose.

COMMUNICATION

There are two communication interfaces on the NCT7290. On power-up you must select which interface you intend on using. This is done via the BUS_SEL pin. Grounding this pin selects the I^2C interface while setting it to V_{DD} will select the SPI interface. The table below show the pins related to each interface.

Table 6. COMMUNICATION PIN CONFIGURATION

BUS_SEL State	GND	V_{DD}
Pin No.	**I^2C**	**SPI**
24	SCL	SCLK
25	SDA	SDI
26	ADD0	SDO
27	ADD1	$\overline{CS}$

Serial Bus Interface – I^2C

Control of the NCT7290 is carried out via the I^2C bus. The NCT7290 is connected to this bus as a slave device, under the control of a master device. The NCT7290 has a 7-bit serial bus address. The upper 3 bits of the device address are fixed at '110'.The lower four bits are set by the state of pins 26 and 27 as shown in Table 7. The address pins are sampled continuously after power-up, so any changes made while power is on changes the I^2C address.

Table 7. ADDRESS SELECTION

ADD1	ADD0	Device Address
0	0	110 0001 (0x61)
0	1	110 0010 (0x62)
1	0	110 0100 (0x64)
1	1	110 0101 (0x65)

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line, SCL, remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/W bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, the master will write to the slave device. If the R/W bit is a 1, the master will read from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low-to-high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10^{th} clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. In the case of the NCT7290, write operations contain two bytes, and read operations contain two bytes and perform the following functions. To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, and then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register. The device address is sent over the bus followed by R/W set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

When reading data from a register there are two possibilities:

1. If the NCT7290's Address Pointer Register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the NCT7290 as

before, but only the data byte containing the register address is sent, as data is not to be written to the register. A read operation is then performed consisting of the serial bus address, R/W bit set to 1, followed by the data word read from the data register. This is shown in Figure 23.

2. If the Address Pointer Register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the Address Pointer Register.

To read from a register it is necessary to first write the register address to the address pointer. The Byte Write protocol is used for this.

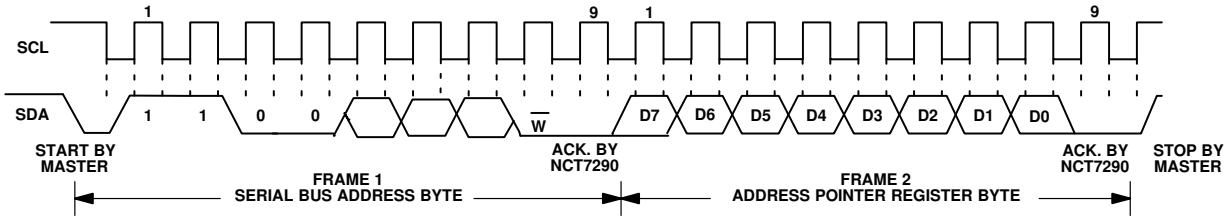


Figure 22. Writing to the Address Pointer

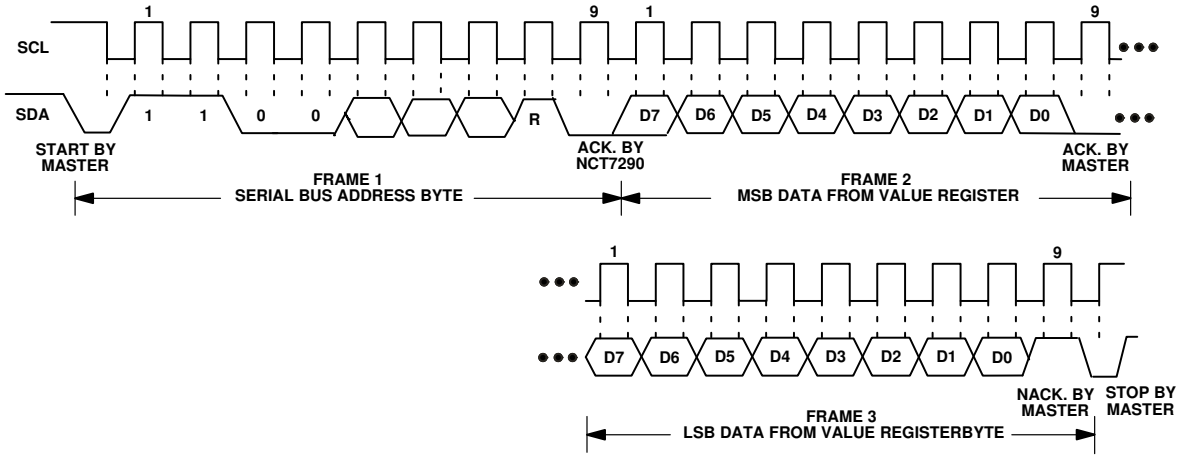


Figure 23. Reading a Word from a Previously Selected Register

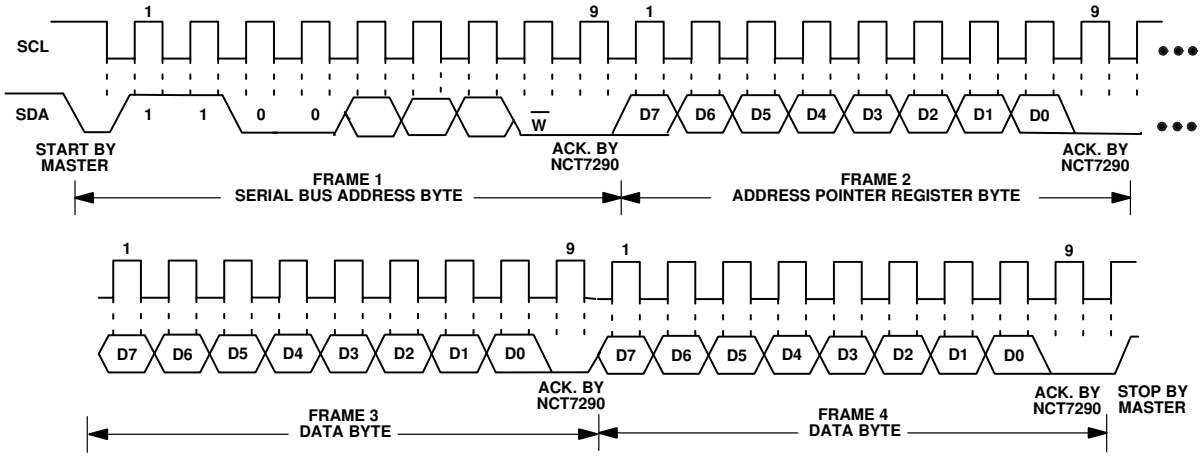


Figure 24. Writing a Word to a Specified Address

Serial Peripheral Interface – SPI

The SPI interface of the NCT7290 consists of 4 wires: CS, SCLK, SDI and SDO. The CS (chip select) pin is used to select the device when more than one device is connected to the serial clock and data lines. It is controlled by the SPI master and must go low at the start of a transmission and high at the end of a transmission. The part operates in a slave mode and requires an externally applied (from the SPI master) serial clock to the SCLK input to access data from the data registers. The master must configure the clock signal polarity with respect to the data. The NCT7290 operates using an active low (inverted) clock (shown in Figure 26). Data is simultaneously transmitted and received on the SDO and SDI pins. This is known as full-duplex communication.

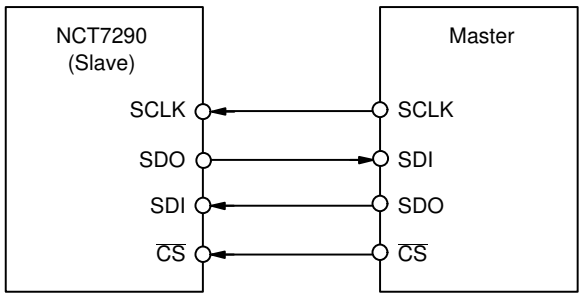


Figure 25. SPI Interface between Master and NCT7290 (Slave)

Data is sampled on the rising edge of SCLK. Data is clocked into the NCT7290 (on the SDI pin) on the falling edge of the clock and data is clocked out of the NCT7290 (on the SDO pin) on the rising edge of the clock When the SDO pin of the slave is not being used it goes into a high impedance state (Hi-Z).

SPI data transmission begins when the $\overline{CS}$ line is asserted (active low). This selects the slave to be communicated with. The 8 register address bits are then sent with the MSB first. Once this is complete the control signal for the Write/Read operation is sent. This is by default set to read (low signal) and can be set to write by setting this bit high. The next 16 bits is then clocked in. The NCT7290 sees all this data on its SDI pin only. The SDO pin is used for read operations (i.e. sending data beck to the master). The data starts appearing on the NCT7290 SDO pin on the clock edge after the control signal has been sent.

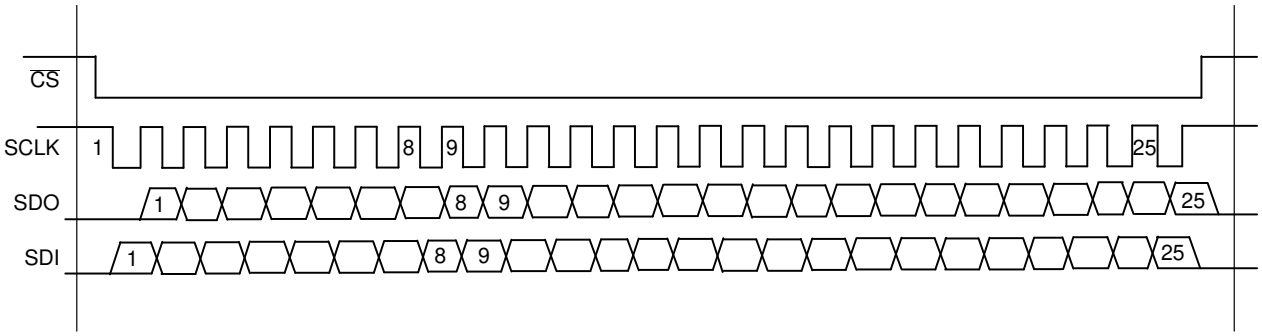


Figure 26. Bit Timing Diagram for SPI Communication

NCT7290 REGISTER MAP

Table 8. REGISTER MAP

Register Address	Register Name	R/W	POR Default
0x00	COMPANYID	RO	0x001A
0x01	DEVICEID	RO	0x1C7A
0x02	REVISIONID	RO	0x0000
0x03	CONFIGURATION1	RW	0x0001
0x04	REMOTE_TEMP_CONV_RATE	RW	0x0005
0x05	GPIO_INOUT	RW	0x0000
0x06	GPIO_POLARITY	RW	0x00FF
0x07	GPIO_DATA_IN	RO	0x0000
0x08	GPIO_DATA_OUT	RW	0x0000
0x09	CHANNEL_SELECTOR1	RW	0x00FF
0x0A	CHANNEL_SELECTOR2	RW	0x00FF
0x0B	CHANNEL_SELECTOR3	RW	0x00C0
0x0C	DAC_CHANNEL	RW	0xFFFF
0x0D	RESERVED	WO	0x0000
0x0E	LOCAL_TEMP_DATA	RO	0x0000
0x0F	REMOTE_TEMP_DATA	RO	0x0000
0x10	STATUS1	RO	0x0000
0x11	STATUS2	RO	0x0000
0x12	STATUS3	RO	0x0000
0x13	STATUS4	RO	0x0000
0x14	STATUS5	RO	0x0000
0x15	MASK1	RW	0x00FF
0x16	MASK2	RW	0x00FF
0x17	MASK3	RW	0x00FF
0x18	MASK4	RW	0x00FF
0x19	MASK5	RW	0x001F
0x1A	VIN1_DATA	RO	0x0000
0x1B	VIN2_DATA	RO	0x0000
0x1C	VIN3_DATA	RO	0x0000
0x1D	VIN4_DATA	RO	0x0000
0x1E	VIN5_DATA	RO	0x0000
0x1F	VIN6_DATA	RO	0x0000
0x20	VIN7_DATA	RO	0x0000
0x21	VIN8_DATA	RO	0x0000
0x22	VIN9_DATA	RO	0x0000
0x23	VIN10_DATA	RO	0x0000
0x24	VIN11_DATA	RO	0x0000
0x25	VIN12_DATA	RO	0x0000
0x26	VIN13_DATA	RO	0x0000
0x27	VIN14_DATA	RO	0x0000
0x28	VIN15_DATA	RO	0x0000
0x29	VIN16_DATA	RO	0x0000
0x2A	VOUT1_DATA	RW	0x0000
0x2B	VOUT2_DATA	RW	0x0000
0x2C	VOUT3_DATA	RW	0x0000

Table 8. REGISTER MAP (continued)

Register Address	Register Name	R/W	POR Default
0x2D	VOUT4_DATA	RW	0x0000
0x2E	VOUT5_DATA	RW	0x0000
0x2F	VOUT6_DATA	RW	0x0000
0x30	VOUT7_DATA	RW	0x0000
0x31	VOUT8_DATA	RW	0x0000
0x32	VOUT9_DATA	RW	0x0000
0x33	VOUT10_DATA	RW	0x0000
0x34	VOUT11_DATA	RW	0x0000
0x35	VOUT12_DATA	RW	0x0000
0x36	VIN1_HIGH_LIM	RW	0x03FF
0x37	VIN2_HIGH_LIM	RW	0x03FF
0x38	VIN3_HIGH_LIM	RW	0x03FF
0x39	VIN4_HIGH_LIM	RW	0x03FF
0x3A	VIN5_HIGH_LIM	RW	0x03FF
0x3B	VIN6_HIGH_LIM	RW	0x03FF
0x3C	VIN7_HIGH_LIM	RW	0x03FF
0x3D	VIN8_HIGH_LIM	RW	0x03FF
0x3E	VIN9_HIGH_LIM	RW	0x03FF
0x3F	VIN10_HIGH_LIM	RW	0x03FF
0x40	VIN11_HIGH_LIM	RW	0x03FF
0x41	VIN12_HIGH_LIM	RW	0x03FF
0x42	VIN13_HIGH_LIM	RW	0x03FF
0x43	VIN14_HIGH_LIM	RW	0x03FF
0x44	VIN15_HIGH_LIM	RW	0x03FF
0x45	VIN16_HIGH_LIM	RW	0x03FF
0x46	VIN1_LOW_LIM	RW	0x0000
0x47	VIN2_LOW_LIM	RW	0x0000
0x48	VIN3_LOW_LIM	RW	0x0000
0x49	VIN4_LOW_LIM	RW	0x0000
0x4A	VIN5_LOW_LIM	RW	0x0000
0x4B	VIN6_LOW_LIM	RW	0x0000
0x4C	VIN7_LOW_LIM	RW	0x0000
0x4D	VIN8_LOW_LIM	RW	0x0000
0x4E	VIN9_LOW_LIM	RW	0x0000
0x4F	VIN10_LOW_LIM	RW	0x0000
0x50	VIN11_LOW_LIM	RW	0x0000
0x51	VIN12_LOW_LIM	RW	0x0000
0x52	VIN13_LOW_LIM	RW	0x0000
0x53	VIN14_LOW_LIM	RW	0x0000
0x54	VIN15_LOW_LIM	RW	0x0000
0x55	VIN16_LOW_LIM	RW	0x0000
0x56	LOCAL_TEMP_HIGH_LIM	RW	0x0154
0x57	LOCAL_TEMP_LOW_LIM	RW	0x0000
0x58	REMOTE_TEMP_HIGH_LIM	RW	0x01B8
0x59	REMOTE_TEMP_LOW_LIM	RW	0x0000
0x5A	LOCAL_TEMP_OFFSET	RW	0x0000
0x5B	REMOTE_TEMP_OFFSET	RW	0x0000

REGISTER DETAILS

Table 9. 0x03 CONFIGURATION REGISTER 1

Bit Field	Name	Description	Access	Default
15:8	Reserved		RO Returns 0s	0x00
7	DAC_12_op_sel	12 V DAC Setting to Output 5 V if set to 0 0: 5 V Output 1: 12 V Output	RW	0
6	Mask_alert	Turns Off ALERT Output 0: ALERT is Unmasked 1: ALERT is Masked	RW	0
5	Sw_reset	Resets All Configuration Registers and Limits to Default Values 0: Reset Disabled 1: Resets All Configuration Registers and Limits to Default Values	RW	0
4:2	Reserved		RO	0
1	Timeout_disable	Disables I^2C Timeout 0: Enable_timeout 1: Disable_timeout	RW	0
0	Start	Enables Monitoring 0: Disable Monitoring 1: Enable Monitoring	RW	1

Table 10. 0x04 REMOTE TEMP CONVERSION RATE

Bit Field	Name	Description	Access	Default
15:5	Reserved		RO Returns 0s	0x000
4	Averaging_off	Average Configuration 0: Turns Averaging On for the Remote Channel 1: Turns Averaging Off for the Remote Channel	RW	0
3:0	Remote_temp_conv_rate	10 Different Timing Options 0x0: 1/16 (Conv/Sec). Averaging On 0x1: 1/8 (Conv/Sec). Averaging On 0x2: 1/4 (Conv/Sec). Averaging On 0x3: 1/2 (Conv/Sec). Averaging On 0x4: 1 (Conv/Sec). Averaging On 0x5: 2 (Conv/Sec). Averaging On 0x6: 4 (Conv/Sec). Averaging Off 0x7: 8 (Conv/Sec). Averaging Off 0x8: 16 (Conv/Sec). Averaging Off 0x9: 20 (Conv/Sec). Averaging Off 0xA: 20 (Conv/Sec). Averaging Off 0xB: 20 (Conv/Sec). Averaging Off 0xC: 20 (Conv/Sec). Averaging Off 0xD: 20 (Conv/Sec). Averaging Off 0xE: 20 (Conv/Sec). Averaging Off 0xF: 20 (Conv/Sec). Averaging Off	RW	0x5