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NCT7491

Remote Thermal Monitor and Fan Controller with PECI 3.0 Interface and SMBus Compatible Master

The NCT7491 is a two−wire serially programmable hardware monitor. It can monitor 2 remote temperature zones and its own ambient temperature. A PECI 3.0 single wire interface allows the NCT7491 to monitor CPU temperatures. The NCT7491 also implements an SMBus compatible master, allowing it to read automatically from thermal sensors on the SMBus. The NCT7491 can automatically control the speed of 3 fans using PWM control, and monitor the speed of 4 fans. There are 4 analog inputs, used for measuring 12 V, 5 V, 2.5 V and Vccp channels. The NCT7491 supply voltage and PECI V_{TT} voltage are also monitored. Each of the measured temperature, voltage and fan speed values are compared with programmable limits and if any channel is outside the programmed limit an interrupt is generated via the ALERT output pin. A THERM output is also available for fail−safe thermal control. Up to 3 GPIO pins are available for digital control or signalling.

Communication with the NCT7491 is accomplished via the SMBus/I^2C interface which is compatible with industry standard protocols. The SMBus address is set by 2 address selection pins.

The NCT7491 is available in a 24−lead QFN or QSOP package and operates over a supply range of 3.0 V to 3.6 V.

Features

- PECI 3.0 Master for CPU Monitoring
- SMBus Compatible Master
- On−chip Temperature Sensor
- 2 Remote Sensor Channels
- Series Resistance Cancellation on Remote Sensors
- 3 PWM Fan Control Outputs
- 4 Tach Monitoring Input
- PWM Automatic Fan Speed Control
- 4 Analog Inputs for Voltage Monitoring
- Vdd Supply Voltage Monitoring
- PECI V_{TT} Voltage Monitoring
- Overtemperature Outputs
- Limit Comparison of Monitored Channels
- SMBus Address Selection Allows up to 3 Devices
- Meets SMBus 2.0 Electrical Specifications (fully SMBus 1.1 compliant)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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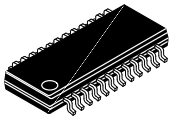
QFN24
MN SUFFIX
CASE 485L



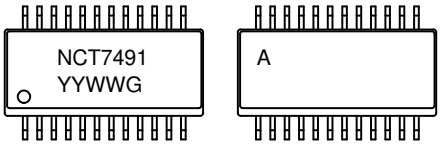
QSOP24
RQ SUFFIX
CASE 492B

MARKING DIAGRAMS

(Top View)

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)



(Top View) (Bottom View)

NCT7491 = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 79 of this data sheet.

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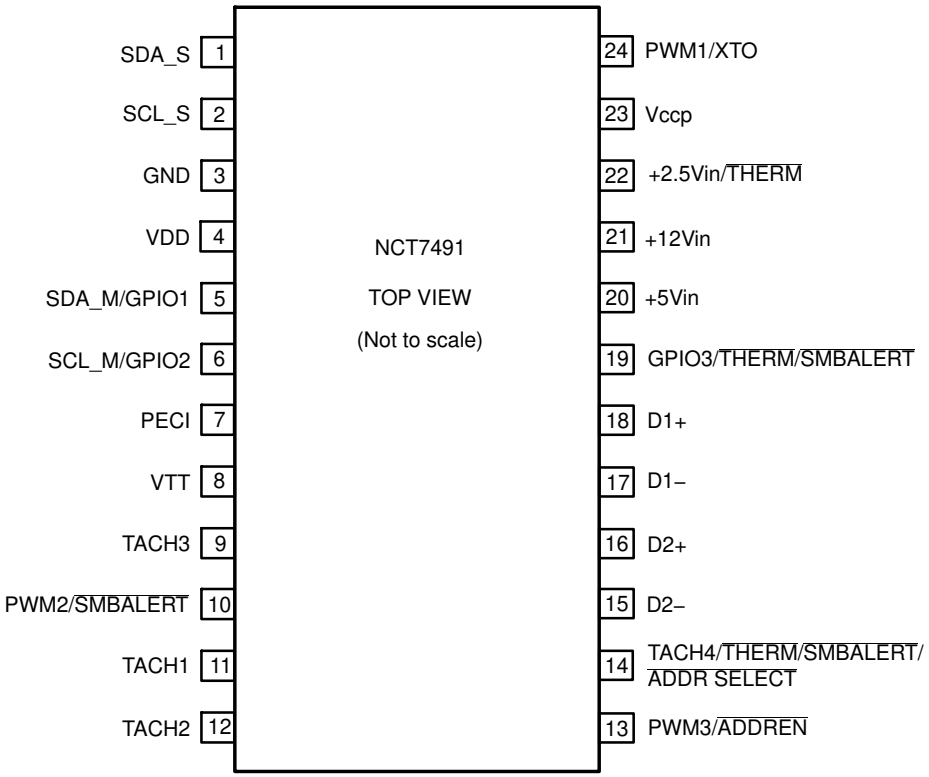
NCT7491 QSOP Pinout



NCT7491 QFN Pinout

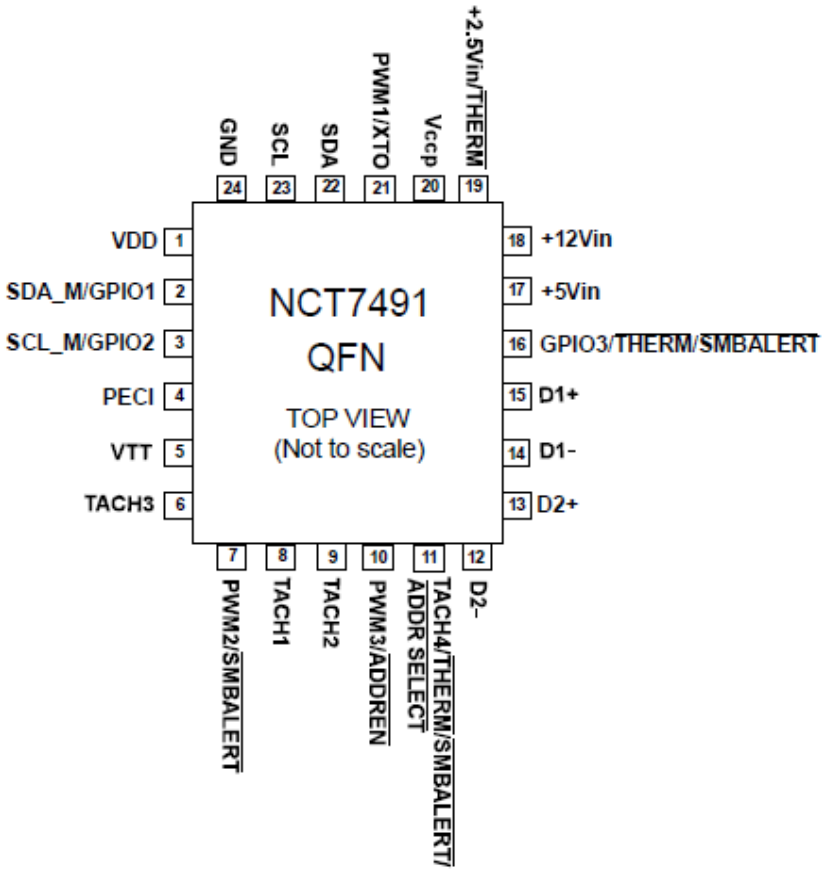


Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Positive Supply Voltage (V_{CC})	3.6 V
Maximum Voltage on +12V_{IN} Pin	14 V
Maximum Voltage on +5V_{IN} Pin	6.25 V
Maximum Voltage on All Open−Drain Outputs (excluding PWM pins)	3.6 V
Maximum Voltage on PWM Pins	+5.5 V
Maximum Voltage on TACH Pins	+5.5 V
Voltage on Remaining Input or Output Pins	−0.3 V to +4.2 V
Input Current at Any Pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature ($T_{J\ max}$)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering	
IR Reflow Peak Temperature	220°C
Pb−Free Peak Temperature	260°C
Lead Temperature (Soldering, 10 sec)	300°C
ESD Rating	
HBM	2 kV
FICDM	0.5 kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Specifications

T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{MIN} to V_{MAX}, unless otherwise noted. All voltages are measured with respect to GND, unless otherwise specified. Typical voltages are at T_A = 25°C and represent a parametric norm. Logic inputs accept input high voltages up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge, and V_{IH} = 2.0 V for a rising edge. SMBus timing specifications are guaranteed by design and are not production tested.

Table 2. SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage	3.0	3.3	3.6	V	
Supply Current, I_{CC}		1.5	5	mA	Interface inactive, ADC active
TEMP−TO−DIGITAL CONVERTER					
Local Sensor Accuracy		±0.5	±3.5	°C	0°C ≤ T_A ≤ 85°C
Local Sensor Resolution		0.25		°C	
Remote Diode Sensor Accuracy		±0.5	±3.5	°C	0°C ≤ T_A ≤ 85°C −40°C ≤ T_D ≤ 125°C
Remote Sensor Resolution		0.25		°C	
Remote Sensor Source Current		30		μA	Low Level 1
		240		μA	High Level 1
		37.5		μA	Low Level 2
		300		μA	High Level 2
Series Resistance Cancellation			270	Ω	

Table 2. SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG−TO−DIGITAL CONVERTER (INCLUDING MUX AND ATTENTUATORS)					
Total Unadjusted Error (TUE)			±2	%	For 12 V channel
			±1.5	%	For all other channels
Differential Nonlinearity (DNL)			±1	LSB	8 bits
Power Supply Sensitivity		±0.1		%/V	
Conversion Time (Voltage Input)		11		ms	Averaging enabled, 16 samples per averaged reading.
Conversion Time (Local Temperature)		38		ms	Averaging enabled, 16 samples per averaged reading.
Conversion Time (Remote Temperature)		38		ms	Averaging enabled, 16 samples per averaged reading.
Input Resistance		224		kΩ	For +12 V channel
		110		kΩ	For all other channels
FAN RPM−TO−DIGITAL CONVERTER					
Accuracy			±10	%	$0°C \le T_A \le 85°C$
			±14	%	$-40°C \le T_A \le 125°C$
Full−Scale Count			65,535		
Nominal Input RPM		109		RPM	Fan count = 0xBFFF
		329		RPM	Fan count = 0x3FFF
		5,000		RPM	Fan count = 0x0438
		10,000		RPM	Fan count = 0x021C
OPEN−DRAIN DIGITAL OUTPUTS, PWM1 TO PWM3, XTO					
Current Sink, I_{OL}			8.0	mA	
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –8.0 mA
High Level Output Current, I_{OH}		0.1	20	μA	$V_{OUT} = V_{CC}$
OPEN−DRAIN SERIAL DATA BUS OUTPUTS (SDA, SDA_M, SCL_M)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –4.0 mA
High Level Output Current, I_{OH}		0.1	1.0	μA	$V_{OUT} = V_{CC}$
SMBus DIGITAL INPUTS (SCL, SDA, SDA_M)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.4	V	
Hysteresis		500		mV	
DIGITAL I/O (PECI PIN)					
V_{TT} Supply Voltage	0.85		1.26	V	
Input High Voltage, V_{IH}	$0.55*V_{tt}$			V	
Input Low Voltage, V_{IL}			$0.5*V_{tt}$	V	
Hysteresis	$0.1V_{tt}$			V	Hysteresis between input switching levels
High level output source current, I_{SOURCE}	–6			mA	Output High Voltage, $V_{OH} = 0.75*V_{tt}$
Low level output sink current, I_{SINK}	0.5		1.0	mA	Output Low Voltage, $V_{OL} = 0.25*V_{tt}$
Signal noise immunity, V_{noise}	300			mV_{p-p}	Noise glitches from 10 – 100MHz Width up to 50ns

Table 2. SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	2.0			V	
			5.5	V	Maximum input voltage
Input Low Voltage, V_{IL}			0.8	V	
	–0.3			V	Minimum input voltage
Hysteresis		0.5		V_{p-p}	
DIGITAL INPUT LOGIC LEVELS ($\overline{\text{THERM}}$)					
Input High Voltage, V_{IH}			0.75 x V_{TT}	V	
Input Low Voltage, V_{IL}			0.4	V	
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}		±1		μA	$V_{IN} = V_{CC}$
Input Low Current, I_{IL}		±1		μA	$V_{IN} = 0$
Input Capacitance, C_{IN}		5		pF	
SLAVE SERIAL BUS TIMING (See Figure 1)					
Clock Frequency, f_{SCLK}	10		100	kHz	
Glitch Immunity, t_{SW}			50	ns	
Bus Free Time, t_{BUF}	4.7			μs	
SCL Low Time, t_{LOW}	4.7			μs	
SCL High Time, t_{HIGH}	4.0		50	μs	
SCL, SDA Rise Time, t_r			1,000	ns	
SCL, SDA Fall Time, t_f			300	ns	
Data Setup Time, $t_{SU;DAT}$	250			ns	
Detect Clock Low Timeout, $t_{TIMEOUT}$	15		35	ms	Can be optionally disabled
MASTER SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}		100		kHz	

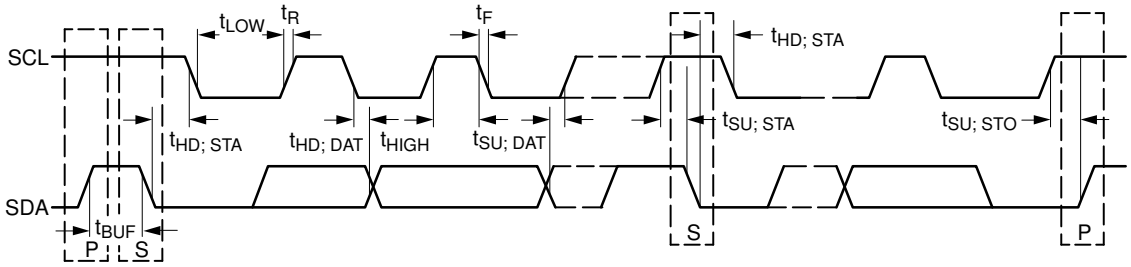


Figure 1. SMBus Timing Diagram for Slave Port and Master Port

Table 3. QSOP & QFN PACKAGE PIN ASSIGNMENTS

QSOP Pin No.	QFN Pin No.	Pin Name	Description
1	22	SDA_S	SMBus/I^{2}C Slave Serial Bi−directional Data Input/Output. Open−drain pin; Requires a pull−up resistor.
2	23	SCL_S	Serial Clock Slave Input. Open−drain pin; Requires a pull−up resistor.
3	24	GND	Ground
4	1	VDD	Positive Supply Voltage
5	2	SDA_M / GPIO1	Open−drain pin; Requires a pull−up resistor. GPIO1 = General purpose I/O pin SDA_M = SMBus/I^{2}C Master Serial Bi−directional Data Input/Output.
6	3	SCL_M / GPIO2	Open−drain pin; Requires a pull−up resistor. GPIO2 = General purpose I/O pin SCL_M = Serial Clock Master Output.
7	4	PECI	PECI input to report CPU Thermal Information. PECI voltage level is referenced to the VTT input.
8	5	VTT	Voltage reference for PECI. This is the supply voltage for the PECI interface and must be present to communicate over the PECI interface.
9	6	TACH3	Fan tachometer input to measure Fan3
10	7	PWM2 / #SMBALERT	PWM output to control Fan2. Can be configured as an SMBALERT output. Open−drain pin; Requires a pull−up resistor.
11	8	TACH1	Fan tachometer input to measure Fan1
12	9	TACH2	Fan tachometer input to measure Fan2
13	10	PWM3 / #ADDREN	PWM output to control Fan3. If pulled low on power−up the NCT7491 enters Address Select mode and the ADDRESS SELECT pin determines the slave address. Open−drain pin; Requires a pull−up resistor.
14	11	TACH4/ #THERM/ #SMBALERT/ #ADDRESS SELECT	Fan Tachometer Input to Measure Speed of Fan 4. May be reconfigured as a bidirectional THERM. Can be connected to thePROCHOT output of a processor, to time and monitor PROCHOT assertions. Can be used as an output to signal an overtemperature condition. The SMBALERT pin is used to signal out−of−limit comparisons of temperature, voltage, and fan speed. This is compatible with SMBus alert. Can also be used at device powerup to assign the SMBus address. If THERM or SMBALERT is enabled then a pull−up resistor is required.
15	12	D2−	Negative Connection for Remote Temperature Sensor 2.
16	13	D2+	Positive Connection for Remote Temperature Sensor 2.
17	14	D1−	Negative Connection for Remote Temperature Sensor 1.
18	15	D1+	Positive Connection for Remote Temperature Sensor 1.
19	16	GPIO3/ #THERM/ #SMBALERT	General−Purpose Open−Drain Digital Input/Output. Requires a pull−up resistor. Can be configured as a bidirectional THERM pin or as an SMBALERT pin.
20	17	+5Vin	Analog Input. 0 V to 5 V.
21	18	+12Vin	Analog Input. 0 V to 12 V.
22	19	+2.5V / #THERM	Analog Input. 0 V to 2.5 V. May be reconfigured as a bidirectional THERM pin. Can be connected to the PROCHOT output of a processor, to time and monitor PROCHOT assertions. Can be used as an output to signal an overtemperature condition. In THERM mode it is an open−drain bidirectional pin and requires a pull up resistor.
23	20	Vccp	Analog input. Monitors CPU core voltage (to maximum 0f 3.0 V). This pin must be connected to the NCT7491 supply voltage if it is unused.
24	21	PWM1 / XTO	PWM output to control Fan 1. Open−drain pin; Requires a pull−up resistor. Also functions as the output for the XNOR tree test enable mode.

Table 4. COMPARISON OF NCT7491 AND ADT7490 QSOP PINOUTS

QSOP Pin No.	NCT7491	ADT7490
1	SDA_S	SDA
2	SCL_S	SCL
3	GND	GND
4	VDD	VDD
5	SDA_M / GPIO1	GPIO1
6	SCL_M / GPIO2	GPIO2
7	PECI	PECI
8	VTT	VTT
9	TACH3	TACH3
10	PWM2 / #SMBALERT	PWM2 / #SMBALERT
11	TACH1	TACH1
12	TACH2	TACH2
13	PWM3 /#ADDREN	PWM3 /#ADDREN
14	TACH4/#THERM/#SMBALERT/ #ADDRESS SELECT	TACH4/#THERM/#SMBALERT/ #ADDRESS SELECT
15	D2–	D2–
16	D2+	D2+
17	D1–	D1–
18	D1+	D1+
19	GPIO3/#THERM/#SMBALERT	IMON
20	+5Vin	+5Vin
21	+12Vin	+12Vin
22	+2.5V / #THERM	+2.5V / #THERM
23	Vccp	Vccp
24	PWM1 / XTO	PWM1 / XTO

Functional Comparison between the NCT7491 and the ADT7490

- NCT7491 supports PECI 3.0 commands.
- NCT7491 uses an SMBus Master port to read digital temperatures.
- I_{MON} voltage monitoring pin (pin 19) on the ADT7490 is replaced with digital pin (SMBALERT/THERM/GPIO) on the NCT7491
- NCT7491 does not support Dynamic Tmin fan control.
- NCT7491 allows any combination of temperature sources to control any fan.
- NCT7491 allows individual PWM responses to THERM events.
- NCT7491 THERM behaviour is more flexible, allowing stepped response to THERM events.
- REPLACE mode for PECI is not supported by the NCT7491
- The NCT7491 register map is organized into two pages. 0x00–0xFF (page 1) and 0x100–0x1FF (page 2)
- The NCT7491 supports PWM look–up table automatic fan control along with the Tmin/Trange control method used in the ADT7490
- The NCT7491 allows temperatures to be written to the device from an external master. These values can be assigned for fan control and Limit/THERM assertion functions
- PECI fan control can be implemented in relative or absolute modes. Absolute mode uses the Tjmax value read from the CPU plus the PECI temperature to determine the actual core temperature.
- The reference for voltage measurement has changed from 2.25 V on the ADT7490 to 2 V on the NCT7491.

Functional Block Diagram

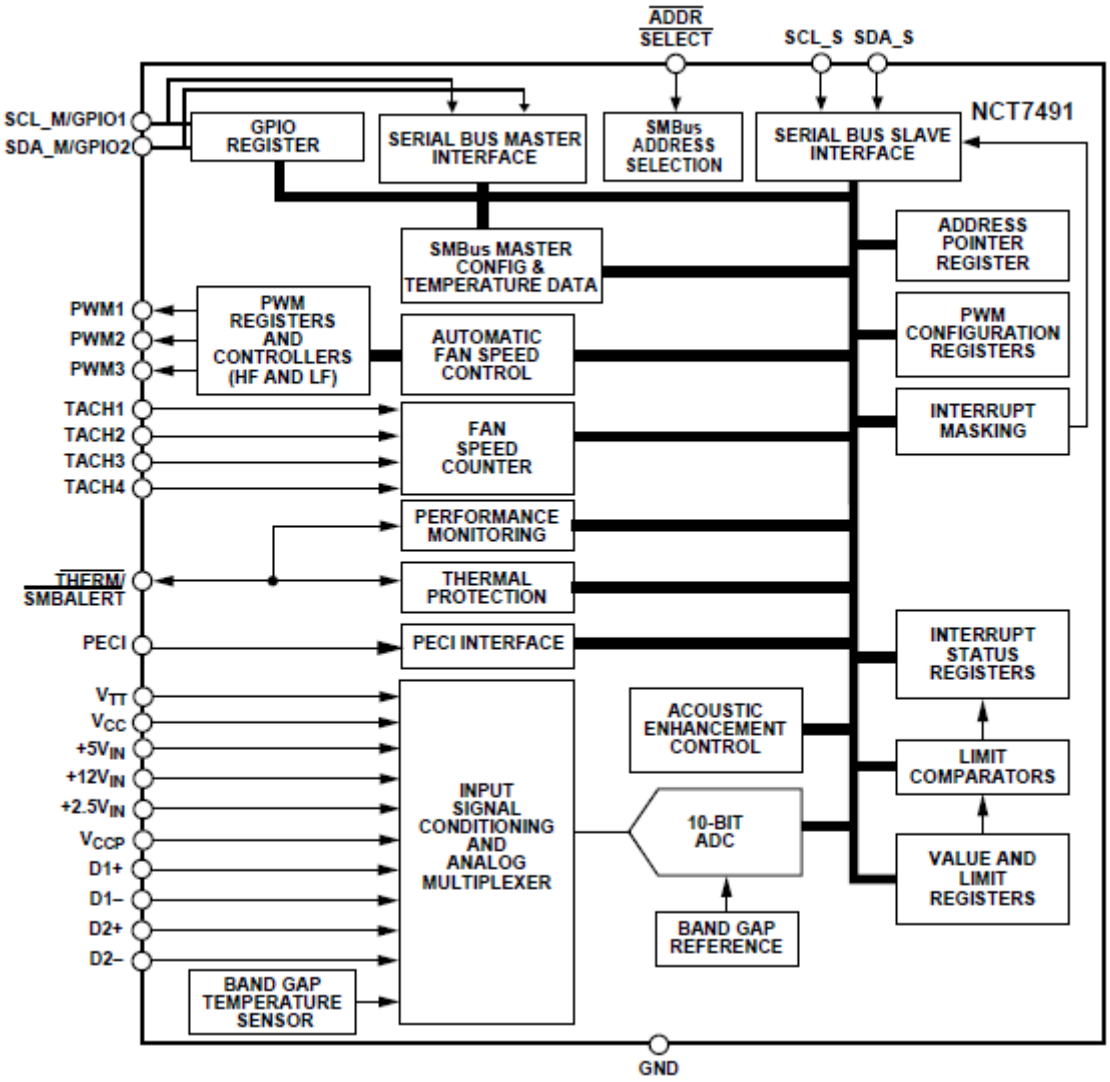


Figure 2. Functional Block Diagram of NCT7491

Typical System Connections

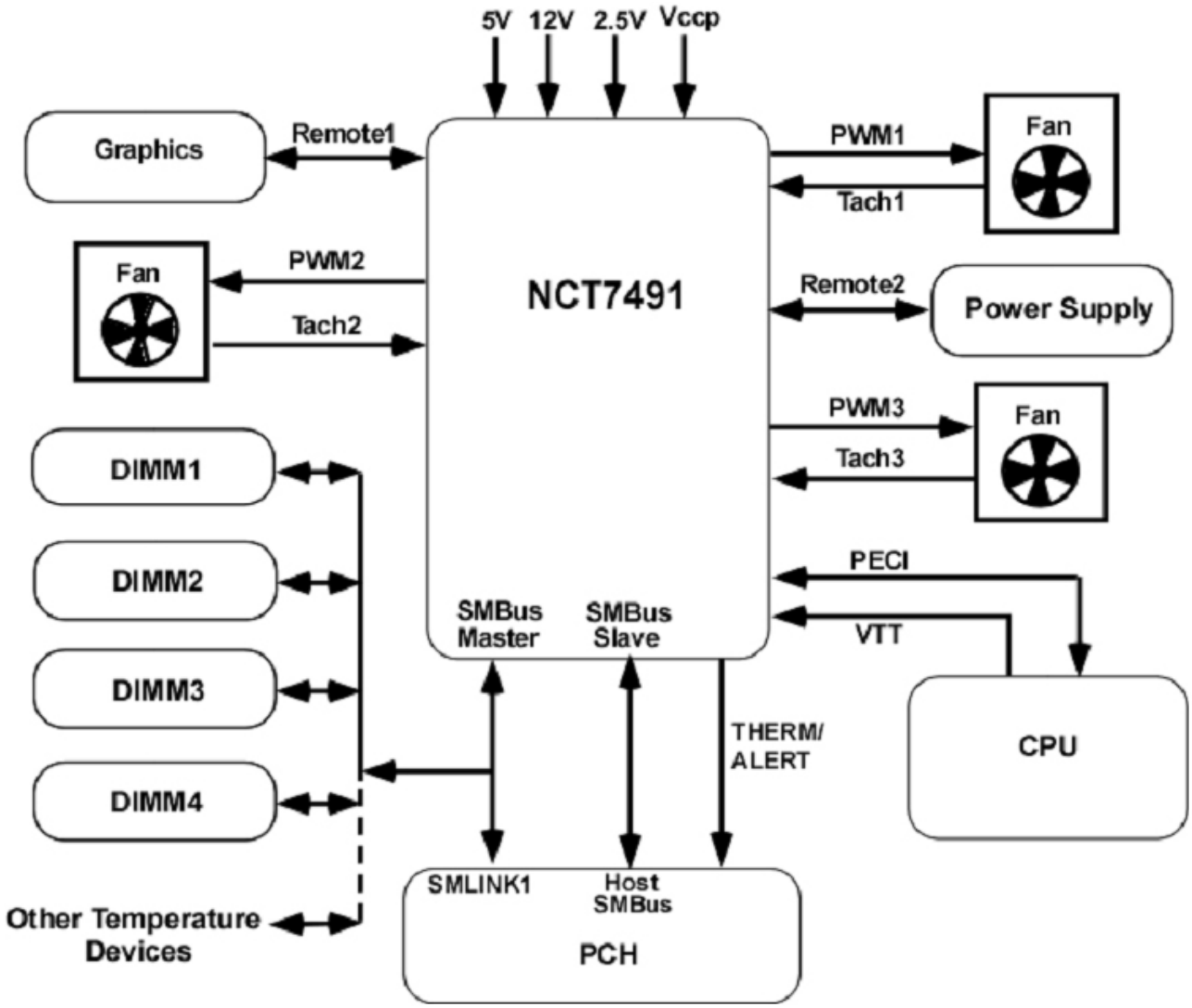


Figure 3. System Connection Diagram

SMBus Slave Interface

Control of the NCT7491 is carried out using the serial system management bus (SMBus). The NCT7491 is connected to this bus as a slave device, under the control of a master controller. The NCT7491 has a 7−bit serial bus address. When the device is powered up with the ADDREN pin high, the NCT7491 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to get the 8−bit address.

If more than one NCT7491 is to be used in a system, each additional NCT7491 is placed in address select mode by strapping ADDREN low on power−up. The logic state of the ADDRESS SELECT pin then determines the device's SMBus address.

The device address is latched on the first valid SMBus transaction, more precisely on the low−to−high transition at the beginning of the eighth SCL pulse, when the serial bus address byte matches the selected slave address. Any attempted changes in the address have no effect after this.

SMBus Addressing Options

Table 5. SETTING THE SMBUS ADDRESS

ADDREN pin state	ADDRESS SELECT pin state	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ pull−up)	0101101 (0x2D)
1	Don't care	0101110 (0x2E)

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low−to−high transition when the clock is high may be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master floats the data line high after the 10th clock rising edge to assert a stop condition. In read mode, the master device overrides the acknowledge bit by floating the data line high during the low period before the ninth clock pulse; this is known as No acknowledge. The master takes the data line low during the low period before the 10th clock rising edge, and then high afetr the 10th clock rising edge to assert a stop condition.

In the NCT7491, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed. Then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation must contain a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 4. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

- If the NCT7491 address pointer register value is unknown or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the NCT7491 as before, but only the data byte containing the register address is sent because no data is written to the register. This is shown in Figure 5.
  A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 6.
- If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, as shown in Figure 6.

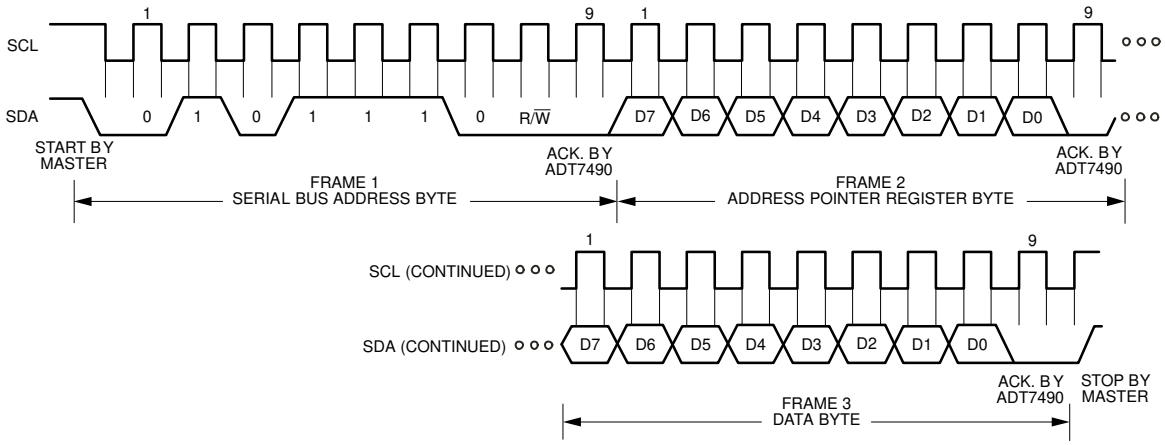


Figure 4. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

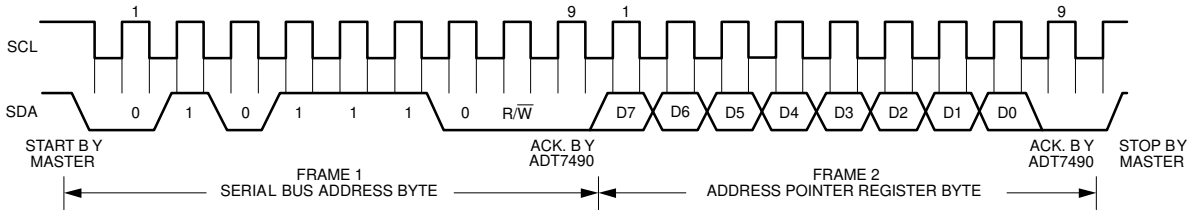


Figure 5. Writing to the Address Pointer Register Only

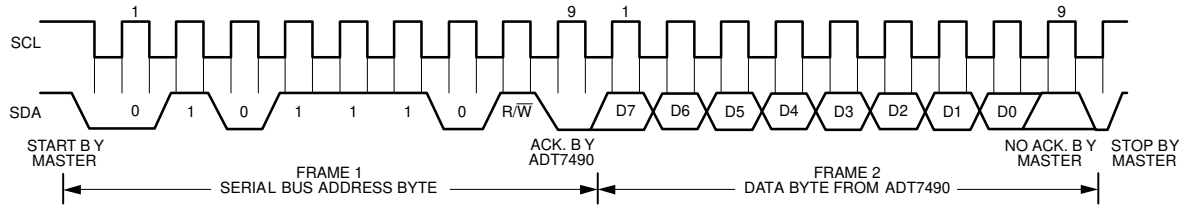


Figure 6. Reading Data from a Previously Selected Register

It is possible to read a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the NCT7491 also supports the read byte protocol (see *System Management Bus Specifications Rev. 2* for more information; this document is available from the SMBus organization).

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the NCT7491 are discussed here. The following abbreviations are used in the diagrams:

- S – Start
- P – Stop
- R – Read
- /$\overline{W}$ – Write
- A – Acknowledge
- /$\overline{A}$ – No acknowledge

The NCT7491 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the NCT7491, the send byte protocol is used to write a register address to RAM for a subsequent single−byte read from the same address. This operation is illustrated in Figure 7.

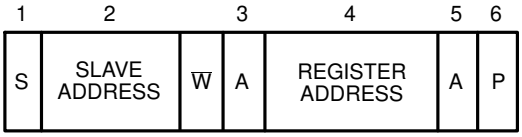


Figure 7. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single−byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA, and the transaction ends.

The byte write operation is illustrated in Figure 8.

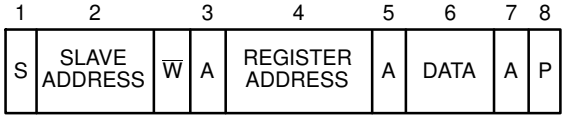


Figure 8. Single Byte Write to a Register

Read Operations

The NCT7491 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must be previously set up. In this operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the NCT7491, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 9.

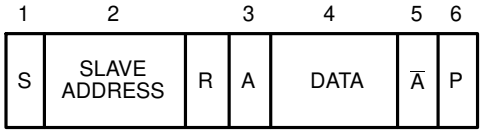


Figure 9. Single−Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The SMBALERT output can be used as either an interrupt output or an SMBALERT. One or more outputs can be connected to a common SMBALERT line connected to the master. If a device's SMBALERT line goes low, the following events occur:

1. SMBALERT is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose SMBALERT output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
4. If more than one device's SMBALERT output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the NCT7491 has responded to the alert response address, the master must read the status registers, and the SMBALERT is cleared only if the error condition is gone.

SMBus Timeout

The NCT7491 includes an SMBus timeout feature. If there is no SMBus activity for 25 ms, the NCT7491 assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot work with the SMBus timeout feature, so it can be disabled.

Register 0x11 <4> TODIS = 0, SMBus timeout enabled (default). <4> TODIS = 1, SMBus timeout disabled.

Register Map Paging

The NCT7491 register map is organized into two pages:

- Page 1 contains register addresses 0x00 to 0xFF
- Page 2 contains register addresses 0x100 to 0x1FF

The default page on power up is page 1, so any SMBus read/writes to the NCT7491 will be to addresses in the range 0x00−0xFF.

To access page 2 of the register map, bit 0 (RGMP) of register 0xFF must be set to 1. Any subsequent read/writes after that bit is set will be to addresses in the range 0x100 to 0x1FF, e.g. reading from address 0x22 when RGMP is set will read from register 0x122. Bit 0 of register 0xFF is, in effect, the MSb of the address pointer. To return to page 1, bit 0 (RGMPCL) of register 0x1FF must be cleared to 0.

All register read/writes referenced in this document refer to registers on SMBus Page 1 unless stated otherwise.

Analog Temperature Measurement

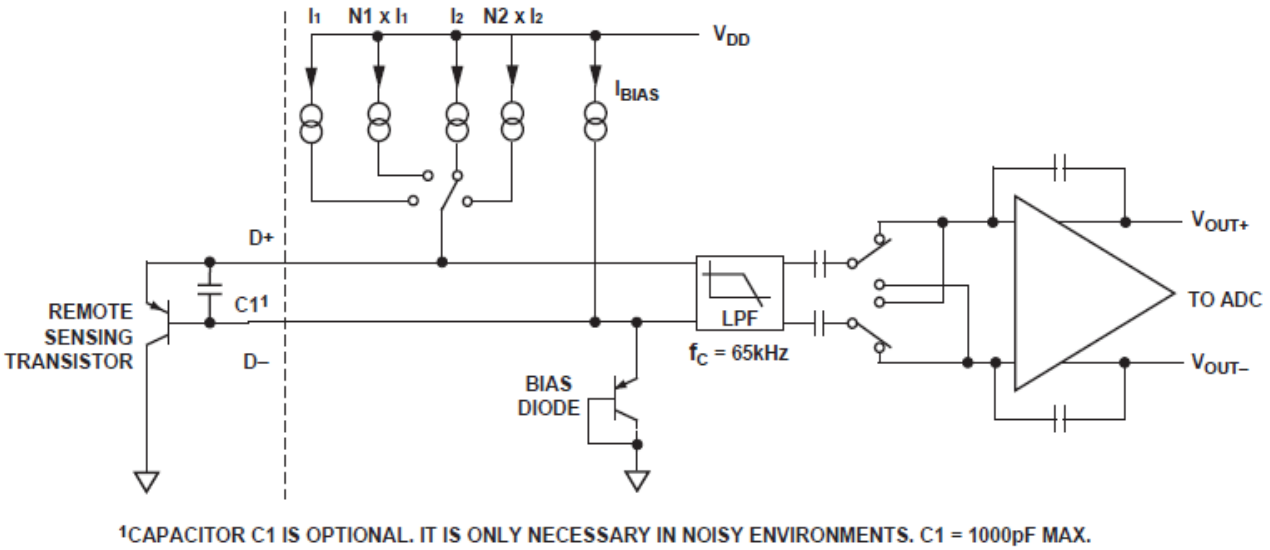
A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode connected transistor, measuring the base emitter voltage (V_{BE}) of a transistor operated at constant current. However, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the NCT7491 measures the change in V_{BE} when the device operates at four different currents.

Figure 10 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it can equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded but is linked to the base.

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D− input. C1 may be added as a noise filter (a recommended maximum value of 1000 pF). However, a better option in noisy environments is to add a filter, as described in the Noise Filtering section.

To measure ΔV_{BE}, the operating current through the sensor is switched among 4 currents, 2 x 2 related currents. As shown in Figure 10, N1 x I_1 is a multiple of I_1 and N2 x I_2 is a multiple of I_2. The currents through the temperature diode are switched between I and N1 x I, giving ΔV_{BE1}; and then between I and N2 x I, giving ΔV_{BE2}. The temperature is then calculated using the two ΔV_{BE} measurements. This method cancels the effect of any series resistance on the temperature measurement.



[1]CAPACITOR C1 IS OPTIONAL. IT IS ONLY NECESSARY IN NOISY ENVIRONMENTS. C1 = 1000pF MAX.

Figure 10. Analog Temperature Measurement Method

Series Resistance Cancellation

Parasitic resistance to the D+ and D− inputs to the NCT7491, seen in series with the remote diode, is caused by a variety of factors, including PCB track resistance and track length and internal resistance in the CPU. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5 degree C offset per ohm of parasitic resistance in series with the remote diode.

The NCT7491 automatically cancels the effect of this series resistance on the temperature reading, giving a more accurate result, without the need for user characterization of this resistance. The NCT7491 is designed to automatically cancel typically up to 270 Ω of resistance in series with the thermal diode. By using an advanced temperature measurement method, this process is transparent to the user. This feature permits resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments.

Temperature Measurement Results

The results of the Local, Remote 1 and Remote 2 temperature measurements are stored in the local (0x26), remote 1 (0x25) and remote 2 (0x27) temperature value registers in two's complement format or Offset 64 format, depending on bit 0 if register 0x7C (1= 2's complement, 0 = Offset 64). These results are then compared with limits programmed into the local, remote 1 and remote 2 high and low limit registers. The high, low and THERM limits for the local, remote 1 and remote 2 channels must be in the same format as the temperature reading i.e. 2's complement or Offset 64.

All the temperature measurement data for each channel is stored in two registers, one for the MSB and one for the LSB. This gives the temperature measurement resolution of 0.25°C. When reading the full external temperature value, read the LSB first. This causes the MSB to be locked (that is, the ADC does not write to it) until it is read. This feature ensures that the results read back from the two registers come from the same measurement.

Theoretically, the temperature sensor and ADC can measure temperatures from −64°C to +127.5°C with a resolution of +0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside the NCT7491 operating temperature range are not possible.

- Remote1 result registers: 0x25 (MSB), 0x77 bits <3:2> (2 LSb)
- Local result registers: 0x26 (MSB), 0x77 bits <5:4> (2 LSb)
- Remote1 result registers: 0x27 (MSB), 0x77 bits <7:6> (2 LSb)

Table 6. TWO'S COMPLEMENT FORMAT

Temperature	Digital Output (10−Bit)
−64°C	1100 0000 **00**
−55°C	1100 1001 **00**
−40°C	1101 1000 **00**
−10°C	1111 0110 **00**
−1°C	1111 1111 **00**
−0.25°C	1111 1111 **11**
0°C	0000 0000 **00**
10.25°C	0000 1010 **01**
25°C	0001 1001 **00**
125°C	0111 1101 **00**
127.5°C	0111 1111 **10**
Diode Fault – 127.75	0111 1111 **11**

NOTE: Bold numbers denote the LSB bits from extended resolution register 0x77.

Offset 64 Format

In Offset 64 mode the range of values monitored is −64°C to 191.5°C (as opposed to −64°C to +127.5°C in 2's complement mode). To read the temperature in this format the user must subtract 64 from the value returned from the temperature register. Offset 64 mode is enabled by setting bit 0 if register 0x7C to zero.

Table 7. OFFSET64

Register Code	Temperature
0	−64°C
32	−32°C
64	0°C
100	36°C
255	191°C

Round Robin Temperature Measurement

The local and remote sensors are read in sequence in a continuous loop when monitoring is enabled (setting bit 0 of register 0x40). The user may decide which temperature channels are included in the monitoring loop using bits <2:0> in register 0x13.

- Setting <0> of register 0x13 includes the local channel in the monitoring loop.
- Setting <1> of register 0x13 includes the remote1 channel in the monitoring loop.
- Setting <2> of register 0x13 includes the remote2 channel in the monitoring loop.

Any channel not required in an application should be removed from the loop to reduce the overall monitoring time. Voltage channels may also be selected for the monitoring loop. See the Voltage Monitoring section for more information.

Temperature Averaging

The number of samples over which the temperature readings (and voltage readings) are averaged is set by bits <7:6> of register 0x40. The options are:

- 4 samples per averaged reading, <7:6> = <00>
- 8 samples per averaged reading, <7:6> = <01>
- 16 samples per averaged reading, <7:6> = <10>
- 32 samples per averaged reading, <7:6> = <11>

Averaging can be disabled for temperature readings by setting bit <4> of register 0x73.

Temperature Limits

Temperature limits can be set for each channel to detect an out of limit condition. These registers are programmed in the same format as the temperature reading, so if Offset64 mode is enabled then these registers must be programmed in that format, otherwise theay are programmed as 2's complement.

- Remote1 Low Limit register: 0x4E
- Remote1 High Limit register: 0x4F
- Local Low Limit register: 0x50
- Local High Limit register: 0x51
- Remote2 Low Limit register: 0x52
- Remote2 High Limit register: 0x53

Offset Registers

Offset errors can be introduced into the temperature measurements by clock noise or when the thermal diode is located away from the hot spot. To achieve the specified accuracy on this channel, these offsets must be removed.

The offset value is stored as an 8−bit, twos complement value. The value in the offset register is added to, or subtracted from, the measured value of the relevant temperature. The offset register has a default value of 0°C and has no effect unless the user writes a different value to it. The resolution of the value in the offset register is determined by bit 1 of register 0x7C. If the bit is 0 then the resolution is 0.5°C. If the bit is 1 then the resolution is 1°C.

- Remote1 Offset, register 0x70
- Local Offset, register 0x71
- Remote2 Offset, register 0x72

Push Registers

The NCT7491 allows the user to program 4 temperatures into the device that can then be used for fan control and THERM/SMBALERT functions in the same way as other temperature sources. These temperatures can be written by the system SMBus master and should be programmed as 2's complement values.

- Push0, register 0xC8
- Push1, register 0xC9
- Push2, register 0xCA
- Push3, register 0xCB

Push Limit Registers

There are high, low and THERM limits associated with the Push channels. The same limits are applied to all 4 channels.

- Push Low Limit register, 0xCF
- Push High limit register, 0xCE
- Push THERM Limit register, 0xD0

Push Tmin/Trange Registers

The Push channels also have associated Tmin/Trange values for Automatic Fan Control. The hysteresis applied at the Tmin value can also be programmed.

- Push Tmin, 0xCC
- Push Trange, 0xCD bits <3:0>
- Push Hysteresis, 0xEB bits <3:0>

PECI 3.0 Interface

The PECI 3.0 interface reads thermal data from the up to 4 CPUs located at PECI addresses between 0x30 and 0x37 (the first 4 addresses populated are used), and from 1 or 2 domains per CPU. The hottest reading from the domains for each CPU is stored in the PECI temperature registers. It can

also write thermal data to the Package Configuration Space in the CPU. A PECI reading is a negative value, in degrees Celsius, which represents the offset from the thermal control circuit (T_{CC}) activation temperature. PECI information is returned as a 16−bit 2's complement value from which the 8−bit 2's complement value is derived. See the Platform Environment Control Interface (PECI) Specification from Intel for more details on the PECI data format. The PECI temperature stored for each CPU is an averaged value; the averaging window is user programmable.

The NCT7491 automatically detects the presence of a CPU at each of the supported addresses, and also detects the number of supported domains for each CPU. The presence of each CPU is indicated in the NCT7491 status registers.

On power up, the PECI interface will become active when the voltage measured on VTT is above 0.5 V and the voltage on Vccp is above 0.5 V. The returned CPU temperature will determine the behavior of the fans on power−up.

Thermal data that is collected by the NCT7491 (e.g. the DIMM temperatures) can be written to the CPU's Package Configuration Space (PCS) over the PECI 3.0 interface. This data can be used by the CPU to modify memory operations based on the DIMM temperature.

There are associated high and low limits for each PECI reading that can be programmed. The limit values take the same format as the PECI reading. Therefore, the programmed limits are not absolute temperatures but a relative offset in degrees Celcius from the TCC activation temperature. An out−of−limit event is recorded as follows:

- High Limit > comparison performed
- Low Limit ≤ comparison performed

An out−of−limit event is recorded in the associated status register and can be used to assert the SMBALERT pin.

A generic PECI 3.0 interface command structure is also available to allow an external master to issue any PECI 3.0 command in addition to the commands implemented by the NCT7491 monitoring loops.

PECI V_{TT} Input

The PECI V_{TT} voltage is used as the reference voltage for the PECI interface. This voltage must be connected to the NCT7491 in order for the PECI interface to be operational. The PECI V_{TT} input is also monitored by the NCT7491 and has associated high and low limits to allow out−of−limit detection on the V_{TT} channel. The valid operational voltage range for PECI V_{TT} is 0.85 V to 1.26 V.

PECI Startup Operation

On power up of the NCT7491 the PECI V_{TT} pin and the Vccp pin are monitored. If the voltage on both of these pins rises above 0.5 V then the NCT7491 will wait 5 ms and then automatically scan the PECI port to check for the presence of PECI 3.0 enabled processors. For any processors that are detected the PECI address, the domain count, the Tcontrol value and the Tjmax value will be read and stored in the NCT7491. The CPU count bits will be set (bits <7:6> of register 0x88). The PDET bit (bit <0> 0f register 0x37) will also be set to indicate that at least one CPU was detected. If any processors are detected then the PECI monitoring loop will automatically start.

The Vccp pin must be connected to an input voltage for the PECI interface to function correctly. If it is not connected to the CPU supply voltage then it should be connected to the NCT7491 supply voltage, Vcc. If the system processor does not support PECI 3.0 then the PECI monitoring loop will not automatically start. In that case the user can write to the PECI registers to manually configure the interface. The register descriptions are given below.

PECI Error Detection

The PECI 3.0 protocol includes FCS (Frame Check Sequence) bytes to guarantee data integrity. If there is a mismatch between the data and the FCS then a status bit indicates the communication failure (COMM status bit, register 0x43 bit <2>). PECI 3.0 also supports processor specific error codes to indicate error conditions relating to the temperature sensor within the processor (DATA status bit, register 0x43 bit <1>). These codes are shown in Table 8:

Table 8. DATA ERROR CODES

DATA code bits <6:4>, 0x43	DATA Error code	Description
<000>	0x8000	General Sensor Error
<001>	0x8002	Temperature below operational range
<010>	0x8003	Temperature above operational range

PECI Completion Code

Each read or write operation to the CPU Package Configuration Space returns a completion code to indicate the success or failure of the operation. The completion codes supported are shown in Table 9:

Table 9. COMPLETION CODES

Completion Code	Description
0x40	Command Passed, data is valid
0x80	Command timed out. Processor cannot generate required response in a timely fashion. Retry is appropriate.
0x81	Command timed out. Processor cannot allocate resources for the request. Retry is appropriate.
0x90	Unknown/Invalid/Illegal request
0x91	PECI Control hardware, firmware or associated logic error. The processor cannot process the request.

The completion code status bit in the NCT7491 (register 0x81 bit <0>) indicates the result of each read/write operation.

PECI Registers

The registers relating to the operation of the PECI 3.0 interface are as follows:

Enabling the Interface:

- PECI Monitor, 0x40 bit 4

Setting PECI Monitor to 1 enables the PECI temperature monitoring loop. This will be automatically enabled on power up if the V_{TT} and V_{CCP} voltages have exceeded preset thresholds and any PECI 3.0 enabled processors have been automatically detected.

NOTE: The PDET bit (bit <0> 0x37) must also be set for correct operation.

Detected number of CPUs:

- CPU Count, 0x88 bits <7:6>
- PDET, 0x37 <0>

CPU Count indicates the number of populated CPUs. CPUs are automatically detected on power up by the NCT7491 and the number found is set here. The number can be overwritten by the user and sets the number of CPUs to be included in the temperature monitoring loop. The number of CPUs is 1 to 4, and the format is as shown in Table 10.

PDET is set if at least one PECI enabled processor is detected. If it is not automatically set then it must be set by the user.

Table 10. CPU COUNT

0x88 <7:6>	CPU Count
<00>	1
<01>	2
<10>	3
<11>	4

Domain Count bits:

- DOM0, 0x36 bit 3
- DOM1, 0x88 bit 5
- DOM2, 0x88 bit 4
- DOM3, 0x88 bit 3

These bits indicate the number of supported domains per CPU (0 = 1 domain, 1 = 2 domains). THE NCT7491 automatically detects these values on power up and sets the appropriate bits. They can be overwritten by the user.

PECI Interval:

- PECI Update Rate, 0x37 bits <5:4>

This determines the rate at which the PECI temperature registers are updated.

Table 11. UPDATE RATE

0x37 <5:4>	PECI Update Rate
<00>	1/sec
<01>	2/sec
<10>	5/sec
<11>	10/sec

PECI CPU Addresses:

- PECI0 CPU Address, 0x00
- PECI1 CPU Address, 0x01
- PECI2 CPU Address, 0x02
- PECI3 CPU Address, 0x03

These are the addresses used to access each CPU on the PECI interface and are automatically populated by the NCT7491 on power up. The values can be overwritten by the user.

PECI Temperature Values:

- PECI0 Temperature, 0x33
- PECI1 Temperature, 0x1A
- PECI2 Temperature, 0x1B
- PECI3 Temperature, 0x1C

These are the relative temperature values returned by the CPU. If a CPU is not populated then its associated temperature register can be written to by an external master. Data is tored in 2's complement format.

PECI Absolute Temperature Values:

- PECI0_Abs Temperature, 0x04
- PECI1_Abs Temperature, 0x05
- PECI2_Abs Temperature, 0x06
- PECI3_Abs Temperature, 0x07

These are the absolute CPU temperature values. They are automatically calculated by the NCT7491 from the relative temperature and the CPU T_{JMAX} value. See the **PECI T_{JMAX} Values** section. Data is stored in unsigned format.

Absolute PECI mode

The user can enable Absolute PECI mode by setting bit 2 of register 0x73 (ABS/REL) which will use the value stored in the PECI absolute temperature registers for fan control, THERM behaviour and SMBALERT behaviour rather than the relative PECI values.

PECI Averaging

The number of samples over which the PECI master will calculate an averaged temperature reading for each CPU can be set in register 0x36, bits <2:0>:

- <000> = No averaging
- <001> = Averaged over 2 samples
- <010> = Averaged over 4 samples
- <011> = Averaged over 8 samples
- <100> to <111> are reserved

PECI Offsets:

- PECI0 Offset, 0x94
- PECI1 Offset, 0x95
- PECI2 Offset, 0x96
- PECI3 Offset, 0x97

Offset values can be assigned to each temperature channel by programming these registers. The value programmed should be in 2's complement format. The resolution is 1°C.

PECI Limits:

- PECI Low Limit, 0x34
- PECI High Limit, 0x35

These registers are used to set the allowable PECI temperature range. If the temperature is above the high limit or below the low limit then a status bit is set and pins configured as SMBALERT will assert. The high and low limit values are common to all PECI channels. The format depends on whether Absolute PECI mode is enabled. If it is then the limits are in unsigned format. If Absolute PECI mode is not enabled then the format is 2's complement.

PECI $T_{CONTROL}$ Values:

- PECI0 $T_{CONTROL}$, 0x3D
- PECI1 $T_{CONTROL}$, 0x08
- PECI2 $T_{CONTROL}$, 0x09
- PECI3 $T_{CONTROL}$, 0x0A

These values set the fail−safe fan assertion temperature. The response of the fans is determined by the THERM configuration registers and is described in the 'THERM Assertion' section of this document. These values can be read from the CPU via the PECI interface or programmed directly by the user.

The format depends on whether Absolute PECI mode is enabled. If it is then the limit is in unsigned format. If Absolute PECI mode is not enabled then the format is 2's complement.

PECI T_{JMAX} Values:

- PECI0 T_{JMAX} , 0x0B
- PECI1 T_{JMAX} , 0x0C
- PECI2 T_{JMAX} , 0x0D
- PECI3 T_{JMAX} , 0x0E

Each CPU has a maximum junction temperature T_{JMAX}. These values for the populated CPUs are read via the PECI 3.0 interface by the NCT7491. They can also be over−written by the user. They are used to determine the absolute PECI temperature. These values are stored as unsigned data.

PECI Fan Control:

- PECI Tmin, 0x3B
- PECI Trange, 0x3C bits <7:4>
- PWM1 Source1, 0x8A bits <6:3>
- PWM2 Source1, 0x8D bits <6:3>
- PWM3 Source1, 0x90 bits <6:3>

Tmin sets the turn−on temperature for any fan that is controlled by a PECI temperature.

Trange sets the range over which the PWM output will increase from PWMmin to PWMmax.

The PECI Tmin and PECI Trange values are common to all PECI channels.

The PWMX Source registers are used to assign temperature control to a fan. The PECI assignment is done with bits <6:3> in those registers.

The user can choose to use the relative or absolute PECI temperature values for fan control. If Absolute PECI mode is used then the maximum valid Tmin value is 175°C.

For full details on the Fan Control implementation see the 'Fan Control' section of this document

PECI Status Bits:

- PECI0 limit error, 0x43 bit 0
- PECI1 limit error, 0x81 bit 3
- PECI2 limit error, 0x81 bit 4
- PECI3 limit error, 0x81 bit 5
- DATA error, 0x43 bit 1
- COMM error, 0x43 bit 2
- DATA type, 0x43 bits <6:4>
- PECI completion code, 0x81 bit 0
- PECI0 $T_{CONTROL}$ exceeded, 0x89 bit 0
- PECI1 $T_{CONTROL}$ exceeded, 0x89 bit 1
- PECI2 $T_{CONTROL}$ exceeded, 0x89 bit 2
- PECI3 $T_{CONTROL}$ exceeded, 0x89 bit 3

The Data Type field indicates the returned code if a DATA error is generated. Status bits in 0x43 and 0x81 can be masked by setting the corresponding mask bits in registers 0x82 and 0x83.

Generic PECI Command Block

- CPU Address, 0xD1
- Data Write Length, 0xD2
- Data Read Length, 0xD3
- Data Write Buffer, 0xD4 to 0xE0
- Data Read Buffer, 0xE1 to 0xE9
- Generic PECI Configuration, 0xEA

These registers define the generic PECI interface. An external master can populate these registers in order to execute any supported PECI 3.0 commands.

The byte definitions for this block are as follows:

CPU Address sets the target address of the PECI client that is to be accessed.

Data Write Length sets the number of bytes to be transferred to the PECI client. This byte should include the AW FCS byte in its count. The AW FCS byte is automatically calculated and appended by the NCT7491.

Data Read Length sets the number of bytes to be returned from the PECI client.

Data Write Buffer is a 13 byte buffer that holds the data to be transferred to the client. The first byte of this buffer is the command code that defines the command to be executed.

Data Read Buffer is a 9 byte buffer that will hold the data returned from the client.

The PECI Configuration 5 register (address 0xEA) enables the generic block and allows the command to be executed. The configuration bits are:

- AW, bit 1
- PEX, bit 2

Setting **AW** to 1 indicates that the transfer is an Assured Write transaction.

Setting **PEX** to 1 causes the NCT7491 to execute the command that has been set up in the generic command block. This bit will automatically clear when the transaction has completed.

If a communication error occurs when a Generic PECI command is sent then the GCOMM status bit is set. This bit can be masked.

- GCOMM, register 0x81 <2>
- GCOMM mask, register 0x83 <2>

SMBus Compatible Master Port

Thermal data is gathered from temperature monitoring devices attached to the SMBus Master port on the NCT7491. This port is used to automatically read temperature data from DIMM sensors, the PCH chipset sensor, graphics thermal sensors, or any thermal sensor with an SMBus interface. Up to 8 thermal slave devices are supported on the SMBus master port. The SMBus slave address for each device is user programmable. The register address of the thermal data within the slave device is also user programmable. This is assumed to be a 1−byte address so devices with a register address range of 0x00 to 0xFF are suitable. Each slave device has associated programmable configuration bits to indicate the protocol required to communicate over the SMBus and the temperature data format returned by the slave device. Status bits will indicate if any checksum errors arise from communicating with the slave devices.

The NCT7491 can be connected to the SMLINK1 port of the PCH to allow the PCH thermal data to be read. Data is automatically read from the PCH using the SMBus Block Read protocol. The device can be configured to read the DIMM temperature registers from the PCH.

The SMBus master and slave ports on the NCT7491 can be connected together if required.

Temperature readings returned from the thermal devices on the SMBus master port are available for use in the Automatic Fan Control algorithm.

The SMBus thermal devices have associated high and low temperature limit registers to allow out−of−limit conditions to be detected. If the SMBus Master interface is disabled then the SMBus master is internally connected to the slave interface, if the pins have not been assigned to GPIO functions. Enabling the SMBus master port overrides any GPIO1/GPIO2 configuration settings.

SMBus Compatible Master Registers

The registers relating to the control of the SMBus compatible master interface are as follows:

Enabling the SMBus Master port:

- SMBus Master Enable, 0xB5 bit 0

Setting this bit configures pins 5 and 6 on the QSOP package, or pins 2 and 3 on the QFN package as the SMBus Master Port. It also enables the Thermal slave temperature monitoring loop which will gather data from the devices configured in the SMBus Master Addressing table.

When this bit is 0 and pins 5 and 6 on the QSOP package, or pins 2 and 3 on the QFN package are not configured as GPIOs then the SMBus slave port is internally connected to the SMBus master port. This allows the master connected to the NCT7491 to communicate directly with devices that are on the NCT7491 master port.

Temperature Addressing Table:

- Device0 Address, 0x98
- Device0 Pointer, 0x99
- Device1 Address, 0x9A
- Device1 Pointer, 0x9B
- Device2 Address, 0x9C
- Device2 Pointer, 0x9D
- Device3 Address, 0x9E
- Device3 Pointer, 0x9F
- Device4 Address, 0xA0
- Device4 Pointer, 0xA1
- Device5 Address, 0xA2
- Device5 Pointer, 0xA3
- Device6 Address, 0xA4
- Device6 Pointer, 0xA5
- Device7 Address, 0xA6
- Device7 Pointer, 0xA7

The DeviceX Address register sets the 7−bit (R/W bit not included) SMBus address of the thermal sensor.

The DeviceX Pointer register sets the register address of the temperature data in the thermal slave device.

Device0 can be used for SMBus Block Read commands. In that case the block read command code should be written to the Device0 Pointer register. If the NCT7491 Master port is connected to the SMLINK1 port of the Intel PCH then the PCH temperature (and possibly the DIMM temperatures) can be read from this port. In that case Device0 should be reserved for the PCH temperature and Device1 to Device 4 reserved for DIMM0 to DIMM3.

The NCT7491 will not attempt to read from a device that has a Device Address byte that is set to 0.

Temperature Values:

- Device0 (PCH), 0xA8
- Device1 (DIMM0), 0xA9
- Device2 (DIMM1), 0xAA
- Device3 (DIMM2), 0xAB
- Device4 (DIMM3), 0xAC
- Device5, 0xAD
- Device6, 0xAE
- Device7, 0xAF

The results of the readings from each of the thermal slave devices are stored here.

Thermal Slave Data Formats

It is necessary for the NCT7491 to be configured so that the data format for each SMBus client device is known, e.g. if the data is 2's Complement or unsigned data, or if a JEDEC standard SPD device is used so that the data can be correctly read from the device. Each SMBus device has a bit field to determine the data format for that device. The format selected for the device determines its behaviour for out−of−limit comparisons, THERM assertions and fan control operation. For Device0, if the format is set to PCH Block Read then the resulting data is stored as unsigned binary. The VR12 literal mode can be selected to allow temperature or power data be read from a VR12 controller via the PMBus.

Table 12. Device0 FORMATS

0xB2 <1:0>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	PCH block reads

Table 13. Device1 FORMATS

0xB2 <3:2>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	reserved

Table 14. Device2 FORMATS

0xB2 <5:4>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	reserved

Table 15. Device3 FORMATS

0xB2 <7:6>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	reserved

Table 16. Device4 FORMATS

0xB3 <1:0>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	reserved

Table 17. Device5 FORMATS

0xB3 <3:2>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	VR12 Literal

Table 18. Device6 FORMATS

0xB3 <5:4>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	VR12 Literal

Table 19. Device7 FORMATS

0xB3 <7:6>	Format
00	2's Complement
01	JEDEC SPD standard
10	Unsigned binary
11	VR12 Literal

SMBus Master Update Rate

The interval between successive reads from an SMBus client device is determined by register 0xC7 bits <7:6>:

Table 20. SMBus UPDATE

0xC7 bits <7:6>	SMBus Update Rate
00	250 ms
01	500 ms
10	750 ms
11	1 sec

Thermal Slave Limits:

- SMB Slave High Limit, 0xC1
- SMB Slave Low Limit, 0xC2

These registers are used to set the allowable Thermal slave temperature range. If the temperature is above the high limit or below the low limit then a status bit is set and pins configured as SMBALERT will assert. The high and low limit values are common to all SMBus Thermal slave readings. The low limit is programmed as a 2's Complement value. The high limit is programmed as an unsigned value. The difference between the two formats is necessary to cover the alternate formats available for the SMBus slave devices.

Thermal Slave THERM Value:

- SMBus THERM Limit, 0xC3

This value sets the fail−safe THERM assertion temperature. The response of the fans is determined by the THERM configuration registers and is described in the 'THERM Assertion' section of this document. This value is programmed as an 8−bit unsigned value.

Thermal Slave Fan Control:

- SMB Device Tmin, 0xC6
- SMB Device Trange, 0xC7 bits <3:0>
- PWM1 Source2, 0x8B
- PWM2 Source2, 0x8E
- PWM3 Source2, 0x91

Tmin sets the turn−on temperature for any fan that is controlled by a Thermal slave device. Trange sets the temperature range over which the PWM output will increase from PWMmin to PWMmax. The Tmin and Trange values apply to all Thermal slave devices. SMB Tmin is programmed as an 8−bit unsigned value. The maximum valid SMBus Tmin value is 175°C.

The PWMX Source registers are used to assign temperature control to a fan.

For full details on the Fan Control implementation see the 'Fan Control' section of this document.

SMBus Master Communication Settings

- Repeated Start Enable, 0xB0 bits <7:0>
- PEC Supported, 0xB1 bits <7:0>

The Repeated Start bits enable/disable the repeated start protocol for each device.

The PEC Supported bits can be set if an SMBus client device supports CRC−8 PEC. If this bit is set for a client device then the NCT7491 will read the PEC byte after the data and set the corresponding bit in the PEC status register (0xB7) if the PEC byte is incorrect.

DIMM Temperatures from PCH

- Read DIMM from PCH, 0xB5 bit 7

If this bit is set to 1 then the SMBus master port will read the DIMM registers from the SMLINK1 port of the PCH and store the results in registers 0xA9 to 0xAC. If it is 0 then it will read DIMM temperatures from SMBus slave devices.

DIMM Temperatures from Remote Sensors

- DIMM 0/1 from Remote1, 0xB5 bit 5
- DIMM 2/3 from Remote2, 0xB5 bit 6

If 0xB5 <5> is 1 then registers 0xA9 and 0xAA are overwritten by the Remote1 temperature reading.

If 0xB5 <6> is 1 then registers 0xAB and 0xAC are overwritten by the Remote2 temperature reading.

If bit 7 of 0xB5 (DIMM from PCH) is set then bits 5 and 6 have no effect.

Writing DIMM temperatures to the CPUs

The DIMM temperatures collected from SPD devices, from the PCH or from the analog thermal sensors can be automatically written to the CPU via PECI. To enable this function set the PWEN bit, register 0x37 <7>. The temperatures written will be the maximum DIMM temperature for each CPU.

DIMM CPU assignments:

- DIMM0 CPU, 0x0F bits <1:0>
- DIMM1 CPU, 0x0F bits <3:2>
- DIMM2 CPU, 0x0F bits <5:4>
- DIMM3 CPU, 0x0F bits <7:6>

These bits set the CPU associated with each DIMM. This information is necessary in order for the PECI loop to program the maximum DIMM temperature for each CPU.

Selecting DIMMs To Be Written

Each DIMM register can be enabled to be written to the CPU individually. This is done in register 0x87 bits <7:4>. If a DIMM is not populated then the corresponding bit in this register should be set to zero:

Setting 0x87 bit <4> to 1 includes DIMM0 in the PECI write

Setting 0x87 bit <5> to 1 includes DIMM1 in the PECI write

Setting 0x87 bit <6> to 1 includes DIMM2 in the PECI write

Setting 0x87 bit <7> to 1 includes DIMM3 in the PECI write

SMBus Thermal Slave Error Response

How the NCT7491 responds to errors on the SMBus master port can be configured in the following ways:

- SMBus Retry Interval, 0x10 bits <4:3>
- PWM1 Response, 0x11 bit 5
- PWM2 Response, 0x11 bit 6
- PWM3 Response, 0x11 bit 7

SMBus Retry Interval: If an error is encountered when communicating with a Thermal slave device then the NCT7491 will attempt to carry out the command up to 3 times. These bits set the interval between the retry attempts.

Table 21. SMBUS ERROR RETRY TIMES

0x10 bits <4:3>	SMBus Retry Interval
00	1 ms
01	2 ms
10	4 ms
11	8 ms

If the device fails 3 consecutive read attempts then the PWMx Response bits determine the fan behaviour.

- If bit 5 of 0x11 is 1 then PWM1 will go to 100% duty or Max duty. If bit 5 is 0 then the error is ignored.
- If bit 6 of 0x11 is 1 then PWM2 will go to 100% duty or Max duty. If bit 6 is 0 then the error is ignored.
- If bit 7 of 0x11 is 1 then PWM3 will go to 100% duty or Max duty. If bit 7 is 0 then the error is ignored.

Whether the PWM outputs go to 100% or Max duty is determined by bits <4:2> of register 0x16. See the **THERM ASSERTION** section of this document for more details.

SMBus Master Status Registers

- Bad Block read byte count, 0x81 bit 6
- NACK bits, 0xB6 bits <7:0>
- PEC error bits, 0xB7 bits <7:0>
- SMBus Timeout bits, 0xB8 bits <7:0>
- High/Low Limit exceeded bits, 0xB9 bits <7:0>
- PCH Data Invalid, 0xBA bits <4:0>
- THERM Limit exceeded, 0xBB bits <7:0>

Bad Block Read Count will assert if the byte count returned by the block read command is insufficient to read the required temperatures.

NACK bits will assert if a device does not acknowledge its SMBus address.

PEC error bits will assert if the PEC byte is incorrect.

SMBus Timeout bits will assert if the bus is locked.

High/Low Limit bits will assert if the temperature returned is at or below the programmed low limit value.

PCH Data Invalid bits will assert if the PCH returns reserved temperature codes

THERM Limit bits will assert if the returned temperature is greater than the programmed THERM limit

The status bits ((except THERM status) will hold their value until the registers are read through the SMBus slave port. Status bits (except THERM status) can be masked by setting the corresponding bits in registers 0xBB to 0xBF. THERM Limit status bits will automatically clear when the temperature is below the SMBus THERM limit, unless THERM hysteresis is enabled (setting bit 0 of register 0x11) in which case the temperature must drop below THERM limit – Hysteresis.

Automatic Fan Control

There are two automatic fan control methods that can be selected in the NCT7491. Each PWM channel can be set to use the Tmin/Trange control method or to use an 8 point PWM Look–Up Table. In both cases one or more temperature channels can be assigned to control each PWM output.

Assigning Temperature Zones for Automatic Fan Control

These registers allow the temperature zone to be assigned to a PWM channel by setting the appropriate bit. Any combination of temperature zones can be assigned to control any fan. If more than one zone is selected then a PWM value will be calculated for each temperature and the highest calculated PWM value will be output. If no temperature sources are selected then the associated PWM channel defaults to manual mode.

Registers for assigning zones to PWM1:

- Local/Remote1/Remote2 Control, 0x8A bits <2:0>
- PECI Control, 0x8A, bits <6:3>
- SMBus Thermal Slave Control, 0x8B bits <7:0>
- Push Temperature Control, 0x8C bits <3:0>

Registers for assigning zones to PWM2:

- Local/Remote1/Remote2 Control, 0x8D bits <2:0>
- PECI Control, 0x8D, bits <6:3>
- SMBus Thermal Slave Control, 0x8E bits <7:0>
- Push Temperature Control, 0x8F bits <3:0>

Registers for assigning zones to PWM3:

- Local/Remote1/Remote2 Control, 0x90 bits <2:0>
- PECI Control, 0x90, bits <6:3>
- SMBus Thermal Slave Control, 0x91 bits <7:0>
- Push Temperature Control, 0x92 bits <3:0>

For example if the user wants to control PWM1 from the hottest of the CPU temperature, PCH temperature and the Remote1 sensor then the Control Source registers would be programmed as:

- 0x8A <3> = 1 (PECI0)
- 0x8A <1> = 1 (Remote1)
- 0x8B <0> = 1 (SMBus Device 0, PCH)

Tmin/Trange Automatic Fan Control

The PWM channels can be put into Tmin/Trange in the following way:

- Setting bit <0> of register 0x10 to 0 puts PWM1 in Tmin/Trange mode
- Setting bit <1> of register 0x10 to 0 puts PWM2 in Tmin/Trange mode
- Setting bit <2> of register 0x10 to 0 puts PWM3 in Tmin/Trange mode

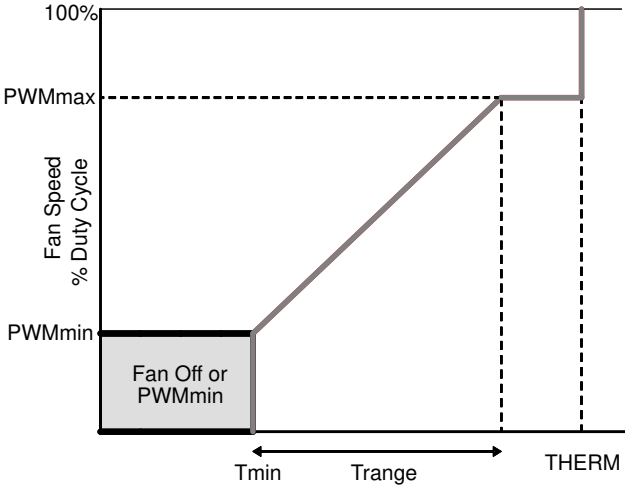


Figure 11. PWM Control Curve in Tmin/Trange Mode

The control loop behaviour in Tmin/Trange mode is determined by the Tmin, PWMmin, Trange and PWMmax values. Tmin sets the temperature at which the fan turns on and PWMmin is the PWM value at Tmin. Trange sets the temperature range over which the PWM output increases from PWMmin to PWMmax. These settings set the slope of the curve. Each temperature source has its own associated Tmin/Trange values. The THERM limit associated with the temperature channel can override the fan control curve if a THERM event occurs.

Minimum PWM values:

- PWM1 Minimum Duty, 0x64
- PWM2 Minimum Duty, 0x65
- PWM3 Minimum Duty, 0x66

These set the lowest PWM at which the fan will run. One Lsb equals 0.39% duty cycle. Minimum PWM values only apply in Tmin/Trange mode.

Maximum PWM values:

- PWM1 Maximum Duty, 0x38
- PWM2 Maximum Duty, 0x39
- PWM3 Maximum Duty, 0x3A

These set the maximum duty at which the fans will run. THERM assertions can be configured to over−ride this to allow the fans to go to 100% duty on a THERM event. See the **THERM ASSERTION** section for more details.

PWM duty cycle registers:

- PWM1 Duty, 0x30
- PWM2 Duty, 0x31
- PWM3 Duty, 0x32

The current duty cycle calculated by the control loop can be read in these registers. If the PWM channel is not associated with a temperature zone then that channel's duty cycle register will become writeable (manual mode).

Tmin/Trange values for all Temperature Sources:

- PECI Tmin. 0x3B
- PECI Trange, 0x3C bits <7:4>
- Remote1 Tmin, 0x67
- Remote1 Trange, 0x5F bits <7:4>
- Local Tmin, 0x68
- Local Trange, 0x60 bits <7:4>
- Remote2 Tmin, 0x69
- Remote2 Trange, 0x61 bits <7:4>
- SMBus slave Tmin, 0xC6
- SMBus slave Trange, 0xC7 bits <3:0>
- Push temperature Tmin, 0xCC
- Push temperature Trange, 0xCD bits <3:0>

PECI Tmin

PECI Tmin values must be programmed in the same format selected for PECI fan control (selected by bit 2 of register 0x73). If relative mode is selected then Tmin is programmed in 2's Complement format. If absolute mode is selected then Tmin is programmed as an unsigned value. If Absolute PECI mode is used then the maximum valid Tmin value is 175°C.

Analog Sensor Tmin

The Tmin value for the analog sensors (Remote1/ Remote2/Local) must be written in the same format as the measurement registers, i.e. if they are in Offset 64 format then the Tmin value for these channels must also be written in Offset 64 format. If they are in 2's Complement format then Tmin must be written in the range 0°C to 127°C.

SMBus Tmin

The SMBus Tmin value should be programmed as an unsigned 8−bit value in the range 0°C to 175°C.

Push Tmin

The Push register Tmin value should be programmed as a value in the range 0°C to 127°C.

Tmin Hysteresis

Hysteresis can be applied to the Tmin temperature to prevent the fan from turning on and off rapidly around Tmin. Each temperature has its own hysteresis value that can be applied. The range of possible values is 0°C to 15°C.

Table 22. HYSTERESIS REGISTERS

Temperature	Hystersis
Remote1	Register 0x6D <7:4>
Local	Register 0x6D <3:0>
Remote2	Register 0x6E <7:4>
PECI	Register 0x6E <3:0>
SMBus slave	Register 0xB5 <4:1>
Push registers	Register 0xEB <3:0>

PWM Behaviour below Tmin:

- PWM1 on below Tmin, 0x62 bit 5
- PWM2 on below Tmin, 0x62 bit 6
- PWM3 on below Tmin, 0x62 bit 7

Setting these bits to 1 will cause the associated PWM output to remain at the minimum PWM value rather than shut off when the control temperature is below its Tmin value minus hysteresis. This setting applies to both Tmin/Trange mode and to Look−Up Table mode.

Trange Values

The Trange values determine the temperature range over which the fan control curve will increase from the PWM minimum value to the PWM maximum value associated with the PWM output.

The 4−bit Trange values that can be assigned for each channel are shown in the following table:

Table 23. TRANGE OPTIONS

Trange Bit Field	Trange Value
0000	2°C
0001	2.5°C
0010	3.33°C
0011	4°C
0100	5°C
0101	6.67°C
0110	8°C
0111	10°C
1000	13.33°C
1001	16°C
1010	20°C
1011	26.67°C
1100	32°C
1101	40°C
1110	53.33°C
1111	80°C

Enabling Enhanced Acoustics on the PWM Outputs:

- PWM1 Max Ramp Rate, 0x62 bits <2:0>
- PWM1 enable acoustics, 0x62 bit 3
- PWM2 Max Ramp Rate, 0x63 bits <6:4>
- PWM2 enable acoustics, 0x63 bit 7
- PWM3 Max Ramp Rate, 0x63 bits <2:0>
- PWM3 enable acoustics, 0x63 bit 3

These settings allow the user to limit the rate at which the PWM output changes whenever the fan control loop calculates a new value. As this prevents instant changes in PWM the acoustic response of the system is improved. These settings apply to both Tmin/Trange mode and to Look−Up Table mode.

Table 24. ENHANCED ACOUSTICS TIMES

Ramp Rate code	Settling time
000	31.75 sec
001	15.7 sec
010	10.5 sec
011	6.33 sec
100	4 sec
101	2.66 sec
110	1.28 sec
111	0.75 sec

Setting the PWM Frequency

Each PWM output can be set to high frequency PWM mode or low frequency PWM mode. In high frequency mode the output will run at 22 kHz. In low frequency mode the frequency can be selected for each PWM output.

Setting bit <3> of register 0x5F to 1 enables high frequency for PWM1

Setting bit <3> of register 0x60 to 1 enables high frequency for PWM2

Setting bit <3> of register 0x61 to 1 enables high frequency for PWM3

If low frequency is enabled (if bit <3> in 0x5F, 0x60 or 0x61 is 0) then the frequency is set as follows:

Table 25. LOW FREQUENCY PWM SELECTION

0x5F, 0x60 or 0x61 bits <2:0>	Frequency
000	11.0 Hz
001	14.7 Hz
010	22.1 Hz
011	29.4 Hz
100	35.3 Hz
101	44.1 Hz
110	58.8 Hz
111	88.2 Hz

Look−Up Table Automatic Fan Control

In this mode the selected PWM output is controlled by an 8−point look−up table, where a temperature and PWM value is programmed for each point. Each channel has its own control table. Any combination of temperature sources can be assigned to control the PWM output. When more than one channel is assigned to control a PWM output in this mode the channel that is the hottest will control the output. The exception to this is if PECI relative temperatures are assigned to contol a channel. Since PECI relative values are always negative they cannot be combined with other channels, since the other channels would always dominate due to the fact that they are positive values. To allow PECI readings to be combined with other readings the user can set bit 2 of register 0x73 (ABS/REL). This will cause the absolute PECI readings to be used for fan control, rather than the relative readings.

- If relative PECI readings are assigned for fan control then the control temperature values for that PWM channel must be programmed in negative 2's complement format (−128°C to 127°C).
- If any temperature source other than relative PECI is assigned for fan control (including absolute PECI readings) then the control temperatures for that PWM channel must be programmed in unsigned format (0°C to 255°C).

- PWM values are programmed in the range 0x00 to 0xFF. The resolution for this register is 1 lsb = 0.392%.

The NCT7491 linearly interpolates between the programmed points. It is not necessary to program all 8 points. If fewer than 8 points are required then the user should program from the lowest to the highest required control temperature and set the unused control temperatures to the maximum value (0x00 if relative PECI is assigned, 0xFF if the PWM channel is controlled by any other temperature source).

- Setting bit <0> of register 0x10 to 1 puts PWM1 in Look−up Table mode
- Setting bit <1> of register 0x10 to 1 puts PWM2 in Look−up Table mode
- Setting bit <2> of register 0x10 to 1 puts PWM3 in Look−up Table mode

The registers used for setting the control temperatures and PWMs for each channel are on page 2 of the register map. To access these registers the user must first set bit 0 of register 0xFF to 1. This will set the register page to page 2. When programming the table is complete the user should clear bit 0 of register 0xFF to zero to return to page 1 of the register map.

Table 26. PWM1 LOOK−UP TABLE VALUES

PWM1 Control Points	Temperature Address	PWM Address
PWM1 Control Point 1	0x00 (0x100)	0x01 (0x101)
PWM1 Control Point 2	0x02 (0x102)	0x03 (0x103)
PWM1 Control Point 3	0x04 (0x104)	0x05 (0x105)
PWM1 Control Point 4	0x06 (0x106)	0x07 (0x107)
PWM1 Control Point 5	0x08 (0x108)	0x09 (0x109)
PWM1 Control Point 6	0x0A (0x10A)	0x0B (0x10B)
PWM1 Control Point 7	0x0C (0x10C)	0x0D (0x10D)
PWM1 Control Point 8	0x0E (0x10E)	0x0F (0x10F)

Table 27. PWM2 LOOK−UP TABLE VALUES

PWM2 Control Points	Temperature Address	PWM Address
PWM2 Control Point 1	0x10 (0x110)	0x11 (0x111)
PWM2 Control Point 2	0x12 (0x112)	0x13 (0x113)
PWM2 Control Point 3	0x14 (0x114)	0x15 (0x115)
PWM2 Control Point 4	0x16 (0x116)	0x17 (0x117)
PWM2 Control Point 5	0x18 (0x118)	0x19 (0x119)
PWM2 Control Point 6	0x1A (0x11A)	0x1B (0x11B)
PWM2 Control Point 7	0x1C (0x11C)	0x1D (0x11D)
PWM2 Control Point 8	0x1E (0x11E)	0x1F (0x11F)

Table 28. PWM3 LOOK−UP TABLE VALUES

PWM3 Control Points	Temperature Address	PWM Address
PWM3 Control Point 1	0x20 (0x120)	0x21 (0x121)
PWM3 Control Point 2	0x22 (0x122)	0x23 (0x123)
PWM3 Control Point 3	0x24 (0x124)	0x25 (0x125)
PWM3 Control Point 4	0x26 (0x126)	0x27 (0x127)
PWM3 Control Point 5	0x28 (0x128)	0x29 (0x129)
PWM3 Control Point 6	0x2A (0x12A)	0x2B (0x12B)
PWM3 Control Point 7	0x2C (0x12C)	0x2D (0x12D)
PWM3 Control Point 8	0x2E (0x12E)	0x2F (0x12F)