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Nuvoton

Hardware Monitoring IC

NCT7802Y

with PECI 3.0 interface

Date: Feb/2012 Revision: 1.2

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1. GENERAL DESCRIPTION

NCT7802Y is a Nuvoton Hardware Monitor IC, which can monitor several critical hardware parameters of the systems, including power supply voltages, fan speeds, and temperatures, to make the system work stably and efficiently, especially for server and workstation applications.

NCT7802Y supports one on-die and up to 5 remote temperature sensors with SMBus interface. There's a 10-bit analog-to-digital converter (ADC) is built inside NCT7802Y, to convert the monitored temperature values. The remote inputs can be connected to CPU/GPU thermal diode or any thermal diode sensors and thermistor, it also can get the Intel® CPU temperature directly via Intel ®PECI3.0 interface.

Additionally, the NCT7802Y can monitor up to 5 analog voltage inputs, 3 fan tachometer inputs and supports up to 6 multifunctional GPIO. The SMART FAN™ IV mode provides 4 sets of temperature setting points, and they can also control the duty cycle of fan outputs. It provides an easy method to implement quiet and cooling solution with maximum safety and flexibility.

Meanwhile, there're 5 pure hardware event pins for independent alarm signals, and the all threshold values could be set for system protection without any timing delay.

2. FEATURES

2.1 Temperature Measurement

- Measure the temperature with high accuracy
- One local on-die thermal sensor
- Two pairs thermal diode (current mode) temperature channels
- Three thermistor mode temperature channels
- Support Intel® PECI 3.0 interfaces for reading Intel®CPU temperature

2.2 Voltage Measurement

- Up to five voltage inputs, three multi-functions with thermal diode pair

2.3 Fan Control

- Three fan control outputs multi-function (PWM mode supported)
- Two fan control outputs support DC mode
- Three fan tachometer input multi-function
- SMART FAN™ IV mode or Manual mode to control the fan speed

2.4 Event Notification

- Support 5 alarm outputs: ALERT#, T_CRIT#, RESET#, SMI#, BEEP signals to activate system protection.
- ALERT# output supports SMBus™ 2.0 ARA function

2.5 General

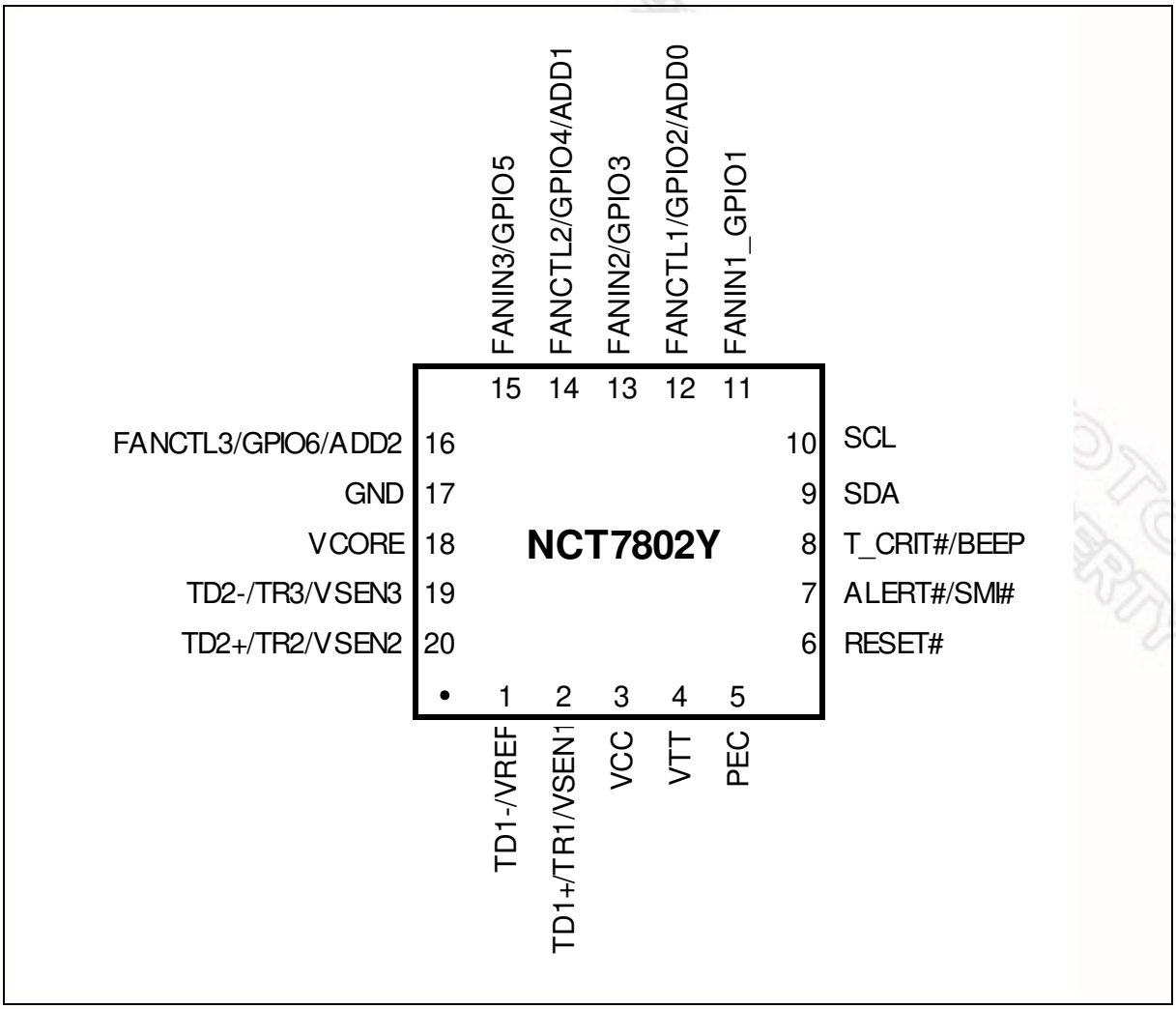
- Provide up to 6 GPIO pins (multi-function with fan control).
- I^2C® Compatible System Management bus (SMBus)
- Support 8 SMBus address selection
- Programming from EEPROM support
- 3.3V±5% V_{CC} operation
- 20-pin QFN package (Halogen free)

3. KEY SPECIFICATIONS

● Voltage monitoring accuracy	
VSEN input	±10mV
VCC input	±80mV
● Temperature Sensor Accuracy	
Remote Diode Sensor Accuracy (25~85°C)	± 1°C typ.
On-chip Temperature Sensor Accuracy (25~70°C)	± 2°C typ.
Remote Temperature Sensor Resolution	0.125°C
On-chip Temperature Sensor Resolution	1 °C
● Supply Voltage	3.3V ± 5%
● Operating Supply Current	
VCC	5mA typ.
VTT	< 1mA
● Operating Temperature Range	-40°C ~ 85°C *1

*1 Guaranteed by design from -40~85 degree C, 100% tested at 85 degree C.

4. PIN CONFIGURATION



5. PIN DESCRIPTION

5.1 PIN TYPE DISCRIPTION

PIN TYPE	PIN ATTRIBUTE
OD_{12}	Open-drain output pin with 12 mA sink capability
IN_{ts}	TTL level input pin and schmitt trigger, with 5V tolerance support
V1	Type of PECI
AIN	Input pin (Analog)
OUT_{12}	Output pin with 12 mA sink/source capability
AOUT	Output pin (Analog)
P	Power or Ground Pin

5.2 PIN DISCRIPTION

PIN NO.	PIN NAME	I/O	FUNCTION
1	**TD1-**	AIN	Connect to Thermal Diode 1 Cathode
	VREF	AOUT	VREF output for Thermistor function
2	**TD1+**	AIN	Connect to Thermal Diode 1 Anode
	TR1		Thermistor 1 sensing input
	VSEN1		Voltage sensing input. Detection range is 0~2.048V
3	**VCC**	P	Power supply, Voltage input 3.3V±5% It is also a voltage sensing input
4	**VTT**	P	Intel® CPU Vtt power
5	**PECI**	V1	Intel® CPU PECI interface
6	**RESET#**	OD_{12}	Reset alarm output, for detect VCC power fault
7	**ALERT#**	OD_{12}	Alarm output, for interrupt control (default)
	SMI#		Alarm output, for interrupt control
8	**T_CRIT#**	OD_{12}	T_CRIT alarm output, for interrupt or shutdown control. (default)
	BEEP		BEEP output when abnormal event occurs (Frequency:300Hz/600Hz, Tone=500mS)
9	**SDA**	IN_{ts}/OD_{12}	SMBus bi-directional data
10	**SCL**	IN_{ts}	SMBus Clock
11	**FANIN1**	IN_{ts}	Fan tachometer input (default)
	GPIO1	IN_{ts}/OD_{12} /OUT_{12}	General purpose I/O function
12	**FANCTL1**	OUT_{12}/OD_{12} /AOUT	Fan speed control PWM/DC output It can be configured to PWM/DC mode by registers. Default is PWM output As DC output, 256 steps output voltage scaled to 0~VCC
	GPIO2	IN_{ts}/OD_{12} /OUT_{12}	General purpose I/O function
13	**FANIN2**	IN_{ts}	Fan tachometer input (default)
	GPIO3	IN_{ts}/OD_{12} /OUT_{12}	General purpose I/O function

PIN NO.	PIN NAME	I/O	FUNCTION
14	**FANCTL2**	OUT_{12}/OD_{12} /AOUT	Fan speed control PWM/DC output It can be configured to PWM/DC mode by registers. Default is PWM output As DC output, 256 steps output voltage scaled to 0~VCC
	GPIO4	IN_{ts} /OD_{12} /OUT_{12}	General purpose I/O function
15	**FANIN3**	IN_{ts}	Fan tachometer input (default)
	GPIO5	IN_{ts} /OD_{12} /OUT_{12}	General purpose I/O function
16	**FANCTL3**	OUT_{12}/OD_{12}	Fan speed control PWM output
	GPIO6	IN_{ts} /OD_{12} /OUT_{12}	General purpose I/O function
17	**GND**	P	Power supply ground
18	**VCORE**	AIN	Voltage sensing input. Detection range is 0~2.048V
19	**TD2-**	AIN	Connect to Thermal Diode 2 Cathode
	TR3		Thermistor 3 sensing input
	VSEN3		Voltage sensing input. Detection range is 0~2.048V
20	**TD2+**	AIN	Connect to Thermal Diode 2 Anode
	TR2		Thermistor 2 sensing input
	VSEN2		Voltage sensing input. Detection range is 0~2.048V

6. DESCRIPTION

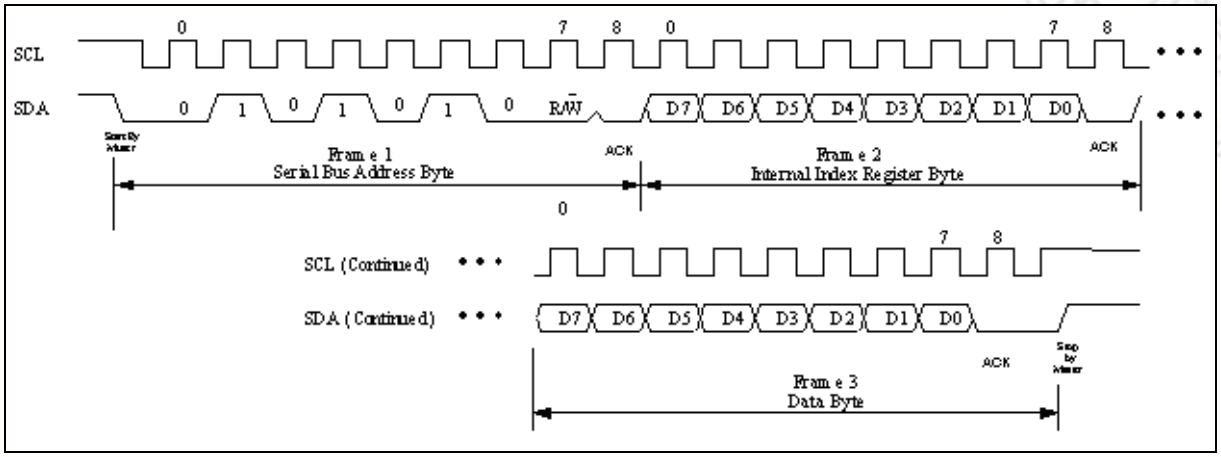
6.1 GENERAL DESCRIPTION

The NCT7802Y is a Nuvoton Hardware Monitor IC, contains one on-die and up to 5 remote temperature sensors, with SMBus and Intel PECI3.0 interface. There're also five voltage monitoring channels, 3 fan control groups, and GPIO functions with SMBus interface. NCT7802Y supports up to 8 sets SMBus address selection, it also provides ALERT#/SMI#/T_CRIT#/BEEP and RESET# alarm signals for event notification.

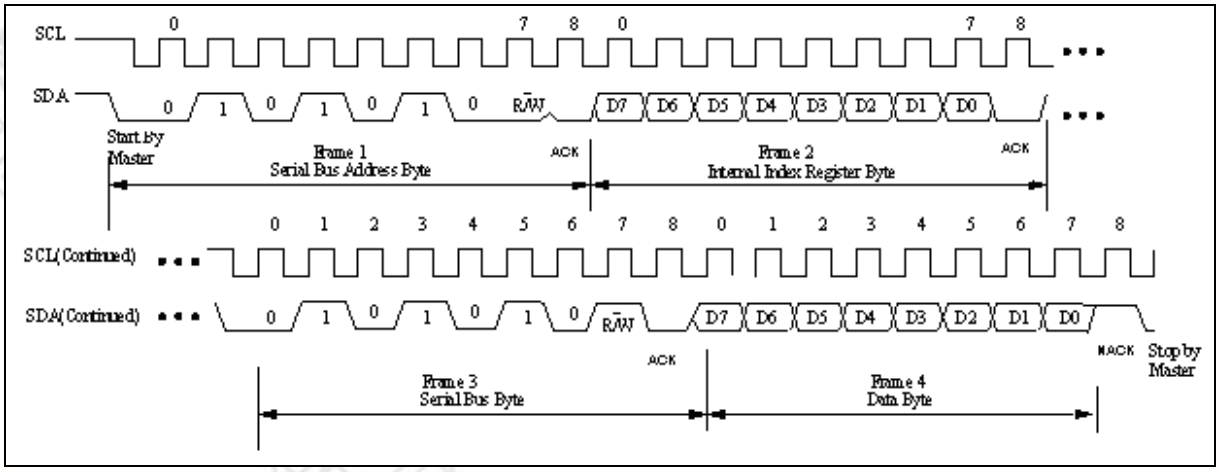
6.2 ACCESS INTERFACE

NCT7802Y provides SMBus to access the internal register, supports SMBus byte write and byte read protocols.

6.2.1 Data write to the internal register



6.2.2 Data read from the internal register



6.3 ADDRESS SETTING

NCT7802Y has three address pins and multi-function with FANCTRL1~3, the SMBus address will be strapped when VCC ready 100mS, during the 100mS, the level of strapping pins must be fixed. The address will be retained as long as the VCC of NCT7802Y is maintained. The pull-up power plane must be the same as the VCC power of NCT7802Y.

ADD0(FANCTRL1)	ADD1(FANCTRL2)	ADD2(FANCTRL3)	ADDRESS
0	0	0	0101 000X
0	0	1	0101 001X
0	1	0	0101 010X
0	1	1	0101 011X
1	0	0	0101 100X
1	0	1	0101 101X
1	1	0	0101 110X*1
1	1	1	0101 111X*2

X=Read/Write# Bit

*1 When set the NCT7802Y to address 5Ch, EEPROM loading function will be enabled, EEPROM address has to be ACh, refer to section 6.15.

*2 When set the NCT7802Y to address 5Eh, EEPROM loading function will be enabled, EEPROM address has to be AEh, refer to section 6.15.

6.4 TEMPERATURE MONITOR DATA FORMAT

6.4.1 The local temperature (on-die) data with 8-bit 2`s complement format

TEMPERATURE	8-BIT DIGITAL OUTPUT
+127°C	0111,1111
+25°C	0001,1001
+2°C	0000,0010
+1°C	0000,0001
+0°C	0000,0000
- 1°C	1111,1111
- 2°C	1111,1110
- 25°C	1110,0111
- 128°C	1000,0000

6.4.2 The remote temperature data with 11-bit 2's complement format

TEMPERATURE	8-BIT DIGITAL OUTPUT HIGH BYTE	3-BIT DIGITAL OUTPUT LOW BYTE
+127.875°C	0111,1111	111X,XXXX
+25.750°C	0001,1001	110X,XXXX
+2.250°C	0000,0010	010X,XXXX
+1.125°C	0000,0001	001X,XXXX
+0.000°C	0000,0000	000X,XXXX
- 1.125°C	1111,1110	111X,XXXX
- 2.250°C	1111,1101	110X,XXXX
- 25.750°C	1110,0110	010X,XXXX
- 127.875°C	1000,0000	001X,XXXX

6.5 VOLTAGE SENSE DATA FORMAT

MNTVSEN Low Byte together with MNTVSEN High Byte forms the 10-bit count value. If MNTVSEN High Byte readout is read successively, the NCT7802Y will latch the MNTVSEN Low Byte for next read. Then voltage readout high byte and low byte are combined to *10-bitVoltageValue*.

For VSEN1~3 and Vcore monitoring, real voltage calculations should follow the formula:

$$Voltage(V) = 10bitCountValue \times 0.002$$

VOLTAGE	MNTVSEN HIGH BYTE	MNTVSEN LOW BYTE
+2 V	1111,1010	00XX,XXXX
+1 V	0111,1101	00XX,XXXX
+0.036 V	0000,0100	10XX,XXXX
+0 V	0000,0000	00XX,XXXX

For VCC monitoring, real voltage calculations should follow the formula:

$$Voltage(V) = 10bitCountValue \times 0.004$$

6.6 FAN_IN Count Calculation

The FAN_IN tachometer high byte and low byte are combined to 13-bitCountValue. Real RPM (Rotate per Minute) calculation should follow the formula:

$$FanSpeed(RPM) = \frac{1.35 \times 10^6}{(13 - bitCountValue) \times (FanPoles/4)}$$

In this formula, FanPoles stands for the number of NS pole pairs inside the fan. Normally an N-S-N-S Fan (FanPoles=4) generates 2 pulses after completing one rotation.

6.7 FAN_OUT Duty Cycle / DC Level Calculation

The NCT7802Y provides 3 set of PWM for fan speed control. The duty cycle of PWM can be programmed by an 8-bit register. The expression of duty cycle can be represented as follow formula:

$$\text{Duty}-\text{cycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The NCT7802Y provides 2 set of DC output for fan speed control on FANCTL1 and FANCTL2. The DC output can be programmed by an 8-bit register. The expression of DC level can be represented as follow formula:

$$\text{Output Voltage (V)} = VCC \times \frac{\text{Programmed 8 - bit Register Value}}{255}$$

6.8 SMART FAN™ IV Control Parameters

In SMART FAN™ IV Mode, there are some Fan control parameters as below descriptions:

6.8.1 Step Up Time / Step Down Time

SMART FAN™ IV is designed for the smooth operation of the fan. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed. On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat. This register should never be set to 0, otherwise, the fan duty will be abnormal.

6.8.2 Fan Output Start-up Value

From still to rotate, the fan usually needs a higher fan output value to generate enough torque to conquer the restriction force. Thus the Fan Output Start-up Value is used to turn on the fan with the specified output value.

6.8.3 Fan Output Nonstop

It takes some time to bring a fan from still to working state. Therefore, Nonstop value are designed with first FANCTL step output to keep the fan working when the system does not require the fan to help reduce heat but still want to keep the fast response time to speed up the fan.

6.8.4 Fan Output Stop Time

A time interval is specified to turn off the fan if SMART FAN™ IV continuously requests to slow down the fan which has already reached the Stop time.

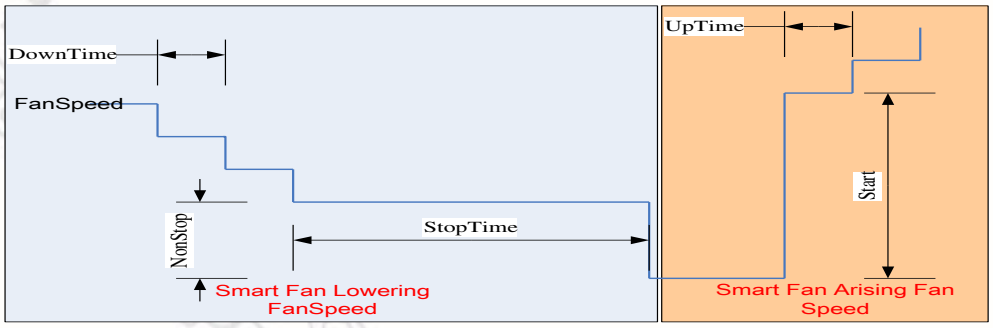


Figure 6-1 SMART FAN™ IV Control Parameters

6.9 SMART FAN™ IV

SMART FAN™ IV supports Fan Duty Outputs Mode and Close Loop Fan Control (RPM) Mode to control the fan speed.

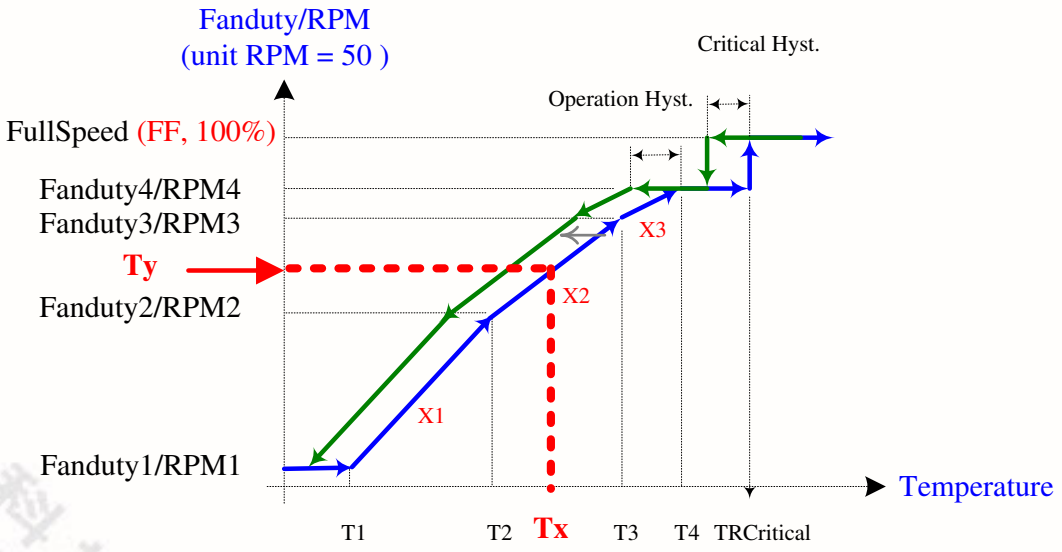
There're 3 slopes can be obtained by setting FanDuty/RPM1~FanDuty/RPM4 and T1~T4 through the registers. When the temperature rises, FAN Output will calculate the target FanDuty/RPM based on the current slope. For example, assuming Tx is the current temperature and FanDuty/RPM is the target, then the slope:

$$X2 = \frac{(FanDuty3/RPM3) - (FanDuty2/RPM2)}{(T3 - T2)}$$

Fan Output:

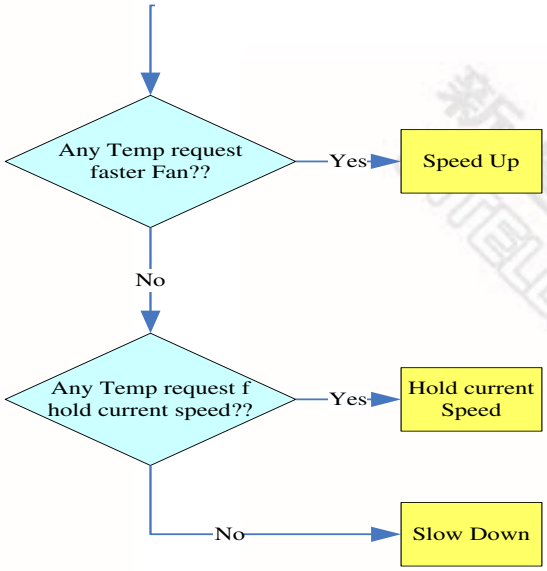
$$Target\ FanDuty\ or\ RPM = (FanDuty2\ or\ RPM2) + (Tx - T2) \cdot X2$$

Figure 6-2 SMART FAN™ IV Mechanism



In addition, SMART FAN™ IV can also set up Critical Temperature and Hysteresis. If the current temperature exceeds Critical Temperature, external fan will be forced by maximum FanDuty to meet the largest target FanDuty or RPM, Which is 0xFF. The target FanDuty & RPM value will be determined in accordance to the slope only when the temperature falls below (TCritical – Critical Hyst).

NCT7802Y provide 3 temperature sources selection to map the fan, the algorithm will make a decision to control the fan as below figure:



6.10 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the NCT7802Y supports. The NCT7802Y contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 6-3 shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

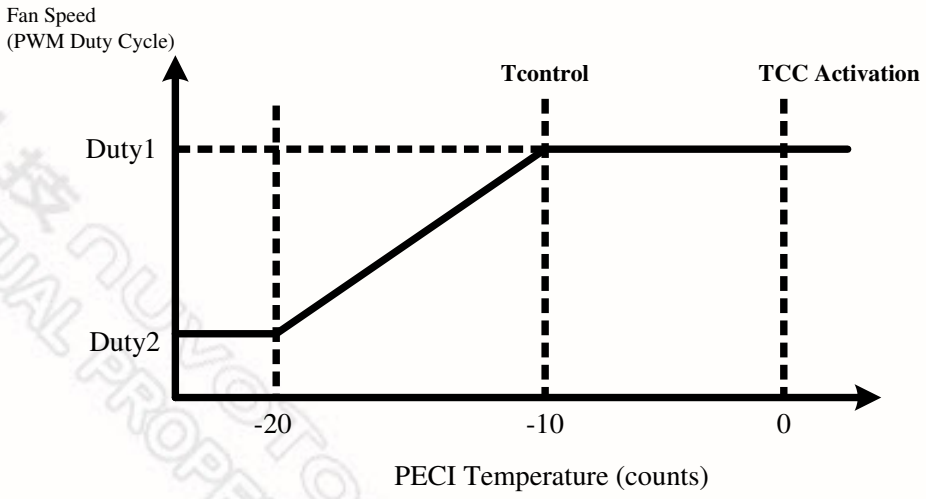


Figure 6-3 PECI Temperature

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At Tcontrol PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of Tcontrol can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The Tcontrol MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, Tcontrol is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

NCT7802Y's fan control circuit can only accept positive real-time temperature inputs and limits setting (when SMART FAN™ IV mode). The device provides offset registers to 'shift' the negative PECI readings to positive values otherwise the fan control circuit will not function properly. The offset registers are the Tbase registers located at Bank1, Index09h and Index0Ah. All default values of these Tbase registers are 8'h00.These registers should be programmed with (positive) values so that the resultant value (Tbase + PECI) is always positive. The unit of the Tbase register contents is "count" to match that of PECI values. The resultant value (Tbase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

Figure 6-4 Temperature and Fan Speed Relation after Tbase Offsets shows the temperature/fan speed relationship after Tbase offsets are applied (based on Figure 6-3 PECI Temperature). This view is from the perspective of the NCT7802Y fan control circuit.

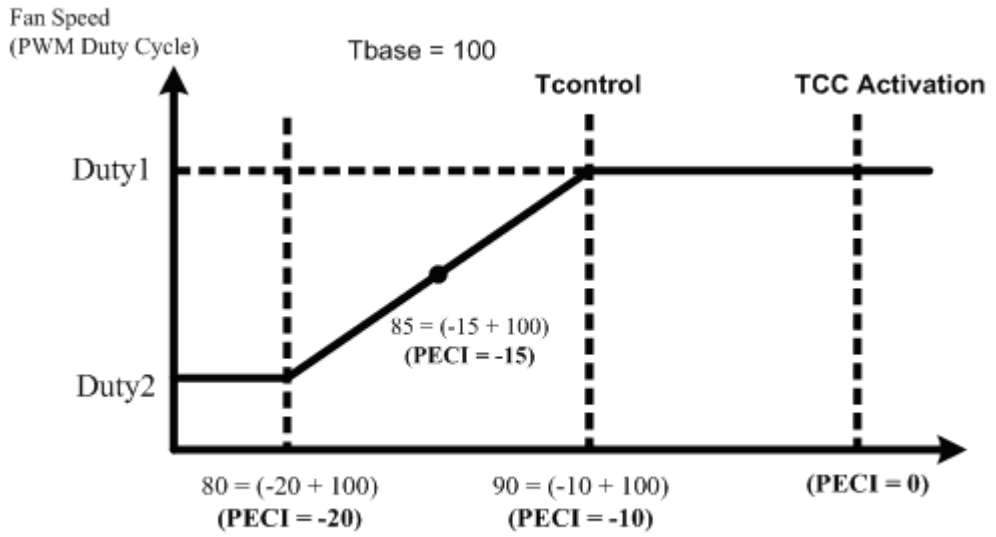


Figure 6-4 Temperature and Fan Speed Relation after Tbase Offsets

Assuming Tbase is set to 100 and the PECI temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using SMART FAN™ IV control function of NCT7802Y, BIOS/software must include Tbase in determining the thresholds (limits). In this example, assuming Tcontrol is -10 and Tbase is set to 100,

the threshold temperature value corresponding to the “100% fan duty cycle” event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

Tcontrol is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of Tcontrol to match the specific application.

6.11 ALERT# Output

The NCT7802Y ALERT# pin is an active-low open-drain output pin which is triggered when temperature measured and fan exceeds the limitation defined in the limit registers.

6.11.1 ALERT# Output Mechanism

Figure 6-5 shows the mechanism of the ALERT# output. In this mode, the NCT7802Y will set the ALERT mask bit of Configuration Register during a read of the Status Register if any flag in Status Register, except the ADC_Busy flag and Remote Diode Open flag, is set. This prevents further ALERT# triggering until the master has reset the ALERT mask bit (write 0 to Alert_MSK in Bank0 CR[21h] Bit7), at the end of the interrupt service routine. The Status Register flags are cleared only upon a read Status Register command from the master and will be re-alerted at the end of the next temperature conversion if the measured temperature still falls outside of the allowed range.

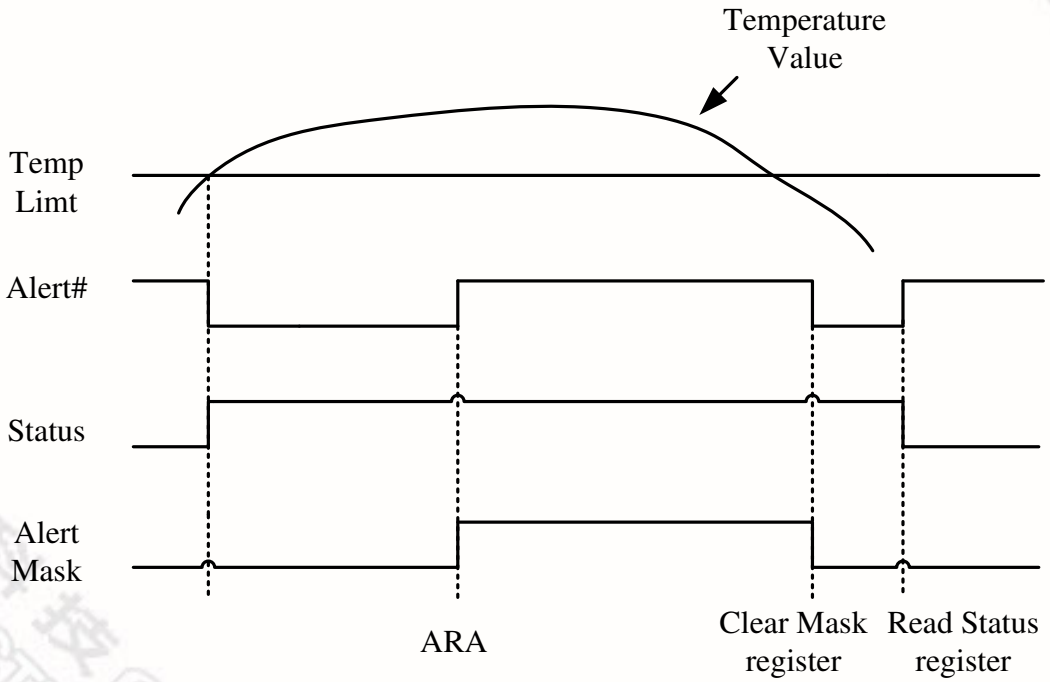


Figure 6-5 ALERT# Output Mechanism

6.11.2 ALERT# Response Address

Figure 6-6 shows the mechanism of the SMBus ALERT# Response Address (ARA) support on ALERT# output. In this mode, the ALERT# output of the NCT7802Y is connected to the SMBus alert line which has more than one device connected to it. Through such and implementation, SMBus alert mode can assist the master in resolving which salve generates an interrupt. When the measured temperature falls outside of the allowed range, the ALERT# pin will be pulled low and the corresponding alert flags in Status Register will be set to 1. The ALERT# mask bit will just be set if there is a read command for Status Register or when ARA occurs from master (Alert Response Address is 0001100x). Meanwhile, the NCT7802Y will generate and return its own address to the master. If the temperature never falls outside of the allowed range, the latched ALERT# pin can release by the reset ALERT mask bit and the latched corresponding alert flags in Status Register can release by reading command for Status Register.

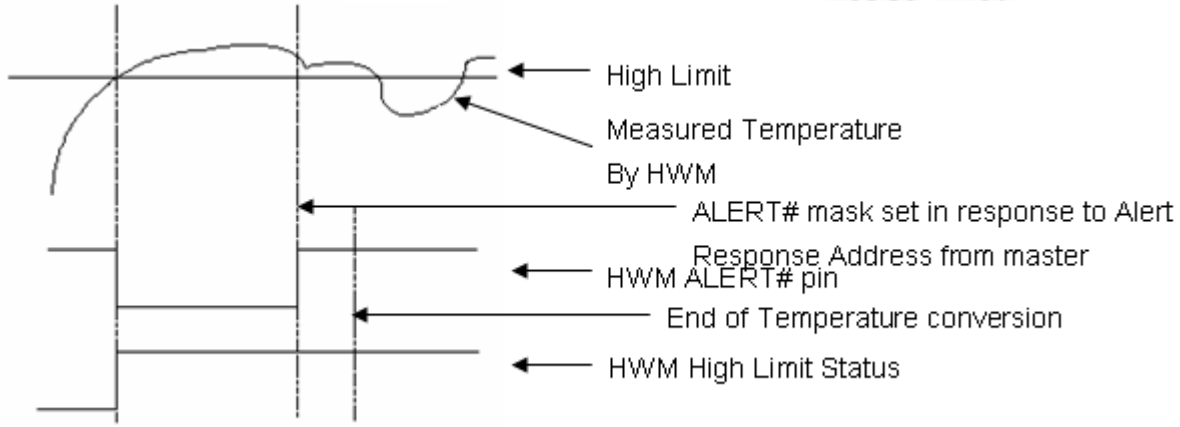


Figure 6-6 SMBus ARA Mechanism

6.12 T_CRIT# Output

T_CRIT# output pulls low when the measured temperature exceeds the critical temperature threshold point. Once the T_CRIT# output pulls low, it will not be set high until the measured temperature is lower than critical temperature threshold point.

6.13 SMI# Output

6.13.1 Temperature

SMI# for temperature monitoring provides 3 modes: Comparator Interrupt Mode, Two-Times Interrupt Mode, and the One-Time Interrupt Mode.

6.13.1.1. Comparator Interrupt Mode

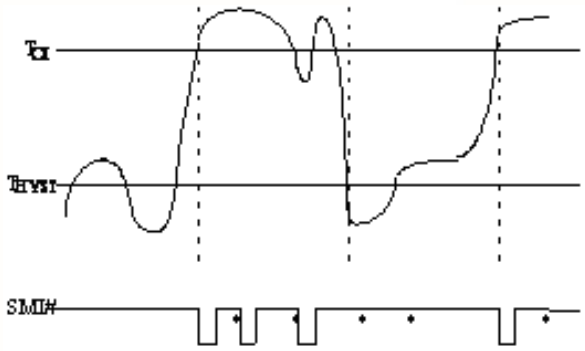
Temperature exceeding T_O causes an interrupt and this interrupt will be reset when reading all of the Interrupt Status Registers. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}.

6.13.1.2. Two-Times Interrupt Mode

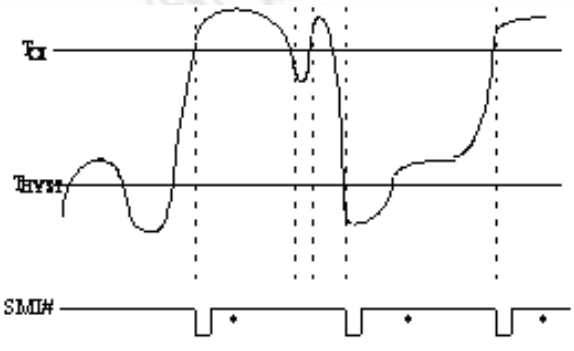
Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur.

6.13.1.3. One-Time Interrupt Mode

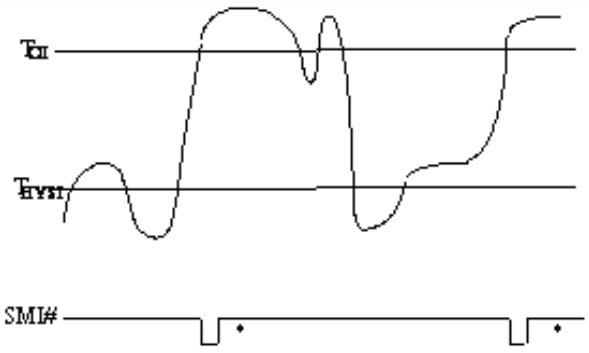
Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeding T_O.



Comparator Interrupt Mode



Two-Times Interrupt Mode



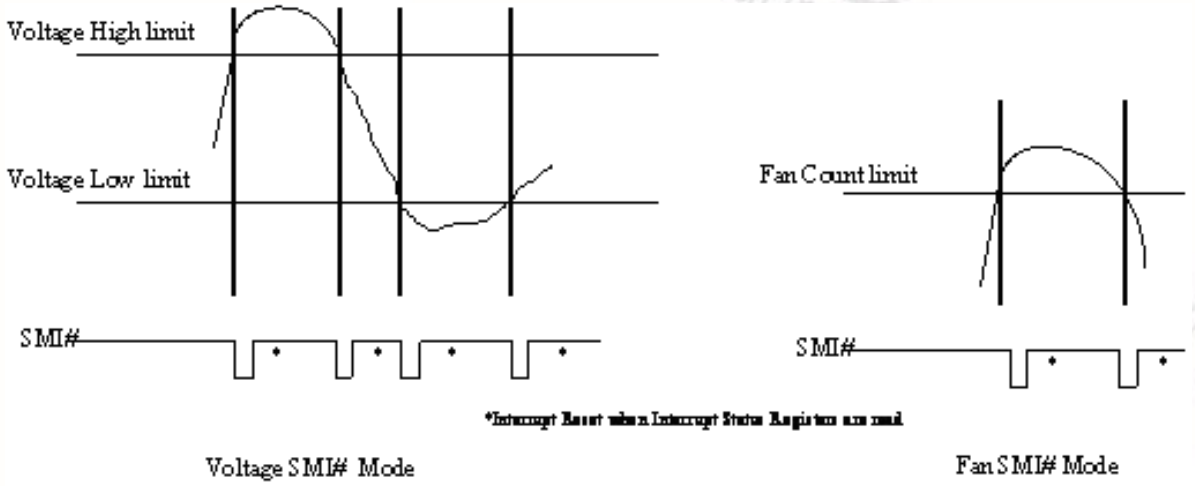
One-Time Interrupt Mode

6.13.2 Voltage

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeds high limit or going below low limit, it will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register.

6.13.3 Fan

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeds the limit, or exceeding and then going below the limit, it will cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are read.

Voltage SMI# Mode

Fan SMI# Mode

6.14 RESET# Output

The NCT7802Y provides a reset controller for the system's 3.3V supply rail. The RESET# pin will pull low pulse when the measured VCC below the threshold voltage. The RESET# pin set to '1' after the 3.3V VCC supply rises above its threshold voltage.

6.15 Self-Programming from EEPROM

The NCT7802Y supports self-programming through an external I2C EEPROM during NCT7802Y power-on. The EEPROM is recommended to be 24C02 type. During 200ms period after power on, NCT7802Y will detect if the external EEPROM exists by issuing the SMBus Byte Read command with 50KHz SMBus clock frequency. If a NACK of SMBus protocol is detected, NCT7802Y will stop self-programming, otherwise, NCT7802Y will keep loading data from external EEPROM sequentially to Bank0 Index 00h~E2h registers. Therefore, other SMBus master has to avoid from accessing NCT7802Y during the 200ms after power-on.

Please also refer to NCT7802Y APN for self-programming implementation.

7. REGISTER DESCRIPTION

7.1 BANK0 REGISTER MAP

Idx	Register Name	Att	Df	7	6	5	4	3	2	1	0
0	Bank Select	R/W	00	RSV							BKSEL
1	Read RTD1 High Byte	R	00	MNTRTD1[10:3]							
2	Read RTD2 High Byte	R	00	MNTRTD2[10:3]							
3	Read RTD3 High Byte	R	00	MNTRTD3[10:3]							
4	Read LTD High Byte	R	00	MNTLTD[7:0]							
5	Read Temp Low Byte	R	00	MNTTD_Lsb[2:0]			RSV				
6	Read PECI 0 Temp High Byte	R	00	MNTPECI0[9:2]							
7	Read PECI1 Temp High Byte	R	00	MNTPECI1[9:2]							
8	Read PECI Low Byte	R	00	MNTPECI_Lsb[1:0]		RSV					
9	Read VCC	R	00	MNTVCC[9:2]							
A	Read VCore	R	00	MNTVCore[9:2]							
C	Read VSEN1	R	00	MNTVSEN1[9:2]							
D	Read VSEN2	R	00	MNTVSEN2[9:2]							
E	Read VSEN3	R	00	MNTVSEN3[9:2]							
F	Read Volt Low Byte	R	00	MNTV_Lsb[1:0]		RSV					
10	Read Fan Count 1High Byte	R	FF	MNTFAN1[12:5]							
11	Read Fan Count 2High Byte	R	FF	MNTFAN2[12:5]							
12	Read Fan Count 3High Byte	R	FF	MNTFAN3[12:5]							
13	Read Fan Count 1Low Byte	R	F8	MNTFAN_Lsb[4:0]					RSV		
15	MNTIMON_Percent	R	00	MNTIMON_Percent							
17	Diode Fault Alert Status	R	00	RSV					STS_DF3	STS_DF2	STS_DF1
18	Low Alert Status	R	00	RSV		STS_PECI1	STS_PECI0	STS_AL4	STS_AL3	STS_AL2	STS_AL1
19	High Alert Status	R	00	RSV		STS_PECI1	STS_PECI0	STS_AH4	STS_AH3	STS_AH2	STS_AH1
1A	Fan Alert Status	R	00	RSV	FAN_TAR3	FAN_TAR2	FAN_TAR1	RSV	FAN_FC3	FAN_FC2	FAN_FC1
1B	TCRIT Alert Status	R	00	RSV		STS_PECI1	STS_PECI0	STS_TC4	STS_TC3	STS_TC2	STS_TC1
1C	GPIO Alert Status	R	00	RSV			STS_GPIO6	STS_GPIO5	STS_GPIO4	STS_GPIO3	STS_GPIO2	STS_GPIO1
1D	SMI Temp Status	R	00	RSV		STS_PECI1	STS_PECI0	STS_LTD	STS_RTD3	STS_RTD2	STS_RTD1
1E	SMI Voltage status	R	00	RSV				STS_VCC	STS_VSEN3	STS_VSEN2	STS_VSEN1
1F	SMI FAN status	R	00	RSV	FAN_TAR3	FAN_TAR2	FAN_TAR1	RSV	FAN_FC3	FAN_FC2	FAN_FC1
20	TCRIT Real Time Status	R	00	RSV				LTD_Texc	RTD3_Texc	RTD2_Texc	RTD1_Texc

Idx	Register Name	Att	Df	7	6	5	4	3	2	1	0
21	START	R/W	01	Msk_Alert	RSV						START
22	Mode Selection	R/W	7F	RSV	EnLTD	RTD3_MD		RTD2_MD		RTD1_MD	
23	PECI Enable	R/W	00	RSV						EnPECI1	EnPECI0
24	Fan Enable	R/W	07	RSV					EnFan3	EnFan2	EnFan1
25	Voltage monitor Enable	R/W	03	RSV						EnVCore	EnVCC
26	Conversion Rate	R/W	03	RSV						ConvRate[1:0]	
27	Fault Queue	R/W	03	RSV						FaultQueue[1:0]	
28	Alert High link to T_CRIT#	R/W	00	RSV					SYS3	SYS2	SYS1
29	Reset time setting	R/W	04	RSV					SetResetTime		
2A	Reset Limit Low Byte	R/W	EE	ResetLimit[7:0]							
2B	Reset Limit High Byte	R/W	80	ResetLimit[9:8]		RSV					
2F	SMI Control	R/W	00	ALERT_SMI_Sel	TCRIT_BEEP_Sel	SMI_MOD	SMI_POL	OVT_MOD	En_SMI	TempSmiMode	
30	RTD1 Temp High Limit	R/W	55	RTD1_HL							
31	RTD1 Temp Low Limit	R/W	00	RTD1_LL							
32	RTD2 Temp High Limit	R/W	55	RTD2_HL							
33	RTD2 Temp Low Limit	R/W	00	RTD2_LL							
34	RTD3 Temp High Limit	R/W	55	RTD3_HL							
35	RTD3 Temp Low Limit	R/W	00	RTD3_LL							
36	LTD Temp High Limit	R/W	55	LTD_HL							
37	LTD Temp Low Limit	R/W	00	LTD_LL							
38	DTS Temp High Limit	R/W	55	DTS_HL							
39	DTS Temp Low Limit	R/W	00	DTS_LL							
3A	RTD1 TCRIT Threshold	R/W	64	TCRIT_RTD1							
3B	RTD2 TCRIT Threshold	R/W	64	TCRIT_RTD2							
3C	RTD3 TCRIT Threshold	R/W	64	TCRIT_RTD3							
3D	LTD TCRIT Threshold	R/W	64	TCRIT_LTD							
3E	DTS TCRIT Threshold	R/W	64	TCRIT_DTS							
3F	Vsen1 High Limit Low Byte	R/W	FF	VSEN1_HL[7:0]							
40	Vsen1 Low Limit low Byte	R/W	00	VSEN1_LL[7:0]							
41	Vsen2 High Limit low Byte	R/W	FF	VSEN2_HL[7:0]							
42	Vsen2 Low Limit low sByte	R/W	00	VSEN2_LL[7:0]							
43	Vsen3 High Limit low Byte	R/W	FF	VSEN3_HL[7:0]							
44	Vsen3 Low Limit low Byte	R/W	00	VSEN3_LL[7:0]							
45	VCC High limit low byte	R/W	FF	VCC_HL[7:0]							
46	VCC Low limit low byte	R/W	00	VCC_LL[7:0]							
47	VSEN high Byte 1	R/W	CC	VSEN1_HL[9:8]		VSEN1_LL[9:8]		VSEN2_HL[9:8]		VSEN2_LL[9:8]	