Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NCT7904D
H/W Monitor

Date: 2014/2/10 Revision: 1.44

Table of Content-

1. GENERAL DESCRIPTION

NCT7904D is an evolving version of the Nuvoton popular Hardware Monitor IC family. NCT7904D provides several innovative features, Intel PECI1.1/2.0/3.0 interface, and PROCESSOR HOT feature. Conventionally, NCT7904D can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system, such as server, workstation…etc, to work stably and efficiently.

A 10-bit analog-to-digital converter (ADC) is built inside NCT7904D. NCT7904D can simultaneously monitor 20 analog voltage inputs (including power 3VDD / 3VSB / VBAT / VTT monitoring), 12 fan tachometer inputs, 4 fan output control, and 4 remote temperature sensor inputs, 2 of which support current mode (dual current source) temperature measurement method, it also supports caseopen detection, Watch Dog Timer function, and GPIO pins. The sense of remote temperature can be performed by thermistors, or directly from thermal diode. NCT7904D provides PWM (pulse width modulation) for each fan control output pin, and DC fan output mode is supported on PWM4 pin. Meanwhile, the NCT7904D provides SMART FAN™ control, the **“** SMART FAN™ IV **”** mode equips with 4 sets of temperatures setting point each could control fan’s duty cycle, to make the fans could be operated at the lowest possible speed and the acoustic could be balanced. As for warning mechanism, NCT7904D provides SMI#, TEMP_ALM#, VOLT_ALM#, and FAN_ALM# to protect the system. NCT7904D has 1 specific pin to provide address selection so that 2 NCT7904D could be wired through SMBus interface at the same time.

All of the monitored parameters of the system could be read from time to time through the BIOS or any management application software. Nuvoton supports the software – “Health Manager” to provide an easy way to monitor and show the hardware parameters, such as temperature, voltage and fan speed inputs, furthermore, it provides a convenient method to do the fan control. It can also show the alarm message when the monitored hardware parameter exceeds the limit, and recodes the history events.

2. FEATURES

2.1 Equipped Specific Interfaces

- I^2C / SMBus2.0 Serial Bus Master (max. 400KHz Clock)
- I^2C / SMBus2.0 Serial Bus Slave (max. 400KHz Clock)
- Intel® PECI (PLATFORM ENVIRONMENT CONTROL INTERFACE) 1.0 / 2.0 / 3.0
- AMD SB-TSI

2.2 Monitoring Items

VOLTAGE

Up to 20 voltage sensing inputs

- 16 general voltage inputs
- 4 power pins. (3VDD, 3VSB, VBAT and VTT)
- 4 multi-functions with thermistor temperature inputs (on VSEN2, VSEN4, VSEN6, VSEN8)
- 2 multi-functions with thermal diode pair (on VSEN2, VSEN3, VSEN4 and VSEN5)

TEMPERATURE

Up to 4 methodologies for capturing temperature information

- ADC

  => 2-pair thermal diode channel (current mode) / 4-channel thermistor mode temperature

  => 1 channel on-chip temperature sensor
- Intel® PECI interface

  => Automatically retrieving CPU temperature
- AMD SB-TSI interface

  => Automatically retrieving CPU temperature
- SMBus Master

  => Reading MCH, PCH, CPU and DIMMs temperature through PCH

  => Reading specific external at most 4 thermal sensors.

FAN SPEED

Up to 12 fan tachometer inputs

2.3 PECI (Platform Environment Control Interface)

- Support PECI 1.0 / 2.0 / 3.0 full commands
- Automatically retrieve CPU temperature and power status
- Automatically retrieve DRAM thermal data which is provided by CPU0 and CPU1 only (Address: 30h and 31h)
- Support 4 CPU sockets (eq. 4 PECI address) and 2 domains per CPU address

2.4 SMART FAN™ PWM Output Control

- Up to 4 PWM Outputs
- Support 2 modes of fan speed control: SMART FAN™ IV mode and Closed Loop Fan Control Mode (RPM mode)
- Provide up to 10 SMART FAN™ tables to characterize 10 relationships between temperature and output fan speed
- The temperature source of table could come from any of temperature information captured from ADC, PECI, TSI and SMBus Master
- Multiple temperature sources could affect multiple fan control outputs
- Up to 4 virtual temperature sources feed by host as the parts of fan temperature sources
- Up to 4 external temperature sources read from SMBus master I/F which can be the part of fan temperature sources
- Support Fan Control for Intel Sandy Bridge-EP/EX DTS specification
- Support DTS (Sensor) Based Thermal Ver. 1.0/2.0 Spec to optimize fan speed control and acoustics at processor run time

2.5 Alarm Output

- Issue SMI# signal to activate system protection
- Issue voltage, temperature and fan alarm signals to activate system protection

2.6 Self-initialization

- Self-configuration by reading external EEPROM with SMBus interface

2.7 SMBus Master

- Support SMBus master function to read EEPROM configuration data and other SMBus devices
- Support SMBus master manual byte read and byte write
- Support accessing PCH Thermal Reporting
- Support accessing external thermal sensors

2.8 General

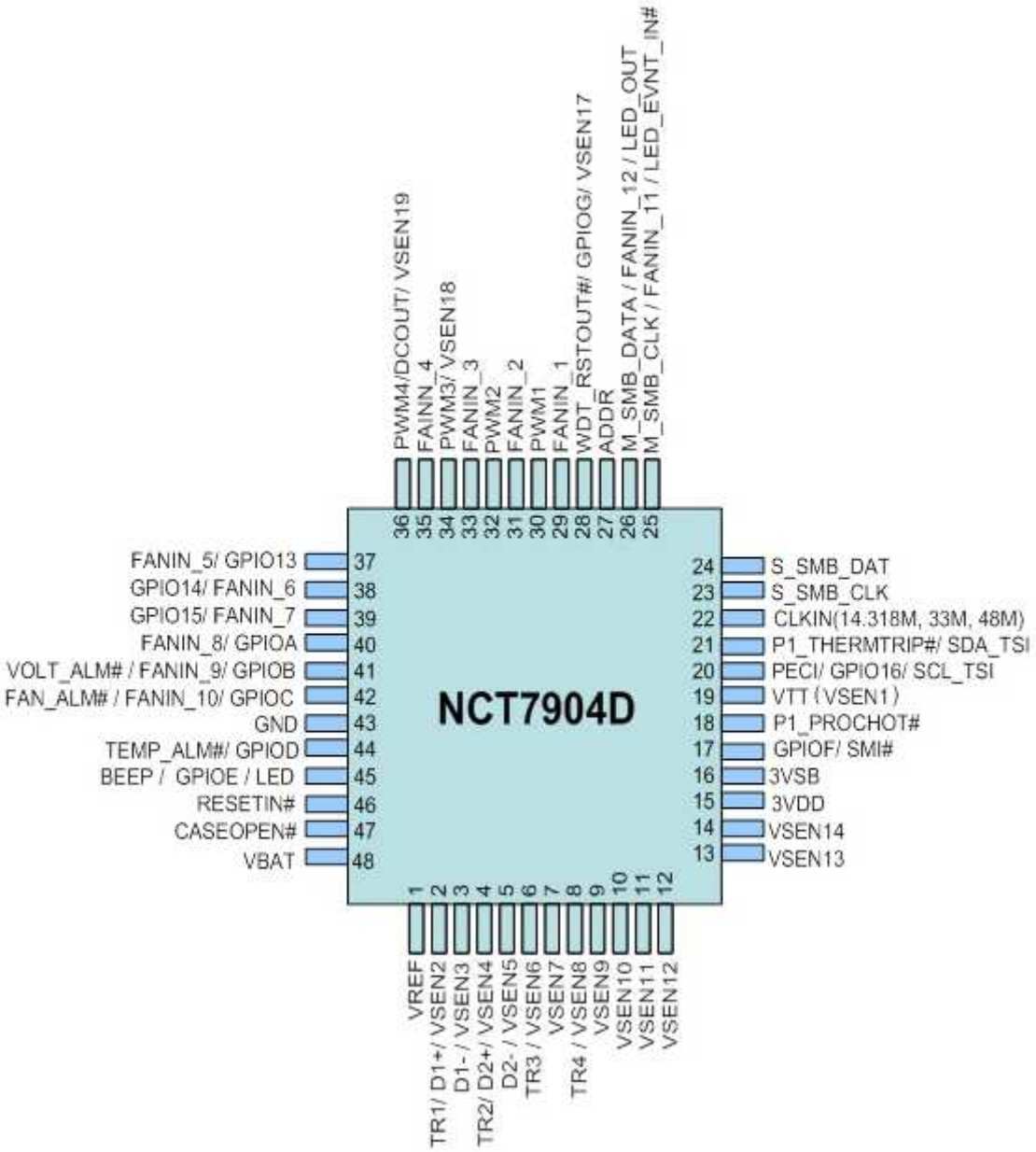
- Provide up to 11 GPIO pins (GPIO13~16, GPIOA~G, multi-function with other function pins)
- LED indication with programmable blinking frequency
- Event trigger LED by the external signal with programmable blinking frequency
- I^2C / SMBus2.0 serial bus interface (max. 400KHz Clock)
- Watch Dog Timer function with an output signal(WDT_RSTOUT#)
- 1 address selection pins provide 2 selectable SMBus addresses
- 3.3V operationPackage
- Packaged in 48-LQFP(7mm x 7mm) type, RoHS-Compliant and Halogen free

3. KEY SPECIFICATIONS

- Voltage monitoring accuracy
  - VSEN inputs ±10mV
  - Power inputs and VSEN17,18,19 inputs ±60mV
- Temperature Sensor Accuracy
  - Remote Diode Sensor Accuracy (25~85°C) ± 1°C typ.
  - On-chip Temperature Sensor Accuracy (25~70°C) ± 1°C typ.
  - Remote Diode Sensor Resolution 0.125 ℃
  - On-chip Temperature Sensor Resolution 0.125 ℃
- Supply Voltage 3.3V ± 5%
- Operating Supply Current 15 mA typ.
- Operating Temperature Range -20°C ~ 100°C *1

*1 Guaranteed by design from -20~100 degree C, 100% tested at 85 degree C.

4. PIN CONFIGURATION



5. PIN DESCRIPTION

5.1 Pin Type Description

SYMBOL	DESCRIPTION
TTL	TTL level
GTL	VTT level
TSI	TSI level
I	Input
O	Output (Push-pull)
OD	Open-drain output
AIN	Input pin(Analog)

5.2 Pin Description List

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VREF	1	3VSB	AOUT	Reference voltage output. This pin is for thermistor application
TR1	2	3VSB	AIN	Thermistor 1 sensing input
D1+				Thermal diode 1 D+
VSEN2				Voltage sensing input. Detection range is 0~2.048V. (default)
D1-	3	3VSB	AIN	Thermal diode 1 D-
VSEN3				Voltage sensing input. Detection range is 0~2.048V
TR2	4	3VSB	AIN	Thermistor 2 sensing input
D2+				Thermal diode 2 D+
VSEN4				Voltage sensing input. Detection range is 0~2.048V.(default)
D2-	5	3VSB	AIN	Thermal diode 2 D-
VSEN5				Voltage sensing input. Detection range is 0~2.048V
TR3	6	3VSB	AIN	Thermistor 3 sensing input

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VSEN6				Voltage sensing input. Detection range is 0~2.048V
VSEN7	7	3VSB	AIN	Voltage sensing input. Detection range is 0~2.048V
TR4	8	3VSB	AIN	Thermistor 4 sensing input
VSEN8				Voltage sensing input. Detection range is 0~2.048V
VSEN9	9	3VSB	AIN	Voltage sensing input. Detection range is 0~2.048V
VSEN10	10	3VSB	AIN	Voltage sensing input. Detection range is 0~2.048V
VSEN11	11	3VSB	AIN	Voltage sensing input. Detection range is 0~2.048V
VSEN12	12	3VSB	AIN	Voltage sensing input. Detection range is 0~2.048V
VSEN13	13	3VSB	AIN	Voltage sensing input. Detection range is 0~2.048V
VSEN14	14	3VSB	AIN	Voltage sensing input. Detection range is 0~2.048V
3VDD	15		POWER	+3V VDD power. It is also a voltage monitor channel Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors
3VSB	16	-	POWER	+3V VSB power. It is also a voltage monitor channel Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors
GPIOF	17	3VSB	TTL I/OD	General Purpose I/O F (default)
SMI#		3VSB	TTL OD	System Management Interrupt.
P1_PROCHOT#	18	3VSB	GTL I/O	CPU1 PROCHOT# signal
VTT (VSEN1)	19	--	POWER	VTT power pin. This power will be also monitored as VSEN1
PECI	20	VTT	GTL I/O	Intel® PECI interface signal. The power source is pin 19 (VTT)
GPIO16		3VSB	TTL I/OD	General Purpose I/O 16

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
SCL_TSI		3VSB	TSI OD	Clock line of AMD® SB_TSI interface
P1_THERMTRIP#	21	3VSB	GTL I	CPU1 THERMTRIP# signal. Pull-down it when unused.
SDA_TSI		3VSB	TSI I/OD	Data line of AMD® SB_TSI interface
CLKIN(33M, 14.318M, 48M)	22	3VSB	TTL I	Clock input. 14.318MHz or 33MHz or 48MHz could be applied to this pin with corresponding register configuration. Default setting is for 33MHz This clock is for PECI and fan speed monitor
S_SMB_CLK	23	3VSB	TTL I	SMBus clock line for this device being slave device
S_SMB_DATA	24	3VSB	TTL I/OD	SMBus data line for this device being slave device
M_SMB_CLK	25	3VSB	TTL OD	SMBus clock line for this device being master device
FANIN_11			TTL I	Fan tachometer input
LED_EVNT_IN#			TTL I	An input event to trigger LED_OUT
M_SMB_DATA	26	3VSB	TTL I/OD	SMBus data line for this device being master device
FANIN_12			TTL I	Fan tachometer input
LED_OUT			TTL OD	When pin LED_EVNT_IN is asserted a low pulse, this pin will output a pulse to drive LED on or blinking
ADDR	27	3VSB	TTL I	SMBus slave address strap selection pin Strapped to low, the 7-bit address is 0101101 Strapped to high, the 7-bit address is 0101110
WDT_RSTOUT#	28	3VSB	TTL OD	Watch dog timer reset output
GPIOG			TTL I/OD	General Purpose I/O G (default)
VSEN17			AIN	Voltage sensing input. Detection range is 0~3.3V
FANIN_1	29	3VSB	TTL I	Fan tachometer input
PWM1	30	3VSB	TTL OD	Fan speed control PWM output. This is 5V tolerant
FANIN_2	31	3VSB	TTL I	Fan tachometer input

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
PWM2	32	3VSB	TTL OD	Fan speed control PWM output. This is 5V tolerant
FANIN_3	33	3VSB	TTL I	Fan tachometer input
PWM3	34	3VSB	TTL OD	Fan speed control PWM output. This is 5V tolerant
VSEN18			AIN	Voltage sensing input. Detection range is 0~3.3V
FANIN_4	35	3VSB	TTL I	Fan tachometer input
PWM4/DCOUT	36	3VSB	TTL OD AOUT	Fan speed control PWM or DC output. A register bit could be programmed to select PWM or DC mode. DC output is default mode. This is without 5V tolerant
VSEN19			AIN	Voltage sensing input. Detection range is 0~3.3V
FANIN_5	37	3VSB	TTL I	Fan tachometer input.(default)
GPIO13		3VSB	TTL I/OD	General Purpose I/O 13
FANIN_6	38	3VSB	TTL I	Fan tachometer input (default)
GPIO14		3VSB	TTL I/OD	General Purpose I/O 14
FANIN_7	39	3VSB	TTL I	Fan tachometer input (default)
GPIO15		3VSB	TTL I/OD	General Purpose I/O 15
FANIN_8	40	3VSB	TTL I	Fan tachometer input (default)
GPIOA		3VSB	TTL I/OD	General Purpose I/O A
VOLT_ALM#	41	3VSB	TTL OD	Voltage abnormal alert output signal (active low)
FANIN_9		3VSB	TTL I	Fan tachometer input (default)
GPIOB		3VSB	TTL I/OD	General Purpose I/O B
FAN_ALM#	42	3VSB	TTL OD	Fan speed abnormal alert output signal (active low)
FANIN_10		3VSB	TTL I	Fan tachometer input (default)

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
GPIOC		3VSB	TTL I/OD	General Purpose I/O C
GND	43		POWER	GROUND
TEMP_ALM#	44	3VSB	TTL OD	Temperature abnormal alert output signal (active low)
GPIOD			TTL I/OD	General Purpose I/O D (default)
LED	45	3VSB	TTL OD	Programmable frequency LED output signal
GPIOE			TTL I/OD	General Purpose I/O E (default)
BEEP			TTL OD	Beeper signal output when over heat event happens
RESETIN#	46	3VSB	TTL I	System reset input
CASEOPEN#	47	VBAT	TTL I	Case Open detection input signal. An active low input from an external device when case is opened. This event will be latched even when the case is closed. Pull-down it when unused.
VBAT	48		POWER	VBAT power for Case Open detection and status log

* **The recommended connection for Unused Pin**

(1) For digital input pin, pull down to GND.
(2) For digital output pin, keep floating.
(3) For analog input pin, keep floating.
(4) For analog output pin, keep floating.
(5) For VTT pin, keep floating.
(6) For VBAT pin, connect to 3VSB.

6. FUNCTIONAL DESCRIPTION

6.1 Access Interface

NCT7904D provides SMBus interface, which is compliant with SMBus 2.0 specification. The 7-bit serial address is selected to be 0101101 or 0101110 by pin ADDR. When pin ADDR is strapped to low, the SMBus address is 0x5A(write)/0x5B(read) ; when pin ADDR is strapped to high, the SMBus address is 0x5C(write)/0x5D(read).

NCT7904D supports the bus speed with 0~400KHz.

6.1.1 Data write to the internal register

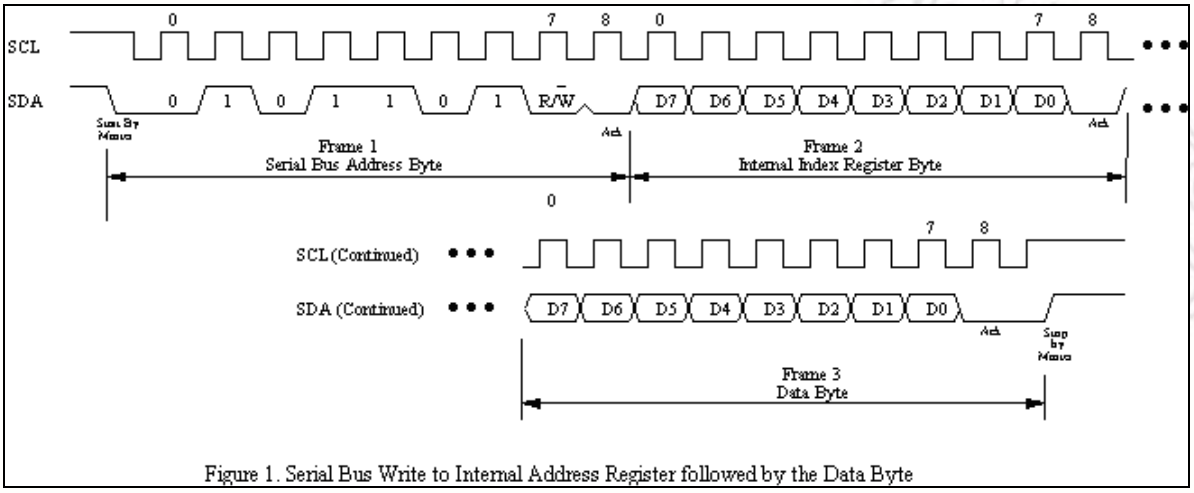


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

6.1.2 Data read from the internal register

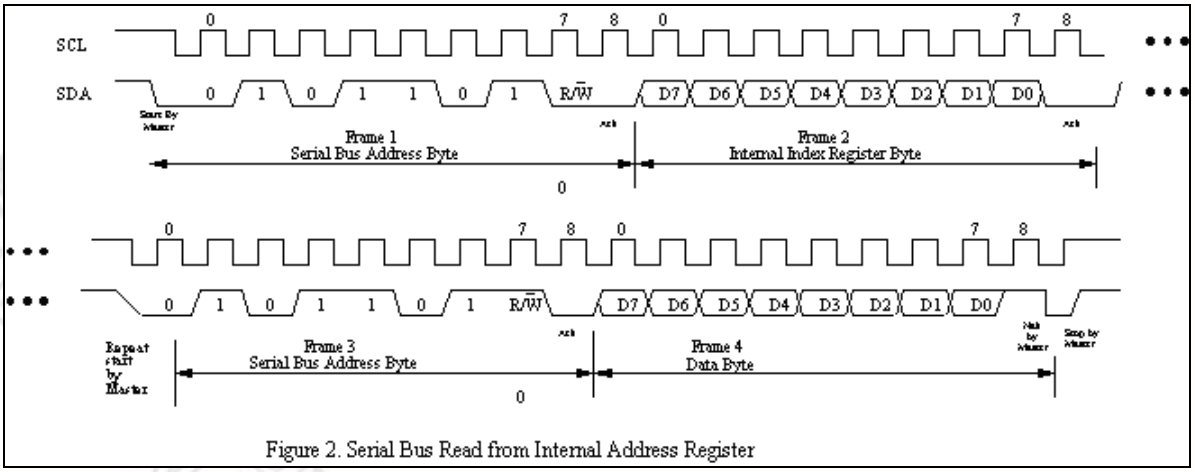


Figure 2. Serial Bus Read from Internal Address Register

6.2 Address Setting

NCT7904D has one address selection pin, the SMBus address will be strapped when 3VSB ready. The address will be retained as long as the 3VSB of NCT7904D is maintained. The pull-up power plane must be the same as the 3VSB power of NCT7904D.

ADDR	ADDRESS
0	0101 101X
1	0101 110X

X=Read/Write Bit

6.3 Temperature Monitor Data Format

The temperature data with 11-bit 2`s complement format

TEMPERATURE	8-BIT DIGITAL OUTPUT HIGH BYTE	3-BIT DIGITAL OUTPUT LOW BYTE
+127.875°C	0111,1111	XXXX,X111
+25.750°C	0001,1001	XXXX,X110
+2.250°C	0000,0010	XXXX,X010
+1.125°C	0000,0001	XXXX,X001
+0.000°C	0000,0000	XXXX,X000
- 1.125°C	1111,1110	XXXX,X111
- 2.250°C	1111,1101	XXXX,X110
- 25.750°C	1110,0110	XXXX,X010
- 127.875°C	1000,0000	XXXX,X001

6.4 Voltage Sense Data Format

VSEN Low Byte together with VSEN High Byte forms the 11-bit count value. If VSEN High Byte readout is read successively, the NCT7904D will latch the VSEN Low Byte for next read. Then voltage readout high byte and low byte are combined to *11-bitVoltageValue*.

For voltage monitoring, real voltage calculations should follow the formula:

VSEN1~14 : $Voltage(V) = 11bitCountValue \times 0.002$

3VSB,3VDD,VBAT,VSEN17,18,19 : $Voltage(V) = 11bitCountValue \times 0.006$

* VSEN17,18,19 are embedded internal voltage divider resistors.

6.5 FAN_IN Count Calculation

The FAN_IN tachometer high byte and low byte are combined to 13-bitCountValue. Real RPM (Rotate per Minute) calculation should follow the formula:

$$FanSpeed(RPM) = \frac{1.35 \times 10^6}{(13 - bitCountValue) \times (FanPoles/4)}$$

In this formula, FanPole stands for the number of NS pole pairs inside the fan. Normally an N-S-N-S Fan (FanPole=4) generates 2 pulses after completing one rotation.

6.6 FAN_OUT Duty Cycle/DC output Calculation

The NCT7904D provides 4 set of PWM and 1 set of DC output for fan speed control. The duty cycle of PWM can be programmed by an 8-bit register. The expression of duty cycle can be represented as follow formula:

$$\text{Duty} - \text{cycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The DC output can be programmed by an 8-bit register. The expression of DC level can be represented as follow formula:

$$\text{DC output (V)} = 3VDD \times \frac{\text{Programmed 8 - bit Register Value}}{255}$$

6.7 Fan Speed Control

Except for traditional Fan Duty control, the latest closed loop fan control (RPM Mode) has been provided by the NCT7904D. Due to PECI negative temperature format, the fan control also supports negative temperature representation. It would be much easy to implement fan control by PECI reading. In addition to PECI CPU temperature, the NCT7904D also supports fan control, which is responded to CPU power.

In Smart Fan Mode, there are some Fan control parameters as below descriptions:

6.7.1 Step Up Time / Step Down Time

Smart Fan is designed for the smooth operation of the fan. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed. On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat. This register should never be set to 0, otherwise, the fan duty will be abnormal.

6.7.2 Fan Output Nonstop Value

It takes some time to bring a fan from still to working state. Therefore, Nonstop value are designed with a minimum fan output to keep the fan working when the system does not require the fan to help reduce heat but still want to keep the fast response time to speed up the fan.

6.7.3 Smart Fan Control Table

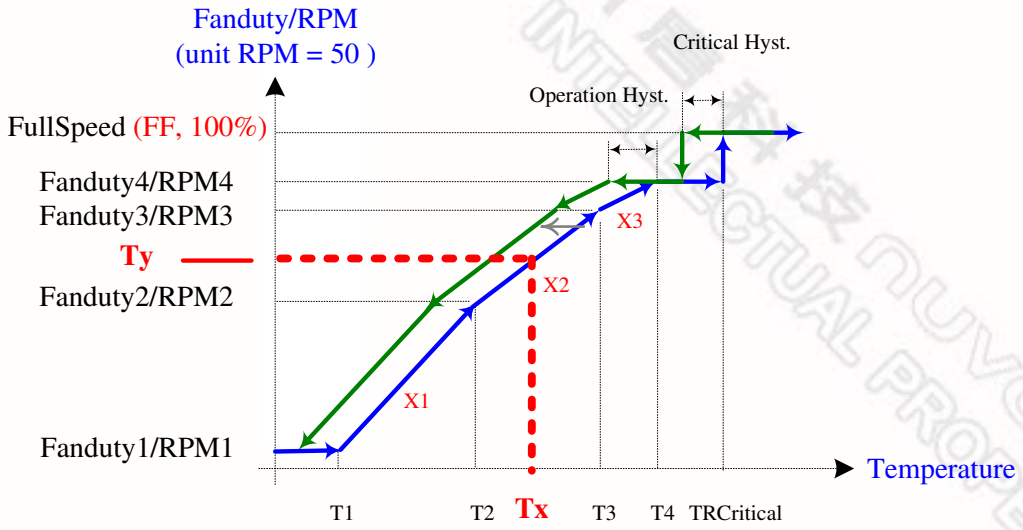
SMART FAN™ IV and Close Loop Fan Control Mode offer 4 slopes to control the fan speed. The 3 slopes can be obtained by setting FanDuty/RPM1~FanDuty/RPM4 and T1~T4 through the registers. When the temperature rises, FAN Output will calculate the target Fan Duty/RPM based on the current slope. For example, assuming Tx is the current temperature and Fan Duty/RPMy is the target, then the slope:

$$X2 = \frac{(FanDuty3/RPM3) - (FanDuty2/RPM2)}{(T3 - T2)}$$

Fan Output:

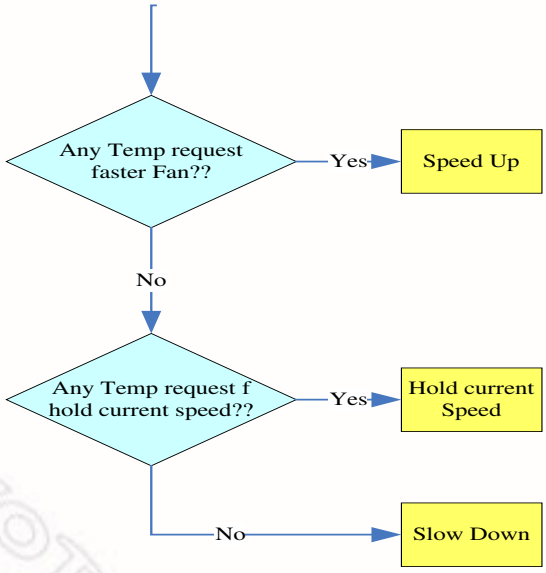
$$T\arg et\ FanDuty\ or\ RPM = (FanDuty2\ or\ RPM2) + (Tx - T2) \cdot X2$$

SMART FAN™ IV & Close Loop Fan Control Mechanism



In addition, SMART FAN™ IV & Close Loop Fan Control can also set up Critical Temperature and Hysteresis. If the current temperature exceeds Critical Temperature, external fan will be forced by maximum Fan Duty to meet the largest target Fan Duty or RPM, Which is 0xFF. The target Fan Duty & RPM value will be determined in accordance to the slope only when the temperature falls below (TCritical – Critical Hyst.)

NCT7904D provides several temperature sources selects to map the fan, the algorithm will make a decision to control the fan as below figure:



6.7.4 DTS (Sensor) Based Fan Control

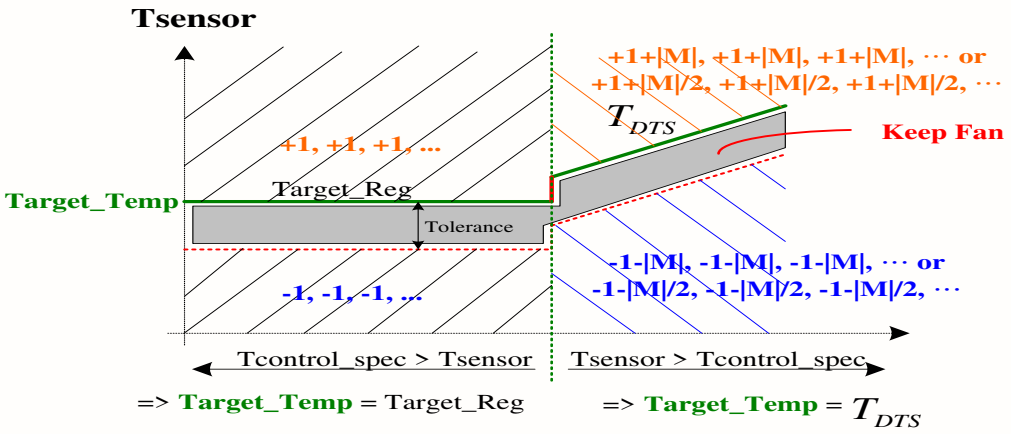
NCT7904D fully follows Intel latest DTS Based Thermal Spec to come out an easy used fan speed control algorithm which has involved traditional thermal cruise mode concept. Users are supposed to have related document to capture Intel's concept.

The principle of DTS based fan control behavior will be described with the figure in the below. First of all, there are two mainly behaviors, which is distinguished by whether Tsensor is larger than Tcontrol_spec.

If Tcontrol_spec is larger than Tsensor, the fan control behavior will obey left plane and thermal cruise mode's Target_Temp is set as Target_Reg. Once Tsensor > Target_Reg, the fan out duty will continuously increases by one duty until Tsensor is under Target_Reg. In contrary, if Tsensor < (Target_Reg – Tolerance), the fan out duty will continuously decreases by one duty until Tsensor is over (Target_Reg – Tolerance).

If Tcontrol_spec is smaller than Tsensor, the fan control behavior will obey right plane and thermal cruise mode's Target_Temp is set as TDTS which just is Intel's DTS thermal profile. Once Tsensor > TDTS, the fan out duty will continuously increases by (1+|M|) duty until Tsensor is under TDTS. The symbol of M represents "Margin". It could be provided by NCT7904D itself. In contrary, if Tsensor < (TDTS – Tolerance), the fan out duty will continuously decreases by (1+|M|) duty until Tsensor is over (TDTS – Tolerance).

For both of plane, the gray region means that the fan out duty is unchanged at this moment.



Thermal Cruise Mode

6.8 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read plentiful information of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer.

6.8.1 Operation Mode

NCT7904D provides two operation modes. One is active mode, the other is passive.

For active mode, NCT7904D serves as a host to initiate a message transaction. NCT7904D provides automatic polling procedure for CPU temperature, CPU power and DRAM temperature. These thermal data could be continuously updated without any firmware intervention. In contrarily, except for what mentioned above, user still could write out or read in data to / from CPU by practicing manual commands which are pre-configured by external firmware.

In passive mode, NCT7904D just monitor the message over the PECI bus with silence and then only extract CPU's DTS thermal data for its fan speed control purpose.

6.8.2 CPU Temperature and Power Reporting

In NCT7904D, it supports CPU temperature and power reporting. And both of reading could be associated to NCT7904D's fan control algorithm.

For CPU temperature, by interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. However NCT7904D has a biasing factor for customer to characterize the relation between "counts" and "temperature".

Figure A shows a typical fan speed (PWM duty cycle) and PECI temperature relationship. SMART FAN™ IV

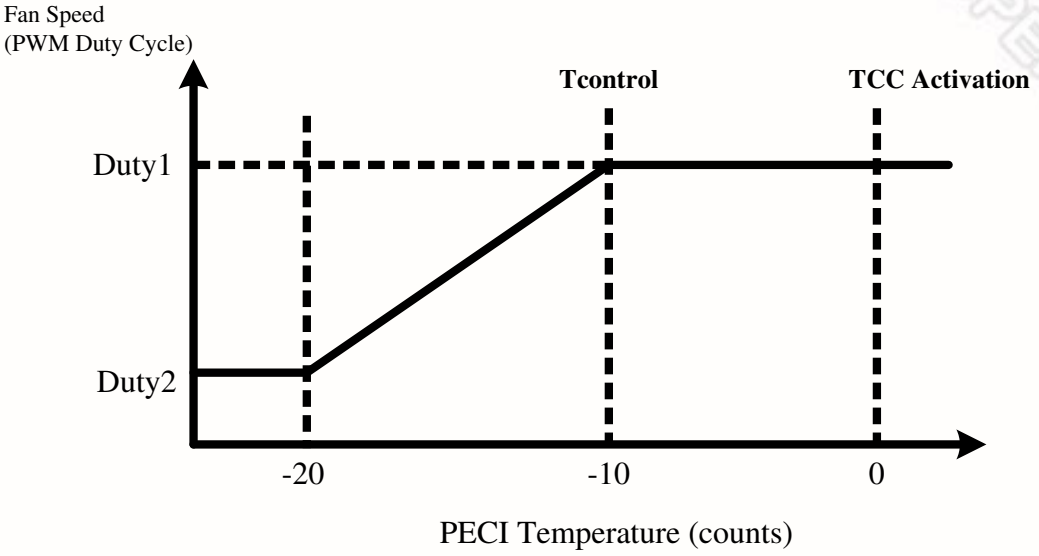


Fig. A PECI Temperature

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At Tcontrol PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of Tcontrol can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The Tcontrol MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, Tcontrol is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

For CPU power reporting, the NCT7904D routinely retrieves CPU energy and then convert it to power. The refreshing rate of power is 0.3 sec. In order to minimize the effect of suddenly huge power changing, the running time average algorithm has been implemented.

6.8.3 DRAM Thermal Data Reporting

NCT7904D can automatically report all 24 DIMMs thermal status which are provided by Intel CPU0 and CPU1 agent. In addition to each DIMM temperature, NCT7904D also records the highest DIMM temperature in the specific channel. Here is the relationship among CPU, Channel and DIMM.

Both the Channel Index<2:0> and DIMM Index<5:3> follow PECI3.0 RdPkgConfig() command format.

Agent Address	Channel_Index<2:0>	DIMM Index<5:3>	Register Location
CPU0_30h	Channel_0	DIMM_0	T_D0C0_C0
		DIMM_1	T_D1C0_C0
		DIMM_2	T_D2C0_C0
	Channel_1	DIMM_0	T_D0C1_C0
		DIMM_1	T_D1C1_C0
		DIMM_2	T_D2C1_C0
	Channel_2	DIMM_0	T_D0C2_C0
		DIMM_1	T_D1C2_C0
		DIMM_2	T_D2C2_C0
	Channel_3	DIMM_0	T_D0C2_C0
		DIMM_1	T_D1C2_C0
		DIMM_2	T_D2C2_C0
CPU1_31h	Channel_0	DIMM_0	T_D0C0_C1
		DIMM_1	T_D1C0_C1
		DIMM_2	T_D2C0_C1
	Channel_1	DIMM_0	T_D0C1_C1
		DIMM_1	T_D1C1_C1
		DIMM_2	T_D2C1_C1
	Channel_2	DIMM_0	T_D0C2_C1
		DIMM_1	T_D1C2_C1
		DIMM_2	T_D2C2_C1
	Channel_3	DIMM_0	T_D0C3_C1
		DIMM_1	T_D1C3_C1
		DIMM_2	T_D2C3_C1

6.8.4 PECI Listening

It provides another way to obtain CPU's DTS thermal data. NCT7904D only recognizes GetTemp() command. Once GetTemp() appears on PECI bus and entire message is without FCS error, the CPU's DTS temperature will be extracted and recorded. These data could be temperature source of fan speed control.

6.9 SMI# Output

6.9.1 Temperature

SMI# for temperature monitoring provides 3 modes.

6.9.1.1. Comparator Interrupt Mode

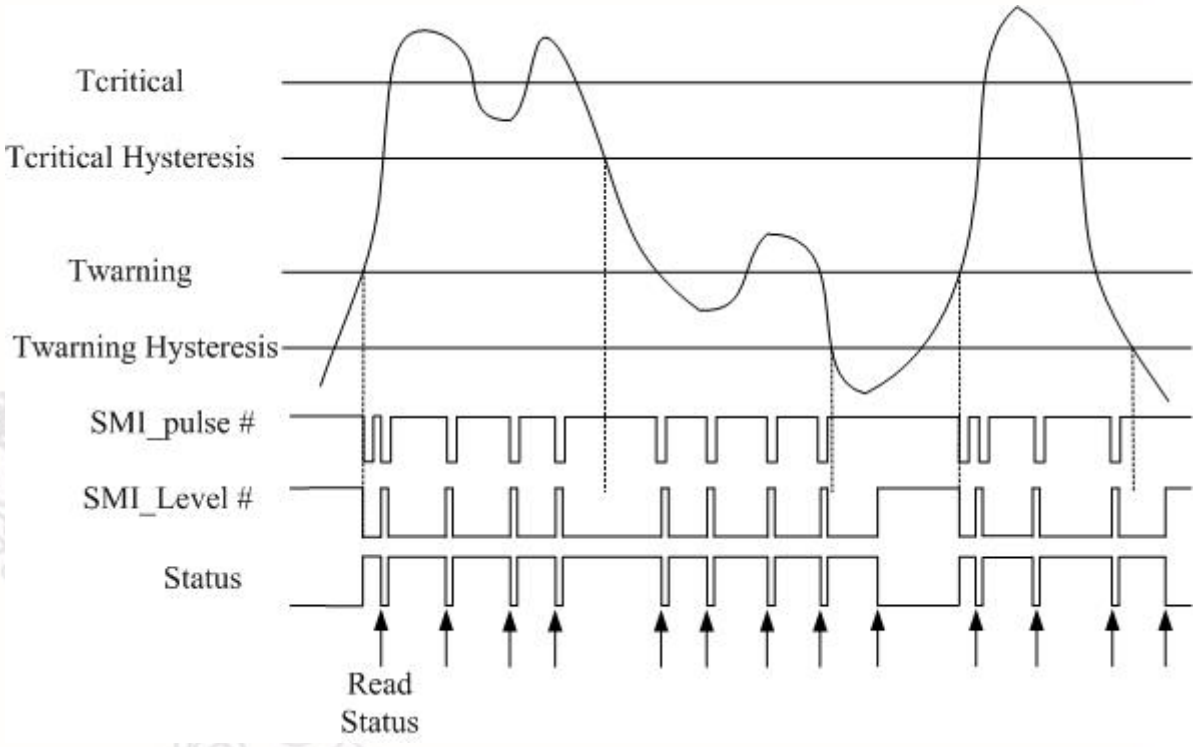
Temperature exceeding Twarning causes an interrupt and this interrupt will be reset when reading all of the Interrupt Status Registers. Once an interrupt event has occurred by exceeding Twarning, then reset, if the temperature remains above the Twarning Hysteresis, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding Twarning and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below Twarning Hysteresis.

6.9.1.2. Two-Times Interrupt Mode

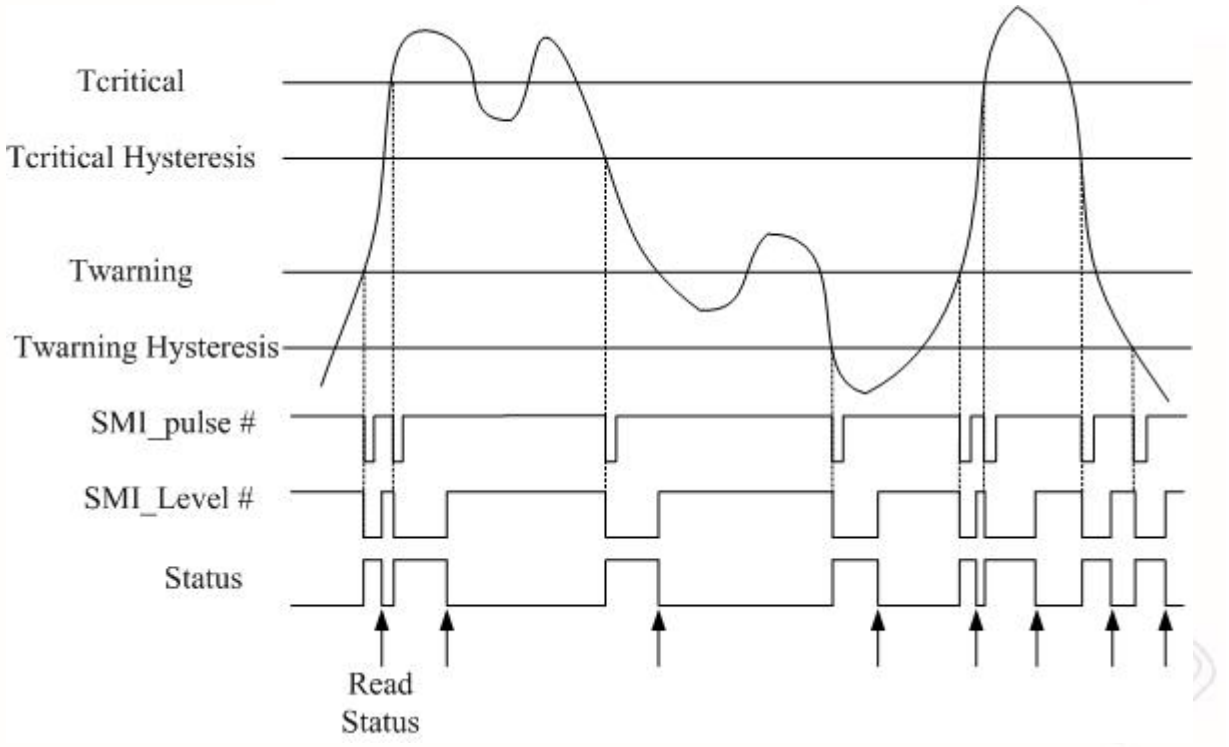
Temperature exceeding Tcritical / Twarning causes an interrupt and then temperature going below Tcritical Hysteresis / Twarning Hysteresis will also cause an interrupt if the previous interrupt has been reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding Tcritical / Twarning, then reset, if the temperature remains above the Tcritical Hysteresis / Twarning Hysteresis, the interrupt will not occur.

6.9.1.3. One-Time Interrupt Mode

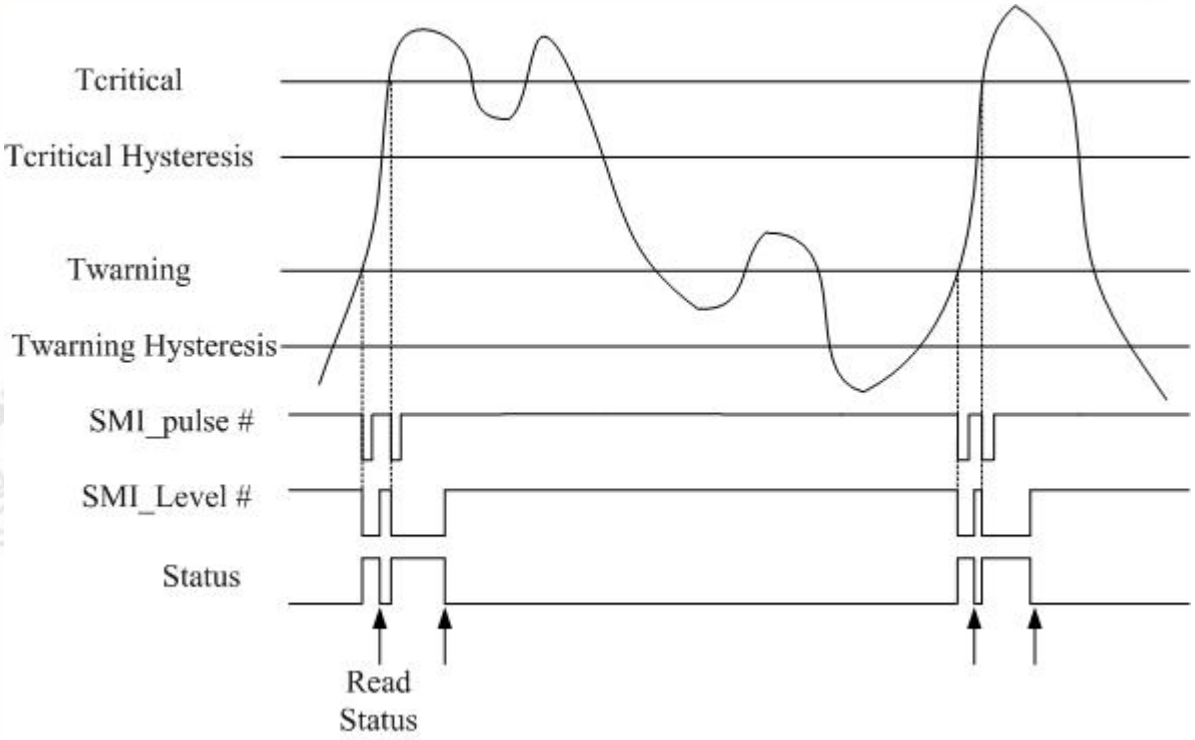
Temperature exceeding Tcritical / Twarning causes an interrupt and then temperature going below Tcritical Hysteresis / Twarning Hysteresis will not cause an interrupt. Once an interrupt event has occurred by exceeding Tcritical / Twarning, then going below Tcritical Hysteresis / Twarning Hysteresis, an interrupt will not occur again until the temperature exceeding Tcritical / Twarning.



SMI comparator mode



SMI two time mode



SMI one time mode