Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Test Procedure for the NCV47411PAAJGEVB Evaluation Board

The NCV47411 is dual channel adjustable Low Dropout Regulator with:

- Two adjustable output voltages from 3.3 V to 20 V
- Two adjustable current limits up to 150 mA
- Enable inputs with 3.3 V Logic compatible thresholds

Power supplying of the chip is possible from one or two independent sources. **INPUT1** must be always supplied and **INPUT2** as optional for $\mathbf{V_{in2}}$ supply.

1. **Power supplying**
   a. **Power supplying from one source**
   Connect the test setup as is shown in **Figure 1** (See **Table 1** with required equipment). Connect power supply to **INPUT1** connector $\mathbf{J_1}$ (Power supplying of **INPUT2** is not needed).
      - **Hi_F –** Positive Force line
      - **Hi_S –** Positive Sense line
      - **Lo_F** – Negative Force line
      - **Lo_S** – Negative Sense line

   Connect $\mathbf{V_{in2}}$ pin to **INPUT1** via appropriate position of jumper "$\mathbf{V_{in2}}$ **to IN1 or IN2 connection**".

   b. **Power supplying from two sources**
   Connect the test setup as is shown in **Figure 1** (See **Table 1** with required equipment). Connect two power supplies to **INPUT1** connector $\mathbf{J_1}$ and to **INPUT2** connector $\mathbf{J_2}$, respectively.
      - **Hi_F –** Positive Force line
      - **Hi_S –** Positive Sense line
      - **Lo_F** – Negative Force line
      - **Lo_S** – Negative Sense line

   Values of input voltages $\mathbf{V_{in1}}$ and $\mathbf{V_{in2}}$ can be different. This option is suitable for reducing of power dissipation on chip.
   Connect $\mathbf{V_{in2}}$ pin to **INPUT2** via appropriate position of jumper "$\mathbf{V_{in2}}$ **to IN1 or IN2 connection**".

2. Connect jumpers $\mathbf{J_{10} – J_{13}}$ for output current limitation from $\mathbf{V_{out1}}$ pin and $\mathbf{J_{20} – J_{23}}$ for output current limitation from $\mathbf{V_{out2}}$ pin.
   - $\mathbf{J_{n0}}$ – I_{LIMn0} ~ 10 mA
   - $\mathbf{J_{n1}}$ – I_{LIMn1} ~ 50 mA
   - $\mathbf{J_{n2}}$ – I_{LIMn2} ~ 100 mA
   - $\mathbf{J_{n3}}$ – I_{LIMn3} – R_{CSOn3} positions available for individual current limit setting by resistor from range 850 Ω to 12.75 kΩ

3. Set Input Voltage and turn on Power Supply/Supplies.

4. Enable output of the channel to power the regulated output voltage by connecting the **ENABLE** pin to corresponding $\mathbf{V_{in}}$ via jumper. Enabling can be performed by external voltage source as well.

5. Load the outputs by resistive loads connected via jumpers:
   - $\mathbf{J_5, J_7}$ – 51 Ω
   - $\mathbf{J_6, J_8}$ – 1 kΩ

   External loads can be used instead build-in resistive loads as well.

6. Monitor Output Voltages, given according to Equation 1.

$$V_{out\_nom\_n} = 1.275\left(1 + \frac{R_{n1}}{R_{n2}}\right) \qquad \text{(eq. 1)}$$

7. Monitor Current Sense Output voltages on appropriate connector. They should be max 2.55 V in steady state. The CSO voltages are proportional to output currents according to Equation 2.

$$V_{CSO\_n} = I_{out\_n}\left(R_{CSO\_n} \times \frac{1}{50}\right) \qquad \text{(eq. 2)}$$

8. Compare your results with measured results in **Table 2.**

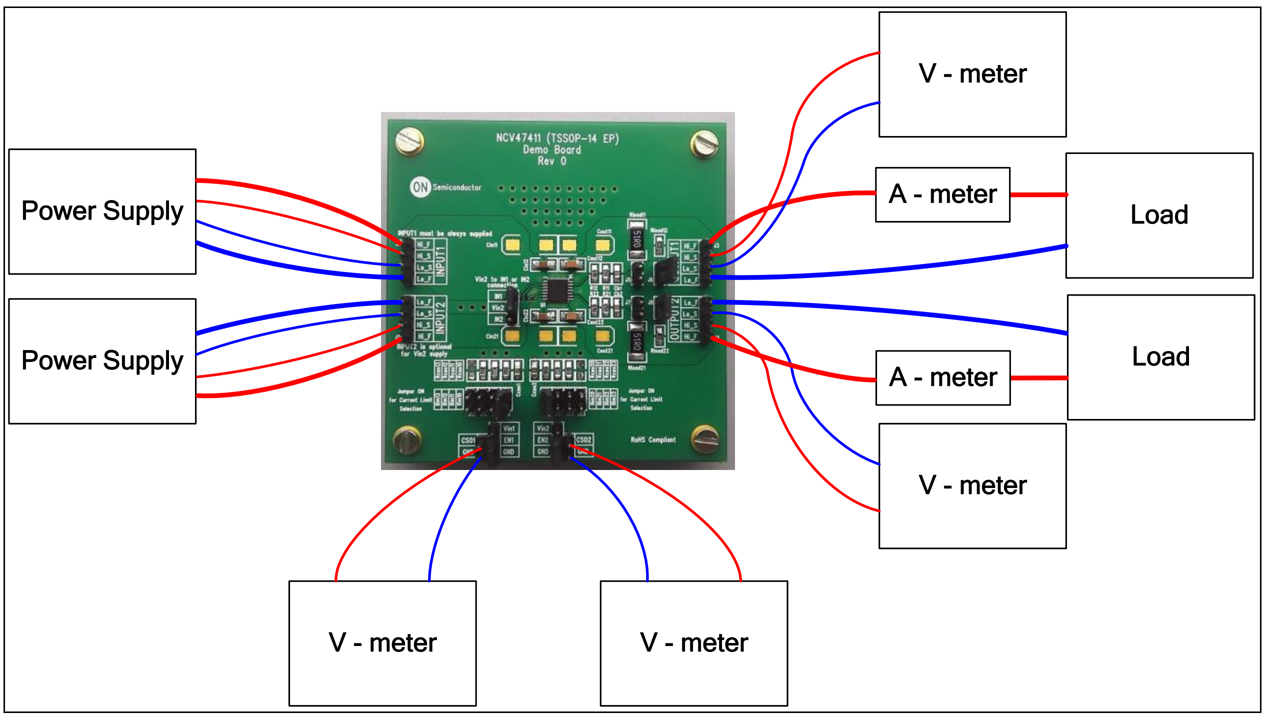

Figure 1. General Test Setup

Table 1: Required Equipment

Equipment	Ranges
Power Supply	0 V – 45 V / 1 A
Load	0 mA – 500 mA
V - meter	0 V – 20 V
A - meter	0 mA – 500 mA

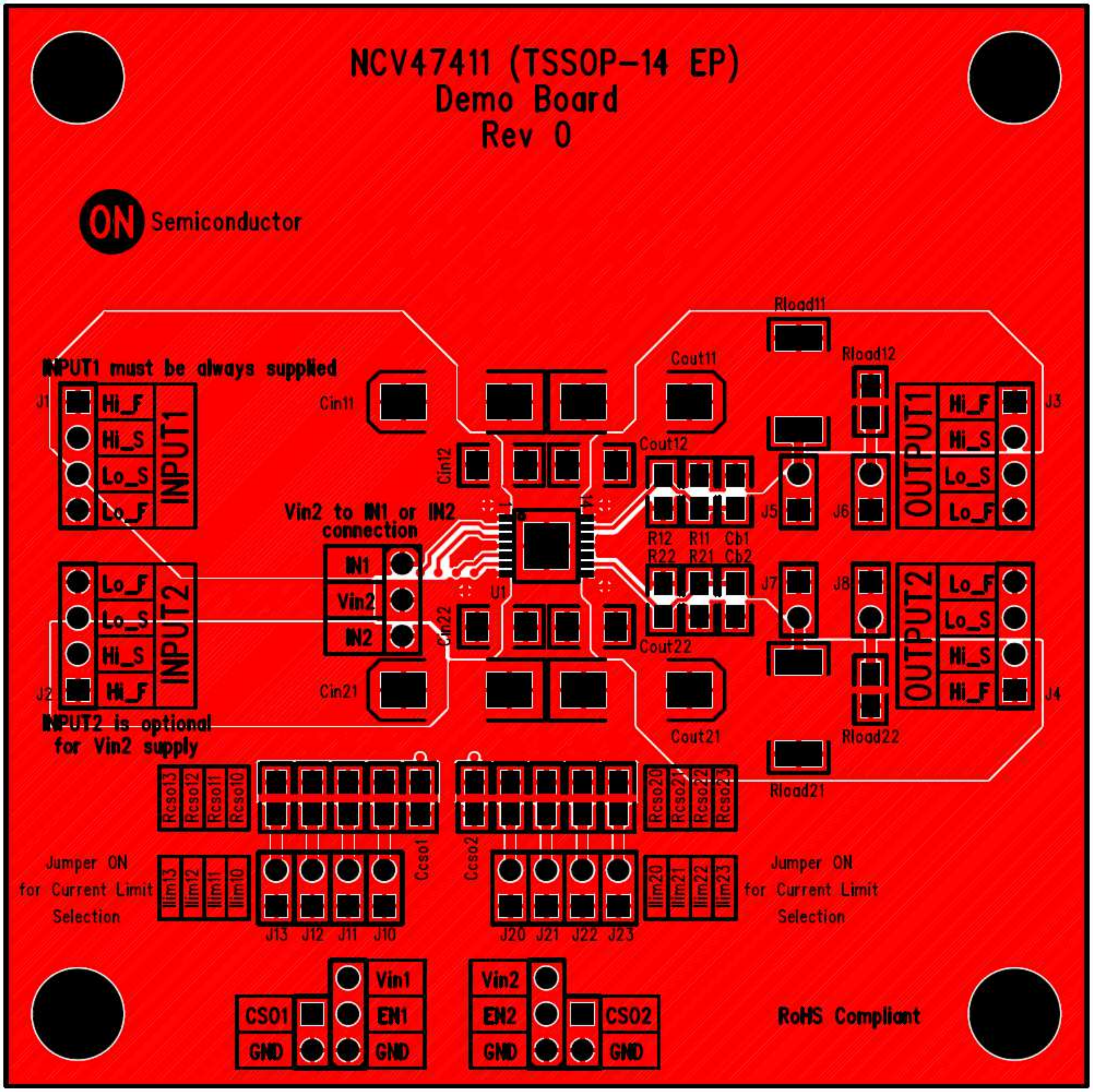

Figure 2. Top side PCB Layout (3 x 3 inch)

Table 2: Measured Results

Parameter	Test Conditions	Symbol	Value		Unit
			Nominal	Measured	
Output Voltage	V_{in} = 13.5 V, $V_{out\_nom\_n}$ = 5.02 V, I_{out_n} = 5 mA, R_{CSO_n} = Short to ground	V_{out1}	5.02	5.006	V
		V_{out2}		5.005	
	V_{in} = 13.5 V, $V_{out\_nom\_n}$ = 5.02 V, I_{out_n} = 100 mA, R_{CSO_n} = Short to ground	V_{out1}		5.005	
		V_{out2}		5.005	
Output Current	V_{in} = 13.5 V, $V_{out\_nom\_n}$ = 5.02 V, V_{out_n} = 90 % of $V_{out\_nom\_n}$, R_{CSO_n} = 12.7 kΩ	I_{out1}	10.04	10.06	mA
		I_{out2}		10	
	V_{in} = 13.5 V, $V_{out\_nom\_n}$ = 5.02 V, V_{out_n} = 90 % of $V_{out\_nom\_n}$, R_{CSO_n} = 2.49 kΩ	I_{out1}	51.2	52.47	
		I_{out2}		52.19	
	V_{in} = 13.5 V, $V_{out\_nom\_n}$ = 5.02 V, V_{out_n} = 90 % of $V_{out\_nom\_n}$, R_{CSO_n} = 1.2 kΩ	I_{out1}	106.25	110.28	
		I_{out2}		109.95	
Output Current	V_{in} = 13.5 V, $V_{out\_nom\_n}$ = 5.02 V, V_{out_n} = 0 V, R_{CSO_n} = 12.7 kΩ	I_{out1}	10.04	10.55	mA
		I_{out2}		10.49	
	V_{in} = 13.5 V, $V_{out\_nom\_n}$ = 5.02 V, V_{out_n} = 0 V, R_{CSO_n} = 2.49 kΩ	I_{out1}	51.2	54.44	
		I_{out2}		54.17	
	V_{in} = 13.5 V, $V_{out\_nom\_n}$ = 5.02 V, V_{out_n} = 0 V, R_{CSO_n} = 1.2 kΩ	I_{out1}	106.25	115.32	
		I_{out2}		114.37	