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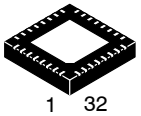
NCV53480

Low-Power OOK/FSK/ASK ISM Band Transceiver

ON Semiconductor®

http://onsemi.com



NQFP 32, 6x6
CASE 560AR

MARKING DIAGRAM

NCV53480−C = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package
CCCCC = Country of Origin*
(*Not required if assembled in USA)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

General Description

The NCV53480 ASSP is a low power OOK/FSK/ASK transceiver designed for operation in the ISM band from 260 MHz to 470 MHz. It is intended for use in narrowband, low data rate applications in the range of 1 kbps to 60 kbps. The receiver architecture is low−IF, and contains image reject filtering to provide 40 dB of image reject. The IF filter is fully integrated on chip with selectable bandwidth settings of 100 kHz, 200 kHz, and 300 kHz. The transmitter output power is programmable from −20 to 10 dBm.

On−chip digital circuitry can be configured to have the part perform periodic channel polling on up to 3 channels, with full control of the polling interval and active receive time for each channel. Additional register control can be used to have the part wake based on a pattern, energy level, or detected ID.

Features

- Single Supply Operation from 2.2 V to 3.63 V
- Temperature Range: −40°C to +125°C
- Simultaneous OOK/FSK (De)modulation
- No External Switch Needed Between LNA Input and PA Output
- Low Current Consumption Mode (< 1 μA)
- Programmable Frequency Band from 280 MHz to 434 MHz with Multichannel Operation (3 Channels)
- Continuous Receive Current Consumption < 10 mA
- FSK Receiver Sensitivity −109 dBm at 10 kbps NRZ
- OOK Receiver Sensitivity −118 dBm at 1 kbps NRZ
- Wake−On−Pattern and Wake−On−Energy capability
- Programmable Data Rates Up to 60 kbps
- Sniff−Mode Utilizing Patented Quick−Start Oscillator
- 128 Bit Receive Buffer
- 18 mA Continuous Transmit Mode at 10 dBm Output Power
- Programmable Output Power from −20 dBm to +10 dBm
- Dual Configurations for Sniffing, Receiving and Transmitting To and From Different Sources
- Internal Self−Calibration Routines
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Two−Way Keyless Entry
- TPMS
- Remote Control
- Remote Sensing
- Automatic Meter Reading
- Consumer Electronics
- Home and Building Automation
- Wireless Security Systems
- Telemetry

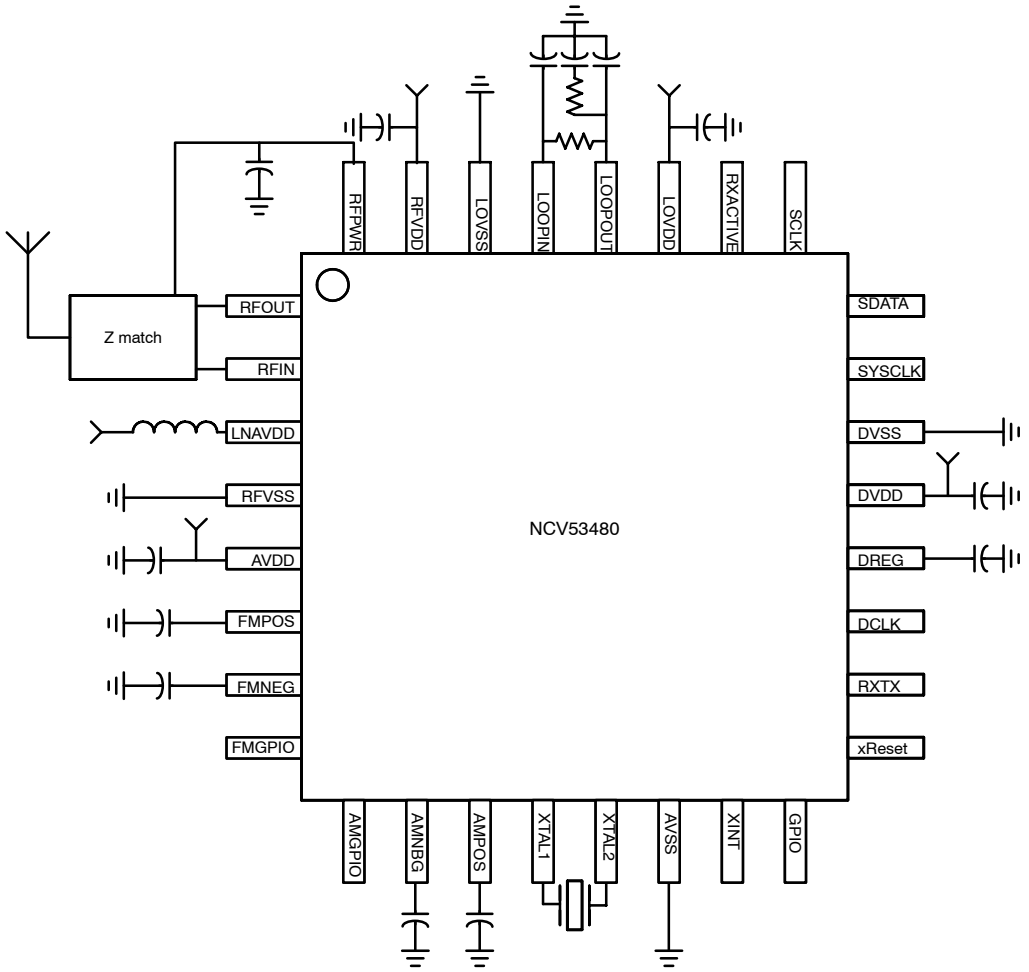


Figure 1. Pinout

Table 1. ORDERING INFORMATION

Part No.	Package	Shipping†
NCV53480MN1G−C	NQFP−32 (Pb−Free)	40 Units / Tube
NCV53480MN1R2G−C	NQFP−32 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

BLOCK DIAGRAM, PINOUT TABLE AND PAD DESCRIPTION

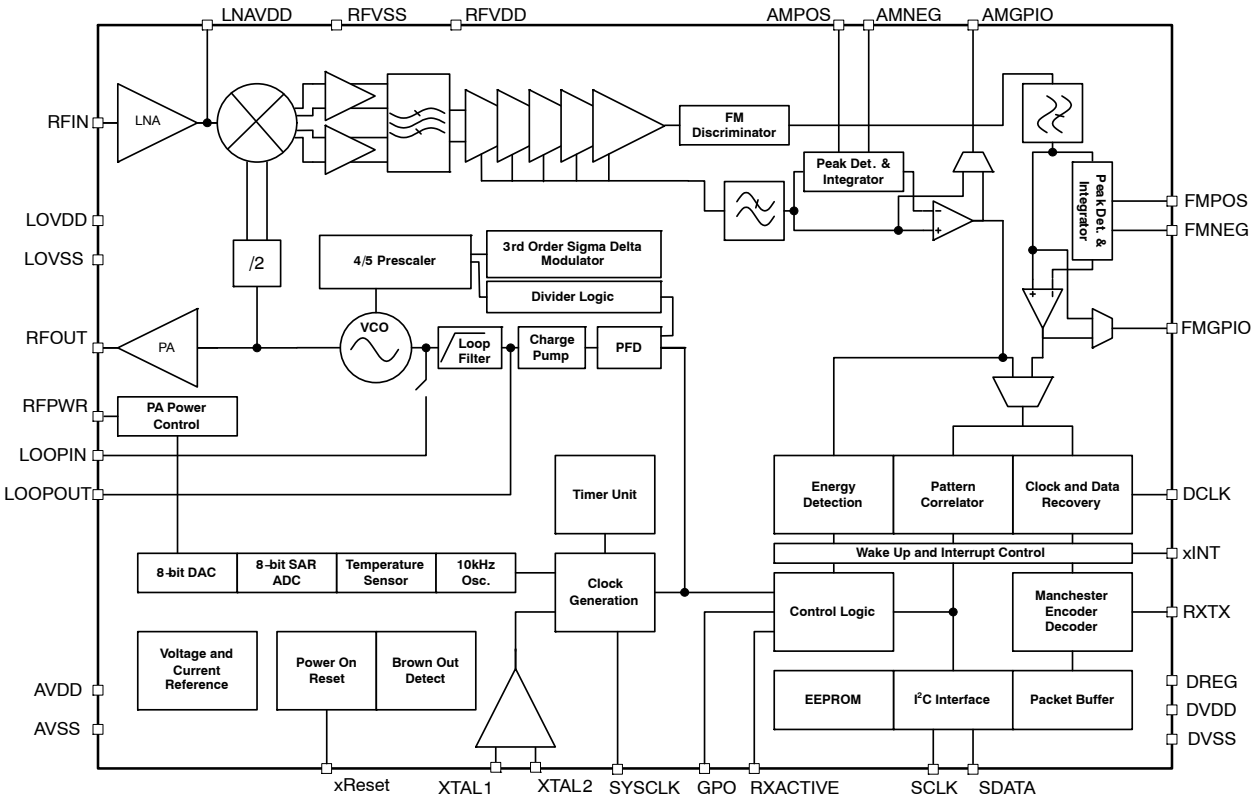


Figure 2. Block Diagram

Table 2. PINOUT AND DESCRIPTION

Pin	Name	Pad Description
1	RFOUT	RF Output
2	RFIN	RF Input
3	LNAVDD	LNA Supply Connection
4	RFVSS	V_{SS} for the RF Section
5	AVDD	V_{DD} for the Analog Section
6	FMPOS	External Cap Connection for the FM Peak Detector, or for the RC Integrator (See FSK Detector Section)
7	FMNEG	External Cap Connection for the FM Negative Peak Detector
8	FMGPIO	Multi−Function Pin Can Provide Analog FM out, FSK Sliced Data Out, and is Used as an Input for FSK Transmit.
9	AMGPIO	Multi−Function Pin Can Provide Analog RSSI, ASK Sliced Data Out, and is Used as an Input for ASK Transmit.
10	AMNEG	External Cap Connection for the AM Negative Peak Detector
11	AMPOS	External Cap Connection for the AM Peak Detector, or for the RC Integrator (See ASK Detector Options)
12	XTAL1	Crystal Oscillator Input Pin
13	XTAL2	Crystal Oscillator Output Pin
14	AVSS	V_{SS} for the Analog Section
15	xINT	Active low output for interrupt of external micro−processor during a receive event
16	GPO	General Purpose Output
17	xReset	Open Drain Digital IO. This Signal Will Go Active (‘0’) During a POR, or Can Be Pulled Active (‘0’) to Reset the Part.
18	RXTX	Recovered Data from the CDR in Receive Mode. Transmit Data for Synchronous Transmit Mode.
19	DCLK	Recovered Clock from the CDR in Receive Mode. Baud Clock for Synchronous Transmit Mode.
20	DREG	External capacitor connection for the internal digital regulator
21	DVDD	V_{DD} for the Digital Section
22	DVSS	V_{SS} for the Digital Section
23	SYSCLK	General Purpose Digital Output that can be Configured to Provide a System Clock to an External Micro−Processor
24	SDATA	Data Pin for the Serial I^2C Register Interface
25	SCLK	Clock pin for the serial I^2C Register Interface
26	RXACTIVE	Pin Used to Indicate the Device is in Receive
27	LOVDD	V_{DD} for the PLL
28	LOOPOUT	Charge Pump Output to External Loop Filter
29	LOOPIN	VCO Control Input When External Loop Filter is Selected
30	LOVSS	V_{SS} for the PLL
31	RFVDD	V_{DD} for the RF Section
32	RFPWR	Transmitter Power Supply for Output Power Regulation

DC SPECIFICATIONS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
DVDD	Digital DC Supply Voltage (Note 1)	−0.4	4.0	V
AVDD	Analog DC Supply Voltage (Note 1)	−0.4	4.0	V
RFVDD	RF DC Supply Voltage (Note 1)	−0.4	4.0	V
Vin	Input Pin Voltage (Note 1)	−0.4	4.0	V
Iin	Input Pin Current	−100	100	mA
MaxRFin	Input RF Level		+10	dBm
ESD	Human Body Model (Note 2)		2	kV
Tstrg	Storage Temperature	−40	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Time limit at maximum V_{DD} must be less than 100 milliseconds.
2. The RFOUT passes up to 1.25 kV.

DC CHARACTERISTICS

Table 4. DC CHARACTERISTICS (Typical Application Circuit, 50 Ω System Impedance, unless otherwise noted) (V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C) Operating outside the recommended operating ranges for extended periods of time may affect device reliability

Parameter	Description	Min	Typ	Max	Unit
VOLTAGE SUPPLY					
DVDD	Digital DC supply voltage	2.2		3.63	V
AVDD	Analog DC supply voltage	2.2		3.63	V
RFVDD	RF DC supply voltage	2.2		3.63	V
GROUND					
RFVSS	RF Ground Pin	0	0	0	V
AVSS	Analog Ground Pin	0	0	0	
DVSS	Digital Ground Pin	0	0	0	
POR					
POR	POR Ramp Rate	0		0.1	V/msec
CURRENT CONSUMPTION					
IDDS	Standby current		1.2		mA
	Sleep mode		1		μA
TRANSMIT CURRENT					
+10 dBm	V_{DD} = 3.3 V as PA reference		18		mA
RECEIVER CURRENT					
Base Receiver	Clock and data recovery off.		10		mA
Wake−On−Pattern	Part configured with ASK detector, pattern correlator, and clock and data recovery enabled.		10.5		mA
REGULATORS					
Digital Regulator		2.0	2.1	2.15	V
DAC					
Dref	DAC reference voltage	1.95	2	2.025	V
DDNL/INL	Differential non−linearity and integral non−linearity.		0.5	1	LSB
LOGIC INPUTS					
VINH	Input High Voltage	0.7 * DVDD		DVDD	V
VINL	Input Low voltage	0		0.3 * DVDD	V
IIN	Input current (input high/input low)	−1		1	μA
LOGIC OUTPUTS					
VOH	Output high voltage	0.8*DVDD		DVDD	
VOL	Output low voltage	0		0.2*DVDD	

STARTUP TIMING

Table 5. STARTUP TIMING

Symbol	Parameter	Description	Min	Typ	Max	Unit
T_{Ready}	Without Quick−Start	Time from low−power standby to crystal enabled, ready for instruction.		10		ms
	With Quick−Start			30		μs
T_{RX}	Without Quick−Start	Time for receiver startup (does not include data filter setting dependant settling time) from low−power state.		10		ms
	With Quick−Start			120		μs
T_{TX}	Without Quick−Start	Time for transmitter startup, ready for data transmission from a low−power state.		10		ms
	With Quick−Start			120		μs
$T_{RXTX}/T_{RXRX}/T_{TXRX}/T_{TXTX}$		Receive to transmit and transmit to receive switching time and channel switching time.		120		μs

RF SPECIFICATIONS

Table 6. OSCILLATORS CHARACTERISTICS (Typical Application Circuit, 50 Ω System Impedance, unless otherwise noted) (V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C)

Parameter	Description	Min	Typ	Max	Unit
CRYSTAL OSCILLATOR					
Frequency	Crystal oscillator is selectable between 20 MHz or 24 MHz		20 / 24		MHz
INTERNAL IC OSCILLATOR					
Frequency	IC oscillator operating frequency	9.95	10.0	10.05	KHz
Temperature Coefficient				500	ppm/C
PHASE−LOCKED LOOP (PLL)					
PLL Frequency Range	PLL Frequency Range	174		470	MHz
Phase Noise at 10 kHz Offset			−80		dBc/Hz
Phase Noise at 100 kHz Offset			−70		
PLL Lock Time	Using internal loop filter		40		μs

Table 7. RECEIVER CHARACTERISTICS (Typical Application Circuit, 50 Ω System Impedance, unless otherwise noted)
(V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C

Parameter	Description	Min	Typ	Max	Unit
RF Frequency Range	Min frequency is 300 MHz with 24 MHz crystal	260		470	MHz
ON OFF KEYING (BER = 1E−3, FRF = 434 MHz, LNA and PA matched separately)					
Sensitivity	IF bandwidth = 100 kHz. 1 kbps with NRZ encoding		−118		dBm
Sensitivity	IF bandwidth = 300 Khz. 1 kbps with NRZ encoding.		−116		dBm
IF Filter Bandwidth		85 180 260	100 200 300	115 220 340	kHz
IF Filter Center		475	500	535	kHz
Image Rejection			35		dB
CHANNEL FILTERING					
1st Adjacent Channel Rejection	Desired signal (1 kbps OOK), IFBW = 100 kHz, 3 dB above input sensitivity level, CW Interferer power level increased until BER = 10E−3, interferer 100 kHz from desired		25		dB
Co−Channel Rejection			−10		dB
RECEIVED SIGNAL STRENGTH INDICATION (RSSI)					
Range		−120		−60	dBm
RSSI Gain			22.5		mV/dB

Table 8. TRANSMITTER CHARACTERISTICS (Typical Application Circuit, 50 Ω system impedance, unless otherwise noted)
(V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C)

Parameter	Description	Min	Typ	Max	Unit
Transmit Power	V_{DD} = 3.0 V, T_A = 25°C, V_{DD} as PA reference		10		dBm
Power variation vs. Temp			±1		dB
Power variation vs. V_{DD}	Using RFPWR for regulated reference		±1		dB
	Using V_{DD} as the PA reference		+2/ −3.5		

3. Supply current, output power, and efficiency are greatly dependent on board layout and PAOUT match.

Table 9. MODULATION CHARACTERISTICS (Typical Application Circuit, 50 Ω System Impedance, unless otherwise noted)
(V_{DD} = 2.2 V to 3.6 V, T_A = −40°C to 105°C, typical is 3.0 V, T_A = 25°C)

Parameter	Description	Min	Typ	Max	Unit
AMPLITUDE SHIFT KEYING (ASK)					
ASK post detection bandwidth filter		0.6		40	kHz
FREQUENCY SHIFT KEYING (FSK)					
Conversion Gain			2.5 5.0 7.5 10		mV/kHz
FVoff	Input referred frequency offset		20		kHz
FSK Filter Cutoff	Filter cutoff frequency which sets the post detection bandwidth of the receiver		72 36 24 18 12 9 6 3		kHz

INTERNAL BLOCK DIAGRAMS AND DESCRIPTION

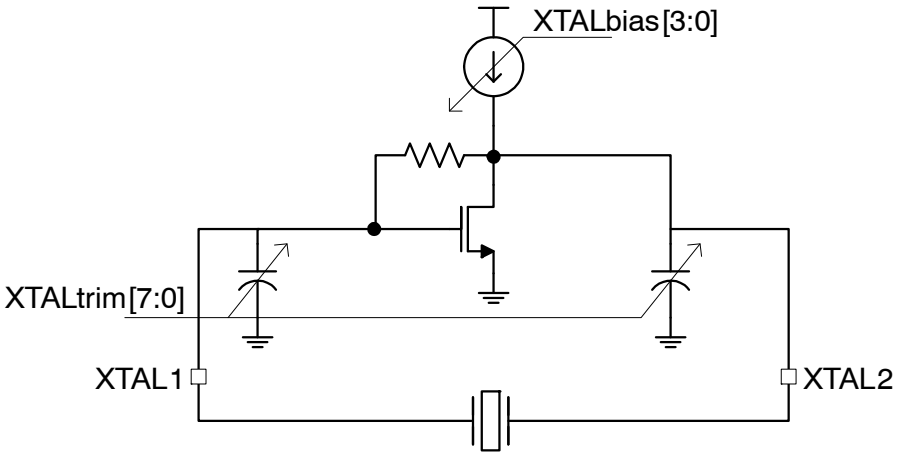


Figure 3. Crystal Oscillator

The internal crystal oscillator circuitry can be used with one of two inexpensive, readily available frequencies: 20 MHz, and 24 MHz. The XTAL Select bit of the General Options register needs to be set correctly based upon the crystal used. An on chip 8−bit capacitive DAC is connected to the crystal pins provide the load caps for the crystal, and allow fine tuning of the crystal frequency. The 8−bit control for the caps is located in the Crystal Trim register. The full scale range for the internal capacitors is 40 pF, the set value should be chosen such that the series value added to any PCB capacitance adds to the load capacitance specified for the crystal.

The current reference for the crystal oscillator amplifier is adjustable via the XTAL Current Trim register. By default, the device is set to 0x8. This provides sufficient gain for crystals with a load specified as 16 pF. For crystals requiring higher values of load capacitance, this setting may need to be increased to ensure reliable startup.

On power−up, the crystal oscillator is enabled, XTALbias is set to 0xF, and the internal load caps are set to 0x40. This ensures proper startup regardless of crystal. Once the device has been powered, then internal state machine will write the values stored in EEPROM for the bias and load−cap trim into the trim registers.

Table 10. CRYSTAL SPECIFICATION

Parameter	Min	Typ	Max	Unit	Notes
Tolerance			50	ppm	
R		20	30		
C	4.4	8.8		fF	
Lm		5	10	mH	The lower the better
C_p			7.0	pF	
C_{load}		10	16	pF	

SYSCLK Output

The NCV53480 can be used to provide a system clock to other external devices for device synchronization. The General Options register contains the control bits for selecting the SYSCLK output frequency.

The output can also be disabled when the NCV53480 is not required to provide a clock output. On power−up or reset, the SYSCLK pin is enabled and defaults to the crystal frequency divided by 160.

Quick−Start Oscillator (QSO)

To save power, and remove timing uncertainty from crystal startup, the NCV53480 includes ON Semiconductor's patented Quick−Start oscillator technology. The Quick−Start oscillator is an internal oscillator trimmed to the crystal frequency. Upon crystal start, the Quick−Start oscillator drives the crystal to quickly build energy in the motional inductance of the crystal, reducing startup time from milliseconds to microseconds.

To use the Quick−Start oscillator, it first needs to be calibrated by writing the Command Register to the Quick−Start Calibration instruction. All of the circuitry for the calibration is on board. During the calibration, the user can poll Status Register A to determine when it has completed by monitoring the Busy bit. After completion, the user should also check the RC/QS calibration bit of Status Register A to ensure the calibration was successful. Once calibrated, the Quick−Start oscillator is automatically enabled and will be used to assist in crystal startup anytime the part transitions from a low power mode to a high power mode. The calibration value is in the Quick Start Trim register, and is stored in EEPROM. The Quick−Start Calibrated bit of the Receiver Trim register stores whether the Quick−Start has been calibrated.

The figure below shows a crystal startup sequence using the Quick−Start oscillator.

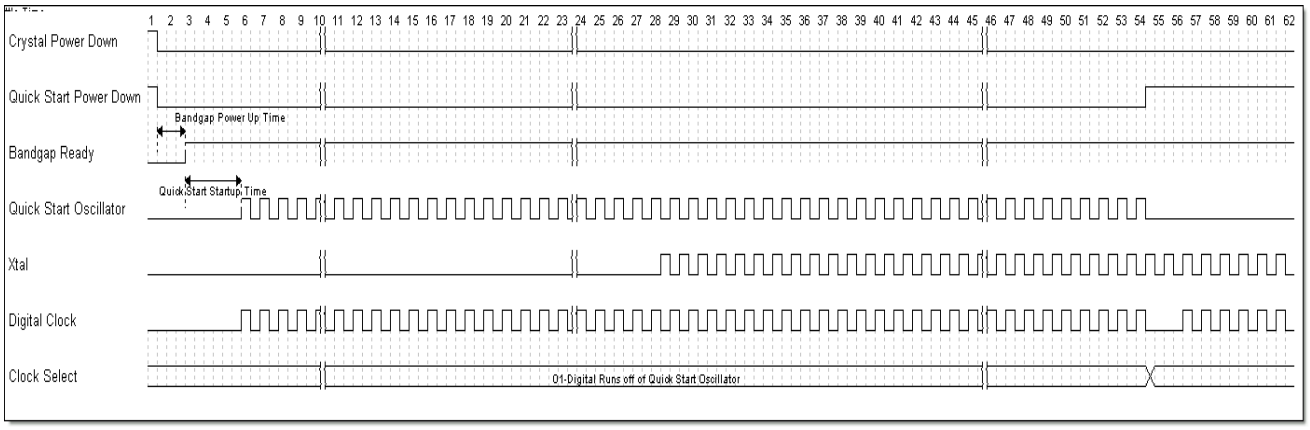


Figure 4. Quick−Start Cycle

To detect that the crystal oscillator has been properly started after a quick start cycle, a frequency and phase detector are utilized. These two detectors operate on the output of the QSO and the output of the crystal oscillator. The frequency detector counts for 400 cycles of the QSO. During that time, a similar counter counts the number of crystal clock cycles. When the QSO counter is finished, if the crystal counter is off by more than 10%, a quick start fail interrupt will occur. The phase detector is a cycle slip phase detector with a slight modification so that it will not trigger until there have been 10 edges of the QSO detected without any edges of the crystal oscillator occurring during that time. The phase detector can be enabled/disabled via bit 1 of register 0x5E.

The outputs of the two counters which form the frequency detector during startup of the crystal oscillator can also be used to adaptively trim the QSO. This is enabled via bit 0 of register 0x5E. When enabled, the output of the crystal counter is used to adjust up or down by one code the trim word for the QSO. If the crystal oscillator counter is greater than the QSO counter, the QSO trim is incremented. Similarly, if the crystal oscillator counter is less, the QSO is decremented. And finally, if they are both 400, no change to the trim is made.

If the adaptive trim function is not used, it is recommended to monitor the temperature sensor and re−calibrate the QSO when the temperature change exceeds 20°C from the last calibration for optimum performance.

A note on the QSO trim register: When the compensation is enabled, the actual trim value presented to the QSO, and the value read from the QSO trim register will differ. Recalibrating the QSO will reset the offset added by the compensation algorithm to 0.

Should the Quick−Start oscillator ever fail to start the crystal, the circuit is disabled and an interrupt is issued to the external controller. Status Register B can be used to determine the cause of the interrupt. In addition to providing an interrupt on fail, the Quick−Start oscillator continues to run in parallel with the crystal oscillator and is used to provide the system clock to ensure the integrity of the whole system. The figure below shows the crystal startup if the Quick−Start oscillator is un−calibrated or if it fails to start.

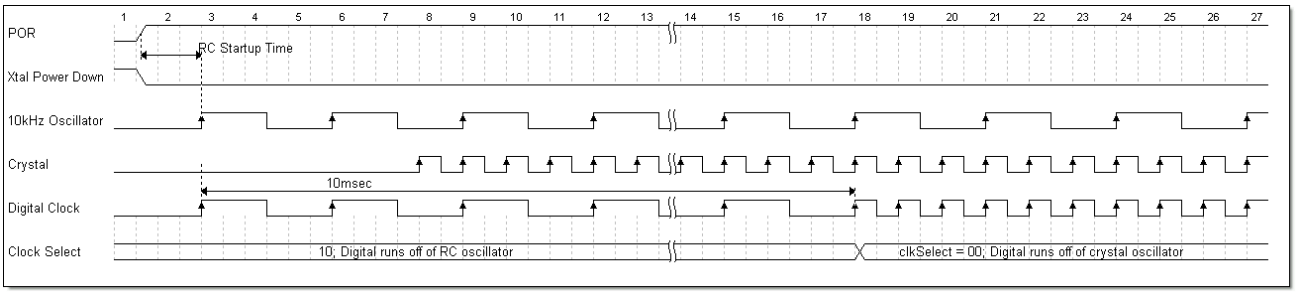


Figure 5. Natural Crystal Startup

10 kHz Oscillator

In addition to the crystal oscillator, a 10 kHz internal IC oscillator is included on chip to provide timing for receiver polling functions in Sniff−Mode. This oscillator is not factory trimmed, so to provide greater accuracy for polling functions, it can be trimmed by writing the Command Register to the RC Calibrate instruction. For applications which require poll timing accuracy better than ±6%, the oscillator should be re−calibrated with changes in temperature.

The 10 kHz Oscillator is calibrated against the crystal frequency to < 0.5% error. The calibration value is in the 10 kHz Oscillator Trim register, and is stored in EEPROM.

Temperature Sensor

An on chip temperature sensor is included in the NCV53480. The analog voltage from the sensor can be pinned out on the AMGPIO pin or using the on−board 8−bit ADC, a digital word can be read from the Temperature ADC register after executing a conversion instruction. The voltage for the temperature sensor is V_{temp} = 1 + (T − 27)/128. The ADC output code for the temperature sensor will be T_{code} = 128 + (T − 27).

To save power, the sensor is not always active. It will be active when one of the following is true:

- The part is in receive
- The Analog Test Mux register is set to output the Temperature sensor voltage on the AMGPIO pin
- An ADC conversion instruction is issued

The sensor offset is factory trimmed at 27°C to ± 1.5C. In addition to the trimmed error, the slope of the sensor is ± 5%.

ADC

The on board 8−bit DAC used for PA output power control and OOK level detection is also utilized to provide an 8−bit SAR ADC. This ADC is used primarily for best channel selection in multi−channel Sniff−Mode, but can also be used to provide a digitized output of the temperature sensor.

To perform a conversion of the temperature sensor without placing the device into multi−channel Sniff−Mode, perform the following:

1. Set any one of bits 1, 2, or 3 to a ‘1’ in either the configuration A or configuration B Sniff Configuration registers
2. Write the Command Register to the ADC conversion command.
3. Read the sensor value in the Temperature ADC register once the conversion is complete

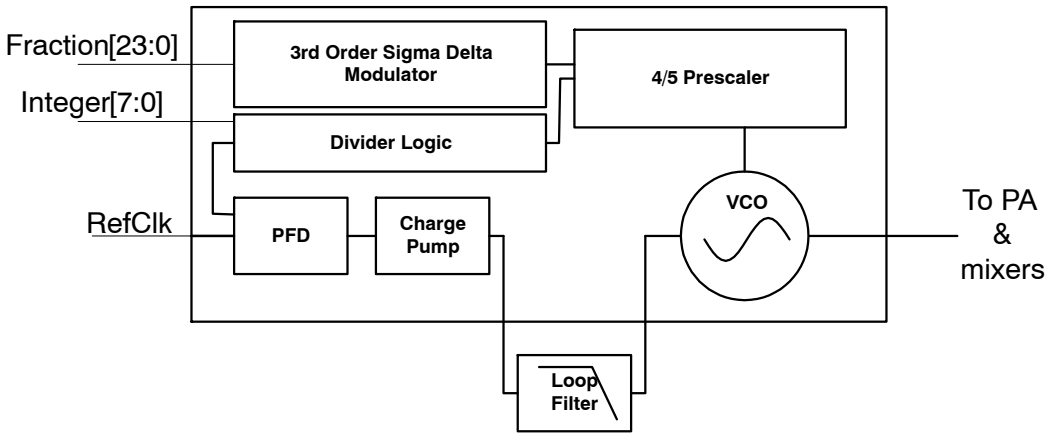


Figure 6. Fractional−N PLL

The NCV53480 uses a Sigma−Delta Fractional−N divider with a ring oscillator to provide continuous coverage of the 280−434 MHz ISM band. The lower frequency limit is 300 MHz with a 24 MHz crystal and 250 MHz with a 20 MHz crystal. In transmit mode, the VCO operates at the RF frequency, and the reference is the crystal frequency. In receive mode, the VCO operates at 2/3 of the RF frequency, and to simplify programming the part, the reference frequency is 2/3 the crystal frequency. This allows the same Integer and Fraction to be used for both receive and transmit, and reduces the number of register writes to switch between transmit and receive to just a single write. The 500 kHz offset for receive is calculated internally.

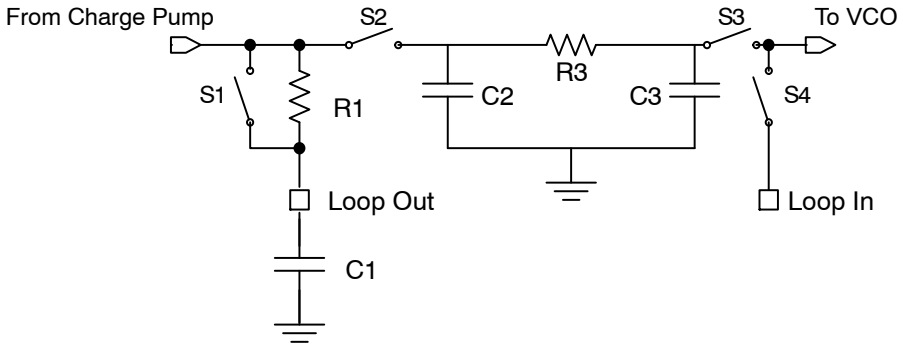


Figure 7. Loop Filter

As shown in Figure 7 above, the loop filter for the PLL can be configured in two ways by setting bit 4 of the RF PLL Trim register. The first is internal mode where S1 and S4 are open, and S1 and S3 are closed. Note that even in internal mode, C1 is still external to reduce total system cost. In external mode, S1 and S4 are closed while S2 and S3 are open allowing complete flexibility in loop filter design.

The table below shows the values of the internal loop filter components and the recommended value for C1 when using internal mode.

Table 11. INTERNAL LOOP FILTER VALUES

Component	R1	C1	C2	R3	C3
Value	1k	2 nF	150 pF	1k	80 pF

The following table provides the parameters of the VCO and charge pump for designing external loop filters.

Table 12. VCO PARAMETERS

Paramter	Kvco	Icp	Fref
Value	800 MHz/V	22.5 μA – 40 μA (Note 4)	$F_{crystal}$

4. Selectable by bits[2:0} of the RF PLL Trim Register

When using the internal loop filter, the charge pump current setting in the RF PLL Trim register should be set according to the following table based on the combination of output and crystal frequency. This will provide a 200 kHz loop bandwidth compatible with the Lock Detection circuitry.

Table 13. CHARGE PUMP CURRENTS

	250 MHz – 300 MHz	300 MHz – 350 MHz	350 MHz– 400 Mhz	400 MHz – 450 MHz
20 MHz	25 μA	30 μA	35 μA	37.5 μA
24 MHz	NA	25 μA	27.5 μA	32.5 μA

When using an external loop filter bandwidth less than approx 100 kHz, the sample time for the lock detection circuit will occur before lock is achieved, and a PLL is Unlocked flag will be set in the Status Register A. See the Lock Detection Section for further detail, and how to disable the lock checking.

Lock Detection

A digital lock detection circuit is built into the NCV53480. The output of this block is used to gate PA operation until the PLL has achieved lock. By default, this circuit is disabled after lock has been achieved. If a PLL loop bandwidth is used which doesn't allow for PLL lock with the default timing of 130 μsec lock will fail and the transmitter will be disabled. To circumvent this, setting the Infinite PLL Lock Time bit in the General Options register will over−ride the lock detect signal, and leave the lock detection on continuously. Pin GPO can be configured to output the lock detect signal for external monitoring using the GPO configuration register.

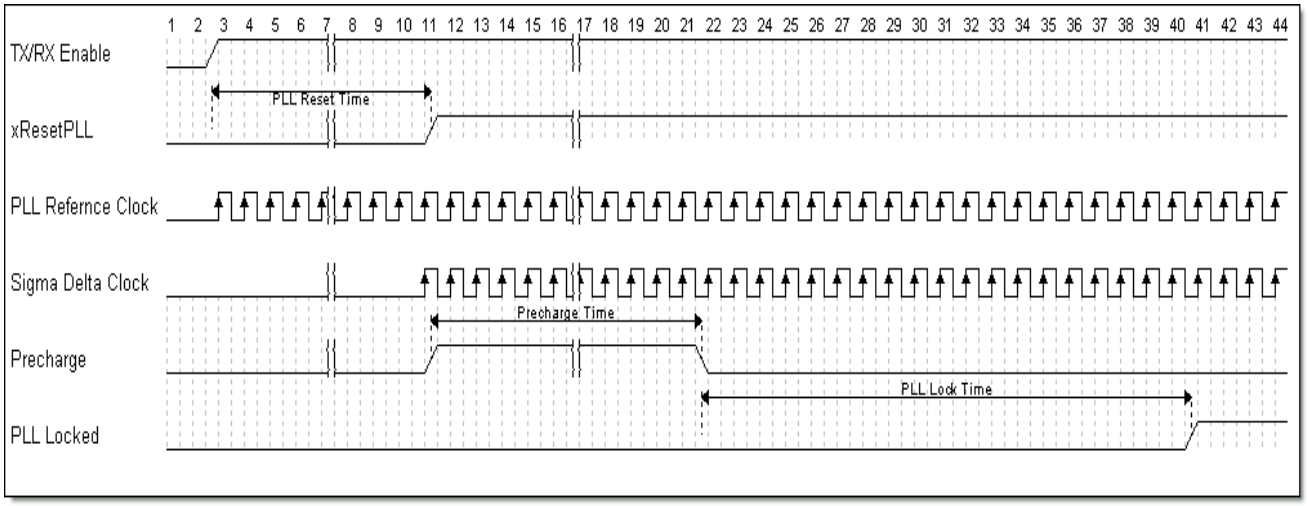


Figure 8. PLL Lock Detect

Transmitter

RF Output

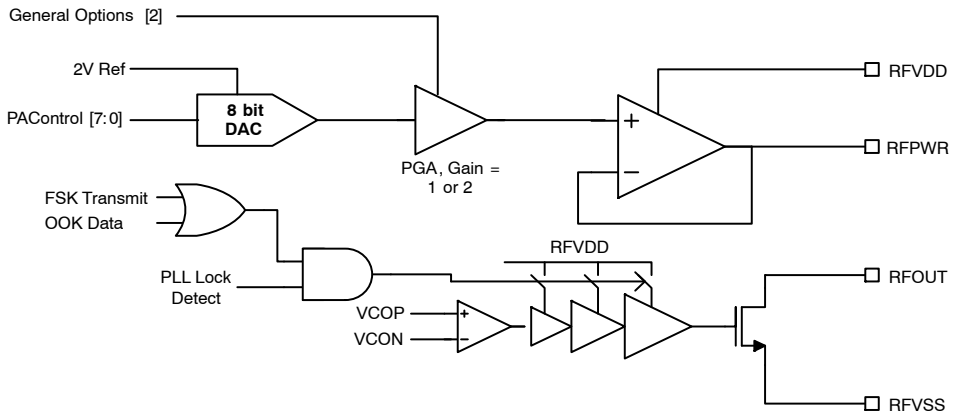


Figure 9. PA Control

The Power Amplifier (PA) of the NCV53480 is a single ended open drain amplifier, which has been designed to deliver up to 10 dBm into a 50 Ω load. The RFPWR pin is used to provide a voltage reference for the PA circuitry, and can be programmed to adjust the output power. The input to the buffer for the RFPWR pin can be either an 8−bit DAC referenced to 2.0 V or the DAC can be run through a 2x buffer allowing voltages up to 3 V on the RFPWR pin. The DAC mode provides a constant voltage over all temperature and voltage conditions, resulting in output power which varies just ±1 dB. The high gain mode, allows for maximum output power and efficiency (10 dBm). When using the 2x gain mode, the RFPWR pin will track V_{DD} if V_{DD} is less than the desired RFPWR voltage setting.

When the device is in receive mode, RFPWR is driven to ground, and the gate of the PA is grounded, facilitating a combined RX/TX match without the need for an external switch.

Asynchronous Transmit

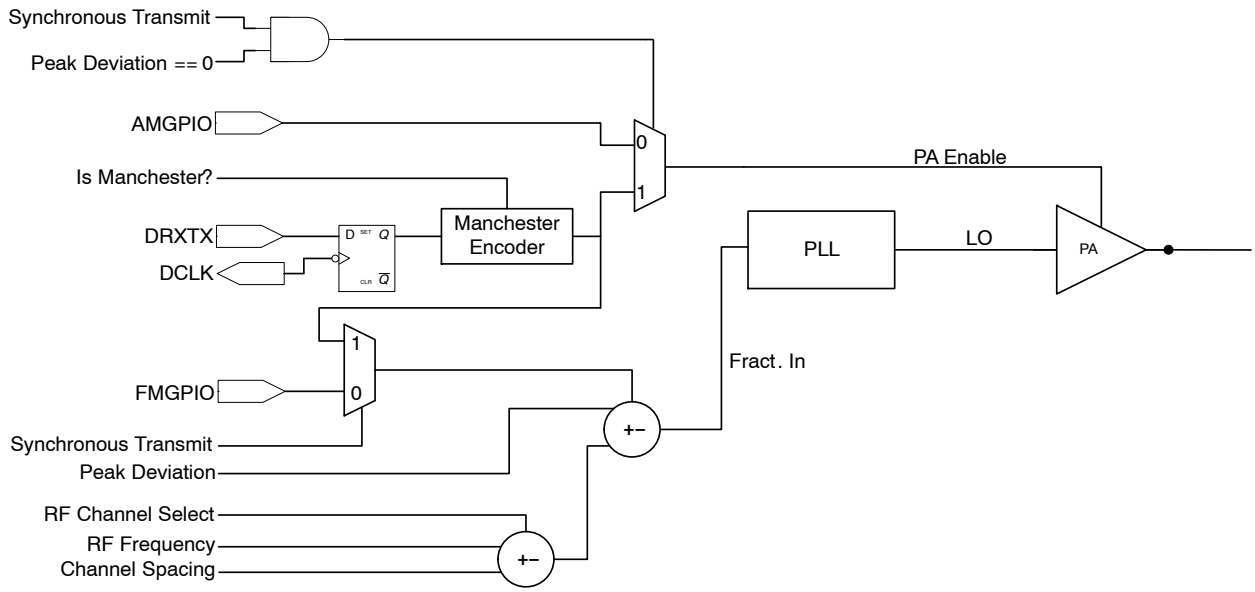


Figure 10. Transmit Control

In asynchronous transmit, the transmit portion of the state machine simply turns on the device with the PLL running, with the AMGPIO and FMGPIO pins configured as inputs. The AMGPIO pad controls the PA enable and the FMGPIO controls the frequency word into the PLL. For AM only transmit, the Peak Deviation register should be set to zero and the FMGPIO pin can be driven high, low or left floating (an internal pull−up is enabled). For FM only transmit, the AMGPIO pin should be driven high to enable the PA. For simultaneous transmit, the AMGPIO and FMGPIO can toggle independently of each other, but the PA will only be enabled when the AMGPIO is driven to a ‘1’. In asynchronous transmit the DCLK will be driven to a ‘1’, signifying when the PLL has gained lock.

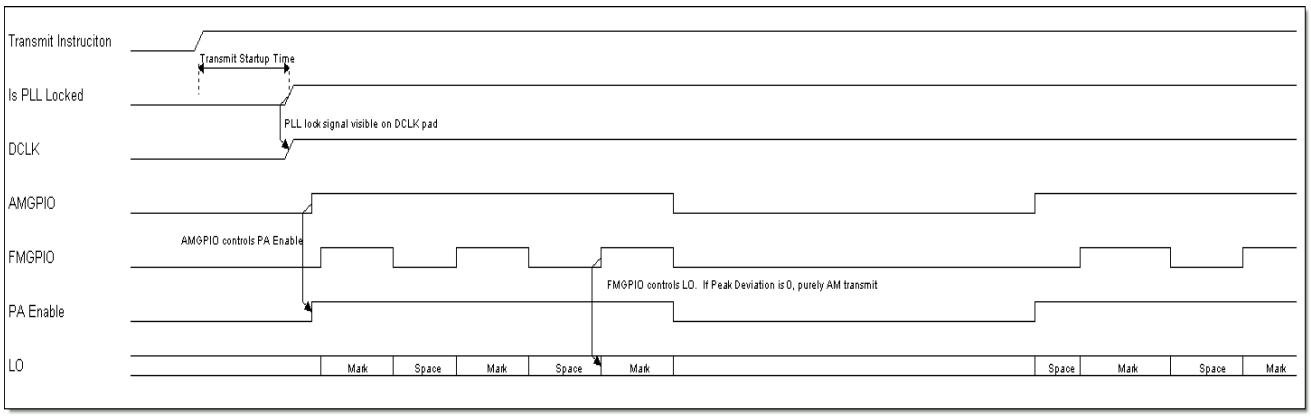


Figure 11. Asynchronous Transmit

Synchronous Transmit

In synchronous transmit the NCV53480 will provide a baud clock on the DCLK pin. The external micro−controller can use this pin to time the data rate, without the use of additional timers. In this mode of operation simultaneous OOK and FSK transmit is not supported. If the Peak Deviation register is zero then OOK modulation is assumed. If the Peak Deviation register is non−zero then FSK modulation is assumed. The below figures show synchronous OOK and synchronous FSK transmit. An internal state machine handles the necessary Manchester encoding, if Manchester is enabled via the Payload Encoding bit in the Transceiver Options register.

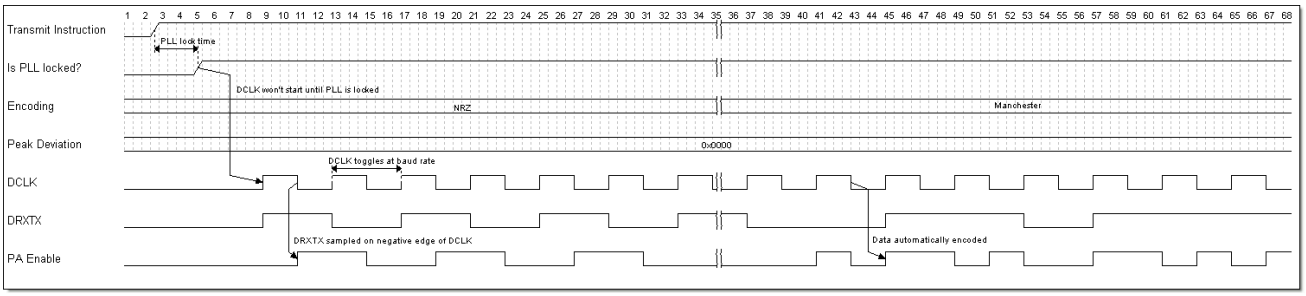


Figure 12. Synchronous OOK Transmit

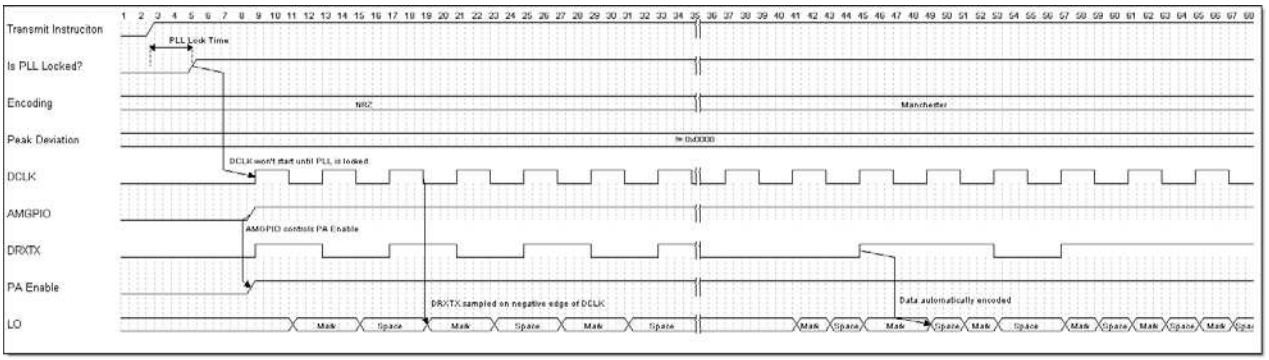


Figure 13. Synchronous FSK Transmit

Receiver

The NCV53480 is a fully monolithic image reject low−IF receiver. The low IF architecture saves considerable power, while the absence of the DC correction necessary for zero−IF reduces timing complexity and permits OOK modulation. The receiver provides outputs to an FSK detector, and an OOK detector.

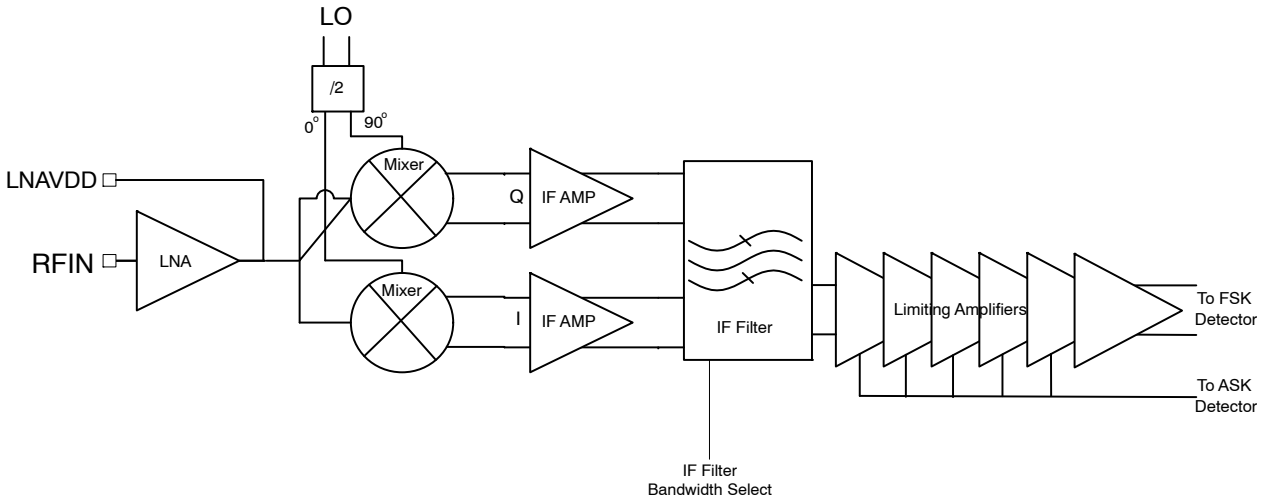


Figure 14. Receive Chain

The single ended LNA is followed by dual mixers, which perform a quadrature down conversion. The LNA is a common gate amplifier requiring a DC path to ground external to the device. The output of the LNA is connected to the pin LNAVDD. This pin should be connected to V_{DD} through an appropriately sized inductor for maximum sensitivity. See the RX/TX Matching Section for matching specifications. For reduced cost/performance, this pin can simply be connected to V_{DD} through a 1 kΩ resistor.

IF Filter

Following the first IF amplifiers, a complex (I,Q) bandpass filter provides both image reject, and channel selection. This filter has selectable bandwidths of 100 kHz, 200 kHz, and 300 kHz and is set by the IF Bandwidth bits of the Receive Options register. The filter roll−off is equivalent to a 5th order low−pass filter centered at the IF frequency of 500 kHz.

Limiting Amplifiers and RSSI

The limiting amplifiers which follow the IF channel selection filter also provide a log−linear current output which is summed onto a resistor to provide a RSSI voltage output. The analog RSSI output is available on the AMGPIO pin, and is fed to the OOK demodulator for data slicing. The digital level output of the limiting amplifiers is fed directly into the FSK detector.

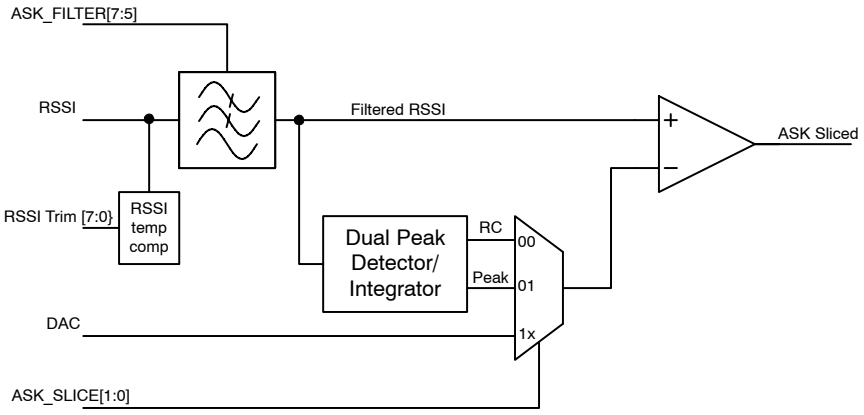


Figure 15. OOK Detector

OOK detection is done using full wave current output rectifiers in each stage of the log amp. These currents are summed onto an internal resistor to create the RSSI signal. The RSSI signal is then filtered and fed into the positive input of the data slice comparator. The reference input to the comparator can be either a DC level from the DAC, a RC integrated version of RSSI, or the midpoint of a dual peak detector. Both the filtered RSSI and the sliced data are available on the AMGPIO pin using the AMGPIO Configuration bits in the Receive Options register.

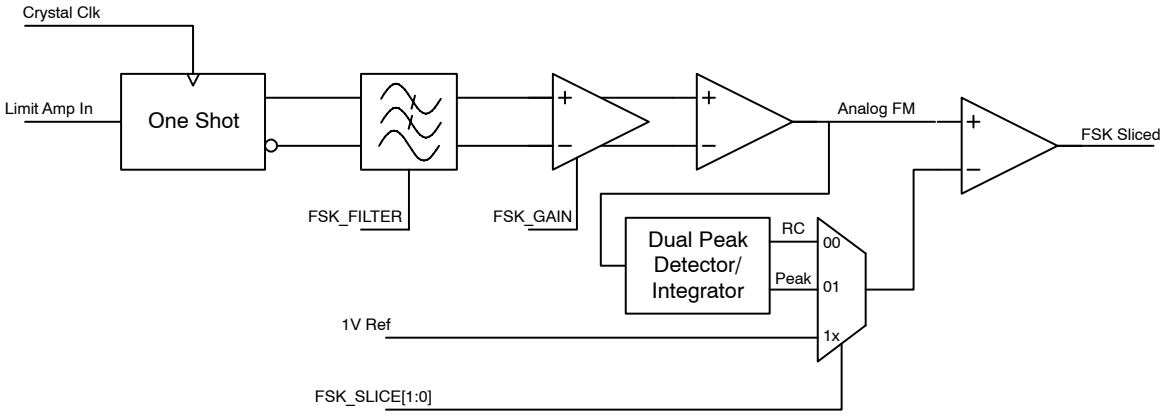


Figure 16. FSK Detector

For FSK detection, the IF signal is limited, and then fed to a one−shot detection block. The output of the one shot discriminator is then filtered by a 3rd order Chebyshev filter, and can then be amplified through the FSK gain block. Finally, data is recovered by comparing the output of the detector to one of three selectable references: 1 V reference (representing the RF frequency center), the mid point of a dual peak detector, or to an RC integrator. Both the discriminator output and the sliced data are available on the FMGPIO pin using the FMGPIO Configuration bits in the Receive Options register.

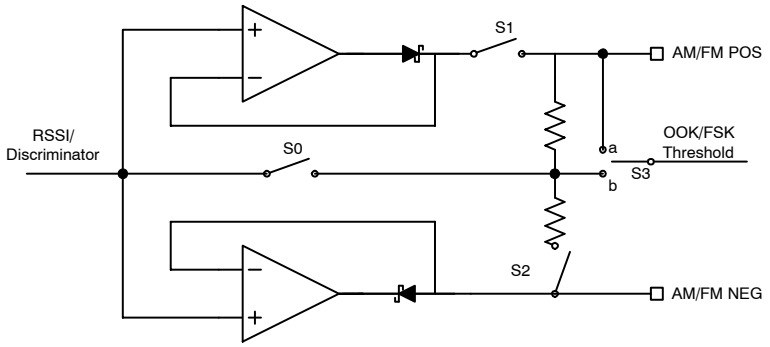


Figure 17. Dual Peak Detector/Integrator

The dual peak detector and integrator in both the OOK and FSK detection blocks are identical. The figure above illustrates the circuitry in this block. In the case where dual peak detection is used to set a threshold at the midpoint of the positive and negative peaks on the output of the detector, S1 and S2 are closed, and S3 is switched to position “b”. The simple resistive divider between the two peak detectors determines the threshold output. For this mode of operation, the capacitors should be sized at 2*TL/1M, where TL is the longest period of no data change, and 1M is the size of the internal resistors.

For RC integrator mode, switch S0 is closed, and S3 is switched to position “a”. The threshold is then simply a low pass version of the input signal. For optimal operation, the capacitor value for this configuration should be chosen to be 3*TL/1M, where TL is again the longest period of no data change.

FSK Squelch

Bit 2 of register 0x5E is used to enable the FSK Squelch function. This function will gate operation of the FSK detection circuitry until RSSI exceeds the threshold programmed in the energy threshold register (0x16, 0x36). A block diagram of this functionality is shown below. Note, the Energy Threshold register setting is common to both this function and the OOK detector when using the programmable DAC setting as a threshold for the OOK slick comparator.

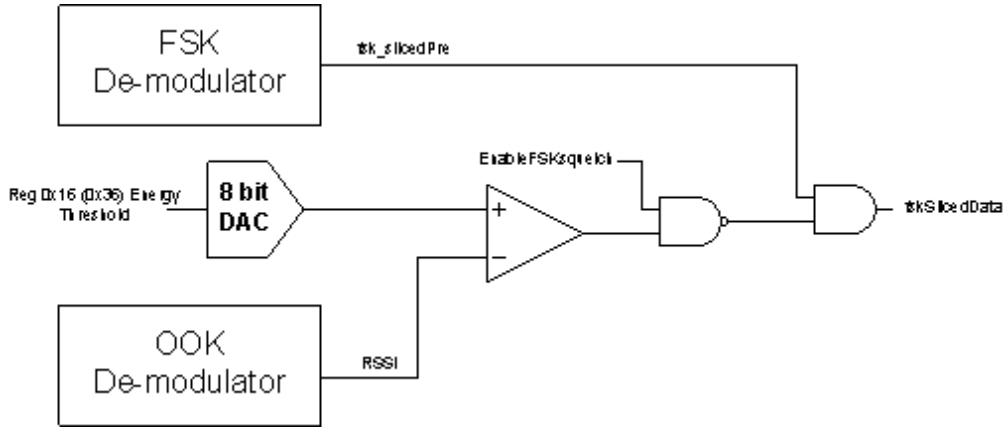


Figure 18.

Receiver Configuration

The NCV53480 receiver's level of autonomy can be configured from simple receiver providing continuous analog outputs to intelligent receiver buffering packets and issuing interrupts to an external controller.

From the top level, the receiver contains two available configurations, Configuration A and Configuration B. These configurations are completely independent from one another, for example, Configuration A can setup the receiver for OOK data detection at 1 kbps Manchester, and Configuration B can setup for FSK at 18 kbps. Further, Configuration A could setup the radio to search for a specific pre−amble, and once found qualify a Chip ID, buffer in 64 bits of data then interrupt an external controller, while Configuration B could simply put the radio in a state where the FM discriminator analog output is available to an external controller on the FMGPIO pin.

Further automation and power reduction of the NCV53480 is achieved by using Sniff−Mode. In Sniff−Mode 3 timers are available:

1. Control receive interval with the settings of Configuration A
2. Control receive interval with the settings of Configuration B
3. How often to do a clear channel assessment.

Additional timers in Sniff−Mode determine the length of time the receiver stays active in either Configuration A and Configuration B.

Note: The following sections apply to both Configuration A and Configuration B.

Receive Mode

The Receive Mode bits in the Transceiver Options register determine the way the receiver will operate. With these bits set to 00, the device will enter normal receive, the selected detectors will be enabled, and if enabled recovered clock and data will be available. All output will be continuous in this state until another command is issued.

Wake−On−Energy

Setting the Receive Mode bits to 01 enables Wake−On−Energy mode. With this mode enabled, the device can issue an interrupt to an external controller upon receiving a signal with RSSI energy greater than the value specified in the Energy Threshold register. When Wake−On−Energy is selected, the Receive Dwell Timer register determines how long the receiver will stay active looking for energy to surpass the energy threshold. When setting the Receive Dwell Timer to 0x00 the receiver will impulse sample for energy. Using this mode of operation with the Receive Dwell Timer set to impulse sample minimizes the receiver on time.

The clock and data recovery block, if enabled, is initially off in Wake−On−Energy mode. Once a threshold has been achieved, the CDR is then enabled. Additional functionality is available once the Wake−On−Energy mode has been selected. Upon finding energy greater than the threshold, the part can then begin searching for a specified Chip ID (CDR must be enabled). This pattern can be up to 32−bits long in Wake−On−Energy mode and is the concatenation of the Wake Pattern and Chip ID registers. The length of the pattern to search for is set in the Pattern and ID Length register. The Code Dwell Time register controls how long the device stays on looking for the pattern after energy has been found. If this timer expires the device returns to Sniff mode. If the pattern has been found, an interrupt can be issued to an external controller to handle the payload data on the DCLK and DRXTX pins. Alternatively the NCV53480 can automatically buffer in the next N bits, where N is set by the Packet Length register. If buffered packet is enabled (anything non−zero in Packet Length register), the interrupt to the external micro−controller will occur after buffering in the packet.

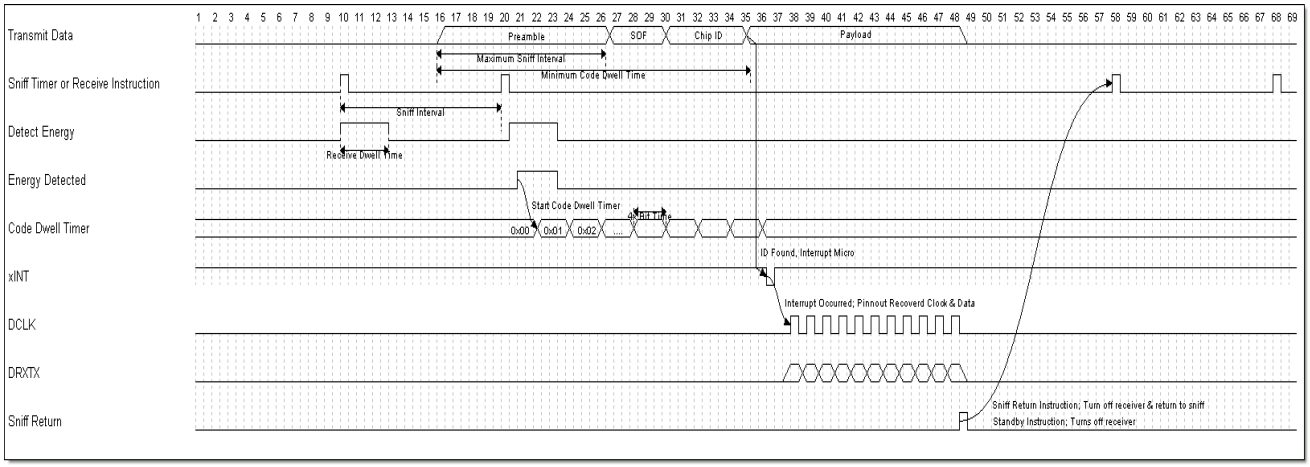


Figure 19. Wake−On−Energy

Wake−On−Pattern

In this mode of operation, enabled by setting Receive Mode bits to 10, the NCV53480 uses an over−sampling operation to find a sequence of bits matching the pattern in the Wake Pattern and Chip ID registers. The Pattern and ID Length register is used to set the length of pattern(s) the part will look for, and the Pattern and ID Threshold register is used to set how well each bit must match the expected. Setting this threshold low can result in false wake−ups, while setting it high will result in reduced sensitivity for Wake−On−Pattern functions. Section Pattern and ID Correlator explains, in detail how this correlation functionality operates.

It is possible to set up the part in this mode in two different ways. The first is to simply find a single sequence with a length from 1 to 16 bits. The second is to find a sequence matching the value in Wake Pattern register, and then after some time find a sequence matching the Chip ID register. The later mode of operation is useful for first finding a repeating pre−amble, and then qualifying a Chip ID before either buffering in the packet or interrupting an external controller.

There are two timers used in Wake−On−Pattern Mode. The first is the Receive Dwell Timer which functions similar to the way it does in Wake−On−Energy mode. It determines how long the receiver should stay active searching for the Wake Pattern. The second timer, Code Dwell Timer, starts once the wake pattern has been found, and determines how long the receiver will stay active looking for the chip id. If the wake pattern is a long repeating preamble such as 1001001001. and the part is configured to look for 1001, each time the device finds the wake pattern, the code dwell timer is reset. In this way, it is possible for the receiver to stay active during long pre−ambles waiting for the chip id to arrive. If both timers time out before finding its target, the part will return to Standby mode.

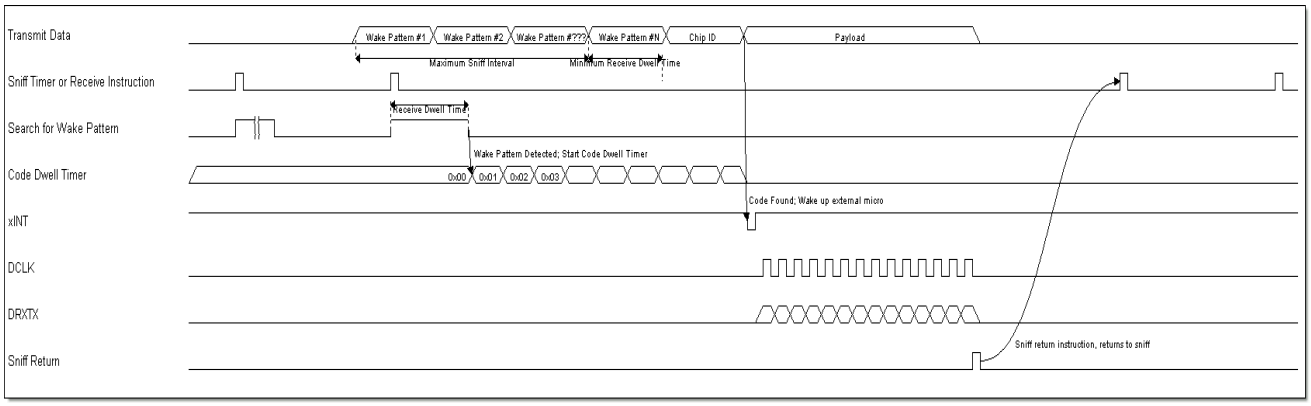


Figure 20. Wake−On−Pattern

Sniff−Mode

In the preceding sections describing Wake−On−Energy and Wake−On−Pattern, it was noted that the receiver simply returns to a low power state should the receiver not find the desired signal before the associated timers expired. Sniff−Mode configures the receiver to automatically return to receive mode at a specified interval, greatly reducing the burden on the external controller, and also reducing overall power consumption.

So as an example: Configuration A is configured to stay on for 10 ms (Receive Dwell) searching for a 5 bit Wake Pattern. By writing the Command register to the Receive Instruction, the part will enable the receiver and look for the wake pattern. If after 10 ms the wake pattern has not been found, the part will simply return to Standby and the controller will need to issue the next command. If however the Configuration A: Sniff Configuration register has been set to 0x03, and the Command register is written to the Sniff−Mode Instruction, the part will similarly enter receive and look for the wake pattern, the difference being that if after 10 ms the wake pattern has not been found, the part will automatically re−enable the receiver at an interval determined by the Configuration A Sniff Interval without intervention from the external controller.

Upon finding either, or both depending on configuration, the wake pattern and chip id the device will issue an interrupt to the external controller. Alternatively the NCV53480 can be configured to buffer in the next N bits as determined by the Packet Length register before issuing an interrupt.

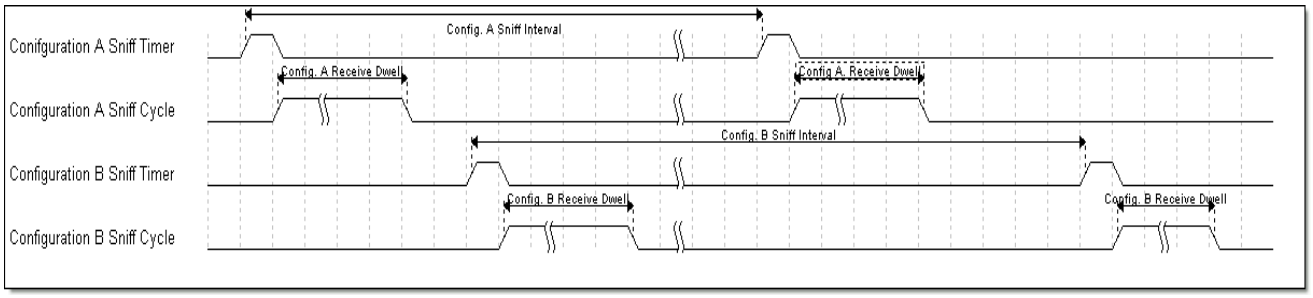


Figure 21. Sniff Cycles

The figure above shows an indicative timing diagram for Sniff−Mode with both Configuration A and Configuration B enabled. Note that Configuration A and Configuration B Sniff Intervals and Receive Dwell values are independent. Note in the timing diagram only the intervals and receive dwell timer are shown, not the chip id dwell, nor the payload receive portions.

Dual Configurations in Sniff−Mode

Using Sniff−Mode, it is possible to have the receiver autonomously enter receive using both the Configuration A and Configuration B device configurations. The NCV53480 has independent Sniff−Mode Configuration registers for Configuration A and Configuration B allowing the two to operate independently from one another. So the radio can be setup to enter receive mode every 20 ms using Configuration A, and also enter receive every 10 seconds using Configuration B.

When a collision occurs between the Configuration A and Configuration B Sniff−Mode timers, Configuration A always has precedence, and the Configuration B timer will be queued until after Configuration A completes its cycle.

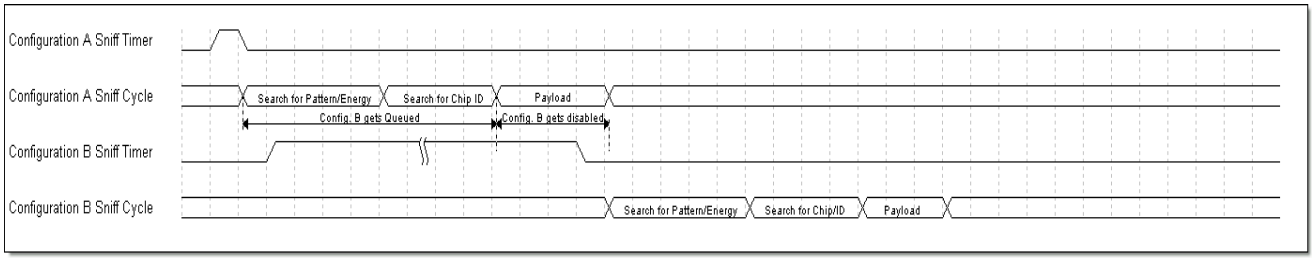


Figure 22. Configuration B Queued

The figure above shows that if the Configuration B Sniff timer overflows while Configuration A is active searching for either energy in Wake−On−Energy mode, or searching for the wake pattern in Wake−On−Pattern mode, then Configuration B will be queued until Configuration A has completed. If Configuration A receives a valid payload during this time, then Configuration B will be disabled such that the receive buffer is not corrupted by the Configuration B Sniff Cycle.

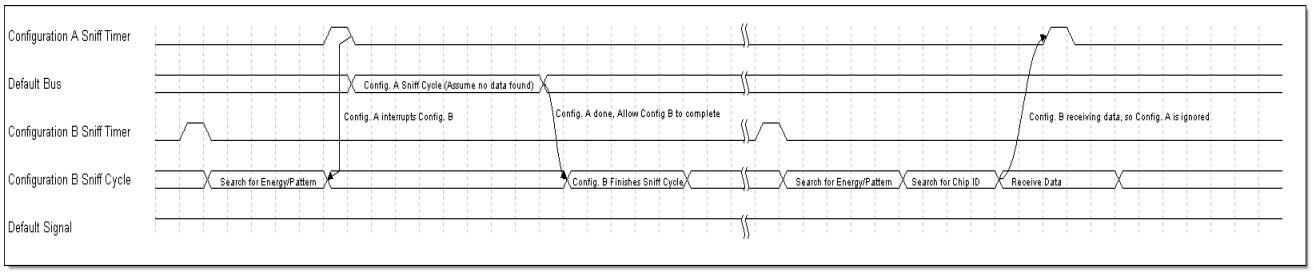


Figure 23. Configuration B Interrupted

If the Configuration A Sniff timer overflows while Configuration B is active searching for either energy in Wake−On−Energy Mode or searching for the wake pattern in Wake−On−Pattern mode, then Configuration A will interrupt the Configuration B Sniff cycle. If Configuration A completes its Sniff cycle without receiving a payload then Configuration B will re−start once Configuration A is complete.

If the Configuration A Sniff timer overflows while Configuration B is actively receiving data, such that Configuration B detected energy in Wake−On−Energy mode or the wake pattern in Wake−On−Pattern mode, then Configuration A will be disabled such that the receive buffer will not be corrupted by the Configuration A Sniff Cycle.

Multi−Channel Operation and Best Channel Selection

The NCV53480 also contains the ability to use multiple channels in both regular receive, and in Sniff−Mode. The channels are defined as ± Channel Spacing from the programmed RF Frequency. For a regular receive instruction, the desired channel is selected by the RF Channel Select bits of the Command register. For Sniff−Mode, the desired channel can be selected in one of two ways:

- Explicitly by enabling just a single Channel Enable bit in the Sniff−Mode Configuration register.
- On the fly by having the radio scan up to three channels and selecting the channel with the lowest noise floor.

When more than one channel is enabled in the Sniff−Mode Configuration register, the radio enables the ADC Poll Timer to automatically scan the enabled channels and select the one which has the lowest noise floor. The channel with the lowest noise floor is then used for all Sniff−Mode cycles until the next event on the ADC Poll Timer. This is not to say that Configuration A and Configuration B cannot operate on separate channels.

Example #1: If channels 1, 2, and 3 are enabled for Configuration A, and only channel 2 on Configuration B, when the Configuration A Sniff−Mode timer expires, it will go into receive mode on the channel with the lowest noise floor determined by the previous noise floor detection cycle. When the Configuration B Sniff−Mode timer expires, Configuration B will always operate on channel 2.

Example #2: Channels 1 and 2 enabled for Configuration A and channels 2, and 3 enabled for Configuration B. After the noise floor detection is completed, it is determined that channel 1 has the lowest floor, followed by 2, and finally 3. In this case Configuration A will operate on channel 1, and Configuration B will operate on channel 2.

Clock and Data Recovery

The Clock and Data Recover (CDR) is implemented using an All Digital Phase Lock Loop (ADPLL). The CDR uses an ADPLL to process the output from the FSK or ASK demodulator circuits to recover a clock signal, and provide a low jitter data output. This module is used for pattern detection and payload recovery. The CDR can recover data from 1 kbps to 60 kbps. In addition to the classical PLL for clock recovery, a fast phase alignment (FPA) feature allows the part to quickly acquire a coarse phase lock with the incoming data. This feature makes it possible to accurately acquire on as few as 4−bits.

To enable the receiver to quickly acquire lock on an incoming data stream, a fast phase alignment feature is implemented which will aid in acquisition by making a coarse phase adjustment to the PLL loop when a programmed sequence is initially detected from a sleep state. This sequence is set by the Start Detect Pattern register. While in an off state, only a minimum of the digital circuitry is enabled to look for the Start Detect Pattern to conserve power. This FPA functionality is only used in Wake−On−Energy mode.

In Wake−On−Pattern mode a separate correlator is used in which is clocked at 8x the set Data Rate. Once the incoming data reaches the threshold for the correlator, the full circuitry for the CDR operation is enabled, and the output phase is adjusted to be within 45 degrees based on the correlation. The start signal goes high, and can be used to gate the recovered clock signal.

Pattern and ID Correlator

The pattern correlator block uses the inputs from the Wake Pattern registers or the Chip Id registers to look for a specific sequence. Each bit set in the pattern/ID register is compared against the over sampled output of the selected demodulator. The output of the demodulator is sampled at 8x the data rate specified in the Data Rate registers.

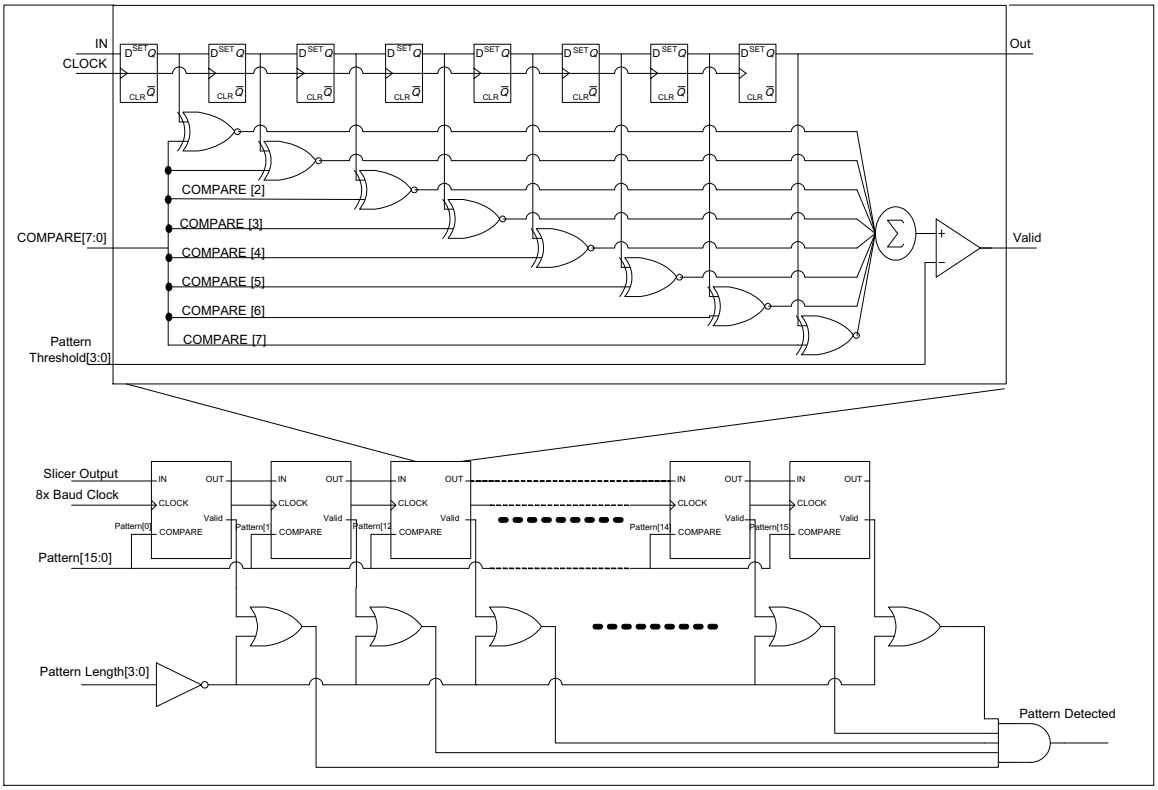


Figure 24. Pattern Correlator

The schematic above illustrates the basic blocks of the correlator. Each bit for comparison utilizes an 8−bit shift register feeding a bank of xnor gates, the other inputs of which come from either the Wake Pattern or Chip Id registers.

The COMPARE word for comparison is determined by the line code format chosen. The wake pattern encoding is specified by the Wake Pattern Encoding bits in the Pattern and ID threshold register. The chip id encoding is specified by the Payload Encoding bit in the Transceiver Options register. The following table shows what COMPARE[7:0] will be for the different line codes.

COMPARE [7:0]

RZ 1	1	1	1	1	0	0	0	0
RZ 0	0	0	0	0	0	0	0	0
Manchester 1	1	1	1	1	0	0	0	0
Manchester 0	0	0	0	0	1	1	1	1
NRZ 1	1	1	1	1	1	1	1	1
NRZ 0	0	0	0	0	0	0	0	0

Data In	1	1	0	1	0	0	0	1
Manchester 1	1	1	1	1	0	0	0	0
XNOR	1	1	0	1	1	1	1	0
SUM								6

Data is a Valid '1' if the Threshold is 6 or less

Figure 25. Correlator Encoding

The outputs of the xnor gates are then summed and compared to the threshold set in the Pattern and ID threshold register. An example is given in the table above: The input data from the demodulator is shown in the top row, the COMPARE value for the example is a Manchester ‘1’. The XNOR row shows the outputs of the xnor gates, the sum of which is 6, so for thresholds of 6 or less, the correlator will treat this input data as a valid ‘1’. For threshold of 7 the correlator will treat this as not correlated.

The final operation of the correlator is to AND all of the bit ‘valid’ signals. The number of bits to use in the correlator for either the wake pattern or the chip id is determined in the Pattern and ID length register.

Once a pattern has been detected, the block continues correlation of the wake pattern word, but then also begins looking for the chip id word. If correlation with the pre−amble is lost, and a chip id has not been found, the device returns to low power mode. An interrupt can be programmed to wake an external micro−processor after either the chip id word has been found or the ASIC has buffered in the packet.

In normal receive mode, the correlator will run continuously when enabled. In Sniff−Mode mode, however, because it is desirable for power consumption to have as short an on time as possible, and because the radio can and will wake up in the middle of a pre−amble out of phase with the programmed value, the contents of the incoming data shift register are circulated around the shift register to check for correlation prior to returning to sleep. This can be shown by the following:

Wake Pattern programmed to: 10000110

Incoming data at end of Sniff−Mode: 00110100

At the end of the Sniff−Mode cycle, the incoming data will be rotated through for comparison:

00110100 → 00011010 → 00001101→ 10000110. Which results in correlation with the desired wake pattern, and the radio will remain on searching for the chip id.

Device Reset and POR

The NCV53480 contains a POR and brownout POR function. After power is applied to the device and the supply exceeds the brownout threshold of 1.4 V, the internal reset for the chip will release < 80 ms later. During this time, the xReset pad will be held low. At any time during operation, if the supply dips below the 1.4 V threshold for the brownout POR, the part will be reset, and xReset will be pulled low. A small counter using the RC oscillator as its source guarantee the pulse width for the reset will nominally be between 100 μs and 200 μs.

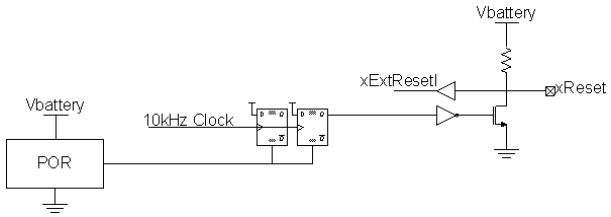


Figure 26.

In addition to the POR and brownout detectors, there are two methods to reset the NCV53480:

- xReset: Pulling the xReset pin low will reset the device with the exception of the digital control for the crystal oscillator and QSO control logic. This is to prevent the need to wait for the 10 ms crystal oscillator start−up timer after a reset.
- I^2C Serial Command: Issuing a serial reset command will reset the chip, inclusive of the oscillator logic, but does not reset the I^2C interface itself. If for some reason the serial interface were to become hung, such as by an external controller terminating a read mid−way through, the I^2C interface can be reset using the xReset.

I^2C Interface

The I^2C interface for the NCV53480 is compatible with standard and fast modes of operation. A control byte is the first byte received following the start condition from the master device. The control byte consists of a 7−bit device address and 1−bit command for read or write. For the NCV53480, the device address is '0110100' binary. The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. Following the start condition, the NCV53480 monitors the SDATA line checking the device type identifier being transmitted. Upon receiving its device address, the NCV53480 outputs an acknowledge signal on the SDATA line. Depending on the state of the R/W bit, the NCV53480 will select a read or write operation.

Single Register Write

Following the start condition from the master and the device address, the R/W bit, which is logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a register address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the register address to be written to. After receiving another acknowledge signal from the NCV53480, the master device will transmit the data word to be written, and the NCV53480 will acknowledge again. The write cycle ends with the master generating a stop condition. Figure 27 shows a pseudo−timing diagram for a single register write.

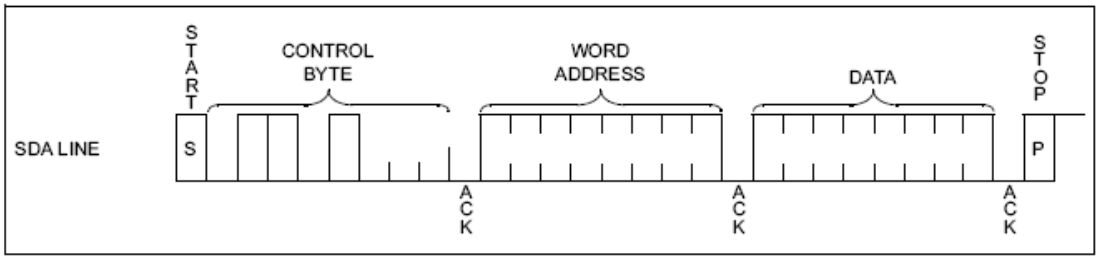


Figure 27. I^2C Single Register Write

Sequential Register Write

The write control byte, register address and first data byte are transmitted to the NCV53480 in the same way as in a byte write. However, instead of generating a stop condition, the master can continue to write register locations. Upon receipt of each word, the address is internally incremented by 1. If the master should transmit more words than the NCV53480 has address locations, the address will roll over. Figure 28 shows a pseudo−timing diagram for a sequential register write.

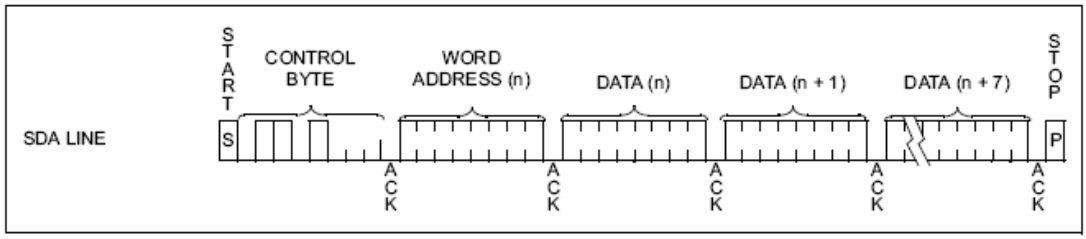


Figure 28. Sequential Register Write

Single Register Read

The single read operation allows the master to access the contents of any register in the device. The process to do so combine a portion of a single register write with a current address read. The sequence of operations is to send a start followed by device address and the R/W set to ‘0’ as in a write sequence. The address to read from is sent following an acknowledge from the slave. After the slave acknowledges the register address, the internal address counter is set to N, and to read the contents of the register, the same procedure for current address read is followed. Figure 29 shows a pseudo−timing diagram for a single register read.

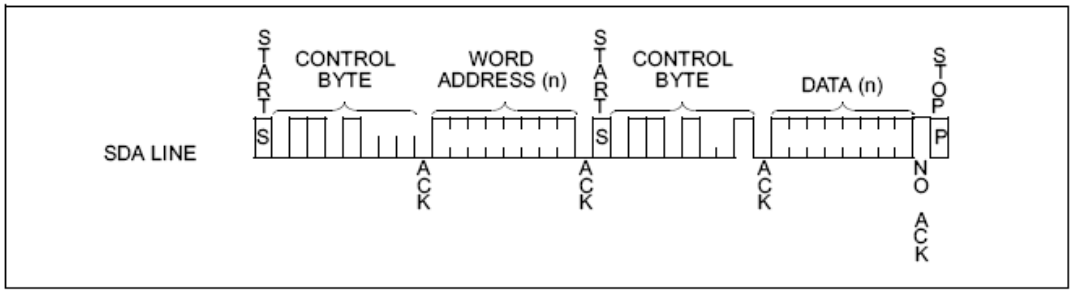


Figure 29. Single Register Read

Sequential Read

Sequential reads are performed in the same was as a random read, except that after the slave has transmitted the first data byte, the master issues an acknowledge, and not a stop bit. The acknowledge instructs the slave to transmit the contents of register N+1. After the master has received the contents of register N+X, the last register to be read, the master does not issue an acknowledge, and generates the stop bit. Figure 30 shows a pseudo−timing diagram for a sequential register read.

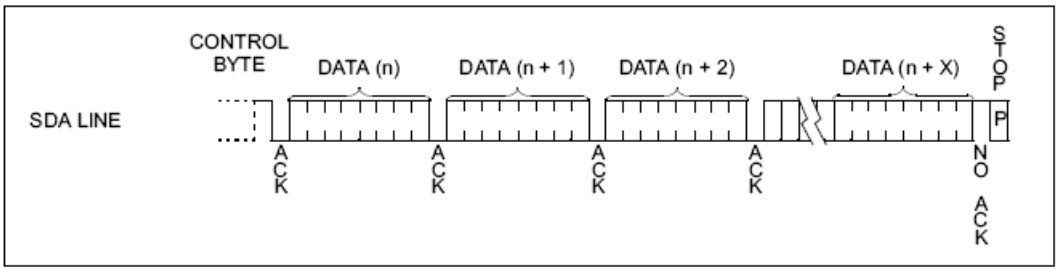


Figure 30. Sequential Register Read