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NCV70627

Micro-stepping Motor Driver

ON Semiconductor®

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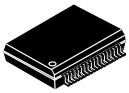
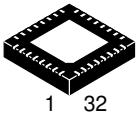


SSOP−EP
36 LEAD
CASE 940AB



QFN32, 5x5
CASE 488AM

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

Introduction

The NCV70627 is a single−chip micro−stepping motor driver with position controller and control/diagnostic interface. It is ready to build dedicated mechatronics solutions connected remotely with a LIN master.

The chip receives positioning instructions through the bus and subsequently drives the motor coils to the desired position. The on−chip position controller is configurable (OTP or RAM) for different motor types, positioning ranges and parameters for speed, acceleration and deceleration. The NCV70627 acts as a slave on the LIN bus and the master can fetch specific status information like actual position, error flags, etc. from each individual slave node.

An integrated sensor−less step−loss detection prevents the positioner from loosing steps and stops the motor when running into stall. This enables silent, yet accurate position calibrations during a referencing run and allows semi−closed loop operation when approaching the mechanical end−stops.

The chip is implemented in I3T50 technology, enabling both high voltage analog circuitry and digital functionality on the same chip. The NCV70627 is fully compatible with the automotive voltage requirements. Due to the technology, the device is especially suited for use in applications with fluctuating battery supplies.

PRODUCT FEATURES

Motordriver

- Micro−stepping Technology
- Sensorless Step−loss Detection
- Peak Current up to 800 mA
- Low Temperature Boost Current up to 1100 mA
- Programmable Current Stabilization Phase
- Fixed Frequency PWM Current−control
- Automatic Selection of Fast and Slow Decay Mode
- No External Fly−back Diodes Required
- Compliant with 14 V Automotive Systems

Controller with RAM and OTP Memory

- Position Controller
- Configurable Speeds and Acceleration
- Input to Connect Optional Motion Switch

LIN Interface

- Physical Layer Compliant to LIN rev. 2.0. Data−link Layer Compatible with LIN rev. 1.3 (Note 1)
- Field−programmable Node Addresses
- Dynamically Allocated Identifiers
- Diagnostics and Status Information

Protection

- Overcurrent Protection
- Open−circuit Detection
- High Temperature Warning and Management
- Low Temperature Flag
- LIN Bus Short−circuit Protection to Supply and Ground
- Lost LIN Safe Operation
- Enhanced Under Voltage Management

Power Saving

- Powerdown Supply Current < 150 μA
- 3.3 V Regulator with Wake−up On LIN Activity

EMI Compatibility

- LIN Bus Integrated Slope Control
- HV Outputs with Slope Control
- This is a Pb−Free Device

1. Minor exceptions to the conformance of the data−link layer to LIN rev. 1.3.

Applications

The NCV70627 is ideally suited for small positioning applications. Target markets include: automotive (headlamp alignment, HVAC, idle control, cruise control), industrial equipment (lighting, fluid control, labeling, process control, XYZ tables, robots...) and building automation (HVAC, surveillance, satellite dish, renewable energy systems). Suitable applications typically have multiple axes or require mechatronics solutions with the driver chip mounted directly on the motor.

Table 1. ORDERING INFORMATION

Part No.	Peak Current	End Market/Version	Package*	Shipping†
NCV70627DQ001G	800/1100 mA (Note 2)	Automotive High Temperature Version	SSOP−36EP (Pb−Free)	47 Units/Rail
NCV70627DQ001R2G	800/1100 mA (Note 2)			1500/Tape & Reel
NCV70627MW002R2G	800/1100 mA (Note 2)	Automotive	QFN32 (Pb−Free)	5000 / Tape & Reel

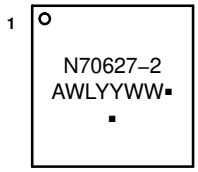
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

2. The device boost current. This applies for operation under the thermal warning level only.

MARKING DIAGRAMS

SSOP



QFN32

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	Unit
V_{BB}, VHW2	Supply voltage, hardwired address pin (Note 4)	−0.3	+40 (Note 3)	V
Vlin	Bus input voltage (Note 4)	−40	+40	V
T_J	Junction temperature range (Note 5)	−50	+175	°C
T_{stg}	Storage temperature range (Note 6)	−55	+160	°C
Vesd (Note 7)	HBM Electrostatic discharge voltage on LIN pin	−4	+4	kV
	HBM Electrostatic discharge voltage on other pins	−2	+2	kV
	MM Electrostatic discharge voltage on other pins	−200	+200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: A mission profile (Note 5) is a substantial part of the operation conditions; hence the Customer must contact ON Semiconductor in order to mutually agree in writing on the allowed missions profile(s) in the application.

3. For limited time: V_{BB} <0.5 s, SWI and HW2 pins <1.0 s.
4. Maximum allowed voltage between two device pins is 60 V.
5. The circuit functionality is not guaranteed outside the Operating junction temperature range.
   A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.
6. For limited time up to 100 hours. Otherwise the maximum storage temperature is 85°C.
7. HBM according to AEC−Q100: EIA−JESD22−A114−B (100 pF via 1.5 kΩ) and MM according to AEC−Q100: EIA−JESD22−A115−A.

Table 3. OPERATING RANGES

Parameter		Min	Max	Unit
V_{BB}	Supply voltage	+5.5	+29	V
T_{JP}	Parametric Operating junction temperature range (Note 8)	−40	+145	°C
T_{JF}	Functional Operating junction temperature range (Note 9)	−40	+160	°C

8. The parametric characteristics of the circuit are not guaranteed outside the parametric operating junction temperature range.
9. The maximum functional operating temperature range can be limited by thermal shutdown Ttsd.

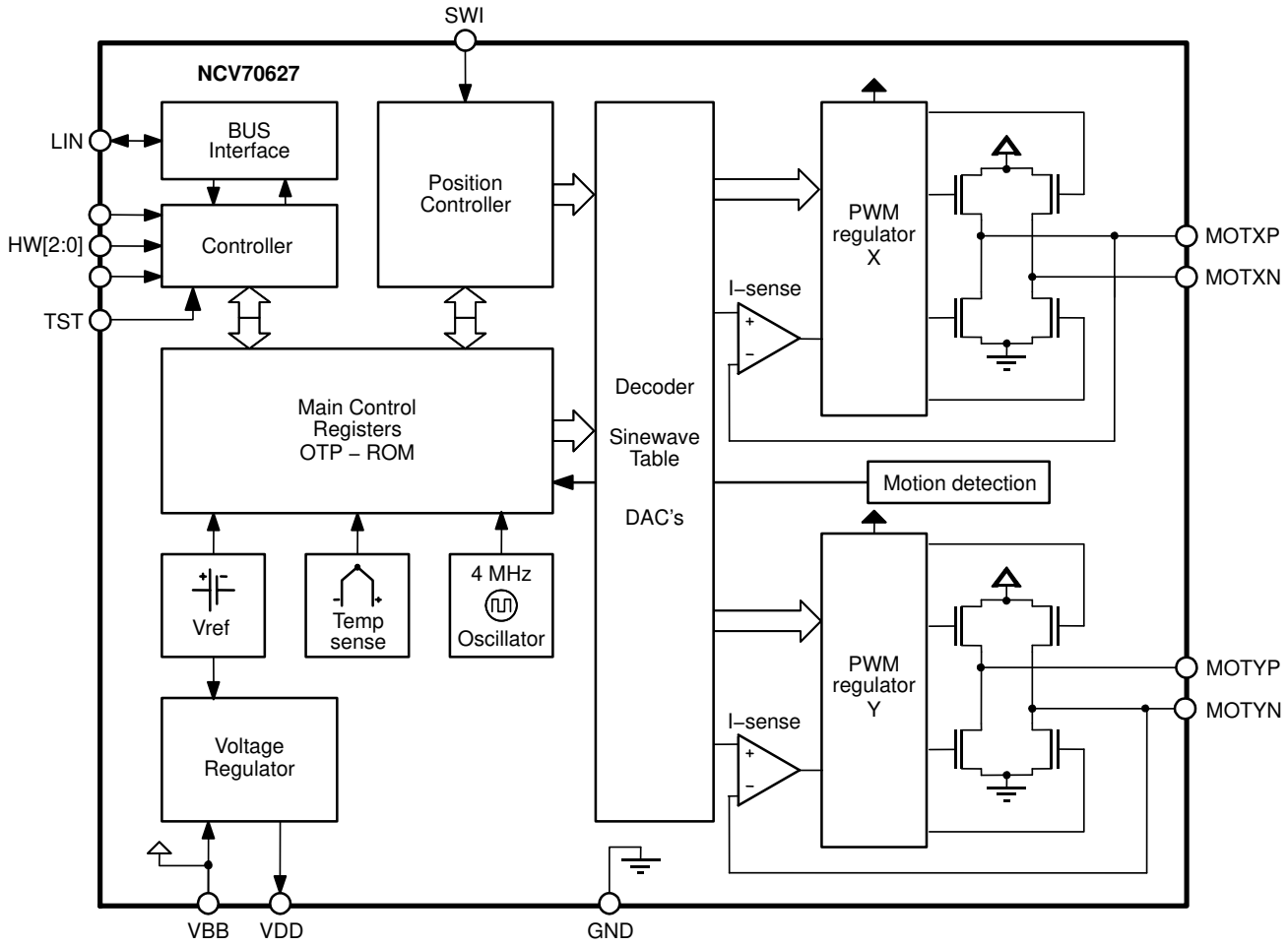


Figure 1. Block Diagram

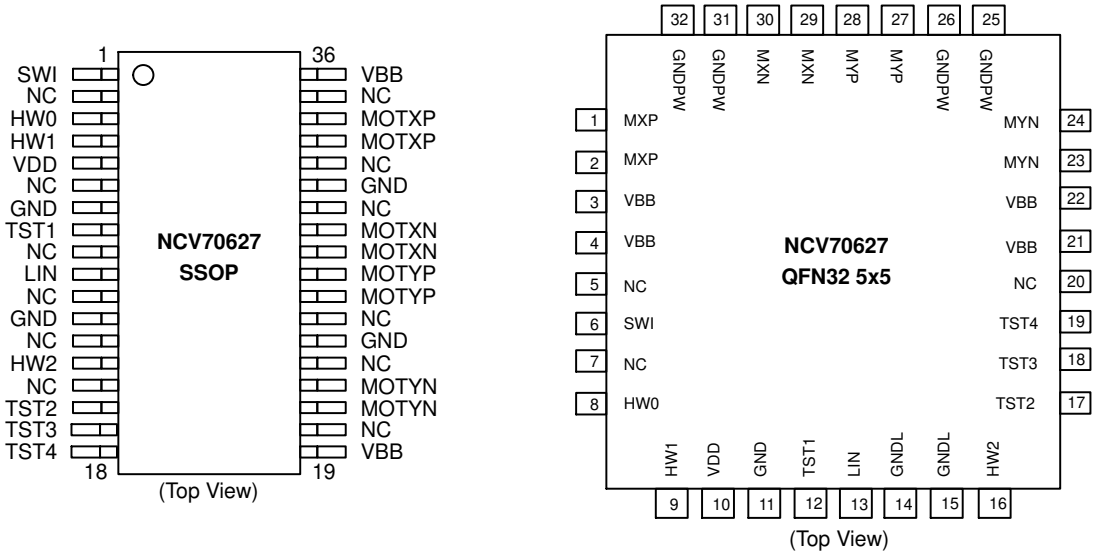


Figure 2. Pinout Diagrams

Table 4. PIN DESCRIPTIONS – SSOP PACKAGE

Pin No.	Pin Name	Pin Description	
1	SWI	Switch input	
3	HW0	Bit 0 of LIN–ADD	To be tied to GND or V_{DD}
4	HW1	Bit 1 of LIN–ADD	
5	VDD	Internal supply (needs external decoupling capacitor)	
7, 12, 24, 31	GND	Ground, heat sink	
8	TST1	Test pin (to be tied to ground in normal operation)	
10	LIN	LIN–bus connection	
14	HW2	Bit 2 LIN–ADD	
16	TST2	Test pin (to be tied to ground in normal operation)	
17	TST3	Test pin (to be tied to ground in normal operation)	
18	TST4	Test pin (to be tied to ground in normal operation)	
19, 36	VBB	Battery voltage supply	
21, 22	MOTYN	Negative end of phase Y coil	
26, 27	MOTYP	Positive end of phase Y coil	
28, 29	MOTXN	Negative end of phase X coil	
33, 34	MOTXP	Positive end of phase X coil	
2, 6, 9, 11, 13, 15, 20, 23, 25, 30, 32, 35	NC	Not used	

Table 5. PIN DESCRIPTIONS – QFN PACKAGE

Pin No.	Pin Name	Pin Description	
1, 2	MXP	Positive end of phase X coil	
3, 4, 21, 22	VBB	Battery voltage supply	
5, 7, 20	NC	Not used	
6	SWI	Switch input	
8	HW0	Bit 0 of LIN–ADD	To be tied to GND or V_{DD}
9	HW1	Bit 1 of LIN–ADD	
10	VDD	Internal supply (needs external decoupling capacitor)	
11	GND	Ground	
12	TST1	Test pin (to be tied to ground in normal operation)	
13	LIN	LIN–bus connection	
14, 15	GNDL	Ground	
16	HW2	Bit 2 LIN–ADD	
17	TST2	Test pin (to be tied to ground in normal operation)	
18	TST3	Test pin (to be tied to ground in normal operation)	
19	TST4	Test pin (to be tied to ground in normal operation)	
23, 24	MYN	Negative end of phase Y coil	
25, 26, 31, 32	GNDPW	Ground	
27, 28	MYP	Positive end of phase Y coil	
29, 30	MXN	Negative end of phase X coil	

Package Thermal Resistance

The NCV70627 is available in thermally optimized SSOP−36 and QFN32 packages. For the optimizations, the package has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer. Figure 3 gives examples for good power distribution solutions.

The thermal resistances are presented in Table 6: Thermal resistance.

Table 6. THERMAL RESISTANCE

Characteristics	Package	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction−to−Exposed Pad (Note 10)	SSOP−36	$R_{\theta JP}$	−	3.3	−	K/W
Thermal Resistance, Junction−to−Exposed Pad (Note 10)	QFN32	$R_{\theta JP}$	−	14	−	K/W

10. Also includes typical solder thickness under the Exposed Pad (EP).

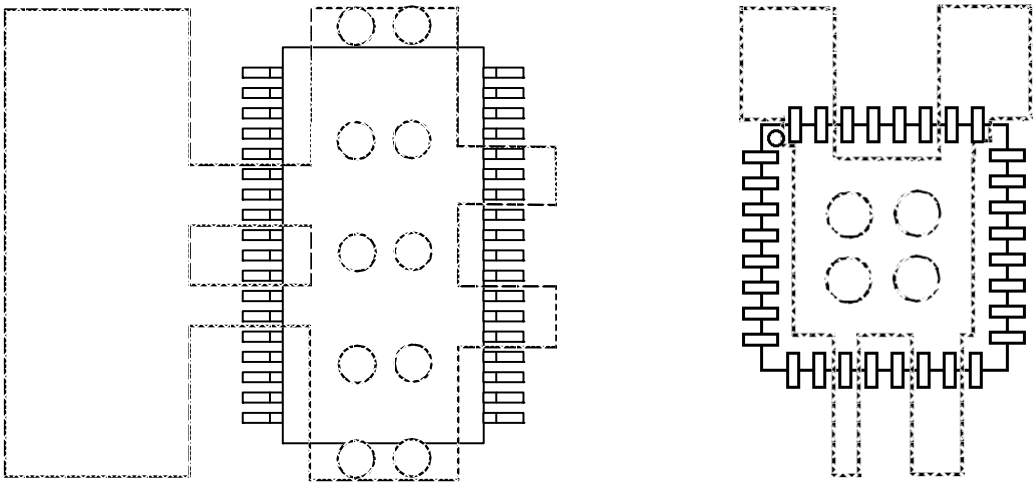


Figure 3. Example of SSOP−36 and QFN32 PCB Ground Plane Layout. Preferred layout at top and bottom connected with through−hole filled vias

DC Parameters

The DC parameters are guaranteed over junction temperature from −40 to 145°C and V_{BB} in the operating range from 5.5 to 29 V, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.

Table 7. DC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
MOTORDRIVER							
$I_{MS-max,Peak}$	MOTXP MOTXN MOTYP MOTYN	Max current through motor coil in normal operation	V_{BB} = 14 V		800		mA
$I_{MS-max,RMS}$		Max rms current through coil in normal operation	V_{BB} = 14 V		570		mA
I_{MSabs}		Absolute error on coil current (Note 11)	V_{BB} = 14 V, T_j =145°C	−10		10	%
I_{MSrel}		Matching of X & Y coil currents	V_{BB} = 14 V	−7	0	7	%
$I_{MS-boost\_Peak}$		Max peak current during booster function	V_{BB} = 14 V, T < T_{tw}		1100		mA
$R_{DS(on)}$		On resistance of High side + Low side Driver at I_{MSmax}	$T_j \le 25°C$			1.8	Ω
			T_j = 145°C			2.4	Ω
LIN TRANSMITTER (Note 19)							
I_{bus_off}	LIN	Dominant state, driver off	V_{bus} = 0 V, V_{BB} = 7 V & 18 V	−1			mA
I_{bus_off}		Recessive state, driver off	V_{bus} = V_{bat}, V_{BB} = 7 V & 18 V			10	μA
I_{bus_off}		Recessive state, driver off	V_{BB} = 0 V (Note 11)			10	μA
I_{bus_lim}		Current limitation	V_{BB} = 7 V & 18 V	50	75	200	mA
R_{slave}		Pullup resistance	V_{BB} = 7 V & 18 V	20	30	47	kΩ
LIN RECEIVER (Note 19)							
V_{bus_dom}	LIN	Receiver dominant state	V_{BB} = 7 V & 18 V	0		0.4 * V_{BB}	V
V_{bus_rec}		Receiver recessive state	V_{BB} = 7 V & 18 V	0.6 * V_{BB}		V_{BB}	V
V_{bus_hys}		Receiver hysteresis	V_{BB} = 7 V & 18 V	0.05 * V_{BB}		0.2 * V_{BB}	V
THERMAL WARNING & SHUTDOWN							
T_{tw}		Thermal warning (Notes 12 and 13)		150	157	165	°C
T_{tsd}		Thermal shutdown (Note 14)			T_{tw} + 10		°C
T_{low}		Low temperature warning (Note 14)			T_{tw} − 167		°C
SUPPLY AND VOLTAGE REGULATOR							
V_{bbOTP}	V_{BB}	Supply voltage for OTP zapping (Note 15)		13.0		18.0	V
UV_2		Stop voltage low threshold		5.48	5.90	6.32	V
UV_3		Decelerated stop voltage low threshold	UV3Thr[2:0] = 000	5.48	5.90	6.32	V
			UV3Thr[2:0] = 001	5.86	6.30	6.74	V
			UV3Thr[2:0] = 010	6.23	6.70	7.17	V
			UV3Thr[2:0] = 011	6.60	7.10	7.60	V

11. Tested in production for 800 mA, 400 mA, 200 mA and 100 mA current settings for both X and Y coil.
12. Parameter guaranteed by trimming relevant OTPs in production.
13. No more than 100 cumulated hours in life time above Tw.
14. Thermal shutdown and low temperature warning are derived from thermal warning. Guaranteed by design.
15. A buffer capacitor of minimum 100 μF is needed between V_{BB} and GND. Short connections to the power supply are recommended.
16. Pin V_{DD} must not be used for any external supply
17. The RAM content will not be altered above this voltage.
18. External resistance value seen from pin SWI or HW2, including 1 kΩ series resistor. For the switch OPEN, the maximum allowed leakage current is represented by a minimum resistance seen from the pin.
19. While LIN is only specified for operation above 7 V $V_{BB,}$ the device can operate LIN at lower voltages down to 5.5 V. Under these conditions the LIN specific parameters are not guaranteed.

Table 7. DC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY AND VOLTAGE REGULATOR							
UV_3	V_{BB}	Decelerated stop voltage low threshold	UV3Thr[2:0] = 100	6.97	7.50	8.03	V
			UV3Thr[2:0] = 101	7.34	7.90	8.46	V
			UV3Thr[2:0] = 110	7.71	8.30	8.89	V
			UV3Thr[2:0] = 111	8.09	8.70	9.31	V
UV_1	V_{BB}	Stop voltage high threshold, Ratio metric coupled to UV3Thr[2:0].	UV3Thr[2:0] = 000	6.18	6.62	7.06	V
			UV3Thr[2:0] = 001	6.60	7.07	7.54	V
			UV3Thr[2:0] = 010	7.02	7.52	8.01	V
			UV3Thr[2:0] = 011	7.44	7.97	8.49	V
			UV3Thr[2:0] = 100	7.86	8.41	8.97	V
			UV3Thr[2:0] = 101	8.28	8.86	9.45	V
			UV3Thr[2:0] = 110	8.70	9.31	9.93	V
			UV3Thr[2:0] = 111	9.12	9.76	10.41	V
I_{bat}		Total current consumption	Unloaded outputs, V_{BB} = 29 V		3.50	10.0	mA
I_{bat_s}		Sleep mode current consumption	V_{BB} = 5.5 V & 18 V			150	μA
V_{DD}	V_{DD}	Regulated internal supply (Note 16)	5.5 V < V_{BB} < 29 V	3.1	3.3	3.5	V
$V_{ddReset}$		Digital supply reset level @ power down (Note 17)				3.0	V
I_{ddLim}		Current limitation	Pin shorted to ground V_{BB} = 14 V			85	mA
SWITCH INPUT AND HARDWIRE ADDRESS INPUT							
$Rt_{\_OFF}$	SWI HW2	Switch OPEN resistance (Note 18)		10			kΩ
$Rt_{\_ON}$		Switch ON resistance (Note 18)	Switch to GND or V_{BB}			1.9	kΩ
V_{bb_sw}		V_{BB} range for guaranteed operation of SWI and HW2		5.5		29	V
I_{lim_sw}		Current limitation	Short to GND or V_{bat} V_{BB} = 29 V	20	30	45	mA
HARDWIRED ADDRESS INPUTS AND TEST PIN							
V_{ihigh}	HW0 HW1 TST	Input level high	V_{BB} = 14 V	1.9			V
V_{ilow}		Input level low	V_{BB} = 14 V			1.4	V
HW_{hyst}		Hysteresis	V_{BB} = 14 V		1		V

11. Tested in production for 800 mA, 400 mA, 200 mA and 100 mA current settings for both X and Y coil.
12. Parameter guaranteed by trimming relevant OTPs in production.
13. No more than 100 cumulated hours in life time above Tw.
14. Thermal shutdown and low temperature warning are derived from thermal warning. Guaranteed by design.
15. A buffer capacitor of minimum 100 μF is needed between V_{BB} and GND. Short connections to the power supply are recommended.
16. Pin V_{DD} must not be used for any external supply
17. The RAM content will not be altered above this voltage.
18. External resistance value seen from pin SWI or HW2, including 1 kΩ series resistor. For the switch OPEN, the maximum allowed leakage current is represented by a minimum resistance seen from the pin.
19. While LIN is only specified for operation above 7 V $V_{BB,}$ the device can operate LIN at lower voltages down to 5.5 V. Under these conditions the LIN specific parameters are not guaranteed.

AC Parameters

The AC parameters are guaranteed over junction temperature from –40 to 145°C and V_{BB} in the operating range from 5.5 to 29 V, unless otherwise specified. The LIN transmitter and receiver physical layer parameters are compliant to LIN rev. 2.0 & 2.1.

Table 8. AC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
POWERUP							
T_{pu}		Power–up time	Guaranteed by design			10	ms
INTERNAL OSCILLATOR							
f_{osc}		Frequency of internal oscillator	V_{BB} = 14 V	3.6	4.0	4.4	MHz
LIN TRANSMITTER CHARACTERISTICS ACCORDING TO LIN V2.0 & V2.1							
D1	LIN	Duty cycle 1 = $t_{Bus\_rec(min)}$ / (2 x t_{Bit}); See Figure 4	THRec(max) = 0.744 x V_{BB} THDom(max) = 0.581 x V_{BB}; V_{BB} = 7.0 V...18 V; t_{Bit} = 50 μs	0.396			
D2		Duty cycle 2 = $t_{Bus\_rec(max)}$ / (2 x t_{Bit}); See Figure 4	THRec(min) = 0.422 x V_{BB} THDom(min) = 0.284 x V_{BB}; V_{BB} = 7.6 V...18 V; t_{Bit} = 50 μs			0.581	
LIN RECEIVER CHARACTERISTICS ACCORDING TO LIN V2.0 & V2.1							
trx_pdr	LIN	Propagation delay bus dominant to RxD = low	V_{BB} = 7.0 V & 18 V; See Figure 4			6	μs
trx_pdf		Propagation delay bus recessive to RxD = high	V_{BB} = 7.0 V & 18 V; See Figure 4			6	μs
trx_sym		Symmetry of receiver propagation delay	trx_pdr – trx_pdf	–2		+2	μs
SWITCH INPUT AND HARDWIRE ADDRESS INPUT							
T_{sw}	SWI HW2	Scan pulse period (Note 20)	V_{BB} = 14 V		1024		μs
T_{sw_on}		Scan pulse duration (Note 20)	V_{BB} = 14 V		128		μs
MOTORDRIVER							
F_{pwm}	MOTx	PWM frequency (Note 20)	PWMfreq = 0 (Note 21)	20.6	22.8	25.0	kHz
			PWMfreq = 1 (Note 21)	41.2	45.6	50.0	kHz
F_{jit_depth}		PWM jitter modulation depth	PWMJen = 1 (Note 21)		10		%
T_{brise}		Turn–on transient time	Between 10% and 90%		170		ns
T_{bfall}		Turn–off transient time			140		ns
T_{stab}		Run current stabilization time (Note 20)	TStab[1:0] = 00	14.4	16	17.6	ms
			TStab[1:0] = 01	19.8	22	24.2	ms
			TStab[1:0] = 10	25.2	28	30.8	ms
			TStab[1:0] = 11	28.8	32	35.2	ms
SUPPLY							
T_{UV1_deb}	VBB	UV1 level debounce time (Note 20)	UV3debT = 0		96		μs
			UV3debT = 1		256		μs

20. Derived from the internal oscillator
21. See `SetMotorParam` and PWM Regulator

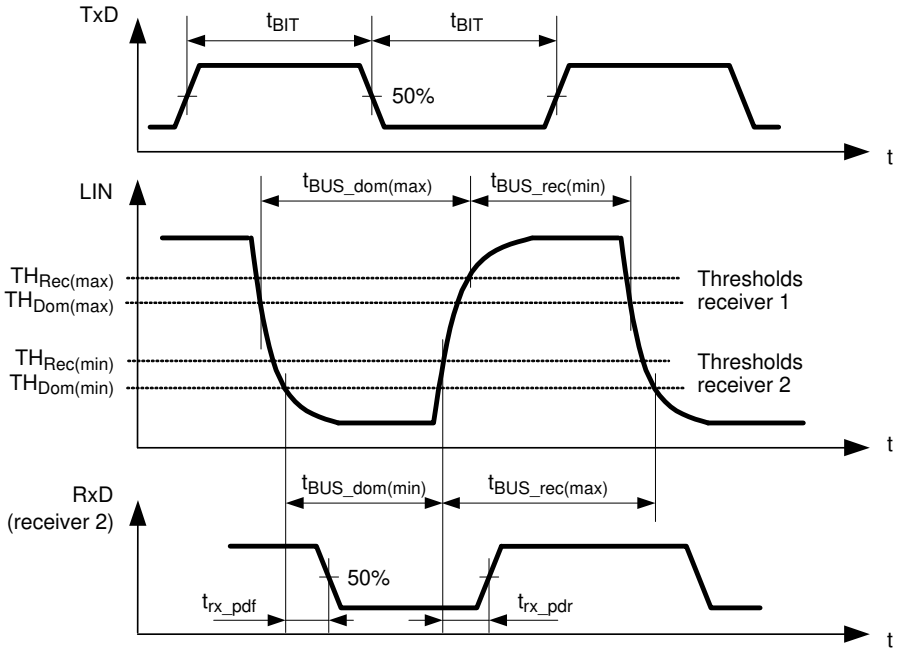


Figure 4. Timing Diagram for AC Characteristics According to LIN 2.0 & 2.1

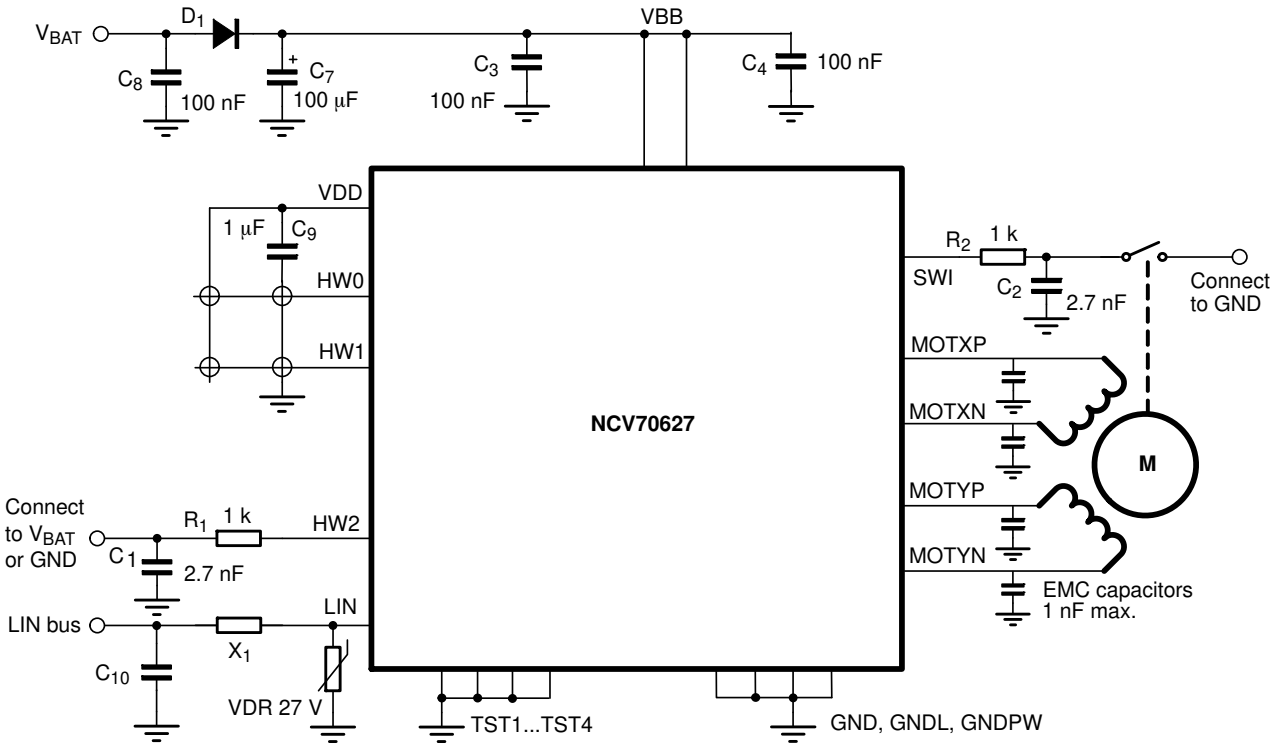


Figure 5. Typical Application

NOTES: All resistors are ± 5%, 1/4 W
C_1, C_2 minimum value is 2.7 nF, maximum value is 10 nF
Depending on the application, the ESR value and working voltage of C_7 must be carefully chosen
C_3 and C_4 must be close to pins V_{BB} and coupled GND directly
C_9 must be a ceramic capacitor to assure low ESR
C_{10} is placed for system level EMC reasons; value depends on EMC requirements of the application, recommended 200 pF
X_1 is placed for system level EMC and ESD reasons. Use e.g. BLM18AG601SN1D 600 OHM or resistor 50 Ω

Positioning Parameters

Stepping Modes

One of four possible stepping modes can be programmed:

- Half−stepping
- 1/4 micro−stepping
- 1/8 micro−stepping
- 1/16 micro−stepping

Maximum Velocity

For each stepping mode, the maximum velocity Vmax can be programmed to 16 possible values given in the table below.

The accuracy of Vmax is derived from the internal oscillator. Under special circumstances it is possible to change the Vmax parameter while a motion is ongoing. All 16 entries for the Vmax parameter are divided into four groups. When changing Vmax during a motion the application must take care that the new Vmax parameter stays within the same group.

Table 9. MAXIMUM VELOCITY SELECTION TABLE

Vmax Index				Stepping Mode			
Hex	Dec	Vmax (full step/s)	Group	Half−stepping (half−step/s)	1/4th Micro−stepping (micro−step/s)	1/8th Micro−stepping (micro−step/s)	1/16th Micro−stepping (micro−step/s)
0	0	99	A	197	395	790	1579
1	1	136	B	273	546	1091	2182
2	2	167		334	668	1335	2670
3	3	197		395	790	1579	3159
4	4	213		425	851	1701	3403
5	5	228		456	912	1823	3647
6	6	243		486	973	1945	3891
7	7	273	C	546	1091	2182	4364
8	8	303		607	1213	2426	4852
9	9	334		668	1335	2670	5341
A	10	364		729	1457	2914	5829
B	11	395		790	1579	3159	6317
C	12	456		912	1823	3647	7294
D	13	546	D	1091	2182	4364	8728
E	14	729		1457	2914	5829	11658
F	15	973		1945	3891	7782	15564

Minimum Velocity

Once the maximum velocity is chosen, 16 possible values can be programmed for the minimum velocity Vmin. The table below provides the obtainable values in full−step/s. The accuracy of Vmin is derived from the internal oscillator. It is not recommended to change the Vmin while a motion is ongoing.

Table 10. OBTAINABLE VALUES IN FULL−STEP/s FOR THE MINIMUM VELOCITY

Vmin Index		Vmax Factor	Vmax (Full−step/s)															
			A	B						C						D		
Hex	Dec		99	136	167	197	213	228	243	273	303	334	364	395	456	546	729	973
0	0	1	99	136	167	197	213	228	243	273	303	334	364	395	456	546	729	973
1	1	1/32	3	4	5	6	6	7	7	8	8	10	10	11	13	15	19	27
2	2	2/32	6	8	10	11	12	13	14	15	17	19	21	23	27	31	42	57
3	3	3/32	9	12	15	18	19	21	22	25	27	31	32	36	42	50	65	88
4	4	4/32	12	16	20	24	26	28	30	32	36	40	44	48	55	65	88	118
5	5	5/32	15	21	26	31	32	35	37	42	46	51	55	61	71	84	111	149
6	6	6/32	18	25	31	36	39	42	45	50	55	61	67	72	84	99	134	179
7	7	7/32	21	30	36	43	46	50	52	59	65	72	78	86	99	118	156	210
8	8	8/32	24	33	41	49	52	56	60	67	74	82	90	97	113	134	179	240
9	9	9/32	28	38	47	55	59	64	68	76	84	93	101	111	128	153	202	271
A	10	10/32	31	42	51	61	66	71	75	84	93	103	113	122	141	168	225	301
B	11	11/32	34	47	57	68	72	78	83	93	103	114	124	135	156	187	248	332
C	12	12/32	37	51	62	73	79	85	91	101	113	124	135	147	170	202	271	362
D	13	13/32	40	55	68	80	86	93	98	111	122	135	147	160	185	221	294	393
E	14	14/32	43	59	72	86	93	99	106	118	132	145	158	172	198	237	317	423
F	15	15/32	46	64	78	93	99	107	113	128	141	156	170	185	214	256	340	454

NOTES: The Vmax factor is an approximation.
In case of motion without acceleration (**AccShape = 1**) the length of the steps = 1/**Vmin.** In case of accelerated motion (**AccShape** = 0) the length of the first step is shorter than 1/**Vmin** depending of **Vmin, Vmax** and **Acc**.

Acceleration and Deceleration

Sixteen possible values can be programmed for Acc (acceleration and deceleration between Vmin and Vmax). The table below provides the obtainable values in full−step/s^2. One observes restrictions for some combinations of acceleration index and maximum speed. It is not recommended to change the Acc value while a motion is ongoing.

The accuracy of Acc is derived from the internal oscillator.

Table 11. ACCELERATION AND DECELERATION SELECTION TABLE

Vmax (FS/s) →		99	136	167	197	213	228	243	273	303	334	364	395	456	546	729	973
↓ Acc Index																	
Hex	Dec	Acceleration (Full−step/s^2)															
0	0	49							106						473		
1	1	218													735		
2	2	1004															
3	3	3609															
4	4	6228															
5	5	8848															
6	6	11409															
7	7	13970															
8	8	16531															
9	9	14785	19092														
A	10		21886														
B	11		24447														
C	12		27008														
D	13		29570														
E	14		29570						34925								
F	15								40047								

The formula to compute the number of equivalent full−steps during acceleration phase is:

$$Nstep = \frac{Vmax^2 - Vmin^2}{2 \times Acc}$$

Positioning

The position programmed in commands SetPosition is given as a number of (micro−) steps. According to the chosen stepping mode, the internal position words is aligned as described in the table below. When using command SetPositionShort the position is given in numbers of half steps, while the Secure Position is given in a number of two Full Steps. The position data is aligned automatically.

Table 12. POSITION WORD ALIGNMENT

Stepping Mode	Position Word: Pos[15:0]																Shift
1/16th	**S**	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	No shift
1/8th	**S**	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	1−bit left ⇔ ×2
1/4th	**S**	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	0	2−bit left ⇔ ×4
Half−stepping	**S**	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	0	0	3−bit left ⇔ ×8
Position Short	**S**	**S**	**S**	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	0	0	No shift
Secure Position	**S**	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	0	0	0	0	No shift

NOTES: LSB: Least Significant Bit
S: Sign bit

Position Ranges

A position is coded by using the binary two's complement format. According to the positioning commands used and to the chosen stepping mode, the position range will be as shown in the following table.

Table 13. POSITION RANGE

Command	Stepping Mode	Position Range	Full Range Excursion	Number of Bits in micro stepping
SetPosition	Half−stepping	−4096 to +4095	8192 half−steps	13
	1/4th micro−stepping	−8192 to +8191	16384 micro−steps	14
	1/8th micro−stepping	−16384 to +16383	32768 micro−steps	15
	1/16th micro−stepping	−32768 to +32767	65536 micro−steps	16
SetPositionShort	Half−stepping	−1024 to +1023	2048 half−steps	11
	1/4th micro−stepping	−2048 to +2047	4096 micro−steps	12
	1/8th micro−stepping	−4096 to +4095	8192 micro−steps	13
	1/16th micro−stepping	−8192 to +8191	16384 micro−steps	14

When using the command SetPosition, although coded on 16 bits, the position word is shifted to the left by a certain number of bits, according to the stepping mode. SetPositonShort is only coded on 11 bits.

Secure Position

A secure position can be programmed. It is mapped to the positioned full range but coded in 11−bits, thus having a lower resolution than normal positions, as shown in the following table. See also command GotoSecurePosition and LIN lost behavior.

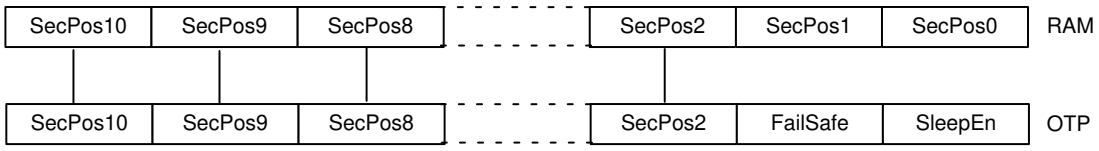
Table 14. SECURE POSITION

Stepping Mode	Secure Position Resolution
Half−stepping	4 half−steps
1/4th micro−stepping	8 micro−steps (1/4th)
1/8th micro−stepping	16 micro−steps (1/8th)
1/16th micro−stepping	32 micro−steps (1/16th)

Important

NOTES: For the FailSafe functionality and SetDualPosition command, the secure position is disabled in case the programmed value has the code "10000000000" (0x400 or most negative position). For the GotoSecurePosition command there is no disabling possible. By receiving this command the secure positioning is always executed, even when the secure position has the value 0x400.

The resolution of the secure position is limited to 9 bit at start−up. The OTP register is copied in RAM as illustrated below. The RAM bits SecPos1 and SecPos0 are set to 0.



Shaft

A shaft bit, which can be programmed in OTP or with command SetMotorParam, defines whether a positive motion is a clockwise (CW) or counter−clockwise rotation (CCW) (an outer or an inner motion for linear actuators):

- Shaft = 0 ⇒ MOTXP is used as positive pin of the X coil, while MOTXN is the negative one.
- Shaft = 1 ⇒ opposite situation

Structural Description

Refer to the Block Diagram in Figure 1.

Stepper Motordriver

The Motordriver receives the control signals from the control logic. The main features are:

- Two H−bridges, designed to drive a stepper motor with two separated coils. Each coil (X and Y) is driven by one H−bridge, and the driver controls the currents flowing through the coils. The rotational position of the rotor, in unloaded condition, is defined by the ratio of current flowing in X and Y. The torque of the stepper motor when unloaded is controlled by the magnitude of the currents in X and Y.
- The control block for the H−bridges, including the PWM control, the synchronous rectification and the internal current sensing circuitry.
- Two pre−scale 4−bit DAC's to set the maximum magnitude of the current through X and Y.
- Two DAC's to set the correct current ratio through X and Y.
- A boost function that increases the current during cold conditions.

Battery voltage monitoring is also performed by this block, which provides the required information to the control logic part. The same applies for detection and reporting of an electrical problem that could occur on the coils.

Control Logic (Position Controller and Main Control)

The control logic block stores the information provided by the LIN interface (in a RAM or an OTP memory) and digitally controls the positioning of the stepper motor in terms of speed and acceleration, by feeding the right signals to the motor driver state machine.

It will take into account the successive positioning commands to properly initiate or stop the stepper motor in order to reach the set point in a minimum time.

It also receives feedback from the motor driver part in order to manage possible problems and decide on internal actions and reporting to the LIN interface.

Motion Detection

Motion detection is based on the back−emf generated internally in the running motor. When the motor is blocked, e.g. when it hits the end position, the velocity, and as a result also the generated back−emf, is disturbed. The NCV70627 senses the back−emf and compares the value with an independent threshold level. If the back−emf becomes lower than the threshold, the running motor is stopped.

LIN Interface

The LIN interface implements the physical layer and the MAC and LLC layers according to the OSI reference model. It provides and gets information to and from the control logic block, in order to drive the stepper motor, to configure the way this motor must be driven, or to get information such as actual position or diagnosis (temperature, battery voltage, electrical status...) and pass it to the LIN master node.

Miscellaneous

The NCV70627 also contains the following:

- An internal oscillator, needed for the LIN protocol handler as well as the control logic and the PWM control of the motor driver.
- An internal trimmed voltage source for precise referencing.
- A protection block featuring a thermal shutdown and a power−on−reset circuit.
- A 3.3 V regulator (from the battery supply) to supply the internal logic circuitry.

Functions Description

This chapter describes the following functional blocks in more detail:

- Position controller
- Main control and register, OTP memory + ROM
- Motor driver

The Motion detection and LIN controller are discussed in separate chapters.

Position Controller

Positioning and Motion Control

A positioning command will produce a motion as illustrated in Figure 6. A motion starts with an acceleration phase from minimum velocity (Vmin) to maximum velocity (Vmax) and ends with a symmetrical deceleration. This is defined by the control logic according to the position required by the application and the parameters programmed by the application during the configuration phase. The current in the coils is also programmable.

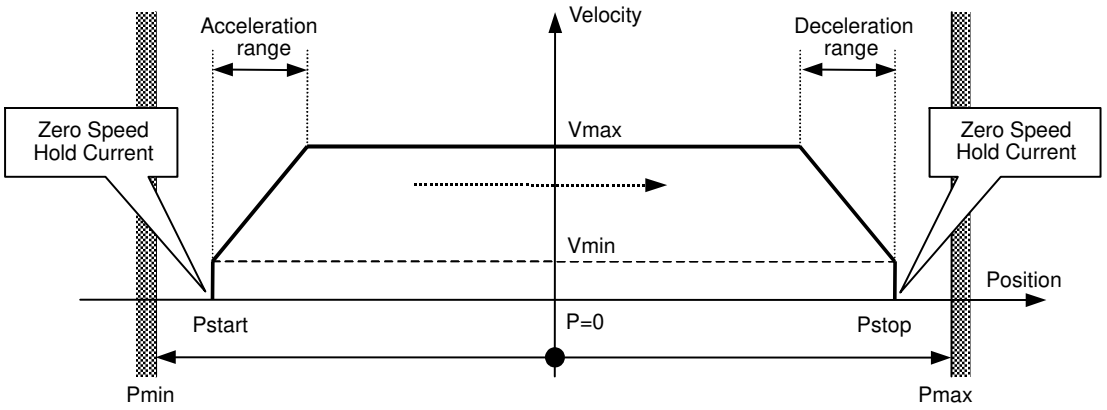


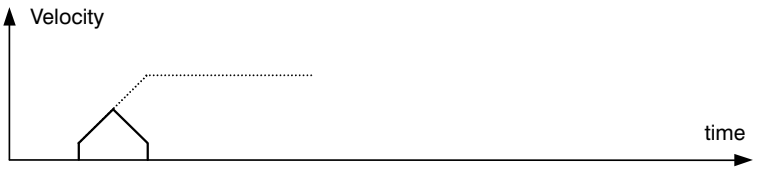
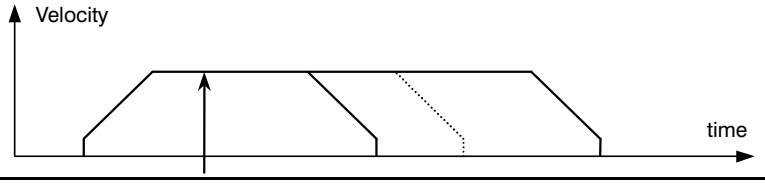
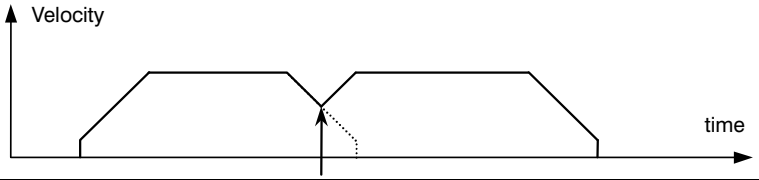
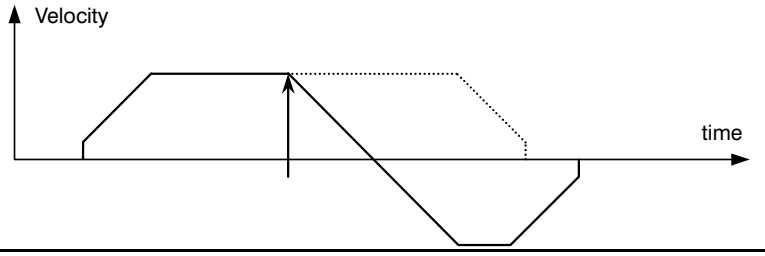
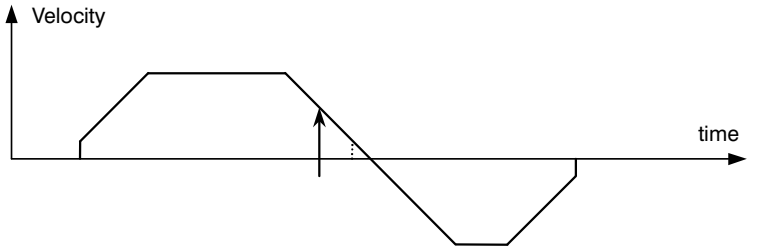
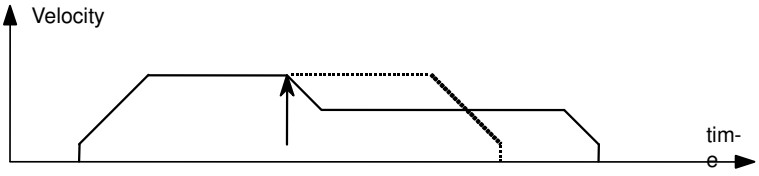
Figure 6. Position and Motion Control

Table 15. POSITION RELATED PARAMETERS

Parameter	Reference
Pmax – Pmin	See Positioning
Zero Speed Hold Current	See Ihold
Maximum Current	See Irun
Acceleration and Deceleration	See Acceleration and Deceleration
Vmin	See Minimum Velocity
Vmax	See Maximum Velocity
Stabilization Time	See Stabilization Time

Different positioning examples are shown in the next table.

Table 16. POSITIONING EXAMPLES

Short motion.	
New positioning command in same direction, shorter or longer, while a motion is running at maximum velocity.	
New positioning command in same direction while in deceleration phase (Note 22) Note: there is no wait time between the deceleration phase and the new acceleration phase.	
New positioning command in reverse direction while motion is running at maximum velocity.	
New positioning command in reverse direction while in deceleration phase.	
New velocity Vmax programming while motion is running.	

22. Reaching the end position is always guaranteed, however velocity rounding errors might occur. The device is automatically compensating the position error. The velocity rounding error will be removed at Vmin (e.g. at end of acceleration or when AccShape=1) by a corrective motion action.

Dual Positioning

A SetDualPosition command allows the user to perform a positioning using two different velocities. The first motion is done with the specified Vmin and Vmax velocities in the SetDualPosition command, with the acceleration (deceleration) parameter already in RAM, to a position Pos1[15:0] also specified in SetDualPosition.

Then a second relative motion to a physical position Pos1[15:0] + Pos2[15:0] is done at the specified Vmin velocity in the SetDualPosition command (no acceleration). Once the second motion is achieved, the ActPos register is reset to zero, whereas TagPos register is not changed.

When the Secure position is enabled, after the dual positioning, the secure positioning is executed. The figure below gives a detailed overview of the dual positioning function. After the dual positioning is executed an internal flag is set to indicate the NCV70627 is referenced.

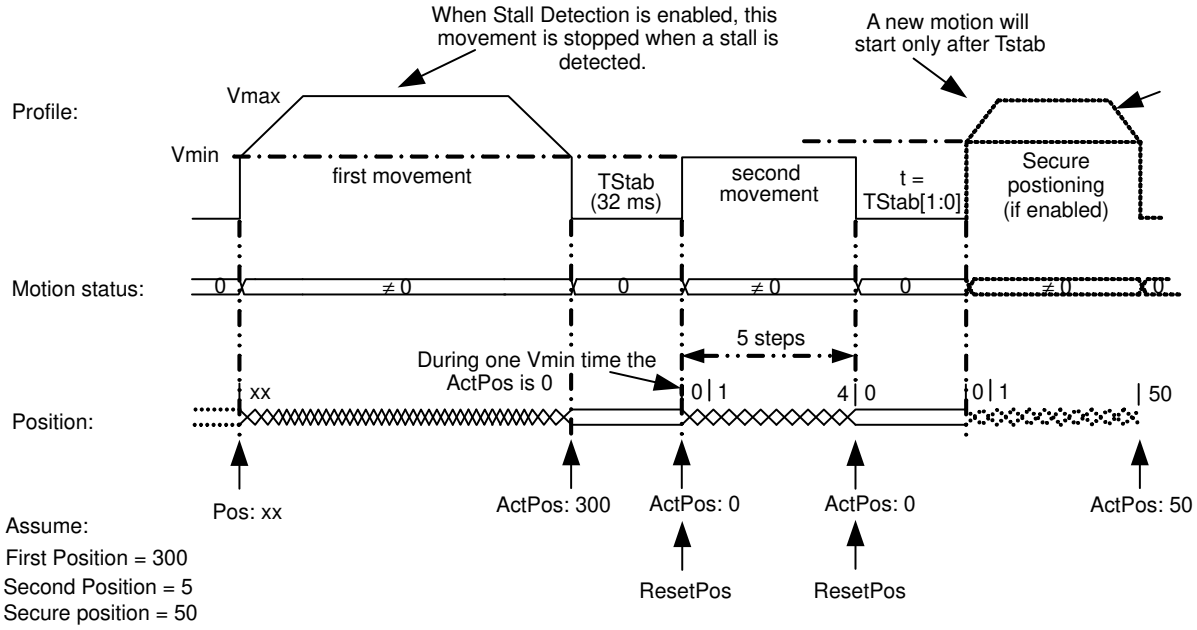


Figure 7. Dual Position

Remark: This operation cannot be interrupted or influenced by any further command unless the occurrence of the conditions driving to a motor shutdown or by a `HardStop` command. Sending a `SetDualPosition` command while a motion is already ongoing is not recommended.

23. The priority encoder is describing the management of states and commands.
24. A DualPosition sequence starts by setting TagPos buffer register to SecPos value, provided secure position is enabled otherwise TagPos is reset to zero. If a SetPosition(Short) command is issued during a DualPosition sequence, it will be kept in the position buffer memory and executed afterwards. This applies also for the commands Sleep, SetPosParam and GotoSecurePosition.
25. Commands such as GetActualPos or GetStatus will be executed while a Dual Positioning is running. This applies also for a dynamic ID assignment LIN frame.
26. The Pos1, Pos2, Vmax and Vmin values programmed in a `SetDualPosition` command apply only for this sequence. All other motion parameters are used from the RAM registers (programmed for instance by a former SetMotorParam command). After the DualPosition motion is completed, the former Vmin and Vmax become active again.
27. Commands ResetPosition, SetDualPosition, and SoftStop will be ignored while a DualPosition sequence is ongoing, and will not be executed afterwards.
28. Recommendation: a SetMotorParam command should not be sent during a `SetDualPosition` sequence: all the motion parameters defined in the command, except Vmin and Vmax, become active immediately.
29. When during the Dual positioning an under voltage UV2 or UV3 happens, the motor will stop (hardstop for UV2 or softstop for UV3). The device will go into the under−voltage and autarkic operational handler function (refer to battery voltage management and autarkic function). Especially for the dual positioning it should be stated that after passing the UV1 level the motion is continued with the parameters Vmax, Vmin and Acceleration from the SetMotorParam command and not from the SetDualPosition command.
30. After the first motion of the dual positioning there is always a fixed stabilization time of 32 ms applied afterwards. After the second motion the programmed stabilization time TStab[1..0] is applied.

Position Periodicity

Depending on the stepping mode the position can range from −4096 to +4095 in half−step to −32768 to +32767 in 1/16th micro−stepping mode. One can project all these positions lying on a circle. When executing the command `SetPosition`, the position controller will set the movement direction in such a way that the traveled distance is minimal.

The figure below illustrates that the moving direction going from `ActPos` = +30000 to `TagPos` = −30000 is clockwise.

If a counter clockwise motion is required in this example, several consecutive `SetPosition` commands can be used.

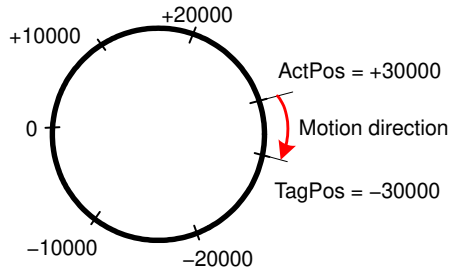


Figure 8. Motion Direction is Function of Difference between ActPos and TagPos

Hardwired Address HW2

In the drawing below, a simplified schematic diagram is shown of the HW2 comparator circuit.

The HW2 pin is sensed via 2 switches. The DriveHS and DriveLS control lines are alternatively closing the top and bottom switch connecting HW2 pin with a current to resistor converter. Closing S_{TOP} (DriveHS = 1) will sense a current to GND. In that case the top I → R converter output is low, via the closed passing switch S_{PASS_T} this signal is fed to the "R" comparator which output HW2_Cmp is high. Closing bottom switch S_{BOT} (DriveLS = 1) will sense a current to V_{BAT}. The corresponding I → R converter output is low and via S_{PASS_B} fed to the comparator. The output HW2_Cmp will be high.

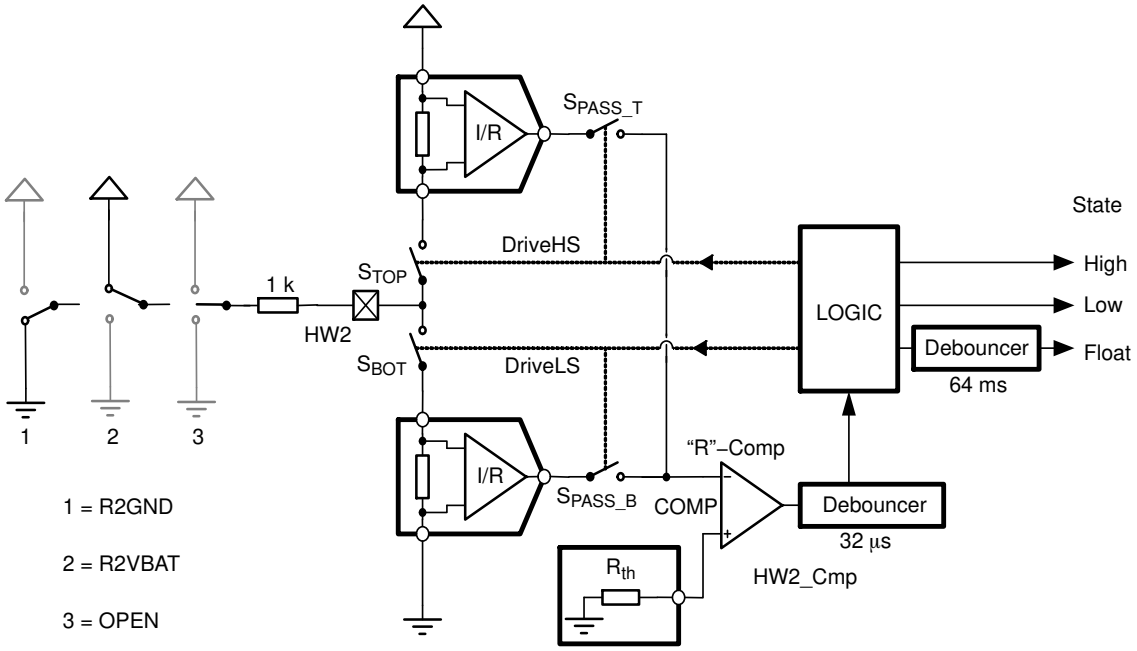


Figure 9.

3 cases can be distinguished (see also Figure 9 above):

- HW2 is connected to ground: R2GND or drawing 1
- HW2 is connected to VBAT: R2VBAT or drawing 2
- HW2 is floating: OPEN or drawing 3

Table 17. STATE DIAGRAM OF THE HW2 COMPARATOR

Previous State	DriveLS	DriveHS	HW2_Cmp	New State	Condition	Drawing
Float	1	0	0	Float	R2GND or OPEN	1 or 3
Float	1	0	1	High	R2VBAT	2
Float	0	1	0	Float	R2VBAT or OPEN	2 or 3
Float	0	1	1	Low	R2GND	1
Low	1	0	0	Low	R2GND or OPEN	1 or 3
Low	1	0	1	High	R2VBAT	2
Low	0	1	0	Float	R2VBAT or OPEN	2 or 3
Low	0	1	1	Low	R2GND	1
High	1	0	0	Float	R2GND or OPEN	1 or 3
High	1	0	1	High	R2VBAT	2
High	0	1	0	High	R2VBAT or OPEN	2 or 3
High	0	1	1	Low	R2GND	1

The logic is controlling the correct sequence in closing the switches and in interpreting the 64 μs debounced HW2_Cmp output accordingly. The output of this small state−machine is corresponding to:

- High or address = 1
- Low or address = 0
- Floating

As illustrated in the table above (Table 17), the state is depending on the previous state, the condition of the 2 switch controls (DriveLS and DriveHS) and the output of HW2_Cmp. Figure 10 shows an example of a practical case where a connection to VBAT is interrupted.

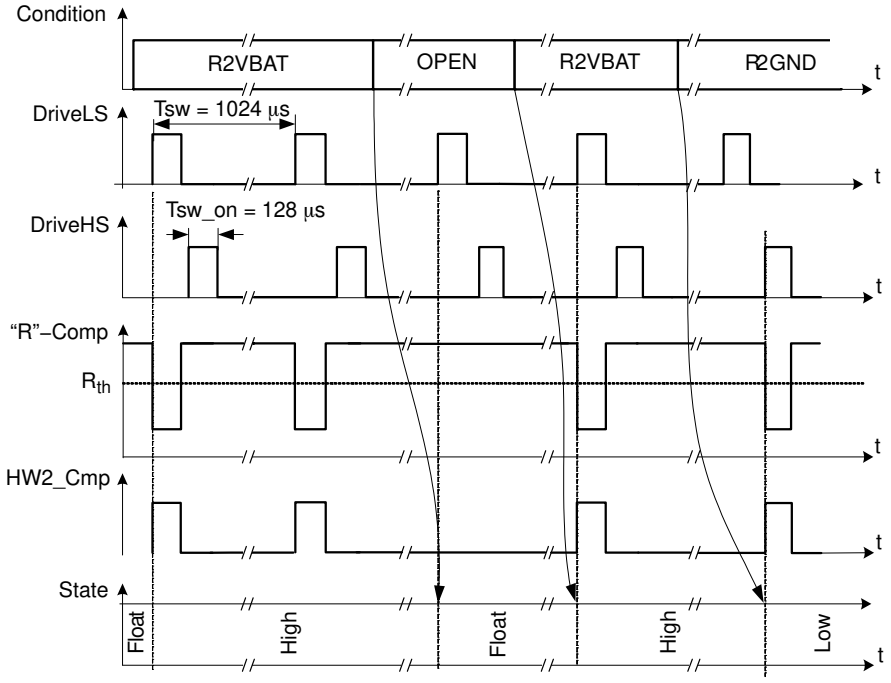


Figure 10. Timing Diagram Showing the Change in State for HW2 Comparator

R2VBAT

A resistor is connected between VBAT and HW2. Every 1024 μs S_{BOT} is closed and a current is sensed. The output of the I ⇒ R converter is low and the HW2_Cmp output is high. Assuming the previous state was floating, the internal logic will interpret this as a change of state and the new state will be high (see also Table 17). The next time S_{BOT} is closed the same conditions are observed. The previous state was high so based on Table 17 the new state remains unchanged. This high state will be interpreted as HW2 address = 1.

OPEN

In case the HW2 connection is lost (broken wire, bad contact in connector) the next time S_{BOT} is closed, this will be sensed. There will be no current, the output of the corresponding I ⇒ R converter is high and the HW2_Cmp will be low. The previous state was high. Based in Table 17 one can see that the state changes to float. This will trigger a motion to secure position after a debounce time of 64 ms, which prevents false triggering in case of micro−interruptions of the power supply.

R2GND

If a resistor is connected between HW2 and the GND, a current is sensed every 1024 μs when S_{TOP} is closed. The output of the top I ⇒ R converter is low and as a result the HW2_Cmp output switches to high. Again based on the stated diagram in Table 17 one can see that the state will change to Low. This low state will be interpreted as HW2 address = 0.

External Switch SWI

As illustrated in Figure 11 the SWI comparator is almost identical to HW2. The major difference is in the limited number of states. Only open or closed is recognized leading to respectively ESW = 0 and ESW = 1.

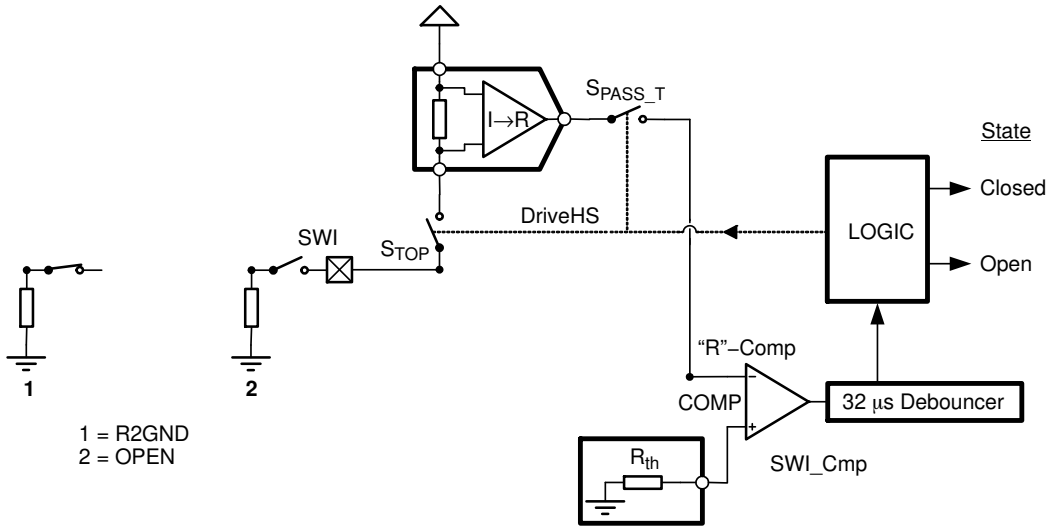


Figure 11. Simplified Schematic Diagram of the SWI Comparator

As illustrated in the drawing above, a change in state is always synchronized with DriveHS or DriveLS. The same synchronization is valid for updating the internal position register. This means that after every current pulse (or closing of S_{TOP} or S_{BOT}) the state of the position switch together with the corresponding position is memorized.

The GetActualPos command reads back the <ActPos> register and the status of ESW. In this way the master node may get synchronous information about the state of the switch together with the position of the motor. See Table 18 below.

Table 18. GetActualPos LIN COMMAND

Reading Frame									
		Structure							
Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Identifier	*	*	1	0	ID3	ID2	ID1	ID0
1	Data 1	ESW	AD[6:0]						
2	Data 2	ActPos[15:8]							
3	Data 3	ActPos[7:0]							
4	Data 4	VddReset	StepLoss	ElDef	UV	TSD	TW	Tinfo[1:0]	
5	Checksum	Checksum over data							

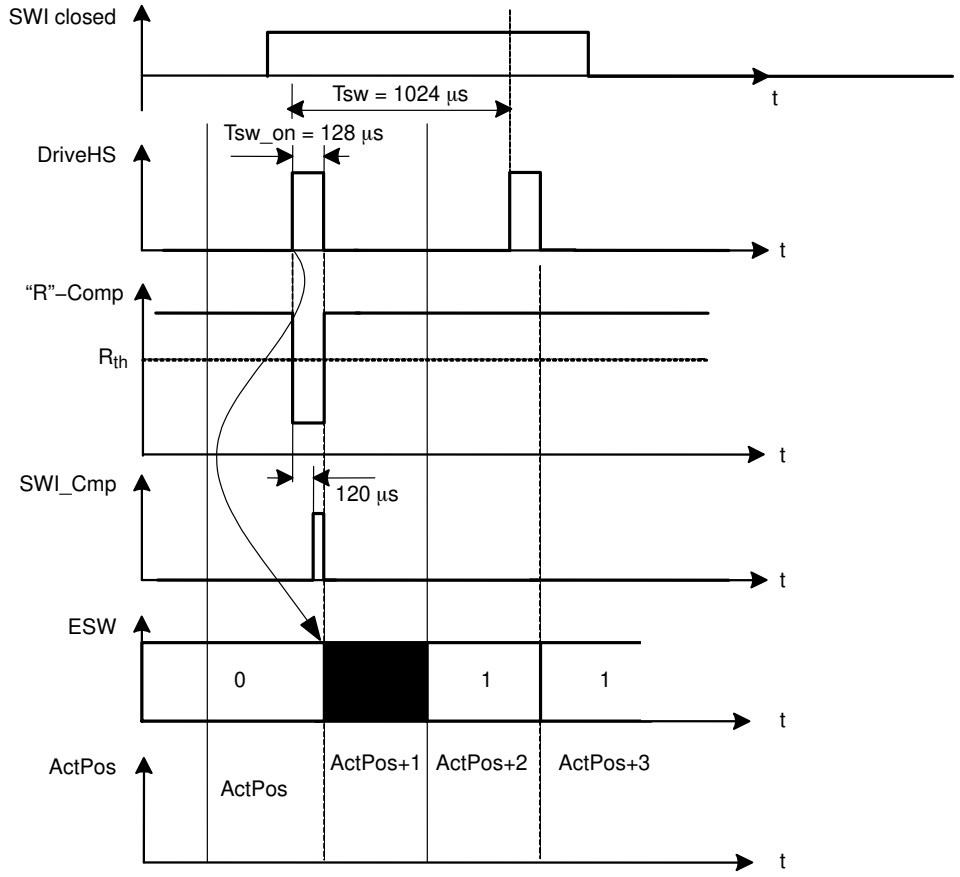


Figure 12. Timing Diagram Showing the Change in States for SWI Comparator

Main Control and Register, OTP memory + ROM

Power−up Phase

Power−up phase of the NCV70627 will not exceed 10 ms. After this phase, the NCV70627 is in standby mode, ready to receive LIN messages and execute the associated commands. After power−up, the registers and flags are in the reset state, while some of them are being loaded with the OTP memory content (see Table 21: RAM Registers).

Reset

After power−up, or after a reset occurrence (e.g. a micro−cut on pin V_{BB} has made V_{DD} to go below VddReset level), the H−bridges will be in high−impedance mode, and the registers and flags will be in a predetermined position. This is documented in Table 21: RAM Registers and Table 22: Flags Table.

Soft−stop

A soft−stop is an immediate interruption of a motion, but with a deceleration phase. At the end of this action, the register <TagPos> is loaded with the value contained in register <ActPos>, (see Table 21: Ram Registers). The circuit is then ready to execute a new positioning command, provided thermal and electrical conditions allow for it.

Sleep Mode

When entering sleep mode, the stepper−motor can be driven to its secure position. After which, the circuit is completely powered down, apart from the LIN receiver, which remains active to detect a dominant state on the bus. In case sleep mode is entered while a motion is ongoing, a transition will occur towards secure position as described in Positioning and Motion Control provided <SecPos> is enabled. Otherwise, <SoftStop> is performed.

Sleep mode can be entered in the following cases:

- The circuit receives a LIN frame with identifier **0x3C** and first data byte containing **0x00**, as required by LIN specification rev 1.3 and <SleepEn> bit = 1. See also Sleep in the LIN Application Command section.
- In case the <SleepEn> bit = 1 and the LIN bus remains inactive (or is lost) during more than 25000 time slots (1.30 s at 19.2 kbit/s), a time−out signal switches the circuit to sleep mode.

The circuit will return to normal mode if a valid LIN frame is received (this valid frame can be addressed to another slave).

Thermal Shutdown Mode

When thermal shutdown occurs, the circuit performs a <SoftStop> command and goes to motor shutdown mode (see Figure 13: State Diagram Temperature Management).

Temperature Management

The NCV70627 monitors temperature by means of two thresholds and one shutdown level, as illustrated in the state diagram and illustration of Figure 13: State Diagram Temperature Management below. The only condition to reset flags <TW> and <TSD> (respectively thermal warning and thermal shutdown) is to be at a temperature lower than Ttw and to get the occurrence of a GetStatus or a GetFullStatus LIN frame.

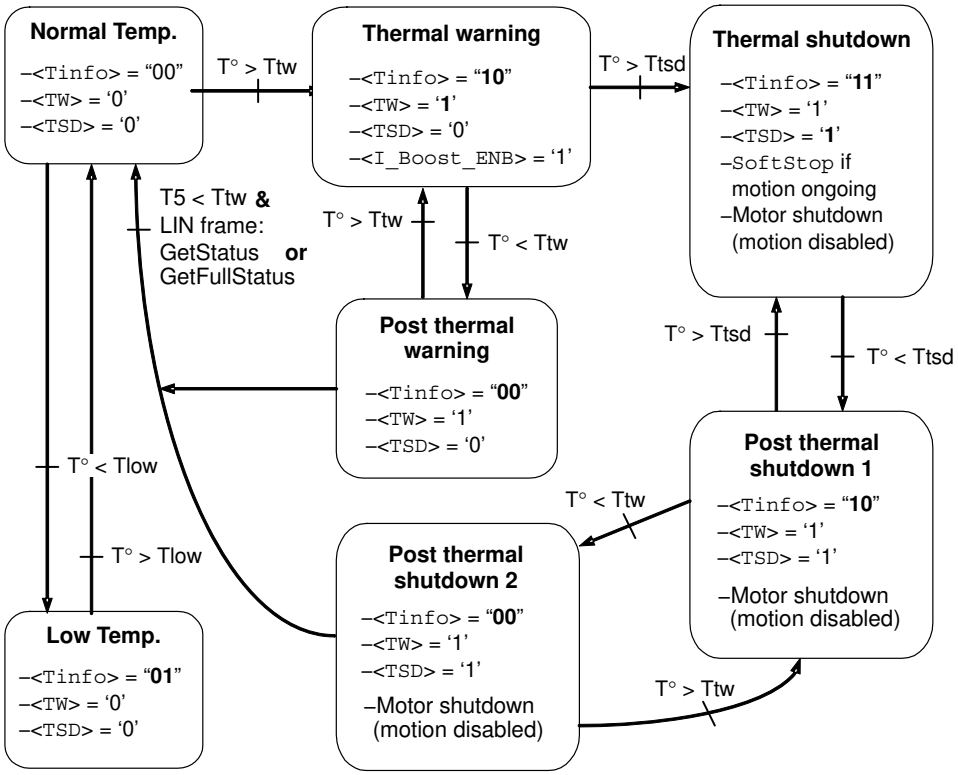


Figure 13. State Diagram Temperature Management

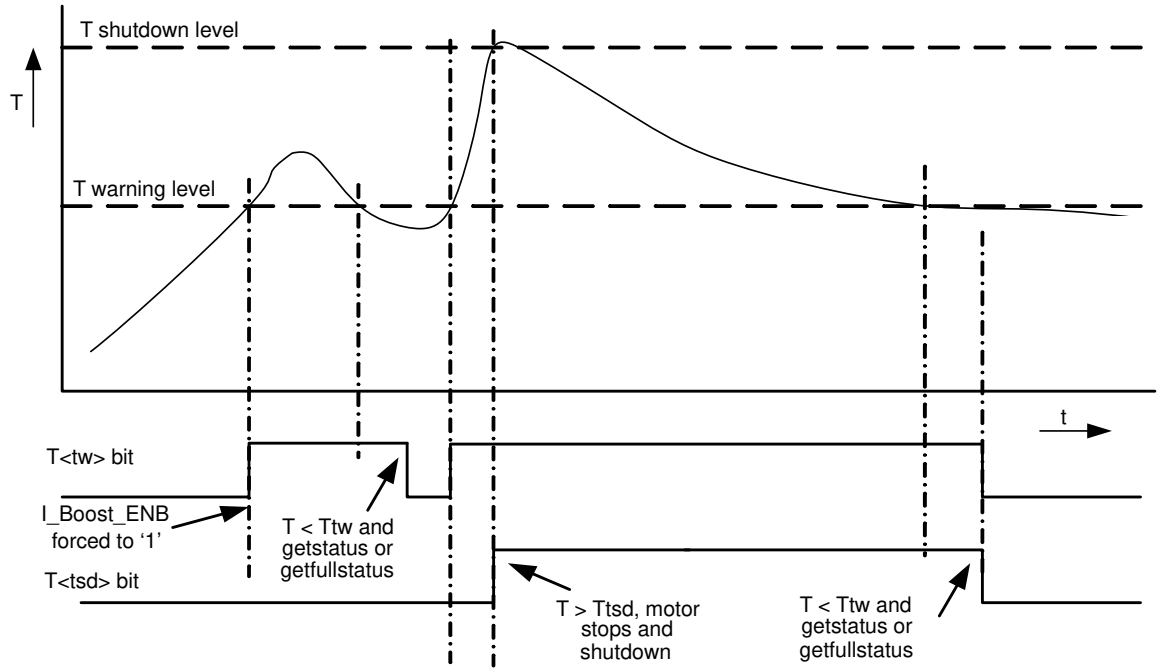


Figure 14. Illustration of Thermal Management Situation

Under−Voltage Condition and Autarkic Functionality

Battery Voltage Management

The NCV70627 monitors the V_{BB} voltage by means of two under voltage threshold UV3 and UV2 and one shutdown level. The only condition to go back to normal operation is to recover by a V_{BB} voltage higher than UV1. The flags <UV2> and <UV3> can only be cleared by receiving the header of a GetStatus or a GetFullStatus command after the V_{BB} voltage higher than UV1.

The UV3 and UV1 levels are programmable by a LIN command. There are 8 levels available for the UV3 threshold voltage. The UV1 level is ratio metric coupled with UV3. UV2 has only a fixed threshold level. Refer to the DC parameter table for the different under voltage levels.

When the battery voltage drops below UV3, the <UV3> flag will be set and a Soft Stop is performed to stop the motion. If during this decelerated motion the battery voltage does not go under the UV2 level, the NCV70627 will go to state <StoppedUnder UV1>" and the original Target Position (TagPos) is saved while the motor is kept in position by the Hold current*. As soon as the V_{BB} voltage rises above the UV1 level the NCV70627 will continue the motion the (TagPos) and will go to the normal <Stopped> state afterwards.

When during a motion the battery voltage drops below the UV2 level, the NCV70627 will stop immediately by a Hard Stop and directly enters the state <HardUnder> followed by <ShutUnder>. The motor is placed in HiZ and the flags <UV2> and <Steploss> are set (see Figure 15).

Note*: In this situation the <Steploss> flag is not set.

Remarks:

If V_{BB} voltage drops below the UV2 level while the NCV70627 is in the motion "stabilization phase", only the <UV2> flag is set; the <Steploss> flag is not set.

When the NCV70627 is in a stopped states <Stopped> or <StoppedUnder UV1> and the V_{BB} voltage drops below UV2 level, the device will directly go to the state <ShutUnder>, but does not raise the <Steppploss> flag.

At the UV3 comparator output, there is implemented an unsymmetrical debouncer which will filter immediate actions during unwanted spikes at the battery supply. For transitions, when supply voltage V_{BB} drops below UV3 level, a 32 μs debouncer is implemented that is derived from the internal oscillator. For transitions when supply voltage V_{BB} rises above UV1 level, the NVC70627 reacts after 96 μs debounce time typically (OTP bit UV3debT is not set). This time is increased to 256 μs when OTP bit UV3debT is zapped to "1". Zapping can be done via the SetOTPparam command.

Autarkic Function

From above described states the device can enter the state <ShutUnder>. When in the <ShutUnder> state, the device will perform the Autarkic Function:

- If in this state V_{BB} becomes > UV1 within 15 seconds, the NCV70627 still will resume the motion to the saved (TagPos) and will go to the <Stopped> state afterwards. It accepts updates of the target position by means of the commands SetPosition, SetPositionShort, SetPosParam and GotoSecurePosition, even if the <UV2> flag and <Steploss> flags are NOT cleared.
- If however the V_{BB} voltage remains below UV2 level voltage level for more than 15 seconds, the device will enter <Shutdown> state and the target position is overwritten by Actual Position. This state can be exited only if V_{BB} is > UV1 voltage level and an incoming command GetStatus or GetFullStatus is received.

Important Notes:

1. In the case of Autarkic positioning, care needs to be taken because accumulated steploss can cause a significant deviation between physical and stored actual position.
2. The SetDualPosition command will only be executed after clearing the <UV2> and <Steploss> flags.
3. RAM reset occurs when Vdd < VddReset (digital Power−On−Reset level).
4. The Autarkic function remains active as long as V_{DD} > VddReset.

OTP Register

OTP Memory Structure

The table below shows how the parameters to be stored in the OTP memory are located.

Table 19. OTP MEMORY STRUCTURE

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	SecPosA	TSD2	TSD1	TSD0	IREF3	IREF2	IREF1	IREF0
0x01	LIN_BR	ADM	BG5	BG4	BG3	BG2	BG1	BG0
0x02	AbsThr3	AbsThr2	AbsThr1	AbsThr0	PA3	PA2	PA1	PA0
0x03	Irun3	Irun2	Irun1	Irun0	Ihold3	Ihold2	Ihold1	Ihold0
0x04	Vmax3	Vmax2	Vmax1	Vmax0	Vmin3	Vmin2	Vmin1	Vmin0
0x05	SecPos10	SecPos9	SecPos8	Shaft	Acc3	Acc2	Acc1	Acc0
0x06	SecPos7	SecPos6	SecPos5	SecPos4	SecPos3	SecPos2	Failsafe	SleepEn
0x07	UV3debT	UV3Thr2	UV3Thr1	UV3Thr0	StepMode1	StepMode0	LOCKBT	LOCKBG
0x08	SecPos10A	SecPos9A	SecPos8A	OSC4	OSC3	OSC2	OSC1	OSC0
0x09	SecPos7A	SecPos6A	SecPos5A	SecPos4A	SecPos3A	SecPos2A	FailsafeA	SleepEnA

Parameters stored at address 0x00 and 0x01 and bit <LOCKBT> are already programmed in the OTP memory at circuit delivery. They correspond to the calibration of the circuit and are just documented here as an indication.

Each OTP bit is at ‘0’ when not zapped. Zapping a bit will set it to ‘1’. Thus only bits having to be at ‘1’ must be zapped. Zapping of a bit already at ‘1’ is disabled. Each OTP byte will be programmed separately (see command SetOTPparam). Once OTP programming is completed, bit <LOCKBG> can be zapped to disable future zapping, otherwise any OTP bit at ‘0’ could still be zapped by using a SetOTPparam command.

Table 20. OTP OVERWRITE PROTECTION

Lock Bit	Protected Bytes
LOCKBT (factory zapped before delivery)	0x00[6:0], 0x01[5:0], 0x08[4:0]
LOCKBG	0x00 to 0x09

The command used to load the application parameters via the LIN bus in the RAM prior to an OTP Memory programming is SetMotorParam. This allows for a functional verification before using a SetOTPparam command to program and zap separately one OTP memory byte. A GetOTPparam command issued after each SetOTPparam command allows verifying the correct byte zapping.

Note: Zapped bits will become active only after a power cycle. After programming the LIN bits the power cycle has to be performed first to guarantee further communication with the device at the new address.

Application Parameters Stored in OTP Memory

Except for the physical address <PA[3:0]> these parameters, although programmed in a non−volatile memory can still be overwritten in RAM by a LIN SetMotorParam writing operation.

PA[3:0] In combination with HW[2:0] it forms the physical address AD[6:0] of the stepper−motor. Up to 128 stepper−motors can theoretically be connected to the same LIN bus.

AbsThr[3:0] Absolute threshold used for the motion detection

Index	AbsThr				AbsThr level (V) (*)
0	0	0	0	0	Disable
1	0	0	0	1	0.6
2	0	0	1	0	1.3
3	0	0	1	1	1.9
4	0	1	0	0	2.6
5	0	1	0	1	3.2
6	0	1	1	0	3.9
7	0	1	1	1	4.5
8	1	0	0	0	5.1
9	1	0	0	1	5.8
A	1	0	1	0	6.4
B	1	0	1	1	7.1
C	1	1	0	0	7.7
D	1	1	0	1	8.3
E	1	1	1	0	9.0
F	1	1	1	1	9.6

(*) Not tested in production. Values are approximations.

UV3Thr [2:0] Under voltage threshold voltage for UV3 and UV1.

Index	UV3Thr			UV3 Level	UV1 Level
0	0	0	0	5.90	6.62
1	0	0	1	6.30	7.07
2	0	1	0	6.70	7.52
3	0	1	1	7.10	7.97
4	1	0	0	7.50	8.41
5	1	0	1	7.90	8.86
6	1	1	0	8.30	9.31
7	1	1	1	8.70	9.76

Irun[3:0] Current amplitude value to be fed to each coil of the stepper−motor. The table below provides the 16 possible values for <IRUN>.

Index	Irun				Run Current (mA)	Run Boost Current (mA)
0	0	0	0	0	59	81
1	0	0	0	1	71	98
2	0	0	1	0	84	116
3	0	0	1	1	100	138
4	0	1	0	0	119	164
5	0	1	0	1	141	194
6	0	1	1	0	168	231
7	0	1	1	1	200	275
8	1	0	0	0	238	327
9	1	0	0	1	283	389
A	1	0	1	0	336	462
B	1	0	1	1	400	550
C	1	1	0	0	476	655
D	1	1	0	1	566	778
E	1	1	1	0	673	925
F	1	1	1	1	800	1100

Ihold[3:0] Hold current for each coil of the stepper−motor. The table below provides the 16 possible values for <IHOLD>.

Index	Ihold				Hold Current (mA)	Hold Boost Current (mA)
0	0	0	0	0	59	81
1	0	0	0	1	71	98
2	0	0	1	0	84	116
3	0	0	1	1	100	138
4	0	1	0	0	119	164
5	0	1	0	1	141	194
6	0	1	1	0	168	231
7	0	1	1	1	200	275
8	1	0	0	0	238	327
9	1	0	0	1	283	389
A	1	0	1	0	336	462
B	1	0	1	1	400	550
C	1	1	0	0	476	655
D	1	1	0	1	566	778
E	1	1	1	0	673	925
F	1	1	1	1	0	0

Note: When the motor is stopped, the current is reduced from <IRUN> to <IHOLD>. In the case of 0 mA hold current (1111 in the hold current table), the following sequence is applied:

1. The current is first reduced to 59 mA or 81 mA during I_Boost function (corresponding to 0000 value in the table).
2. The PWM regulator is switched off; the bottom transistors of the bridges are grounded.

Step Mode Setting of step modes.

Step Mode		Step Mode
0	0	1/2 stepping
0	1	1/4 stepping
1	0	1/8 stepping
1	1	1/16 stepping

Shaft This bit distinguishes between a clock−wise or counter−clock−wise rotation.

SecPos[10:2] Secure Position of the stepper−motor. This is the position to which the motor is driven in case of a LIN communication loss or when the LIN error−counter overflows. If <SecPos[10:2]> = “100 0000 00xx”, secure positioning is disabled for the FailSafe function and the SetDualPosition command while it is not disabled for the GotoSecurePosition and even is still executed for the position “100 0000 00xx”.

Note: The Secure Position is coded on 11 bits only, providing actually the most significant bits of the position, the non coded least significant bits being set to ‘0’. The Secure Position in OTP has only 9 bits. The two least significant bits are loaded as ‘0’ to RAM when copied from OTP.

SecPosA If <SecPosA> = 0 then <SecPos[10:2]>, <Failsafe> and <SleepEn> stored in bytes 0x05 and 0x06 are used during operation
If <SecPosA> = 1 then <SecPos[10:2]>, <Failsafe> and <SleepEn> stored in bytes 0x08 and 0x09 are used during operation

Programming SecPosA with “1” makes the OTP bytes 0x05 and 0x06 obsolete. In this case the OTP bytes at 0x08 and 0x09 will be read at the positions of bytes 0x05 and 0x06 when reading the OTP via the GetOTPparam command.