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NCV7471, NCV7471A

System Basis Chip with a High-Speed CAN, Two LINs and a Boost-Buck DC/DC Converter

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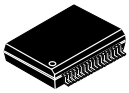
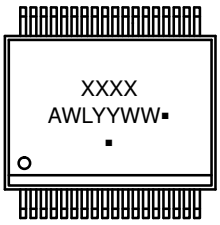


SSOP36−EP
DQ SUFFIX
CASE 940AB

MARKING DIAGRAM



XXXX = NCV7471−5 or NCV7471A−5
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

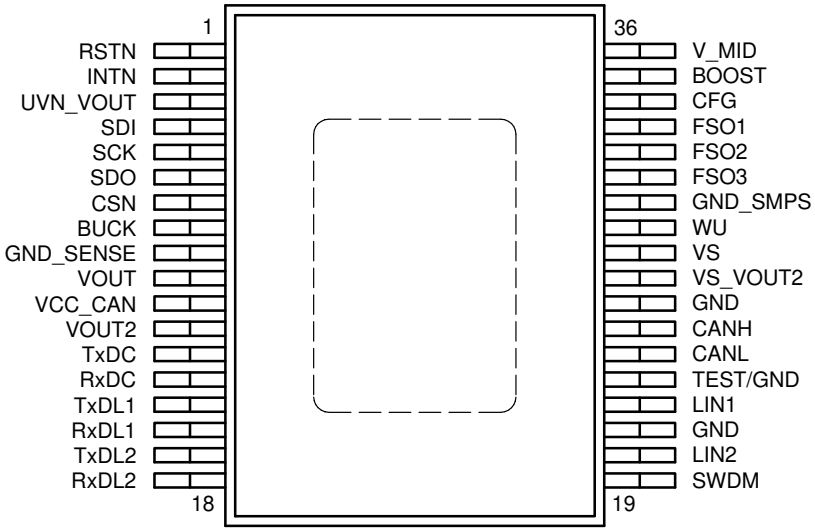
ORDERING INFORMATION

See detailed ordering and shipping information on page 50 of this data sheet.

NCV7471(A) is a System Basis Chip (SBC) integrating functions typically found in automotive Electronic Control Units (ECUs) in the body domain. NCV7471 provides and monitors the low−voltage power supplies for the application microcontroller and other loads, monitors the application software via a watchdog and includes high−speed CAN and LIN transceivers allowing the ECU to host multiple communication nodes or to act as a gateway unit. The on−chip state controller ensures safe power−up sequence and supports low−power modes with a configurable set of features including wakeup from the communication buses or by a local digital signal WU. The status of several NCV7471(A) internal blocks can be read by the microcontroller through the serial peripheral interface or can be used to generate an interrupt request.

Features

- Control Logic
  - Ensures safe power−up sequence and the correct reaction to different supply conditions
  - Controls mode transitions including the power management and wakeup treatment − bus wakeups, local wakeups (via WU pin) and cyclic wakeups (through the on−chip timer)
  - Generates reset and interrupt requests
- Serial Peripheral Interface
  - Operates with 16−bit frames
  - Ensures communication with the ECU's microcontroller unit
  - Mode settings, chip status feedback and watchdog are accessible through eight twelve−bits registers
- 5 V VOUT Supply from a DC/DC Converter
  - Can deliver up to 500 mA with accuracy of ±2%
  - Supplies typically the ECU's microcontroller
- 5 V VOUT2 Low−drop Output Regulator
  - Can supply external loads – e.g. sensors
  - Controlled by SPI and the state machine
  - Protected against short to the car battery
- A High−speed CAN Transceiver
  - ISO11898−2 and ISO11898−5 compliant
  - Communication speed up to 1 Mbps
  - TxD dominant time−out protection
- Two LIN Transceivers
  - LIN2.X and J2602 compliant
  - TxD dominant time−out protection
- Wakeup Input WU
  - Edge−sensitive high−voltage input
  - Can be used as a wake−up source or as a logical input polled through SPI
- Protection and Monitoring Functions
  - Monitoring of the main supply through the V_MID point
  - Monitoring of VOUT supply output with programmable threshold
  - VOUT2 supply diagnosis through SPI and interrupt
  - Thermal warning and thermal shutdown protection
  - Programmable watchdog monitoring the ECU software
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



Pin Connections

Table of Contents

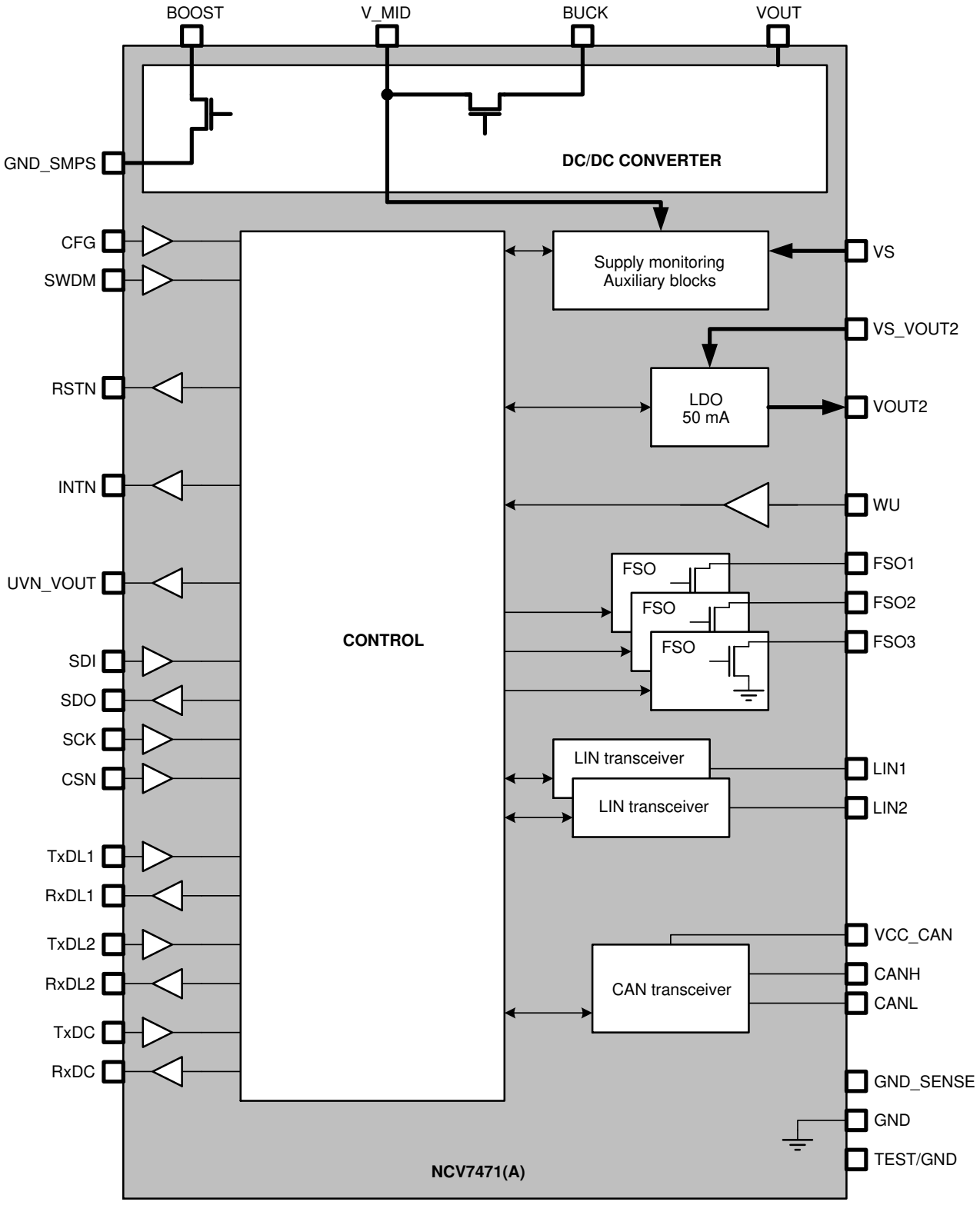


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Pin Type (LV = Low Voltage; HV = High Voltage)	Pin Function
1	RSTN	LV digital input/output; open drain; internal pull−up	System reset
2	INTN	LV digital output; open drain; internal pull−up	Interrupt request to the MCU
3	UVN_VOUT		VOUT under−voltage signal to the MCU
4	SDI	LV digital input; internal pull−down	SPI data input
5	SCK	LV digital input; internal pull−down	SPI clock input
6	SDO	LV digital output; push−pull with tri−state	SPI data output
7	CSN	LV digital input (HV tolerant); internal pull−up	SPI chip select input
8	BUCK	HV analog input/output	Connection of L_{buck} coil to the integrated serial switch
9	GND_SENSE	Ground connection	Ground sense for the internal circuitry (e.g. VOUT2 regulator)
10	VOUT	LV supply input	Feedback of the DC/DC converter output; main 5 V LV supply for the digital IO's
11	VCC_CAN	LV supply input	Core supply for the CAN transceiver
12	VOUT2	LV supply output	Output of the 5 V/50 mA low−drop regulator for external loads
13	TxDC	LV digital input; internal pull−up	Input of the data to be transmitted on CAN bus
14	RxDC	LV digital output; push−pull	Output of data received from CAN bus
15	TxDL1	LV digital input; internal pull−up	Input of the data to be transmitted from LIN1 bus
16	RxDL1	LV digital output; push−pull	Output of data received on LIN1 bus
17	TxDL2	LV digital input; internal pull−up	Input of the data to be transmitted from LIN2 bus
18	RxDL2	LV digital output; push−pull	Output of data received on LIN2 bus
19	SWDM	HV digital input; internal pull−down	Input to select the SW Development configuration
20	LIN2	LIN bus interface	LIN2 bus line
21	GND	Ground connection	Ground connection
22	LIN1	LIN bus interface	LIN1 bus line
23	TEST/GND	LV digital input; internal pull−down	Test−mode entry pin for production testing; should be grounded in the application
24	CANL	CAN bus interface	CANL line of the CAN bus
25	CANH	CAN bus interface	CANH line of the CAN bus
26	GND	Ground connection	Ground connection
27	VS_VOUT2	HV supply input	Separate line input for the VOUT2 low−drop regulator
28	VS	HV supply input	Line supply for the battery−related core blocks
29	WU	HV digital input	Input for monitoring of external contacts
30	GND_SMPS	Ground connection	Power ground connection for the DC/DC converter
31	FSO3	HV digital output; open drain low−side	Indication of a fail−safe event by rectangular signal of 100 Hz with 20% duty cycle; high−impedant in normal operation
32	FSO2	HV digital output; open drain low−side	Indication of a fail−safe event by rectangular signal of 1.25 Hz with 50% duty cycle; high−impedant in normal operation
33	FSO1	HV digital output; open drain low−side	Indication of a fail−safe event by static Low level; high−impedant in normal operation
34	CFG	HV digital input; internal pull−down	Configuration of fail−safe behavior; in SW Development, CFG enables boost stage operation
35	BOOST	HV analog input/output	Connection of L_{boost} coil to the integrated switch to ground.
36	V_MID	HV analog input/output	Intermediate point connecting the step−up and step−down stages of the DC/DC converter

APPLICATION INFORMATION

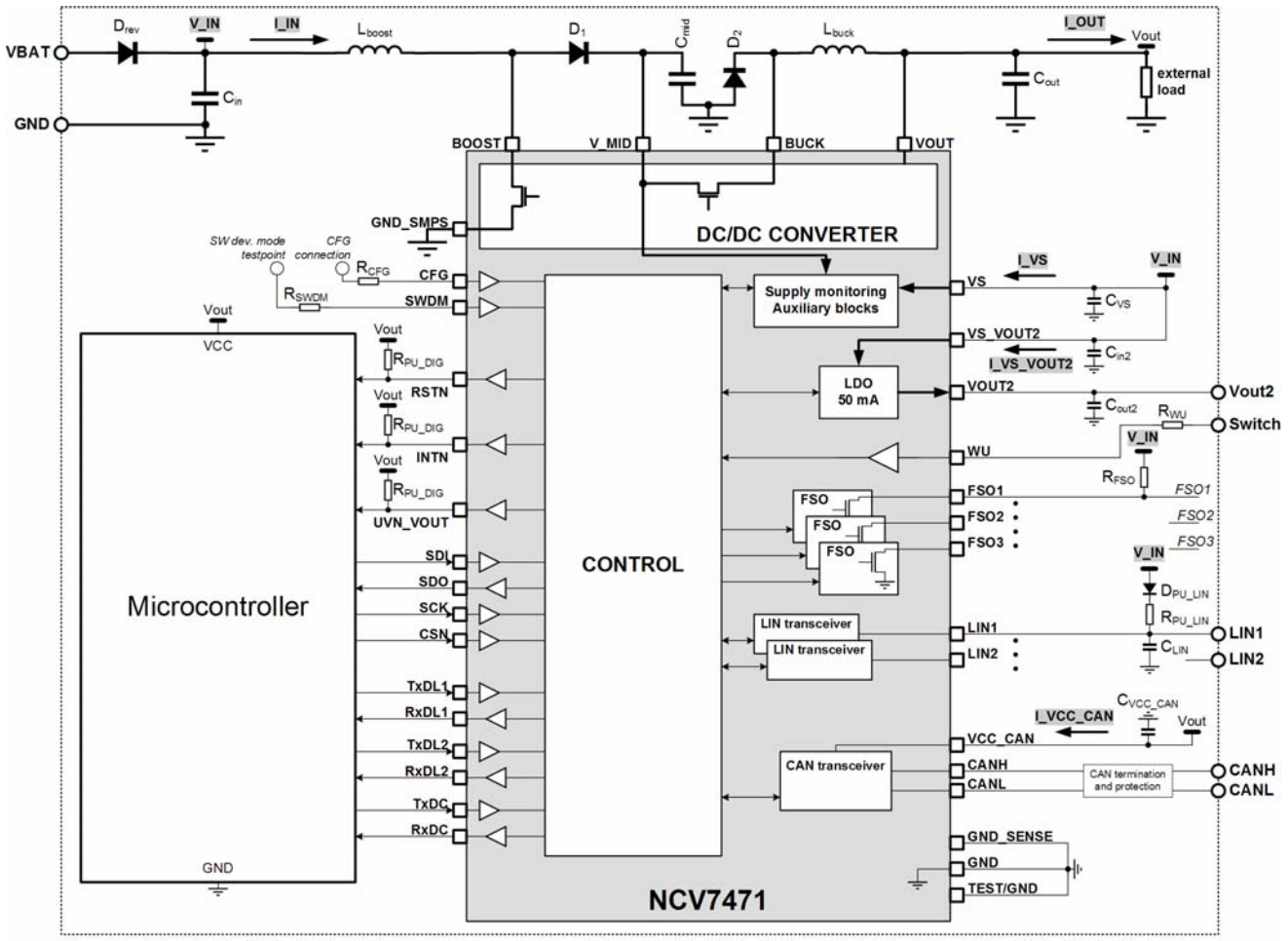


Figure 2. Example Application Diagram

External Components

Overview of external components from application schematic in Figure 2 is given in Table 2 together with their recommended or required values.

Table 2. EXTERNAL COMPONENTS OVERVIEW

Component Name	Description	Value	Note
D_{rev}	Reverse−protection diode	parameters application−specific; e.g. 0.5 A / 50 V	Values and types depend on the application needs and conditions. Guidelines for their selection can be found in the product's application note. The given examples are suitable for VOUT loads of up to 250 mA, and for V_IN above 3.3 V.
C_{in}	Filtering capacitor for the DC/DC converter input	≥ 1 μF ceramic; e.g. 1 μF / 40 V	
L_{boost}	Inductor for the converter boost stage; EMC filtering inductance	recommended range 3.3 μH – 10 μH; e.g. 3.3 μH / 0.77 A, type B82422H1332+000	
D_1	Diode for the converter boost stage	Shottky or ultra−fast; parameters application−specific; e.g. 0.5 A / 50 V	
C_{mid}	Filtering and stabilization capacitor for the converter intermediate voltage	≥ 1 μF ceramic; e.g. 1 μF / 40 V	
D_2	Diode for the converter buck stage	Shottky or ultra−fast; parameters application−specific; e.g. 0.25 A / 50 V	
L_{buck}	Inductor for the converter buck stage	recommended range 10 μH – 22 μH; e.g. 10 μH / 0.5 A, type B82422H1103+000	
C_{out}	Filtering and stabilization capacitor for the converter output voltage	≥ 10 μF ceramic; e.g. 10 μF / 10 V	
C_{VS}	Filtering capacitor for the VS input supplying LIN and auxiliary internal circuitry	recommended >100 nF ceramic	optional; depends on the application PCB
C_{in2}	Filtering capacitor for the VOUT2 regulator input	recommended >100 nF ceramic	optional; depends on the application PCB
C_{out2}	Filtering and stabilization capacitor for the VOUT2 regulator output	>1 μF ceramic (recommended 2.2 μF nominal)	required for VOUT2 stability
R_{WU}	Protection and filtering resistor for the WU input	recommended 33 kΩ nominal	optional; depends on the application needs
R_{FSO}			depends on the application needs
D_{PU_LIN}	Pull−up diode on LIN line		required only for master LIN node
R_{PU_LIN}	Pull−up resistor on LIN line	1 kΩ nominal	
C_{LIN}	Filtering capacitor on LIN line	Typically 100 pF – 220 pF nominal	optional; is function of the entire LIN network
C_{VCC_CAN}	Filtering capacitor on the CAN transceiver supply input	recommended >100 nF ceramic	optional; depends on the application PCB
CAN termination and protection			optional; is function of the entire CAN network
R_{PU_DIG}	Pull−up resistor for the open−drain digital outputs (INTN, RSTN, UVN_VOUT)	recommended 10 kΩ nominal	optional; only if the integrated pull−ups are not sufficient for the application
R_{SWDM}	Protection resistor on SWDM input	recommended 10 kΩ nominal	optional; depends on the application
R_{CFG}	Protection resistor on CFG input	recommended 10 kΩ nominal	optional; depends on the application CFG connection details can be found in the product's application note.

FUNCTIONAL DESCRIPTION

POWER SUPPLIES

VS Supply Input

VS pin of NCV7471(A) is typically connected to the car battery through a reverse−protection diode and can be exposed to all relevant automotive disturbances (ISO7637 pulses, system ESD...). VS supplies mainly the integrated LIN transceivers. Filtering capacitors should be connected between VS and GND.

V_MID Supply Point

V_MID node is the connection point between the two stages of the DC/DC converter. If only the buck (i.e. step−down) function of the converter is active (because the input voltage is sufficient or because boosting is not enabled), V_MID level stays two diode drops below the battery input to the application – see Figure 2. In case the boost stage of the converter is active, V_MID voltage is regulated to *V_MID_reg* (6.5 V typically).

V_MID pin is used to supply the core auxiliary blocks of the device – namely the voltage reference, biasing, internal regulator and the wakeup detector of the CAN bus. When the DC/DC converter is boosting, it is ensured that the internal core blocks remain functional even for low input supply level.

During power−up of the battery supply, V_MID point must reach *V_MID_PORH* level in order for the circuit to become functional – the internal state machine is initiated and the converter is activated in buck−only mode. The circuit remains functional until V_MID falls back below *V_MID_PORL* level, when the device enters the Shut−down mode.

VOUT DC/DC Converter

The main application low−voltage supply is provided by an integrated boost−buck DC/DC converter, delivering a 5 V output VOUT. The converter can work in two modes:

- **Buck−only mode** is the default mode of the VOUT power−supply. In this mode, the boosting part of the converter is never activated and the resulting VOUT voltage can be only lower than the input line voltage. Buck−only mode is applied during the initial power−up (after the V_IN connection), wakeup from Sleep−mode and also recovery from the Fail−safe mode.
- **Boost−buck mode** ensures that the correct VOUT voltage is generated even if the input line voltage falls below the required VOUT level. This mode can be requested through the corresponding SPI control register. If selected, the boost−buck mode is used during Reset, Start−up, Normal, Standby, and Flash modes. It is also preserved during VOUT under−voltage recovery through Power−up mode. In SW Development configuration, boost−buck mode can be additionally enabled by High level on CFG pin. No SPI communication is therefore necessary to select the DC/DC mode in SW Development – see Table 3.

Table 3. CONTROL OF DC/DC CONVERTER MODES (“X” Means “Don’t Care”)

Device Configuration	SPI enBOOST Bit	Signal on CFG Pin	Applied DC/DC Mode
Config 1, 2, 3, 4	Low	X	Buck−Only
	High		Boost−Buck
SW Development	Low	Low	Buck−Only
		High	Boost−Buck
	High	X	Boost−Buck

By default, the converter works with a fixed switching frequency *fsw_DCDC* (typ. 485 kHz). Through the SPI settings, a switching frequency modulation can be applied with fixed modulation frequency of 10 kHz and three selectable modulation depth values – 10%, 20% or 30% of the nominal frequency.

VOUT level is monitored by an under−voltage detector with multiple thresholds:

- Comparison with selectable threshold *VOUT_RESx*. By default, the lowest threshold (typ. 3.1 V) applies for the state machine control and the activation of the RSTN signal. This reset threshold can be changed via SPI to any of the four programmable values.
- A second monitoring signal – UVN_VOUT – is generated based on comparison of the VOUT level with the highest monitoring level (typ. 4.65 V).
- VOUT is compared with a fixed threshold *VOUT_FAIL* (typ. 2 V). If VOUT stays below *VOUT_FAIL* level for longer than *t_VOUT_powerup*, a VOUT short−circuit is detected and Fail−safe mode is entered with the corresponding fail−safe information stored in SPI.

Both UVN_VOUT and RSTN pins provide an open drain output with integrated pull−up resistor. The split between reset−generating level VOUT_RESx and an under−voltage indication allows coping with VOUT dips in case of high loads coinciding with low input line voltages. The function of the VOUT and V_MID monitoring is illustrated in Figure 3 and Figure 4. FSO1 output activation and Fail−safe mode entry caused by VOUT undervoltage are shown in Figure 5 and Figure 6 (NCV7471A only).

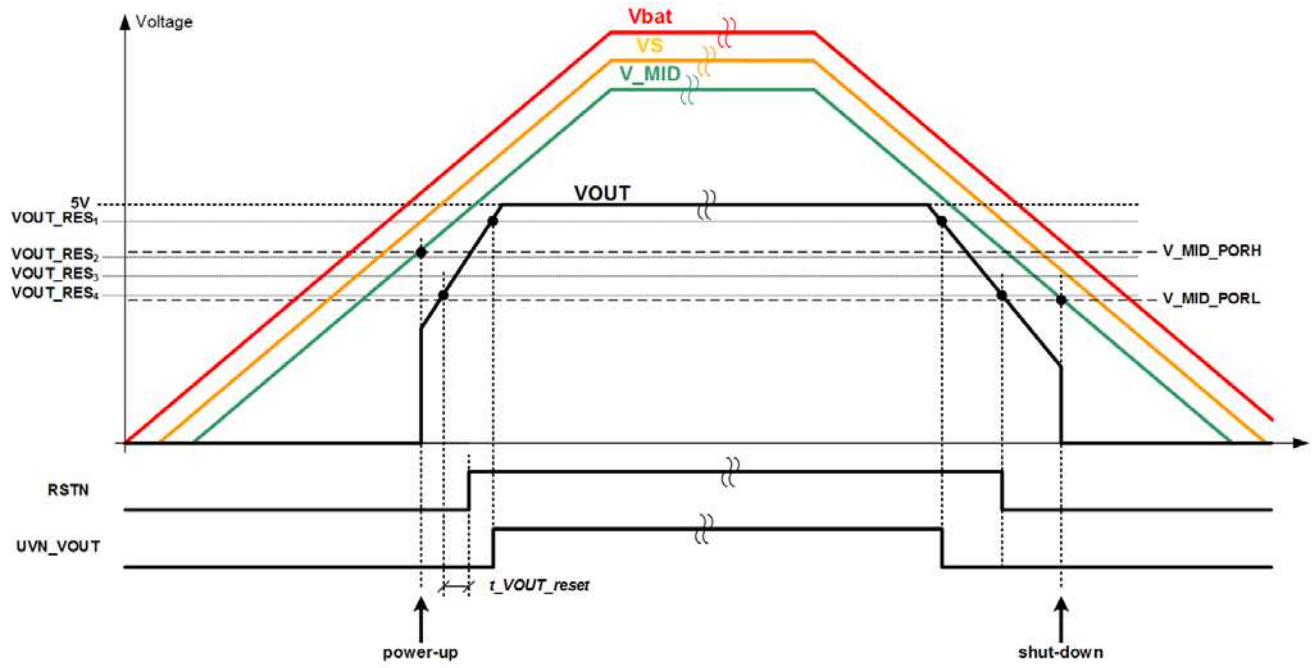


Figure 3. V_MID and VOUT Supply Monitoring (Filtering times are neglected)

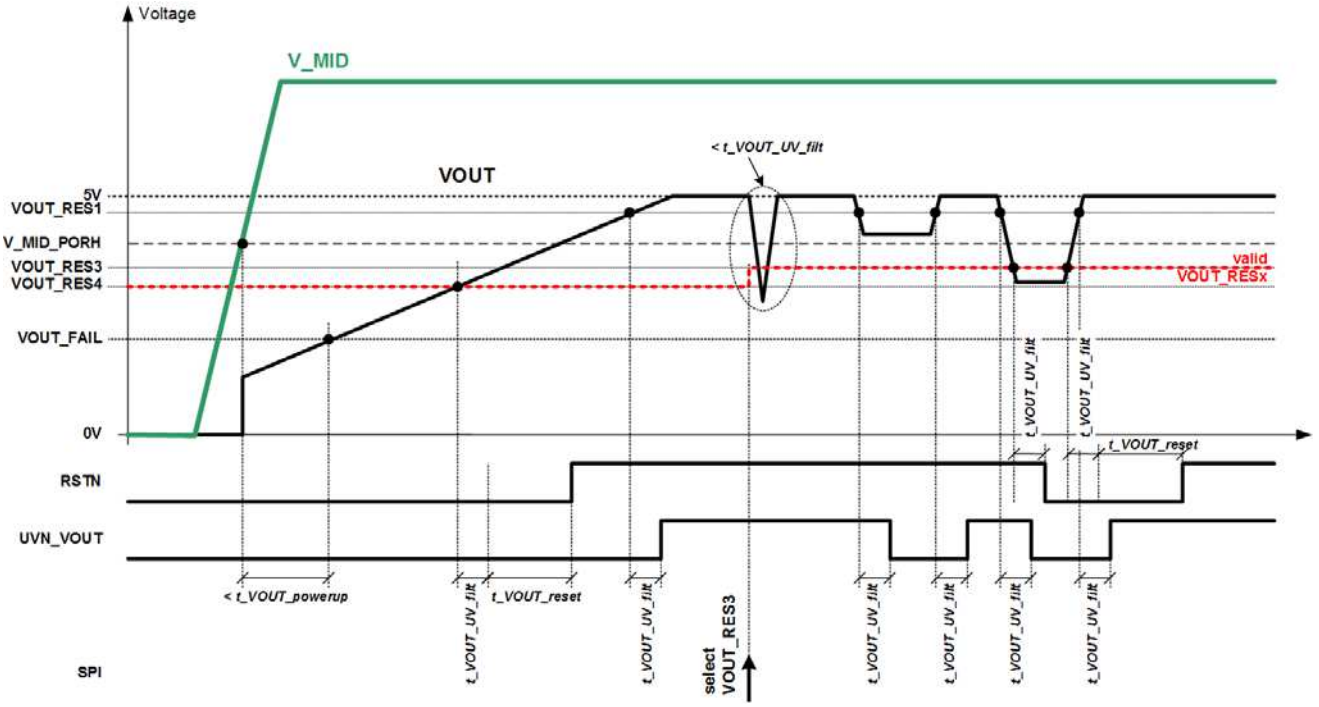


Figure 4. VOUT Monitoring

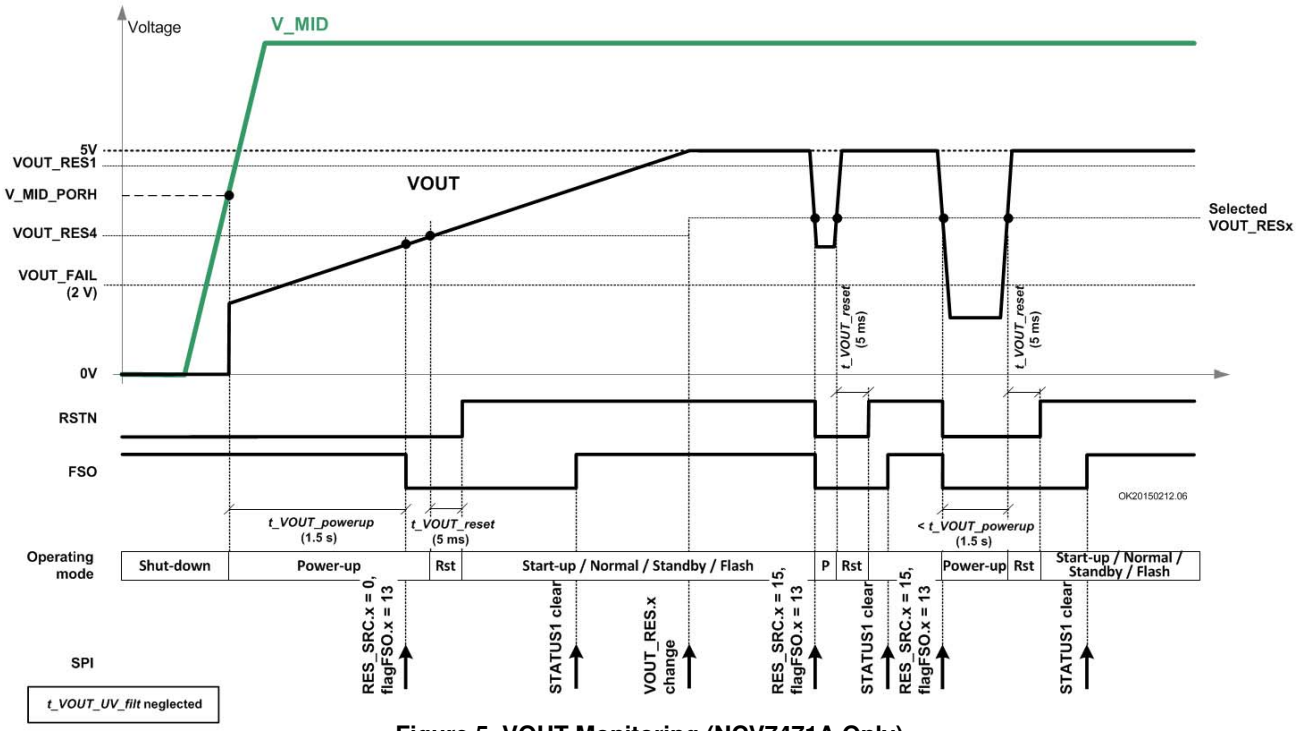


Figure 5. VOUT Monitoring (NCV7471A Only)

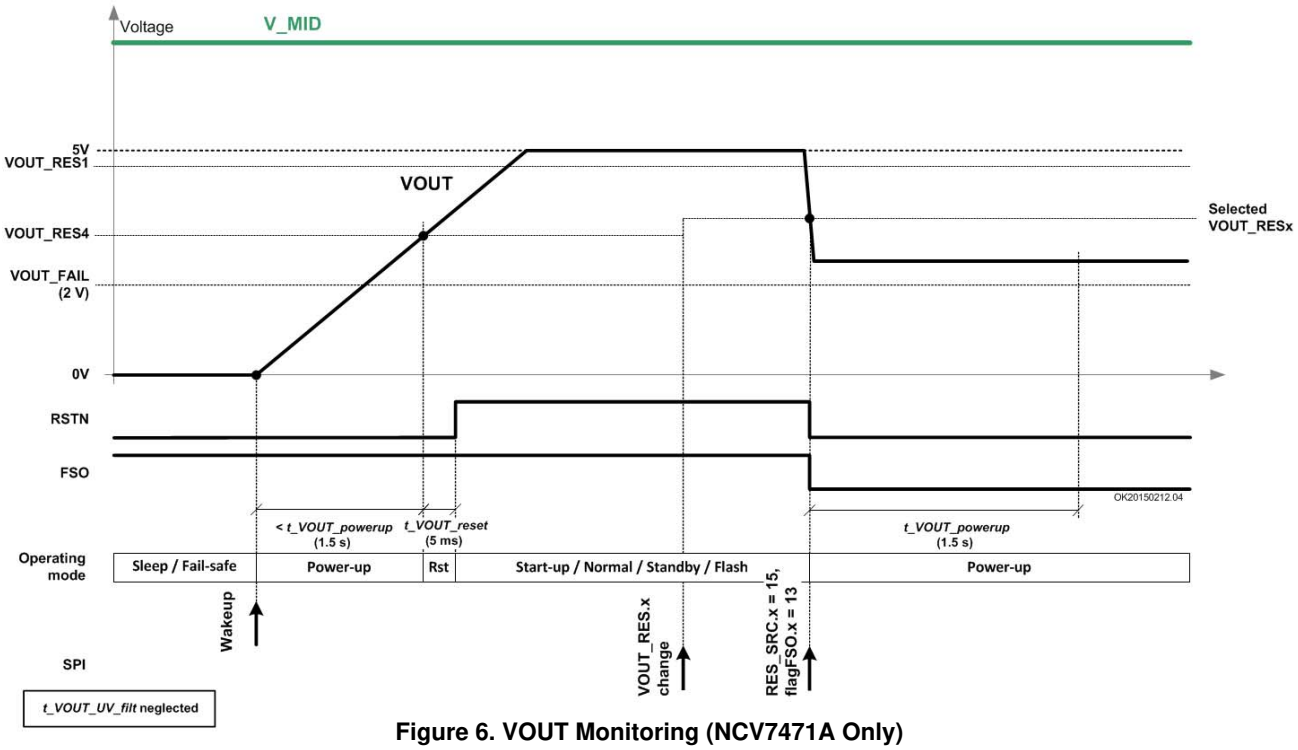


Figure 6. VOUT Monitoring (NCV7471A Only)

VOUT2 Auxiliary Supply

An integrated low−drop regulator provides a second 5 V supply VOUT2 to external loads, typically sensors. The regulator's input is taken from a dedicated pin VS_VOUT2, which does not feature an explicit under−voltage monitoring. VS_VOUT2 would be typically connected to the VS pin or, in function of the application needs, might be taken from other nodes like, e.g., the DC/DC converter's auxiliary node V_MID.

After a power−up or a reset event, as well as in Sleep mode, VOUT2 regulator is switched off. In Start−up, Normal, Standby and Flash modes, it can be freely activated or deactivated via SPI control register.

VOUT2 is diagnosed for under−voltage and over−voltage via comparators with fixed thresholds *VOUT2_UV* and *VOUT2_OV*, respectively. Under−voltage detection is working only when VOUT2 regulator is on, while the over−voltage is monitored regardless the VOUT2 regulator activation. Output of both detectors can be polled via SPI status bits. Change of the detection status (in either direction) is recorded as an SPI flag bit and, if enabled, can lead to an interrupt.

VCC_CAN Transceiver Supply

The integrated CAN transceiver uses a dedicated supply input VCC_CAN. The transceiver is supplied by VCC_CAN when configured for full−speed transmission or reception. When configured for wakeup detection, the transceiver is internally supplied from the V_MID pin.

A 5 V supply must be externally connected to VCC_CAN pin for the correct transceiver's functionality in full−speed mode ("CAN Normal" or "CAN Receive−only"). VCC_CAN input has no dedicated monitoring and its correct level shall be ensured by the application – e.g. if VOUT is connected to VCC_CAN, then VOUT under−voltage monitoring can also cover the correct VCC_CAN level.

Communication Transceivers

High−Speed CAN Transceiver

NCV7471(A) contains a high−speed CAN transceiver compliant with ISO11898−2 and ISO11898−5 standards, consisting of a transmitter, receiver and wakeup detector. The CAN transceiver can be connected to the bus line via a pair of pins CANH and CANL, and to the digital control through pins TxDC and RxDC. The functional mode of the CAN transceiver depends on the chip operating mode and on the status of the corresponding SPI bits – see Table 4, Table 5 and Figure 7.

Table 4. CAN TRANSCEIVER SPI CONTROL

SPI Control Bits		CAN Transceiver Function in Operating Modes				
modCAN.1	modCAN.0	Power−up Reset	Start−up Normal Flash	Standby	Sleep	Fail−safe (except thermal shut−down)
0	0	CAN Off	CAN Off	CAN Off	CAN Off	CAN Wakeup
0	1	CAN Off	CAN Wakeup	CAN Wakeup	CAN Wakeup	CAN Wakeup
1	0	CAN Off	CAN Receive−only	CAN Receive−only	CAN Off	CAN Wakeup
1	1	CAN Off	CAN Normal	CAN Off	CAN Off	CAN Wakeup

Table 5. CAN TRANSCEIVER MODES

Mode	Transceiver	RxDC Pin	TxDC Pin	CANH/CANL Pins	Supply
CAN Off	Fully off	High (if VOUT available)	Ignored	Biased to GND	n.a.
CAN Wakeup	Wakeup detector active	Low if wakeup detected; High otherwise (if VOUT available)	Ignored	Biased to GND	V_MID
CAN Receive−Only	Receiver active	Received data	Ignored	Biased to VCC_CAN/2	VCC_CAN
CAN Normal	Transmitter and Receiver active	Received data	Data to transmit; checked for time−out	Biased to VCC_CAN/2	VCC_CAN

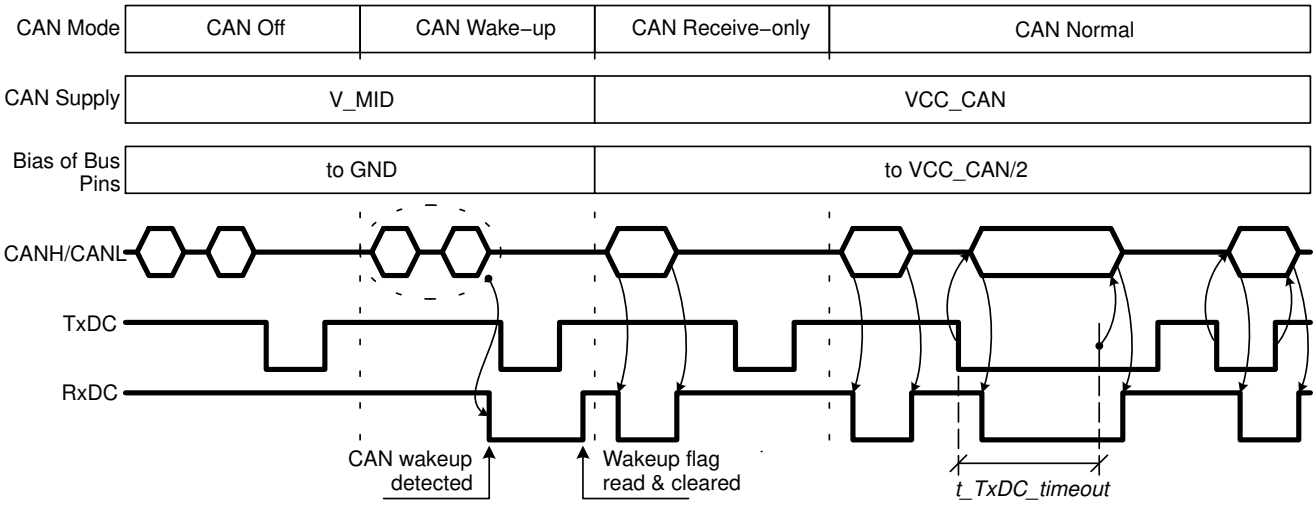


Figure 7. CAN Transceiver Modes

In **CAN Off** mode, the CAN transceiver is fully deactivated. Pin RxDC stays High (as long as VOUT is provided) and logical level on TxDC is ignored. The bus pins are weakly biased to ground via the input impedance.

In **CAN Wakeup** mode, the CAN transceiver, being supplied purely from V_MID pin, detects wakeups on the CAN lines. A valid wakeup on the CAN bus corresponds to a pattern of two dominants at least *t_CAN_wake_dom* long, interleaved by a recessive at least *t_CAN_wake_rec* long. The total length of the pattern may not exceed *t_CAN_wake_timeout.* The CAN wakeup handling is illustrated in Figure 8.

In function of the current operating mode, a CAN wakeup can lead either to an interrupt request or to a reset. A CAN wakeup is also indicated by a Low level on the RxDC pin (which otherwise stays High as long as VOUT is available). Logical level on TxDC pin is ignored. The bus pins remain weakly biased to ground in the wakeup CAN mode.

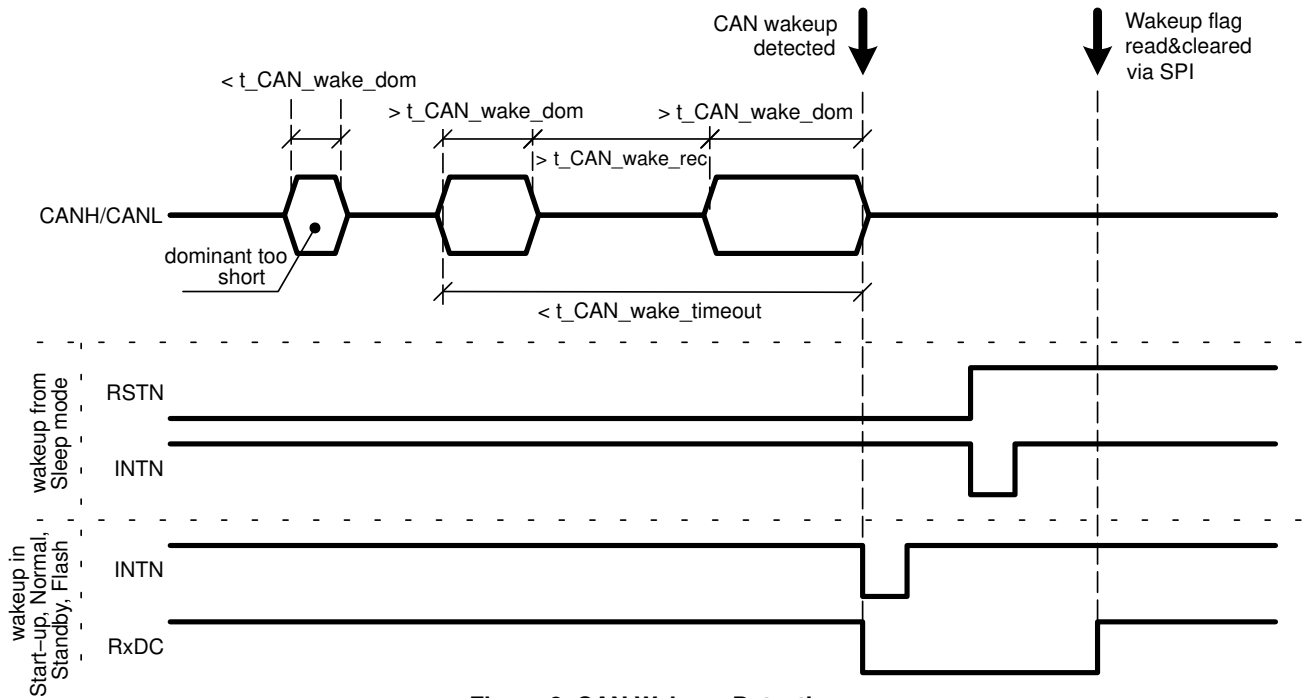


Figure 8. CAN Wakeup Detection

In **CAN Receive−Only** mode, the receiver part of the CAN block detects data on the bus with the full speed and signals them on the RxDC pin. Logical level on TxDC pin is ignored. The receiver is supplied from the VCC_CAN supply input. The bus pins are biased to VCC_CAN/2 level through the input circuitry.

In **CAN Normal** mode, the full CAN transceiver functionality is available. Both reception and transmission at the full speed can be used. Received data are signaled via RxDC pin, while logical level on TxDC pin is translated into the corresponding bus level (TxDC = High or Low leading to a recessive or dominant being transmitted, respectively). Both the receiving and the transmitting part are supplied from the VCC_CAN supply input. The bus pins are biased to VCC_CAN/2 level through the input circuitry. TxDC input signal is monitored with a time−out timer. If a dominant longer than *t_TxDC_timeout* is requested (i.e. TxDC is Low for longer than *t_TxDC_timeout*), the transmission is internally disabled. The reception from the CAN bus remains functional and the internally set CAN transceiver mode does not change. The transmission is again enabled when TxDC becomes High.

LIN Transceivers

NCV7471(A) integrates two on−chip LIN transceivers − interfaces between physical LIN buses and the LIN protocol controllers compatible to LIN2.1 and J2602 specifications − consisting of a transmitter, receiver and wakeup detector. Each LIN transceiver can be connected to the bus line via LINx pin, and to the digital control through pins TxDLx and RxDLx. The functional mode of the LIN transceivers depends on the chip operating mode and on the status of the corresponding SPI bits − see Table 6, Table 7, and Figure 9. The LIN transceivers are supplied directly from the VS pin.

Table 6. LIN TRANSCEIVERS SPI CONTROL

SPI Control Bits x = 1 ... 2		LINx Transceiver Function in Operating Modes				
modLINx.1	**modLINx.0**	**Power−up Reset**	**Start−up Normal Flash**	**Standby**	**Sleep**	**Fail−safe (except thermal shut−down)**
0	0	LINx Off	LINx Off	LINx Off	LINx Off	LINx Wakeup
0	1	LINx Off	LINx Wakeup	LINx Wakeup	LINx Wakeup	LINx Wakeup
1	0	LINx Off	LINx Receive−only	LINx Receive−only	LINx Off	LINx Wakeup
1	1	LINx Off	LINx Normal	LINx Normal	LINx Off	LINx Wakeup

Table 7. LIN TRANSCEIVERS MODES

Mode	Transceiver	RxDLx Pin	TxDLx Pin	LINx Pin Bias
LINx Off	Fully off	High (if VOUT available)	Ignored	Pull−up current source to VS
LINx Wakeup	Wakeup detector active	Low if wakeup detected; High otherwise (if VOUT available)	Ignored	Pull−up current source to VS
LINx Receive−Only	Receiver active	Received data	Ignored	Pull−up current source to VS
LINx Normal	Transmitter and Receiver active	Received data	Data to transmit; checked for time−out (if enabled via SPI); transmitted if VS>*VS_MON*	30 kΩ pull−up

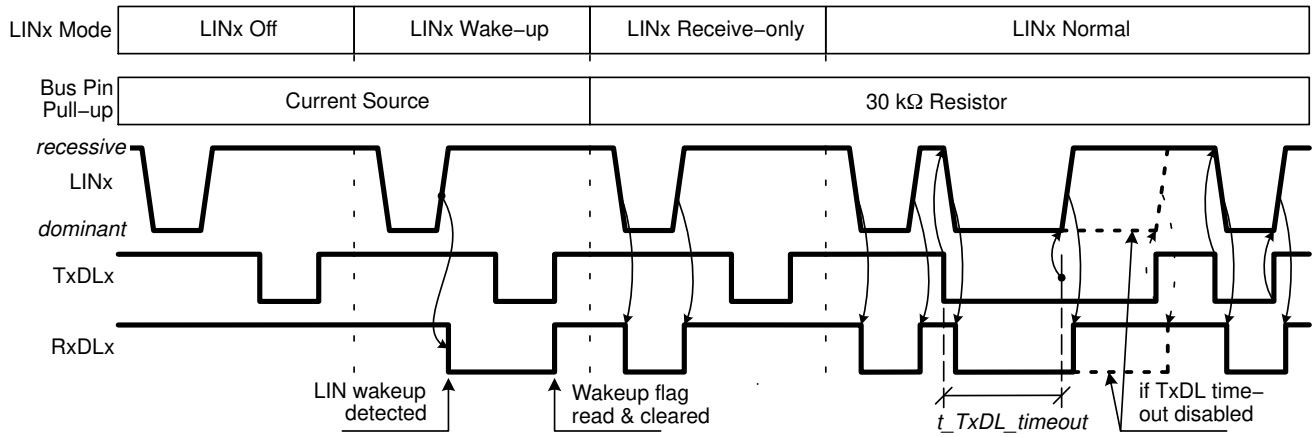


Figure 9. LIN Transceiver Modes

In **LINx Off** mode, the respective LIN transceiver is fully deactivated. Pin RxDLx stays High (as long as VOUT is provided) and logical level on TxDLx is ignored. The bus pin is internally pulled to VS with a current source (thus limiting VS consumption in case of a permanent LINx short to GND).

In **LINx Wakeup** mode, the LIN transceiver detects wakeups on the LIN line. A valid wakeup on the LIN bus corresponds to a dominant at least *t_LIN_wake* long, followed by a recessive. Thus the wakeup will not be detected in case of a permanent LIN short to GND, because a rising edge on LIN is necessary for the wakeup detection – see Figure 10.

In function of the current operating mode, a LIN wakeup can lead to an interrupt request or to a reset. A LIN wakeup is also indicated by a Low level on the corresponding RxDLx pin (which otherwise stays High as long as VOUT is available). Logical level on TxDLx pin is ignored; bus pin is internally pulled to VS with a current source.

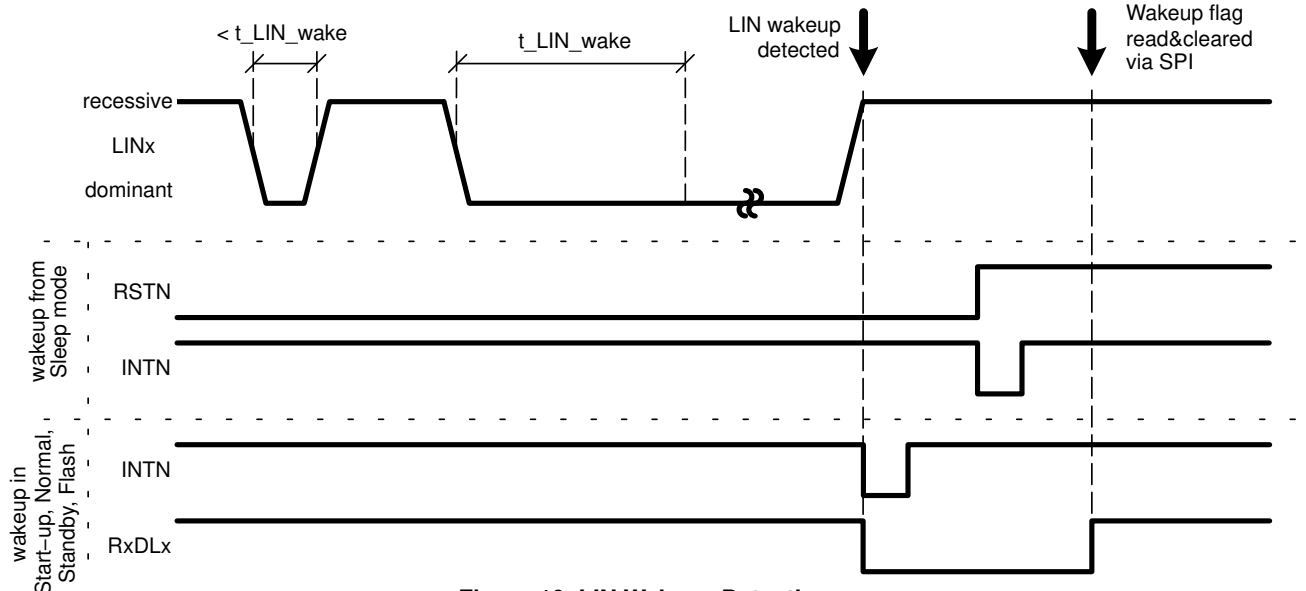


Figure 10. LIN Wakeup Detection

In **LINx Receive−Only** mode, the receiver part of the LINx block detects data on the bus with the normal speed and signals them on the RxDLx pin. Logical level on TxDLx pin is ignored; bus pin is internally pulled to VS with a current source.

In **LINx Normal** mode, the full LIN transceiver functionality is available. Both reception and transmission at the normal speed can be used. Received data are signaled via RxDLx pin, while logical level on TxDLx pin is translated into the corresponding bus level (TxDLx = High or Low leading to a recessive or dominant being transmitted, respectively). The LINx pin is internally pulled to VS via a 30 kΩ resistive path. TxDLx input signal is monitored with a time−out timer. If a dominant longer than *t_TxDL_timeout* is requested (i.e. TxDLx is Low for longer than *t_TxDL_timeout*), the transmission is internally disabled. The reception from the LINx bus remains functional and the internally set LINx transceiver mode does not change. The transmission is again enabled when TxDLx becomes High. The TxDL dominant time−out feature can be disabled via SPI (a common setting for both LIN blocks).

Transmission onto the bus is blocked if VS supply falls below *VS_MON* level. VS monitoring does not influence the LIN reception or the TxDLx time−out detection. Indication of the VS monitoring is accessible through SPI bit *statVS_LOW*.

For applications with lower required bit rates, the transmitted LIN signal slope can be decreased by a dedicated SPI setting (“LIN low−slope mode”).

WU – Local Wakeup Input

WU pin is a high−voltage input typically used to monitor an external contact or switch. A stable logical level of the WU signal is ensured even without an external connection:

- if the WU level is High for longer than *t_WU_filt*, an internal pull−up current source is connected to WU
- if the WU level stays Low for longer than *t_WU_filt*, an internal pull−down current source is connected to WU

The logical level on pin WU can be polled through SPI or used as a wakeup source:

- **WU Signal Polling:** in Start−up, Normal, Standby and Flash modes, the current WU logical level is directly reflected in SPI bit *statWU*, available for readout
- **WU Edge Detection / Wake−up:** by setting SPI bits *modWU.1* and *modWU.0*, edge detection is applied to WU signal. The device can be set to detect rising, falling or both edges on the WU signal. When the selected edge is detected, the event is latched in SPI bit *flagWakeWU*. In function of the current operating mode, edge on WU leads to an interrupt request (Start−up, Normal, Standby and Flash modes) or reset (Sleep mode). More details on the event handling, applicable also to WU edges, are given in the Event Flags and Interrupt Requests section.

Handling of the WU pin signal is illustrated in Figure 11.

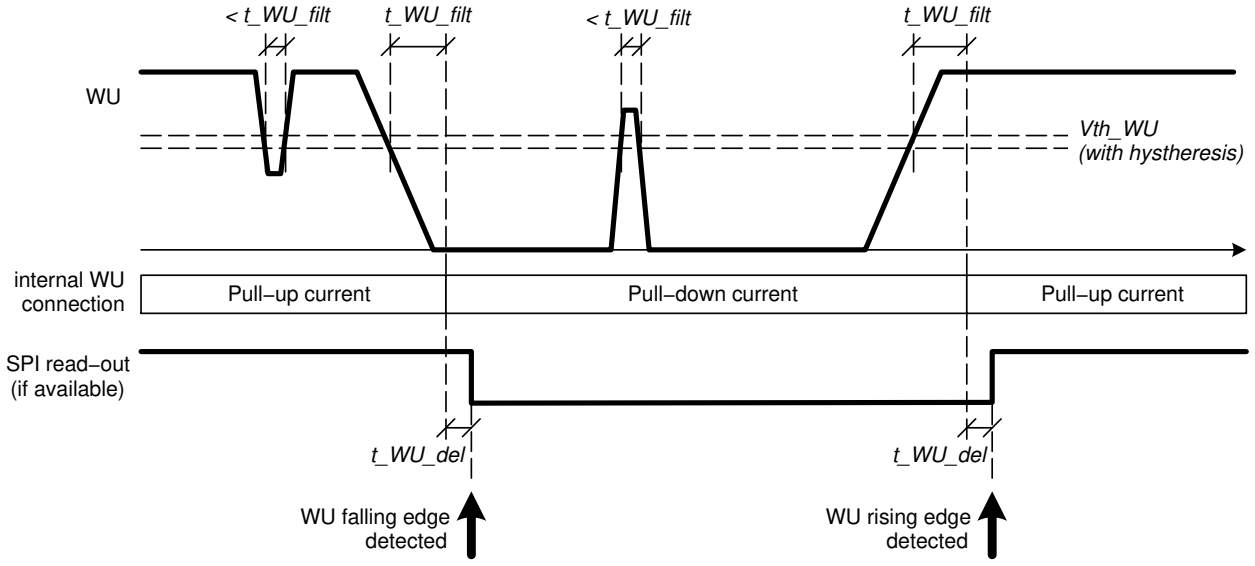


Figure 11. WU Pin Handling

Operating Modes

The principal operating modes of NCV7471(A) are shown in Figure 12 and described in the following paragraphs.

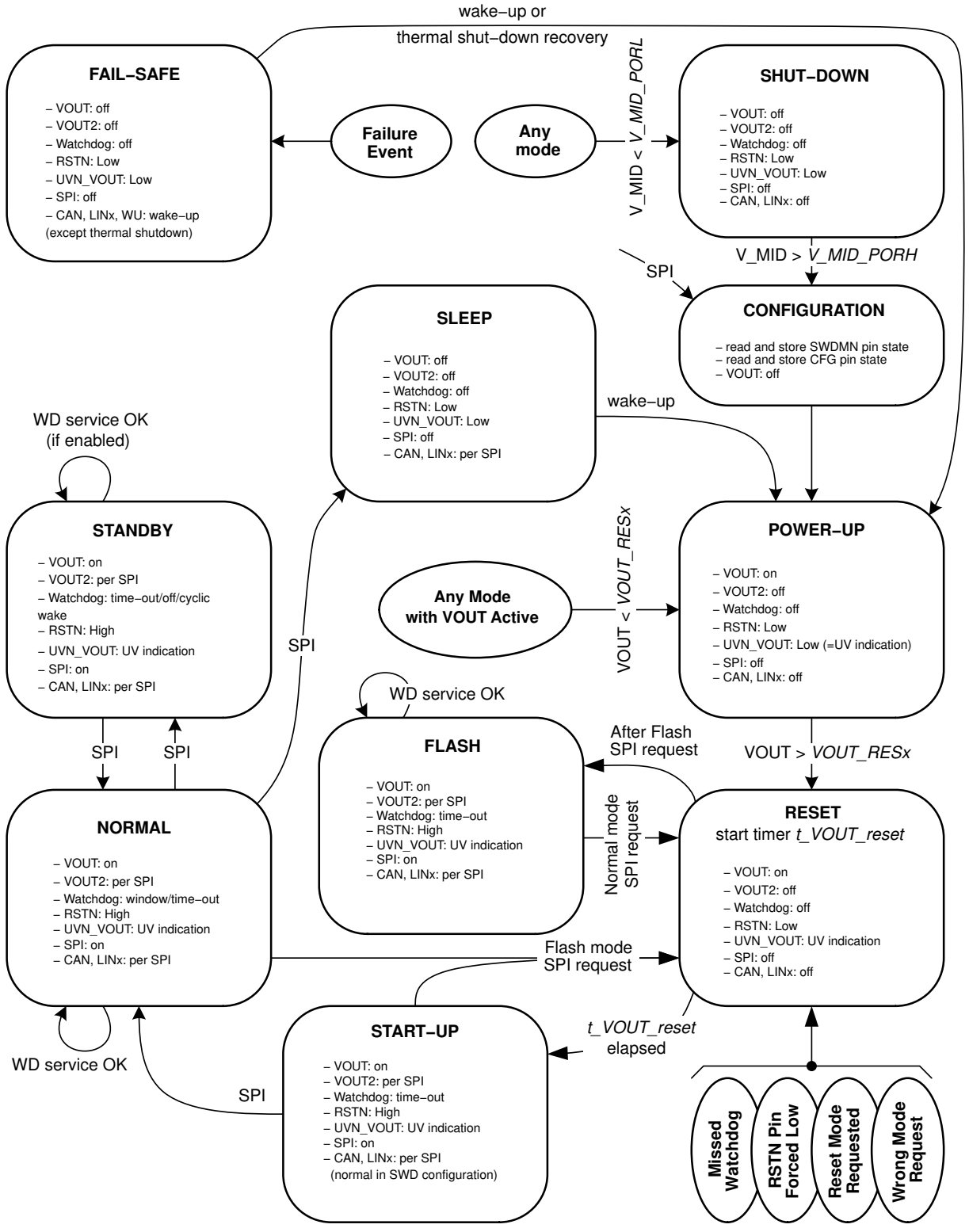


Figure 12. Operating Modes

Shut−Down Mode

The Shut−down mode is a passive state, in which all NCV7471(A) resources are inactive. The Shut−down mode provides a defined starting point for the circuit in case of supply under−voltage or the first supply connection.

Both on−chip power−supplies – VOUT and VOUT2 – are switched off and the CAN/LINx transceiver pins (CANH, CANL and LINx) remain passive so that they do not disturb the communication of other nodes connected to the buses. No wakeups can be detected. The SPI interface is disabled (SDO pin remains high−impedant). Pins RSTN and UVN_VOUT are forced Low – RSTN/UVN_VOUT Low level is guaranteed, when V_MID supply is above *V_MID_DigOut_Low* or VOUT pin is above *VOUT_DigOut_Low*. Pins RxDx are kept High (i.e. at VOUT level).

The Shut−down mode is entered asynchronously whenever the V_MID level falls below the power−on−reset level *V_MID_PORL*.

The Shut−down mode is left only when the V_MID supply exceeds the high power−on−reset level *V_MID_PORH*. When exiting the Shut−down mode, NCV7471(A) always enters the Configuration mode.

Configuration Mode

Configuration is a transient mode, in which NCV7471(A) reads logical input levels on pins SWDM and CFG. The SWDM and CFG values in Configuration mode define watchdog and fail−safe behavior of the chip, respectively. After leaving the Configuration mode, the device configuration can be changed neither by the SPI communication nor by signal modifications on the SWDM and CFG pins and is kept until the next V_MID under−voltage. The application software can also force Configuration mode by an SPI request from Start−up or Normal mode. Table 8 summarizes the available configurations and their characteristics. After reading both pins' levels, NCV7471(A) automatically transitions into the Power−up mode. Because the SMPS is off in Configuration mode, SPI−initiated transition from a functional mode to Configuration may result in a short dip on VOUT, which is not disturbing the device operation and which is recovered immediately after the Configuration mode is left.

CFG pin connection details can be found in the product's application note.

Two SPI bits are foreseen to reflect the state of SWDM and CFG pins:

- statSWDM bit latches the SWDM pin logical value read during Configuration mode. The bit remains unchanged until the Configuration mode is entered again.
- statCFG bit either latches the CFG value read in Configuration mode and remains unchanged afterwards (in Config 1,2,3,4), or keeps reflecting the current CFG signal throughout the IC operation (in SW Development).

Table 8. POSSIBLE CONFIGURATIONS ("X" Means "Don't care")

FastFSON SPI bit	Values Latched in Configuration Mode		Resulting Configuration	Behavior	
	SWDM	CFG		At Watchdog Failure	At RSTN Clamped Low
1	0	1	Config 1	1st failure activates FSOx; Fail−safe mode not entered	FSOx activated; external reset controls the operating mode
1	0	0	Config 2	1st failure puts the chip into Fail−safe mode	FSOx activated; Fail−safe mode entered
0	0	1	Config 3	2nd failure activates FSOx; Fail−safe mode not entered	FSOx activated; external reset controls the operating mode
0	0	0	Config 4	2nd failure activates FSOx and puts the chip into Fail−safe mode	FSOx activated; Fail−safe mode entered
X	1	X	SW Development	No FSOx activation; no Fail−safe mode entry; stored in SPI, can lead to interrupt (if enabled)	External reset controls the operating mode; no FSOx activation

Power−Up Mode

The Power−up mode ensures correct activation of the on−chip VOUT DC/DC converter or recovery of VOUT after an under−voltage event.

In the Power−up mode, the VOUT DC/DC converter is switched on (or kept on) while VOUT2 regulator remains in the previous state (e.g. VOUT2 is off coming from the Shut−down and Configuration modes). The CAN/LINx transceiver pins (CANH, CANL and LINx) remain passive so that they do not disturb the communication of other nodes connected to the buses. No wakeups can be detected. The SPI interface is disabled (SDO pin remains high−impedant). Pins RSTN and UVN_VOUT are forced Low. Pins RxDx are kept High (i.e. at VOUT level).

The Power−up mode is entered from the Configuration mode or after a wakeup from Sleep mode (in both cases, VOUT DC/DC converter needs to be activated). It will be also entered from any state with VOUT already active (Normal, Standby, Reset, Start−up, Flash) if the VOUT level falls below the *VOUT_RESx* level (the valid *VOUT_RESx* level is set via SPI).

The Power−up mode is correctly left when VOUT exceeds the SPI−selected *VOUT_RESx* level. An overload/short−circuit failure is detected if VOUT does not reach the failure threshold *VOUT_FAIL* within time *t_VOUT_powerup*. NCV7471(A) then goes to the Fail−safe mode. VOUT staying between *VOUT_FAIL* and *VOUT_RESx* levels will keep the device in the Power−up mode, unless the thermal shutdown temperature is reached (e.g. because of VOUT overload).

Reset Mode

The Reset mode is a transient mode providing a defined RSTN pulse for the application microcontroller.

VOUT supply is kept on, while VOUT2 regulator remains in its previous state. The CAN/LINx transceiver pins (CANH, CANL and LINx) are passive so that they do not disturb the communication of other nodes connected to the buses. No wakeups can be detected. The SPI interface is disabled (SDO pin remains high−impedant). Pin RSTN is forced Low while pin UVN_VOUT indicates the VOUT under−voltage with respect to the highest reset level. Pins RxDx are kept High (i.e. at VOUT level).

Reset mode will be entered as a consequence of one of the following events:

- Power−up mode is exited
- RSTN pin is forced Low externally
- Flash mode has been requested via SPI
- Flash mode exit has been requested via SPI
- Reset mode has been requested via SPI
- An un−authorized operating mode has been requested via SPI
- Watchdog has been missed in Config 1 or Config 3

Normally, the Reset mode is left after a defined time *t_VOUT_reset* when the RSTN pin is internally released to High – the chip then goes to the Start−up mode. Overdriving the RSTN pin to Low externally will extend the Reset mode duration. If RSTN is still forced Low externally even after time *t_VOUT_Clamped_Low* elapses, a “RSTN clamped Low” event is detected. The reaction depends on the chip configuration (SW Development or Config 1/2/3/4). “RSTN clamped Low” can lead to FSOx signal activation, Fail−safe mode entry or just to the Reset mode being kept as long as RSTN is driven Low – see Table 9.

If the Reset mode is entered due to external RSTN Low pulse during Start−up mode, FSOx outputs are activated (unless the device is in the SW Development configuration). This condition fosters that the external MCU sends at least one correct watchdog message before applying an external reset.

Information about the cause of a reset pulse is stored in the SPI registers and can be read by the application software. The “Reset source” information is kept unchanged until the next reset event.

Start−Up Mode

During the Start−up mode, the microcontroller supplied by VOUT is expected to initialize correctly and to perform successful communication via the SPI interface.

Start−up mode is the first mode in which SPI is enabled and the watchdog is started. The application software is able to read any SPI register. Write access to SPI depends on the FSO_internal flag (i.e. whether a failure condition preceded the Start−up mode – see the FSO1/2/3 − Fail−safe Outputs section for details):

- In case FSO_internal = 0 (inactive), any SPI register can be written and all features can be configured in the Start−up mode (e.g. CAN/LIN transceivers can be activated, VOUT2 can be activated)
- In case FSO_internal = 1 (active), all SPI write frames will be ignored by the chip, with the exception of the watchdog service frame (write access to the MODE_CONTROL register).

The watchdog is activated and works in the timeout mode. A correct watchdog service is expected from the MCU before the watchdog period elapses. The correct watchdog−serving SPI message should arrive in time and should contain either a request to enter Normal mode or a request to enter the Flash mode. The Start−up mode is then exited into the requested mode.

If the microcontroller software fails to serve the watchdog in time, the chip detects the “1st Watchdog Missed” event which is handled according the configuration (SW Development or Config 1/2/3/4) – see the FSO1/2/3 − Fail−safe Outputs section.

In the SW Development configuration, the following exceptions are applied for the Start−up mode:

- the device remains in the Start−up mode as long as the watchdog is not served correctly – thus also in case no microprocessor is connected.
- when entering the Start−up mode, CAN and both LIN transceivers are automatically put to their Normal mode

As a result, device in SW Development mode keeps on providing VOUT supply and full CAN and LIN functionality even if no application software is available or if no microprocessor is connected. In addition, no RSTN pulses are generated and FSOx pins remain inactive.

Normal Mode

The Normal mode allows using all NCV7471(A) resources (VOUT2, CAN transceiver, LINx transceivers) which can be monitored and configured by the microcontroller via the SPI interface. The watchdog is working in the window mode with selectable period which can be changed at each watchdog−service SPI message.

VOUT is kept on. INTN pin provides the Interrupt Requests (IRQ’s) depending on the device status and the interrupt mask settings. The application software can poll all

SPI status bits or enable the corresponding interrupt requests. Pin RSTN remains High while pin UVN_VOUT indicates the VOUT under−voltage with respect to the highest reset level. WU pin and transceivers can be configured for wake−up recognition which is then signalled as an interrupt request.

In a software−controlled way, the microcontroller can either keep NCV7471(A) in the Normal mode or request a transition into another mode (including Reset and Configuration).

Standby Mode

Standby is the first low−power mode of NCV7471(A). It is entered after the corresponding SPI request is made in the Normal mode. In the Standby mode, the application microcontroller remains supplied by VOUT DC/DC converter and can continue the SPI communication. VOUT remains monitored by the reset and failure comparators. The functionality of the LINx blocks remains fully available while the CAN transceiver is limited – it can be put to Receive−only, Wakeup or Off mode. Active CAN transmission is not available.

Three types of wakeup can be used during the Standby mode – a local wakeup through the WU pin change, a bus wakeup (via a CAN or LINx bus) and a cyclic wakeup generated by the watchdog timer. A detected wakeup will cause an interrupt request through INTN pin.

During Standby mode, at least one of the following conditions must be fulfilled:

- Watchdog is requested to be on
- Cyclic wakeup is enabled
- CAN wakeup is enabled
- LIN wakeup is enabled at least on one of the LINx channels

If none of the above conditions is respected, all CAN and LIN wakeups will be automatically enabled as well as WU wakeup on both edges. Note, that allowing only the local WU wakeup is not sufficient for successful Standby mode entry without watchdog. This SPI setting condition is monitored and fostered throughout the Standby mode duration.

Standby will be kept as long as the microcontroller can correctly serve the watchdog and the interrupts according the SPI settings. Standby is left either by an SPI request for a mode change or by a reset event.

Sleep Mode

Sleep mode is the second low−power mode of NCV7471(A). The microcontroller is not supplied and most resources are inactive beside the blocks needed for wakeup detection.

Sleep mode can be entered from Normal mode by the corresponding SPI request. Immediately after the Sleep mode entry, RSTN and UVN_VOUT pins are pulled Low in order to stop the microcontroller software. Both power supplies – VOUT and VOUT2 – are switched off; SPI and watchdog are de−activated. Depending on the SPI settings prior to the Sleep mode entry, CAN and LINx transceivers can be either switched off or configured for bus wakeup detection.

Two types of wakeup can be used during the Sleep mode – a local wakeup through the WU pin change, and a bus wakeup (via a CAN or LINx bus). A detected wakeup will cause entry into Power−up mode.

When Sleep mode is requested, at least one of the following conditions must be fulfilled:

- CAN wakeup is enabled
- LIN wakeup is enabled at least on one of the LINx channels

If none of the above conditions is respected, all CAN and LIN wakeups will be automatically enabled as well as WU wakeup on both edges. Note, that allowing only the local WU wakeup is not sufficient. Sleep mode can be only left through a wakeup or V_MID under−voltage.

Fail−Safe Mode

Fail−safe mode ensures a defined reaction of NCV7471(A) to a failure event. Both power supplies – VOUT and VOUT2 – are switched off, and the Fail−safe outputs are activated. RSTN and UVN_VOUT pins are pulled Low in order to ensure that the microcontroller software execution stops immediately.

Fail−safe mode will be entered as a consequence of one of the following events:

- Watchdog has been missed in Config 2 or Config 4
- “RSTN clamped Low” has been detected in Config 2 or Config 4
- “RSTN clamped High” has been detected
- VOUT power supply has not reached the failure level VOUT_FAIL after *t_VOUT_powerup* – this situation can be encountered during failed chip start−up or during too long and deep under−voltage
- Fail−safe mode has been requested via SPI (in SW Development only)
- Thermal shut−down has been encountered

All CAN and LINx transceivers are automatically configured to wakeup detection; wakeup from WU pin is also enabled on both edges. A detected bus or WU wakeup will bring NCV7471(A) into Power−up mode. Only in case of a thermal shut−down, no wakeups are detected and the Fail−safe mode is exited as soon as the junction temperature decreases below the warning level.

Throughout the Fail−safe mode, some SPI settings and status bits are preserved, and become effective after Fail−safe mode recovery. Namely CONTROL2 register (with SMPS mode settings and VOUT reset level settings), STATUS1 register (with wake−up flags and FSO flags) and GENERAL PURPOSE register are not reset when Fail−safe is entered, and keep their previous content. Fail−safe

recovery is therefore different compared to wakeup from Sleep mode, after which CONTROL2 is reset.

Flash Mode

Flash mode offers a relaxed watchdog timing enabling transfer of bigger amounts of data between the microcontroller software and, e.g., an external programmer connected to a CAN or LIN bus. The watchdog is running in time−out mode and its period can be selected from the full range of available values including longer times compared to Normal mode. The control of other resources – power supplies, transceivers, WU pin, interrupt requests, etc. – remains identical to Normal mode.

Flash mode can be entered by a specific SPI request in Start−up or Normal mode. The entry into Flash is accompanied by a reset pulse with “Flash requested” flag. Similarly, Flash mode can be left by an SPI request which will result in a reset pulse with “Flash exit requested” flag. Reset−source information in the SPI flags then allows the application to branch in function of the Flash mode. The handling of Flash mode requests is shown in Figure 13.

In SW Development configuration, CAN and both LIN transceivers are automatically put to their Normal mode when the device enters Flash operating mode.

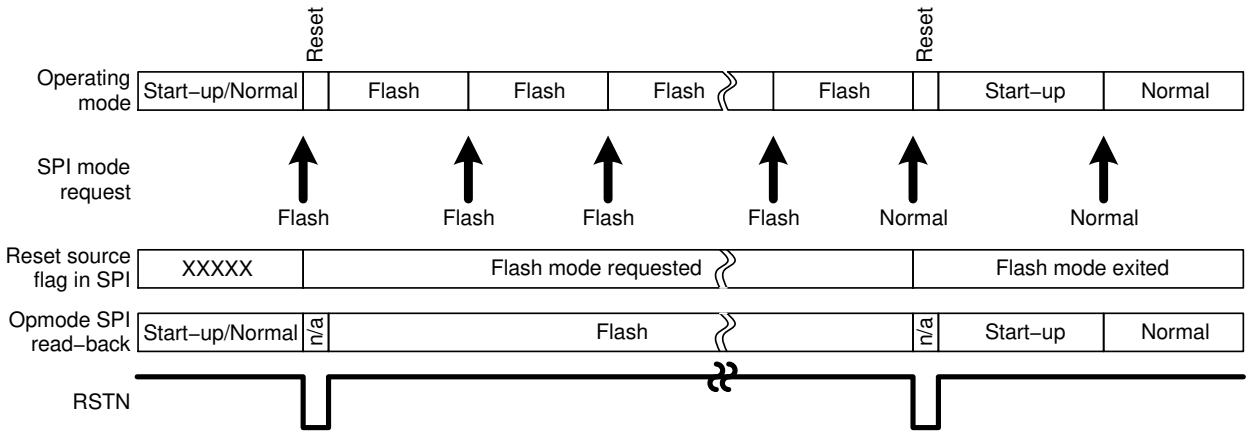


Figure 13. Flash Mode Sequence

Watchdog

The NCV7471(A) watchdog timer monitors the correct function of the application software – the microcontroller is required to send correct and timely watchdog−service (or “WD trigger”) SPI messages. A failure in the watchdog service is handled in function of the chip’s configuration (see the Configuration Mode section): it leads to a reset, to the Fail−safe mode entry or – in the SW Development configuration – generates an interrupt event (maskable).

The available modes of the watchdog timer are shown in Figure 14, with the watchdog period specified in Figure 15:

- **Time−out mode watchdog:** the microcontroller is expected to send the watchdog−service SPI message any time before the watchdog period elapses. The time−out watchdog mode is automatically used during Start−up and Flash modes. It can be used in Standby and Normal modes. In Standby and Flash modes, the watchdog period can be selected from a broader range of values compared to the Normal mode.
- **Window mode watchdog:** the microcontroller must send the required SPI message during an “open window” – this window is situated between 50% and 100% of the watchdog period. A watchdog−service SPI message sent before or after the open window is treated as a watchdog failure. The window watchdog can be used during the Normal mode.
- **Off:** the watchdog will be inactive by default in Shut−down, Configuration, Power−up, Reset, and Fail−safe modes. It can be requested to be off in the Standby mode.
- **Timer Wakeup:** in the Standby mode, the watchdog timer can be configured to generate wakeup events. In the Standby mode an interrupt request will be generated with a period defined by the watchdog setting.

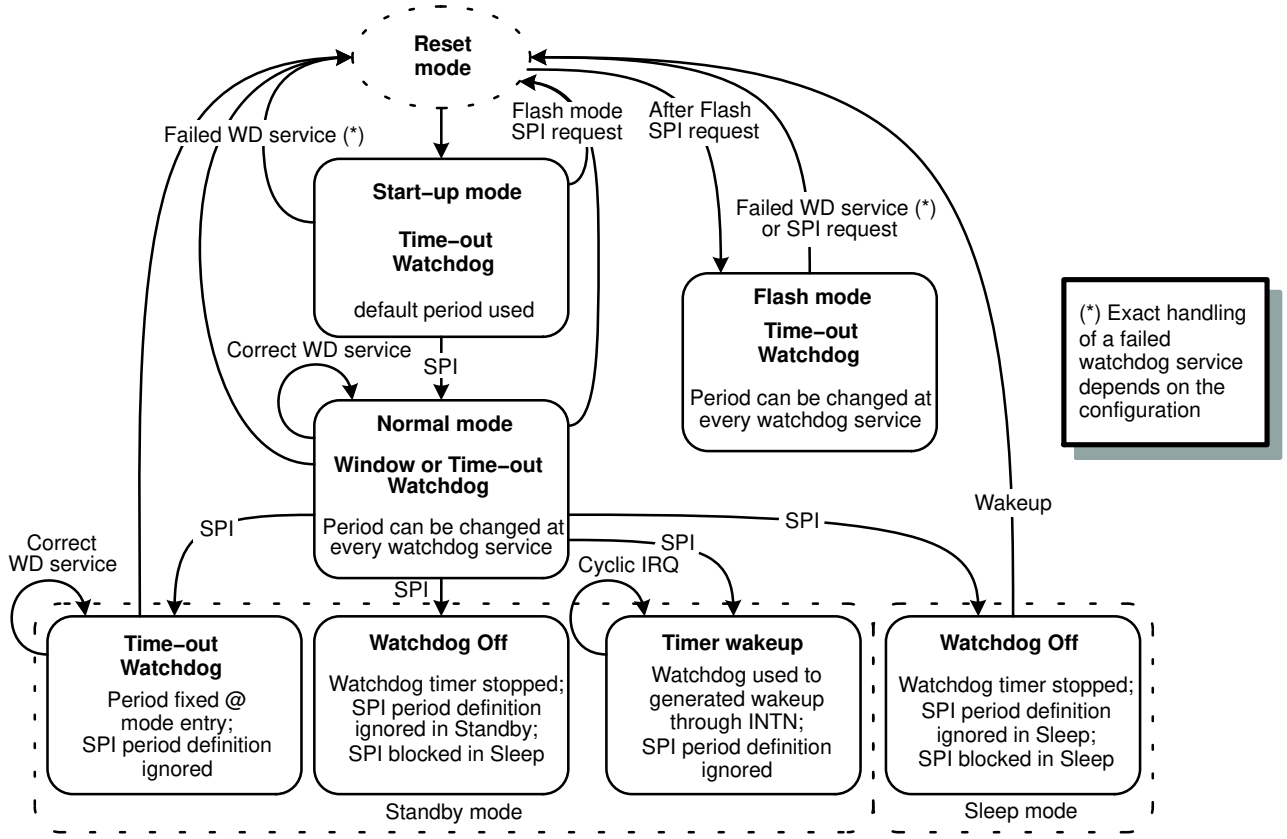


Figure 14. Watchdog Modes

A watchdog−service corresponds to a write access to SPI CONTROL0 register, containing watchdog mode, watchdog period and operating mode settings. The CSN rising edge of the CONTROL0 SPI write access is considered as the watchdog trigger moment. The watchdog service is evaluated as successful if all below conditions are fulfilled:

- The write SPI frame is valid
- The watchdog trigger moment falls into the correct watchdog trigger interval (see Figure 15) – in the case of the time−out watchdog, it arrives before the watchdog period expires; in the case of the window watchdog, it arrives during the second half of the window interval. In both cases, tolerance of the watchdog timing parameters shall be taken into account.
- The requested watchdog mode and the requested operating mode form an allowed combination

The watchdog period value written during a successful watchdog service is immediately used during the subsequent operation.

In the SW Development configuration, a failed watchdog service does not lead either to Reset or to Fail−safe mode:

- A failed WD service event is stored into the corresponding SPI register
- If the event is not masked, an interrupt request is generated.
- If a time−out watchdog is missed in the Start−up operating mode, Start−up mode is kept, and the watchdog is restarted with the default time−out period.
- If a too early window WD service is encountered in the Normal mode, a new watchdog period will be immediately started with the newly written settings; Normal mode is preserved
- If a window−watchdog is missed in the Normal mode (no service arrives), a new watchdog period will be immediately started with the current settings; Normal mode is preserved
- If a time−out watchdog is missed in the Standby mode, a new time−out watchdog period is immediately started with the same period; Standby mode is preserved

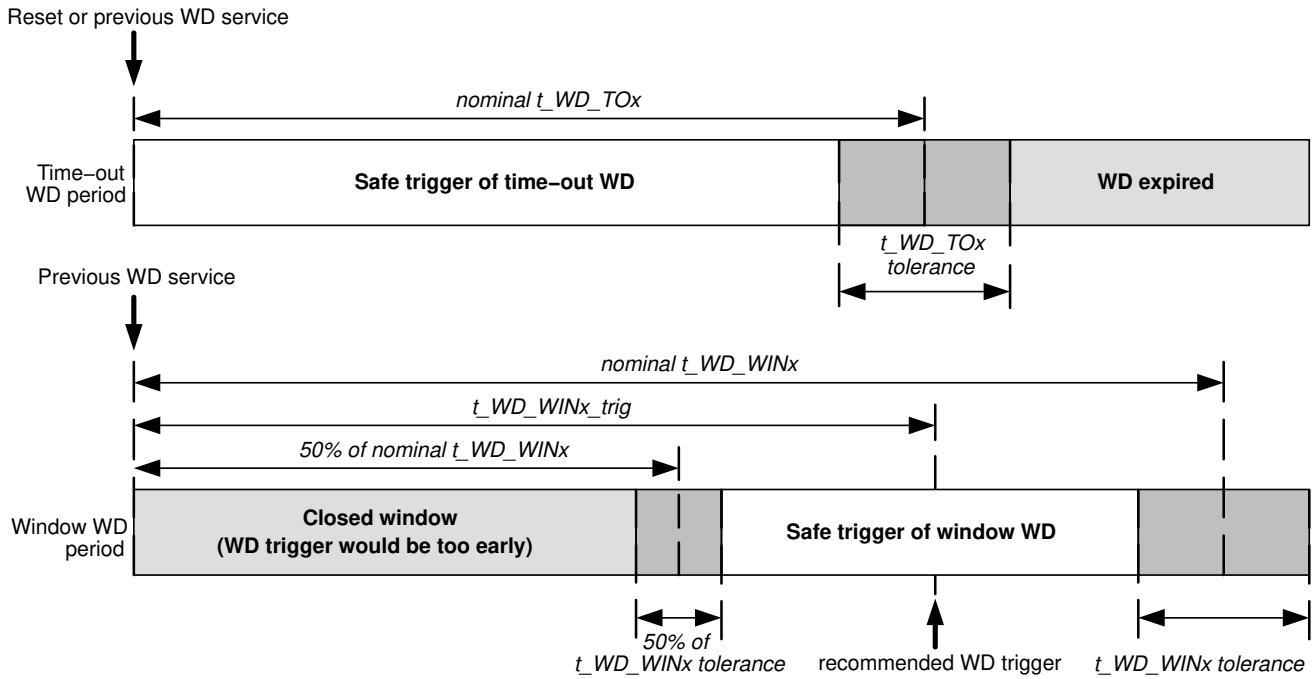


Figure 15. Structure of the Time−out and Window Watchdog Period

System Reset

A reset to the application microcontroller is signaled by Low level on the RSTN pin. RSTN pin is a bidirectional digital pin using an open−drain output structure with an internal pull−up resistor. An external reset source can overrule the High level generated by NCV7471(A) on RSTN pin. The RSTN logical level is then a superposition of the internally and externally driven reset request.

The RSTN pin level is compared with the internally driven RSTN signal – the comparison is used to control the operating mode of the circuit and to monitor a clamped condition of the RSTN pin – see Table 9.

With the exception of the SW Development configuration, applying an external reset during the Start−up mode will result in the FSO outputs activation. This condition fosters that the external MCU sends at least one correct watchdog message before applying an external reset.

Table 9. RSTN PIN FUNCTION (“X” Means “Don’t Care”)

	RSTN				
	internally driven	sensed at the pin	Configuration	Mode	Action
RSTN pin follows internal drive	Low	Low	X	X	Follow normal state diagram
	High	High	X	X	Follow normal state diagram
RSTN pin clamped High	Low	High	X	Configuration, Power−up, Reset, Sleep	Go to Fail−safe after *t_RSTN_ClampedHigh*
RSTN pin clamped Low	High	Low	X	Normal, Standby, Flash	Go to Reset mode after *t_RSTN_filt*
			Config 1, 2, 3, 4	Start−up	Go to Reset mode after *t_RSTN_filt;* activate FSO
			SW Development	Start−up	Go to Reset mode after *t_RSTN_filt;* do **NOT** activate FSOx
			Config 1 and 3	Trying to exit Reset mode	Keep Reset mode; activate FSOx after *t_RSTN_ClampedLow*
			Config 2 and 4	Trying to exit Reset mode	Keep Reset mode Go to Fail−safe after *t_RSTN_ClampedLow*
			SW Development	Trying to exit Reset mode	Keep Reset mode do **NOT** go to Fail−safe do **NOT** activate FSOx

Event Flags and Interrupt Requests

An interrupt request can be signaled by the NCV7471(A) to the attached microcontroller via the open−drain output pin INTN. The active level of the INTN pin is logical Low. Pin INTN is provided with an internal pull−up resistor. An additional external pull−up is recommended − see Figure 2. The interrupt request generation is available during the Start−up, Normal, Standby and Flash modes.

The following events are handled by the interrupt sub−system:

- CAN, LIN and WU wakeups (cannot be masked)
- Timer wakeup in Standby mode (cannot be masked)
- VOUT2 supply crossing the under−voltage level in either direction if VOUT2 is on
- VOUT2 supply crossing the over−voltage level in either direction
- TxD dominant time−out for CAN or LINx (valid only if the respective transceiver is configured in its normal mode)
- The junction temperature crosses the thermal warning level in either direction
- Internal DC/DC converter signals changing their status − these events indicate entering or leaving limit conditions for both stages of the converter (run−state of the boost, overload of the boost or buck, out−of−regulation state of buck)
- Watchdog missed in SW Development configuration

If an event is encountered, it always causes the corresponding SPI flag go High. If the event is masked by the SPI interrupt mask setting (the corresponding mask bit is Low), pin INTN will not be forced Low and no interrupt request will be issued. The interrupt flag remains available for later readout until the next read−and−clear access through the SPI interface. TxD dominant time−out flags will remain set even after a read&clear access if the excessively long dominant signal is still present on the corresponding TxD pin. Note, that wakeup events cannot be masked. An overview of event flags is given in Table 10.

In case an un−masked interrupt event takes place, not only the corresponding event flag is set High, but also INTN pin is driven Low for *t_INTN_active*, indicating an interrupt request to the microcontroller. The microcontroller software is expected to read and clear the interrupt status register, otherwise the interrupt request remains pending (with the exception of flagRES_SWD). Pending or new interrupt requests will lead to a new INTN Low pulse no sooner than *t_INTN_inactive* after the previous pulse. In this way, it is ensured that multiple new or pending interrupts will not slow−down the execution of the application software. Control of the INTN pin in conjunction with the internal flags is illustrated in Figure 16.

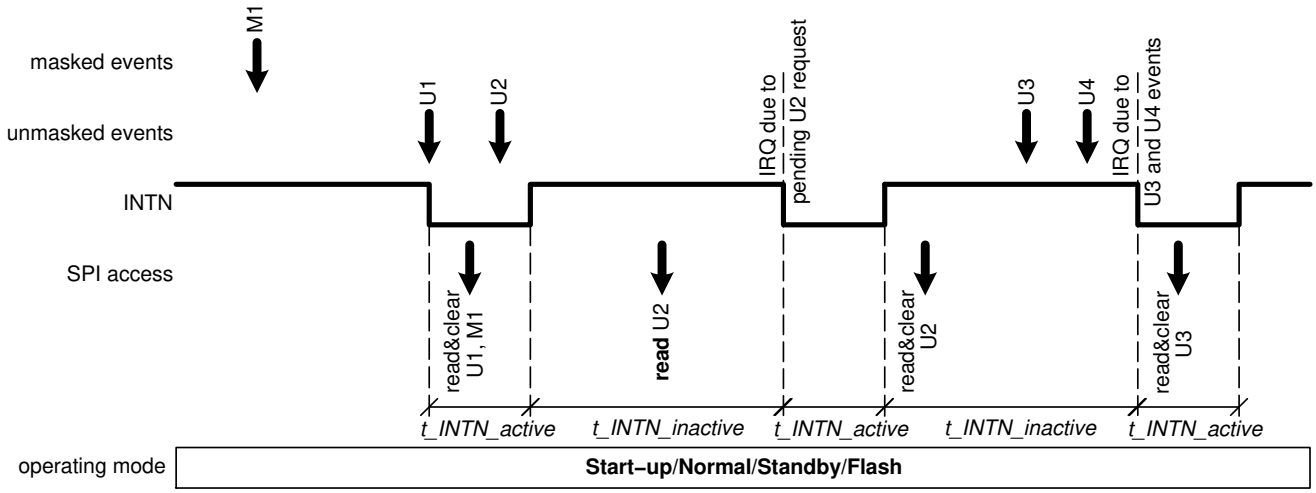


Figure 16. Interrupt Request Handling in Start−up, Normal, Standby and Flash Modes

In order to prevent that a pending interrupt request gets ignored by the application software, NCV7471(A) offers the following mechanisms:

- All event flags are preserved when transitioning from Start−up to Normal mode − see Figure 17.
- All event flags are preserved when transitioning from Standby to Normal mode − see Figure 17.
- All event flags are preserved when transitioning from Normal to Standby mode. If Standby mode is requested while an un−masked interrupt is pending, a new interrupt request is issued according the *t_INTN_inactive* timing − see Figure 18.
- If Sleep mode is requested while a wakeup flag is pending, the chip immediately performs a “wakeup from Sleep” mode sequence − see Figure 19. In this way, the information on the pending wakeup is not missed by the application.

Any transition through the Reset mode erases all SPI event flags, except the wakeup flags, and sets all maskable events to masked (i.e. not causing an interrupt request).

Table 10. EVENT FLAGS SUMMARY

	Event Flag Bit	Related Status Bit (Note 1)	Related Interrupt Mask Bit	Set Condition	Reset Condition
TxDx Time−out	flagTO_TxDC	none	intenTO_TxDC	TxDx (Note 2) pin is kept Low for longer than the time−out period **and** corresponding transceiver in normal mode	read&clear access to register STATUS0 **and** {TxDx (Note 2) dominant time−out condition disappeared **or** transceiver mode other then “normal”}
	flagTO_TxDL1		intenTO_TxDL1		
	flagTO_TxDL2		intenTO_TxDL2		
SMPS	flagBUCK_NOREG	statBUCK_NOREG	intenBUCK_NOREG	BUCK SMPS stage enters or leaves range of no regulation (i.e. extreme switching duty cycle); indicates (in)ability to reach nominal VOUT	read&clear access to register STATUS0
	flagBUCK_OL	statBUCK_OL	intenBUCK_OL	BUCK SMPS stage enters or leaves over−load condition (i.e. current limitation encountered or disappeared)	
	flagBOOST_RUN	statBOOST_RUN	intenBOOST_RUN	BOOST SMPS stage changes activity – it starts or stops	
	flagBOOST_OL	statBOOST_OL	intenBOOST_OL	BOOST SMPS stage enters or leaves over−load condition (i.e. current limitation encountered or disappeared)	
	flagTWAR	statTWAR	intenTWAR	junction temperature crosses the warning level in either direction	
	flagRES_SWD (Note 4)	none	intenRES_SWD	incorrect watchdog service encountered **and** device in SW Development configuration	
VOUT2	flagVOUT2_UV	statVOUT2_UV	intenVOUT2_UV	VOUT2 under−voltage detector changes state in either direction **and** VOUT2 is switched on	
	flagVOUT2_OV	statVOUT2_OV	intenVOUT2_OV	VOUT2 over−voltage detector changes state in either direction	
	flagSPIFail (Note 5)	none	intenSPIFail	SPI frame failure occurs: – number of SPI clocks different from 0 or 16, or – SCK High when CSN changes state	
Wakeups	flagWakeWU	none	none	WU wakeup detected (Note 3)	Read&clear access to register STATUS1
	flagWakeCAN			CAN wakeup detected (Note 3)	
	flagWakeLIN1			LIN1 wakeup detected (Note 3)	
	flagWakeLIN2			LIN2 wakeup detected (Note 3)	
	flagWakeTimer			Timer wakeup detected (Note 3)	

1. When a related status bit exists, the event is linked to a change (in either direction) of the status bit. Even if the event flag is cleared, the corresponding status bit still indicates the current status of the observed feature and can be polled by SPI at any time.
2. “x” = “C”, “L1 or “L2”. In case of LIN transceivers, the time−out feature can be enabled/disabled by SPI.
3. The respective wakeup source must be enabled through the corresponding control SPI register – timer wakeup in CONTROL0; CAN, LIN1/2 and WU wakeups in CONTROL1
4. For a missed WD in SW Development, INTN pulse is generated only once per event – it is not repeated even if the corresponding flag is still set. New INTN pulse occurs only if WD is missed again in SW Development.
5. During VOUT power−up (e.g. when going from Shut−down mode, or when waking−up from Sleep or Fail−safe mode), flagSPIFail can be set because of transient toggling of internal CSN and SCK signals. It is therefore recommended to ignore flagSPIFail immediately after VOUT power−up, until the STATUS0 register is reset. Except flagSPIFail, the remaining SPI register content is not influenced by the possible internal toggling of CSN and SCK signals during power−up.

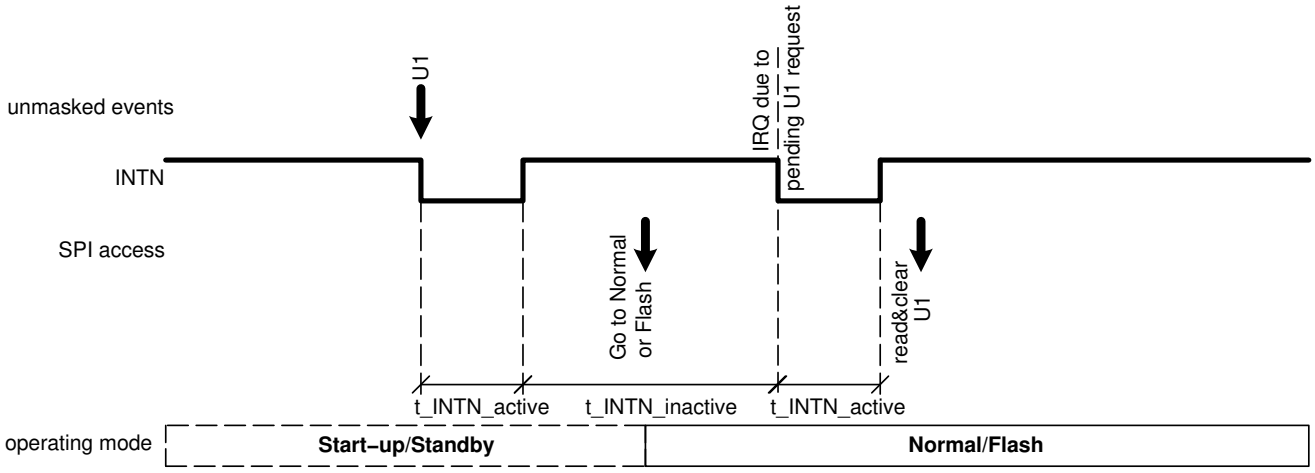


Figure 17. Interrupt Request Handling during a Transition to Normal Mode

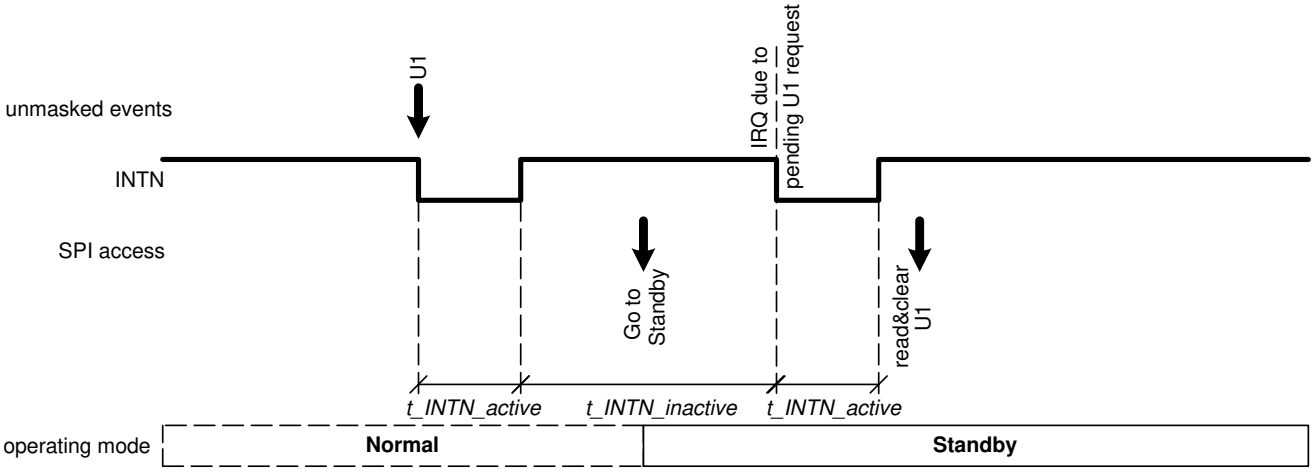


Figure 18. Transition to Standby Mode with a Pending Interrupt Request

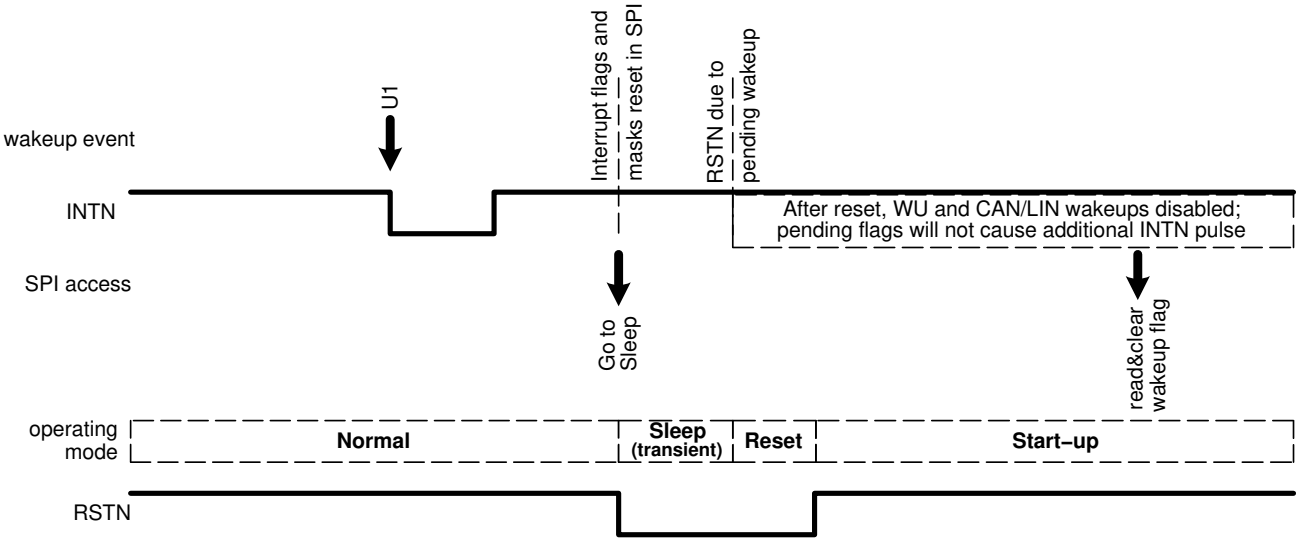


Figure 19. Attempted Transition to Sleep Mode with a Pending Wakeup Flag

Junction Temperature Monitoring

The device junction temperature is monitored in order to avoid permanent degradation or damage of the chip. Two distinct junction temperature thresholds are used:

- Thermal warning level *Tj_WAR*. The status of the current junction temperature compared with the Tj_WAR threshold is available in the corresponding SPI status register. A change of the junction temperature across the warning threshold in either direction sets the SPI bit flagTWAR. If not masked, an interrupt request can be generated in order to signal to the application that the junction temperature exceeded or cooled below the warning level.
- Thermal shut−down level *Tj_SD*. Junction temperature exceeding the shut−down level puts the chip into Fail−safe mode. In this specific case, no wakeups are detected in the Fail−safe mode; the mode is automatically left only when the junction cools down below the warning level, thus providing a thermal margin for the application software to cope with the event.

The junction temperature monitoring circuit is active in all operating modes with VOUT supply switched on (Power−up, Reset, Start−up, Standby, Flash) and also in the Fail−safe, provided that it has been entered as the consequence of a thermal shut−down. The function of the junction temperature monitoring of NCV7471(A) is shown in Figure 20.

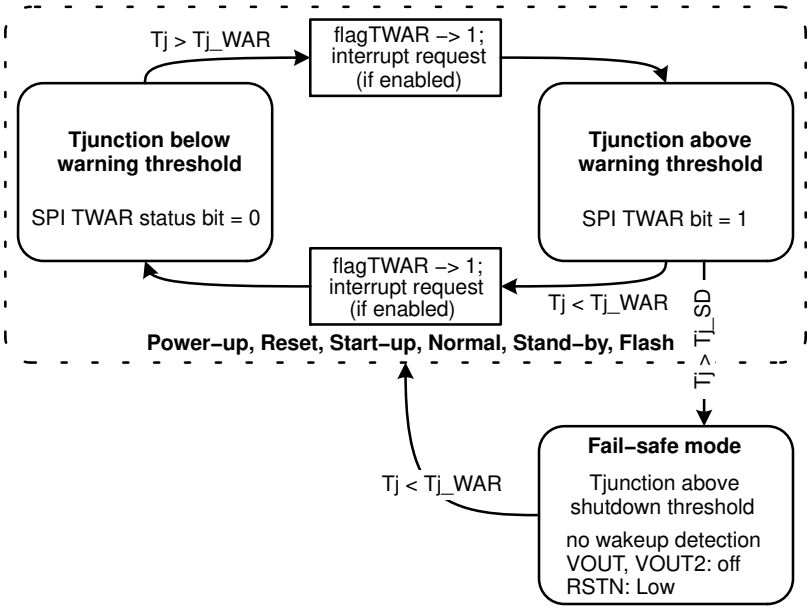


Figure 20. Junction Temperature Monitoring