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NCV7518, NCV7518A

FLEXMOS™ Hex Low-side MOSFET Pre-driver

The NCV7518 / NCV7518A programmable six channel low-side MOSFET pre-driver is one of a family of FLEXMOS automotive grade products for driving logic-level MOSFETs. The product is controllable by a combination of serial SPI and parallel inputs. The device offers 3.3 V/ 5 V compatible inputs and the serial output driver can be powered from either 3.3 V or 5 V. An internal power-on reset provides controlled power up. A reset input allows external re-initialization and an enable input allows all outputs and diagnostics to be simultaneously disabled.

Each channel independently monitors its external MOSFET's drain voltage for fault conditions. Shorted load fault detection thresholds are fully programmable using an externally programmed reference voltage and a combination of discrete internal ratio values. The ratio values are SPI selectable and allow different detection thresholds for each channel.

Fault recovery operation for each channel is programmable and may be selected for latch-off or automatic retry. Status information for each channel is 3-bit encoded by fault type and is available through SPI communication.

The FLEXMOS family of products offers application scalability through choice of external MOSFETs.

Features

- 16-bit SPI with Parity and Frame Error Detection
- 3.3 V/5 V Compatible Parallel and Serial Control Inputs
- 3.3 V/5 V Compatible Serial Output Driver
- Reset and Enable Inputs
- Open-drain Fault Flag
- Priority Encoded Diagnostics with Latched Unique Fault Type Data
  - Shorted Load, Short to GND
  - Open Load with Fast Charge Option
  - On and Off State Pulsed Mode Diagnostics
- Ratiometric Diagnostic References and Currents
- Programmable
  - Shorted Load Fault Detection Thresholds
  - Fault Recovery Mode
  - Blanking Timers
- Wettable Flanks Pb-Free Packaging
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This is a Pb-Free Device

Benefits

- Scalable to Load by Choice of External MOSFET

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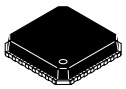
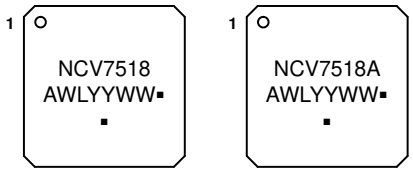


QFN32
MW SUFFIX
CASE 485CZ

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCV7518MWTXG	QFN32 (Pb-Free)	5,000 / Tape & Reel
NCV7518MWATXG	QFN32 (Pb-Free)	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

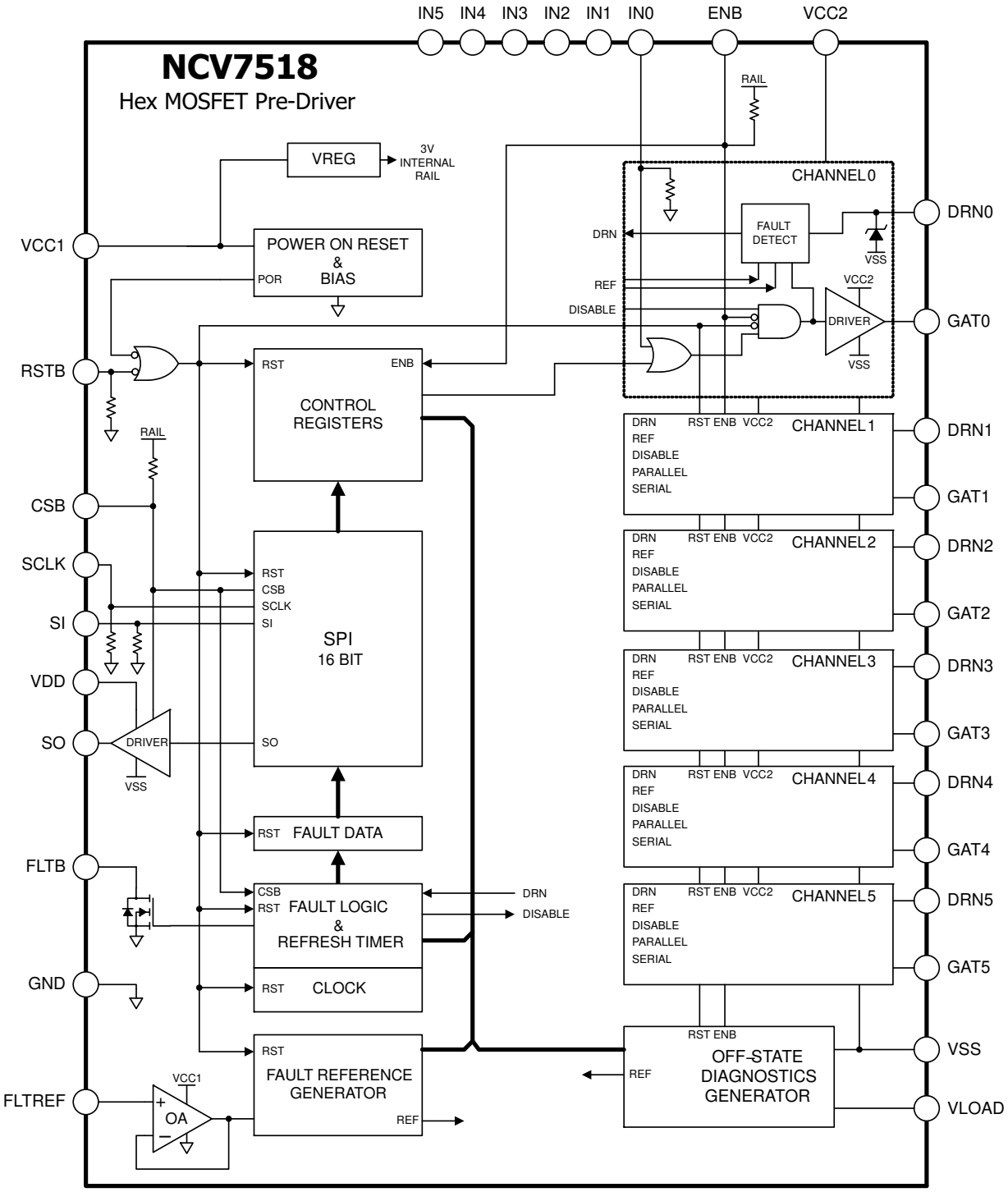
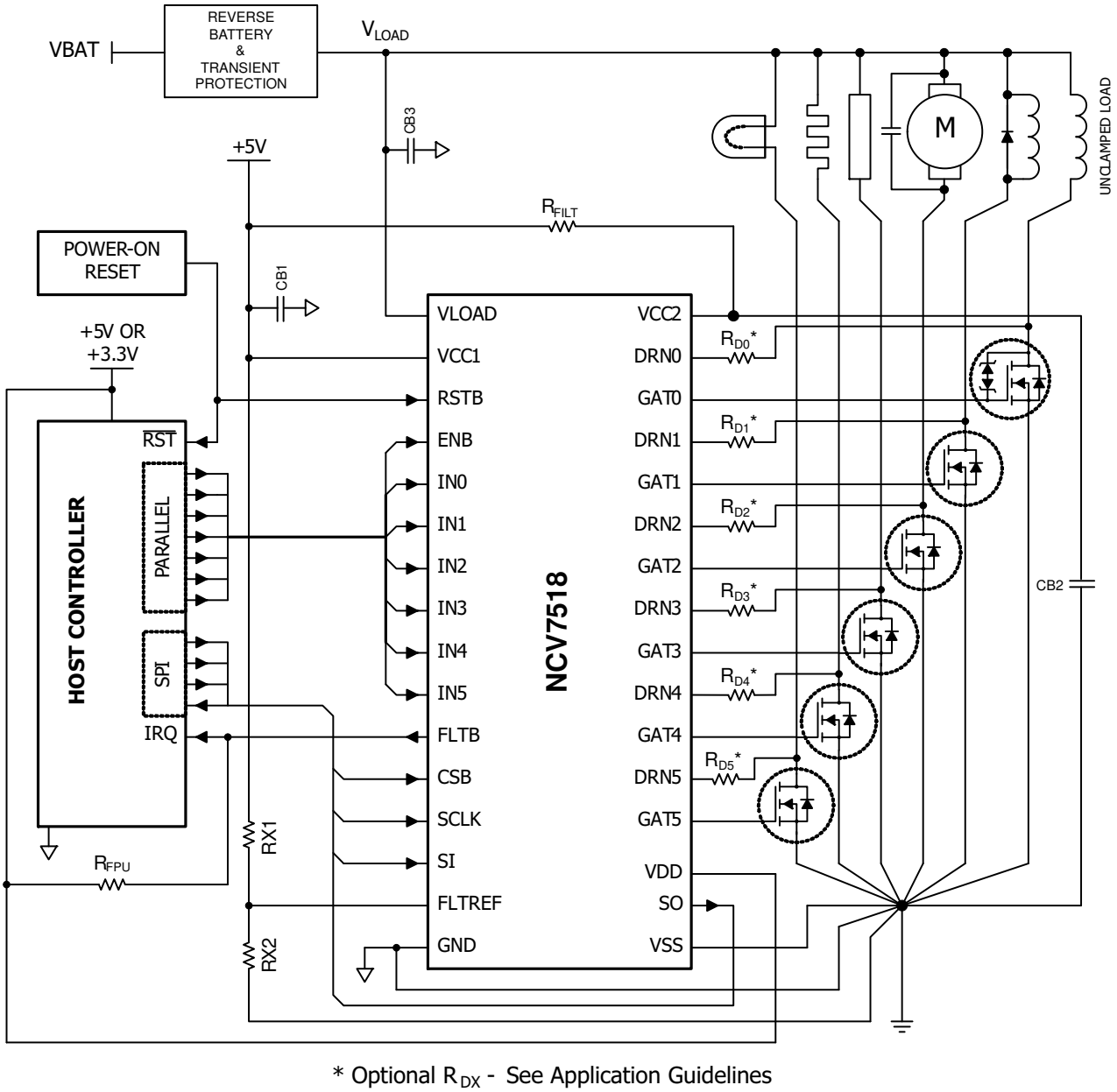


Figure 1. Block Diagram



* Optional R_{DX} - See Application Guidelines

Figure 2. Application Diagram

PACKAGE PIN DESCRIPTION 32 PIN QFN EXPOSED PAD PACKAGE

Label	Description
FLTREF	Analog Fault Detect Threshold: 5 V Compliant
DRN0 – DRN5	Analog Drain Feedback
GAT0 – GAT5	Analog Gate Drive: 5 V Compliant
RSTB	Digital Master Reset Input: 3.3 V/5 V (TTL) Compatible
ENB	Digital Master Enable Input: 3.3 V/5 V (TTL) Compatible
IN0 – IN5	Digital Parallel Input: 3.3 V/5 V (TTL) Compatible
CSB	Digital Chip Select Input: 3.3 V/5 V (TTL) Compatible
SCLK	Digital Shift Clock Input: 3.3 V/5 V (TTL) Compatible
SI	Digital Serial Data Input: 3.3 V/5 V (TTL) Compatible
SO	Digital Serial Data Output: 3.3 V/5 V Compliant
FLTB	Digital Open-Drain Output: 3.3 V/5 V Compliant
VLOAD	Power Supply – Diagnostic References and Currents
VCC1	Power Supply – Low Power Path
GND	Power Return – Low Power Path – Device Substrate
VCC2	Power Supply – Gate Drivers
VDD	Power Supply – Serial Output Driver
VSS	Power Return – VLOAD, VCC2, VDD
EP	Exposed Pad – Connected to GND – Device Substrate

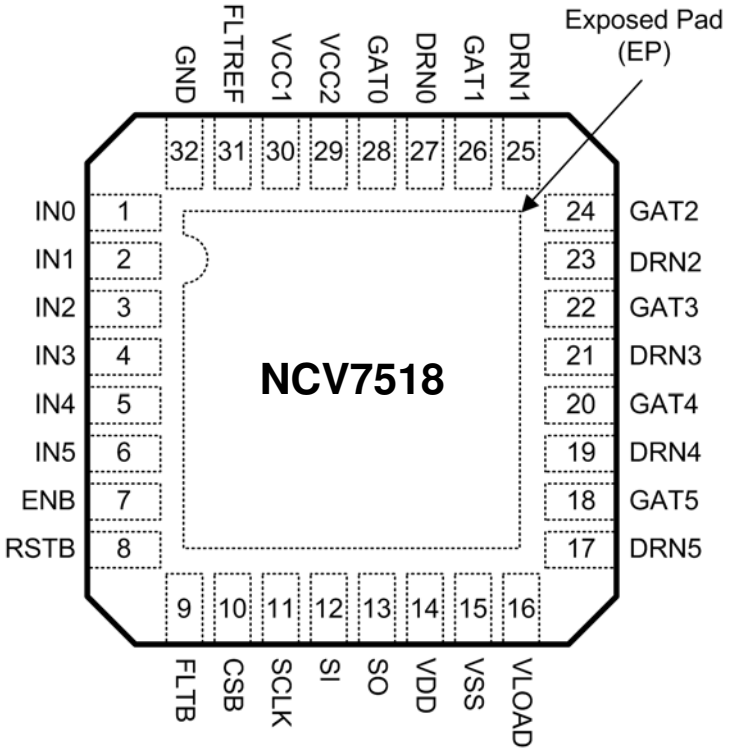


Figure 3. 32 Pin QFN Exposed Pad Pinout (Top View)

MAXIMUM RATINGS (Voltages are with respect to device substrate.)

Rating	Value	Unit
DC Supply – V_{LOAD}	–0.3 to 40	V
DC Supply – V_{CC1}, V_{CC2}, V_{DD}	–0.3 to 5.8	V
Difference Between V_{CC1} and V_{CC2}	±0.3	V
Difference Between GND (Substrate) and V_{SS}	±0.3	V
Drain Input Clamp Forward Voltage Transient (≤2 ms, ≤1% duty)	78	V
Drain Input Clamp Forward Current Transient (≤2 ms, ≤1% duty)	10	mA
Drain Input Clamp Energy Repetitive (≤2 ms, ≤1% duty)	1.56	mJ
Drain Input Clamp Reverse Current $V_{DRNX} \geq -1.0$ V	–50	mA
Input Voltage (Any Input Other Than Drain)	–0.3 to 5.8	V
Output Voltage (Any Output)	–0.3 to 5.8	V
Junction Temperature, T_J	–40 to 150	°C
Storage Temperature, T_{STG}	–65 to 150	°C
Peak Reflow Soldering Temperature: Lead-free 60 to 150 seconds at 217°C (Note 1)	260 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. See or download ON Semiconductor's Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ATTRIBUTES

Characteristic		Value
ESD Capability Human Body Model per AEC–Q100–002	Drain Feedback Pins (Note 3) VLOAD Pin All Other Pins	≥ ±4.0 kV ≥ ±1.5 kV ≥ ±2.0 kV
Moisture Sensitivity	(Note 2)	MSL3
Package Thermal Resistance – Still-air Junction-to-Ambient, $R\theta_{JA}$ Junction-to-Exposed Pad, $R\Psi_{JPAD}$	 (Note 4) (Note 5) 	 95°C/W 46°C/W 3.2°C/W

2. See or download ON Semiconductor's Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
3. With GND & V_{SS} pins tied together – path between drain feedback pins and GND, or between drain feedback pins.
4. Based on JESD51–3, 1.2 mm thick FR4, 2S0P PCB, 2 oz. signal, 20 thermal vias to 400 mm^2 spreader on bottom layer.
5. Based on JESD51–7, 1.2 mm thick FR4, 1S2P PCB, 2 oz. signal, 20 thermal vias to 80 x 80 mm 1 oz. internal spreader planes.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	MIN	MAX	Unit
V_{LOAD}	Diagnostic References and Currents Power Supply Voltage	7.5	18.0	V
V_{DRNX}	Drain Input Feedback Voltage	–0.3	60	V
V_{CC1}	Main Power Supply Voltage	4.75	5.25	V
V_{CC2}	Gate Drivers Power Supply Voltage	V_{CC1} – 0.3	V_{CC1} + 0.3	V
V_{DD}	Serial Output Driver Power Supply Voltage	3.0	V_{CC1}	V
V_{FLTREF}	Fault Detect Threshold Reference Voltage	0.35	2.75	V
V_{IN} High	Logic High Input Voltage	2.0	V_{CC1}	V
V_{IN} Low	Logic Low Input Voltage	0	0.8	V
T_A	Ambient Still-air Operating Temperature	–40	125	°C
t_{RESET}	Startup Delay at Power-on Reset (POR) (Note 6)	500	–	μs

6. Minimum wait time until device is ready to accept serial input data.

PARAMETRIC TABLES

ELECTRICAL CHARACTERISTICS

(4.75 V ≤ V_{CCX} ≤ 5.25 V, V_{DD} = V_{CCX}, 4.5 V ≤ V_{LOAD} ≤ 18 V, RSTB = V_{CCX}, ENB = 0, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 7)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
V_{CC1} SUPPLY						
Operating Current – V_{CC1} = 5.25 V, V_{FLTREF} = 2.75 V	I_{CC1A}	RSTB = 0	–	2.80	5.0	mA
	I_{CC1B}	ENB = 0, RSTB = V_{CC1}, V_{DRNX}=0 V, GAT_X Drivers Off	–	3.10	5.0	mA
	I_{CC1C}	ENB = 0, RSTB = V_{CC1}, GAT_X Drivers On	–	2.80	5.0	mA
Power-On Reset Threshold	POR	V_{CC1} Rising	3.65	4.125	4.60	V
Power-On Reset Hysteresis	PORH		0.150	0.385	–	V
V_{CC2} SUPPLY						
Operating Current	I_{CC2}	V_{CC2} = 5.25 V, ENB = 0, RSTB = V_{CC1} = 5.25 V V_{DRNX} = 0 V, GAT_X Drivers Off	–	2.80	5.0	mA
V_{DD} SUPPLY						
Standby Current	I_{DD1}	V_{DD} = 5.25V, ENB = 0, RSTB = V_{CC1} = 5.25 V SO = Z	–	25.0	34.0	μA
Operating Current	I_{DD2}	V_{DD} = 5.25V, ENB = 0, RSTB = V_{CC1} = 5.25 V SO = H or L	–	625	850	μA
V_{LOAD} SUPPLY						
Standby Current	V_{LDSBY}	V_{LOAD} = 13.2 V, 0 ≤ V_{CC1} ≤ 5.25, ENB = RSTB = V_{CC1}, T_A ≤ 85°C	–	–	5.0	μA
Operating Current	V_{LDOP}	V_{LOAD} = 18 V, ENB = 0, RSTB = V_{CC1}, V_{DRNX} = 0 V	–	11	15	mA
DIGITAL I/O						
V_{IN} High	V_{IHX}	RSTB, ENB, IN_X, SI, SCLK, CSB	2.0	–	–	V
V_{IN} Low	V_{ILX}	RSTB, ENB, IN_X, SI, SCLK, CSB	–	–	0.8	V
V_{IN} Hysteresis	IN_{HY}	RSTB, ENB, IN_X, SI, SCLK, CSB	100	330	500	mV
Input Pullup Resistance	R_{PUX}	ENB, CSB, V_{IN} = 0 V	50	125	200	kΩ
Input Pulldown Resistance	R_{PDX}	RSTB, IN_X, SI, SCLK, V_{IN} = V_{CC1}	50	125	200	kΩ
SO Low Voltage	V_{SOL}	V_{DD} = 3.0 V, I_{SINK} = 2 mA	–	–	0.4	V
SO High Voltage	V_{SOH}	V_{DD} = 3.0 V , I_{SOURCE} = 2 mA	V_{DD} – 0.6	–	–	V
SO Output Resistance	R_{SO}	Output High or Low	–	25	–	Ω
SO Tri-State Leakage Current	SO_{LKG}	CSB = 3.0 V	–5.0	–	5.0	μA
FLTB Low Voltage	V_{FLTB}	FLTB Active, I_{FLTB} = 1.25 mA	–	–	0.4	V
FLTB Leakage Current	I_{FLTLKG}	V_{FLTB} = V_{CC1}	–	–	10	μA
FAULT DETECTION – GATX ON						
FLTREF Input Current	I_{FLTREF}	0 V ≤ V_{FLTREF} ≤ 2.75 V	–1.0	–	1.0	μA
FLTREF Input Linear Range	V_{REFLIN}	(Note 8)	0.35	–	2.75	V
FLTREF Op-amp V_{CC1} PSRR	PSRR	(Note 8)	30	–	–	dB

7. Min/Max values are valid for the temperature range –40°C ≤ T_J ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.
8. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)
(4.75 V ≤ V_{CCX} ≤ 5.25 V, V_{DD} = V_{CCX}, 4.5 V ≤ V_{LOAD} ≤ 18 V, RSTB = V_{CCX}, ENB = 0, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 7)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
FAULT DETECTION – GATX ON						
DRN_X Shorted Load Threshold V_{FLTREF} = 0.35V	V_{25}	Register R2.C[11:9] = 000 (DEFAULT)	20	25	30	% V_{FLTREF}
	V_{40}	Register R2.C[11:9] = 001	35	40	45	
	V_{50}	Register R2.C[11:9] = 010	45	50	55	
	V_{60}	Register R2.C[11:9] = 011	55	60	65	
	V_{70}	Register R2.C[11:9] = 100	65	70	75	
	V_{80}	Register R2.C[11:9] = 101	75	80	85	
	V_{90}	Register R2.C[11:9] = 110	85	90	95	
	V_{100}	Register R2.C[11:9] = 111	95	100	105	
DRN_X Input Leakage Current	ID_{LKG}	0 V ≤ V_{CC1} = V_{CC2} = V_{DD} ≤ 5.25 V, RSTB = 0 V, V_{DRNX} = 32 V T_A ≤ 25°C	–5.0 –1.0	– –	5.0 1.0	μA
DRN_X Clamp Voltage	V_{CL}	I_{DRNX}= $I_{CL(MAX)}$ =10 mA; Transient (≤2 ms, ≤1% Duty)	60	–	78	V
Fault Detection – GATX OFF (7.5 V ≤ V_{LOAD} ≤ 18 V, Register R3.D[11:0] = 1)						
DRN_X Diagnostic Current – Proportional to V_{LOAD}	I_{SG}	Short to GND Detection, V_{DRNX} = 43%V_{LOAD}	– 81	–60	– 39	μA / V
	I_{OL}	Open Load Detection, V_{DRNX} = 61%V_{LOAD}	2.73	4.20	5.67	μA / V
	I_{CHG}	Transient Fast Charge Current, 0 < V_{DRNX} < V_{CTR}, t < $t_{BL(OFF)}$	–270	–200	–130	μA / V
Diagnostic Current Limit Point	V_{LIM}	Current Clamped and No Longer Proportional to V_{LOAD}	20	–	–	V
DRN_X Fault Threshold Voltage	V_{SG}	Short to GND Detection	39.56	43	46.44	%V_{LOAD}
	V_{OL}	Open Load Detection	56.12	61	65.88	%V_{LOAD}
DRN_X Off State Bias Voltage	V_{CTR}		46.92	51	55.08	%V_{LOAD}
VLOAD Undervoltage Threshold	V_{LDUV}	VLOAD Decreasing	4.1	6.3	7.5	V
FAULT TIMERS						
Channel Fault Blanking Timers (Figure 6)	$t_{BL(ON)}$	V_{DRNX} = V_{LOAD}; IN_X rising to FLTB Falling Register R2.C[6:5] = 00	4.8	6	7.2	μs
		Register R2.C[6:5] = 01	9.6	12	14.4	
		Register R2.C[6:5] = 10 (DEFAULT)	19.2	24	28.8	
		Register R2.C[6:5] = 11	28.8	48	57.6	
	$t_{BL(OFF)}$	V_{DRNX} = 0V; IN_X falling to FLTB Falling Register R2.C[8:7] = 00	44	55	66	μs
		Register R2.C[8:7] = 01	65	81	97	
		Register R2.C[8:7] = 10 (DEFAULT)	130	162	195	
		Register R2.C[8:7] = 11	260	325	390	
Channel Fault Filter Timer (Figure 7)	$t_{FF(ON)}$ $t_{FF(OFF)}$		2.0 44	3.0 55	4.0 66	μs
Global Fault Retry Timer (Figure 8)	t_{FR}	Register R0.M[5:0] = 1	6	8	10	ms
Timer Clock	f_{CLK}	RSTB = V_{CC1}	–	4.0	–	MHz

7. Min/Max values are valid for the temperature range –40°C ≤ T_J ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.
8. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)
(4.75 V ≤ V_{CCX} ≤ 5.25 V, V_{DD} = V_{CCX}, 4.5 V ≤ V_{LOAD} ≤ 18 V, RSTB = V_{CCX}, ENB = 0, –40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 7)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GATE DRIVER OUTPUTS						
GAT_X Output Resistance	R_{GATX}	Output High or Low	200	350	500	Ω
GAT_X High Output Current	I_{GSRC}	V_{GATX} = 0 V	–26.25	–	–9.5	mA
GAT_X Low Output Current	I_{GSNK}	V_{GATX} = V_{CC2}	9.5	–	26.25	mA
Turn-On Propagation Delay	$t_{P(ON)}$	IN_X to GATx (Figure 4)	–	–	1.0	μs
		CSB to GAT_X (Figure 5)				
Turn-Off Propagation Delay	$t_{P(OFF)}$	IN_X to GAT_X (Figure 4)	–	–	1.0	μs
		CSB to GAT_X (Figure 5)				
Output Rise Time	t_R	20% to 80% of V_{CC2}, C_{LOAD} = 400 pF (Figure 4, Note 8)	–	–	277	ns
Output Fall Time	t_F	80% to 20% of V_{CC2}, C_{LOAD} = 400 pF (Figure 4, Note 8)	–	–	277	ns
SERIAL PERIPHERAL INTERFACE (Figure 9) V_{CCX} = 5.0 V, V_{DD} = 3.3 V, F_{SCLK} = 4.0 MHz, C_{LOAD} = 200 pF						
SO Supply Voltage	V_{DD}	3.3 V Interface	3.0	3.3	3.6	V
		5 V Interface	4.5	5.0	5.5	V
SCLK Clock Period	t_{SCLK}		–	250	–	ns
Maximum Input Capacitance	C_{INX}	SI, SCLK (Note 8)	–	–	12	pF
SCLK High Time	t_{CLKH}	SCLK = 2.0 V to 2.0 V	125	–	–	ns
SCLK Low Time	t_{CLKL}	SCLK = 0.8 V to 0.8 V	125	–	–	ns
SI Setup Time	t_{SISU}	SI = 0.8 V/2.0 V to SCLK = 2.0 V (Note 8)	25	–	–	ns
SI Hold Time	t_{SIHD}	SCLK = 2.0 V to SI = 0.8 V/2.0 V (Note 8)	25	–	–	ns
SO Rise Time	t_{SOR}	(20% V_{SO} to 80% V_{DD}) C_{LOAD} = 200 pF (Note 8)	–	25	50	ns
SO Fall Time	t_{SOF}	(80% V_{SO} to 20% V_{DD}) C_{LOAD} = 200 pF (Note 8)	–	–	50	ns
CSB Setup Time	t_{CSBSU}	CSB = 0.8 V to SCLK = 2.0 V (Note 8)	60	–	–	ns
CSB Hold Time	t_{CSBHD}	SCLK = 0.8 V to CSB = 2.0 V (Note 8)	75	–	–	ns
CSB to SO Time	t_{CS-SO}	CSB = 0.8 V to SO Data Valid (Note 8)	–	65	125	ns
SO Delay Time	SO_{DLY}	SCLK = 0.8 V to SO Data Valid (Note 8)	–	65	125	ns
Transfer Delay Time	CS_{DLY}	CSB Rising Edge to Next Falling Edge (Note 8)	1.6	–	–	μs

7. Min/Max values are valid for the temperature range –40°C ≤ T_J ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.
8. Guaranteed by design.

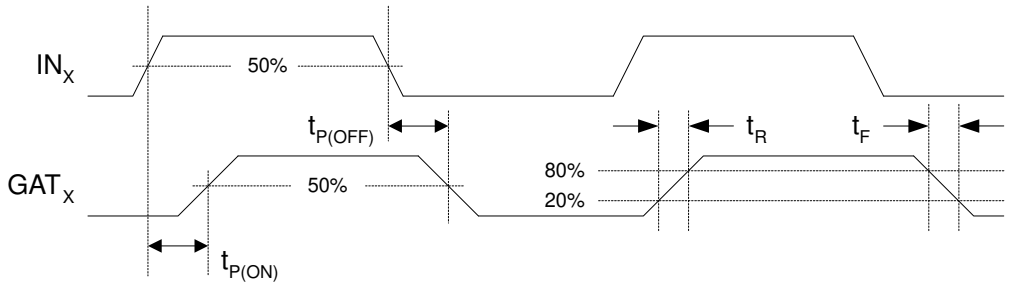


Figure 4. Gate Driver Timing Diagram – Parallel Input

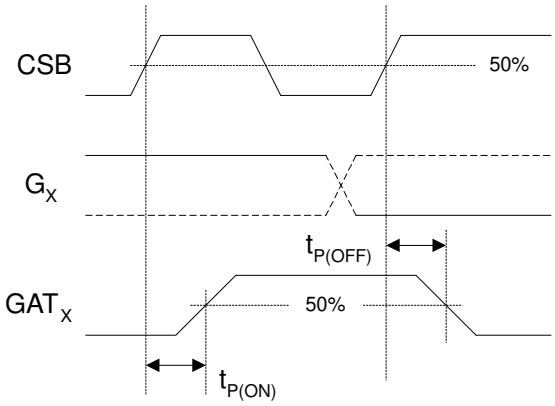


Figure 5. Gate Driver Timing Diagram – Serial Input

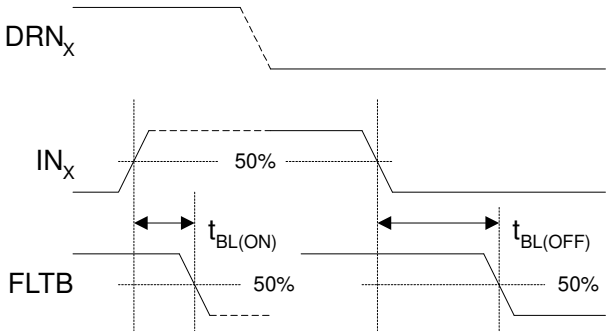


Figure 6. Blanking Timing Diagram

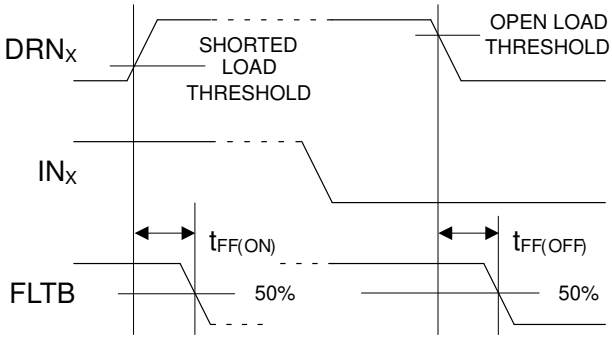


Figure 7. Filter Timing Diagram

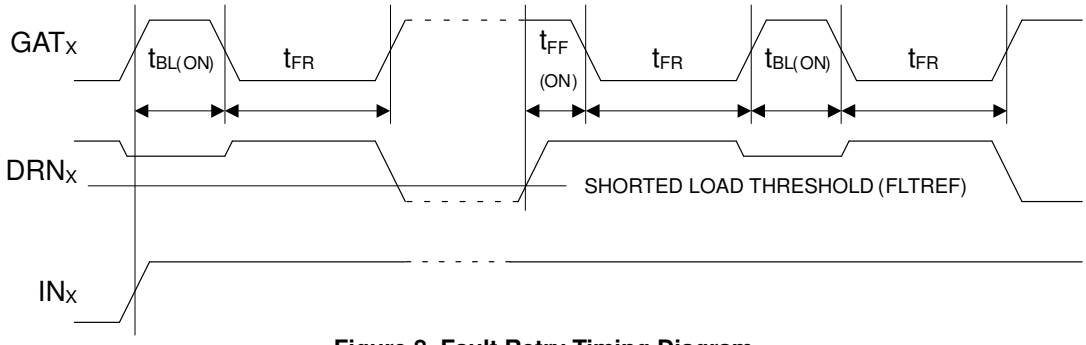
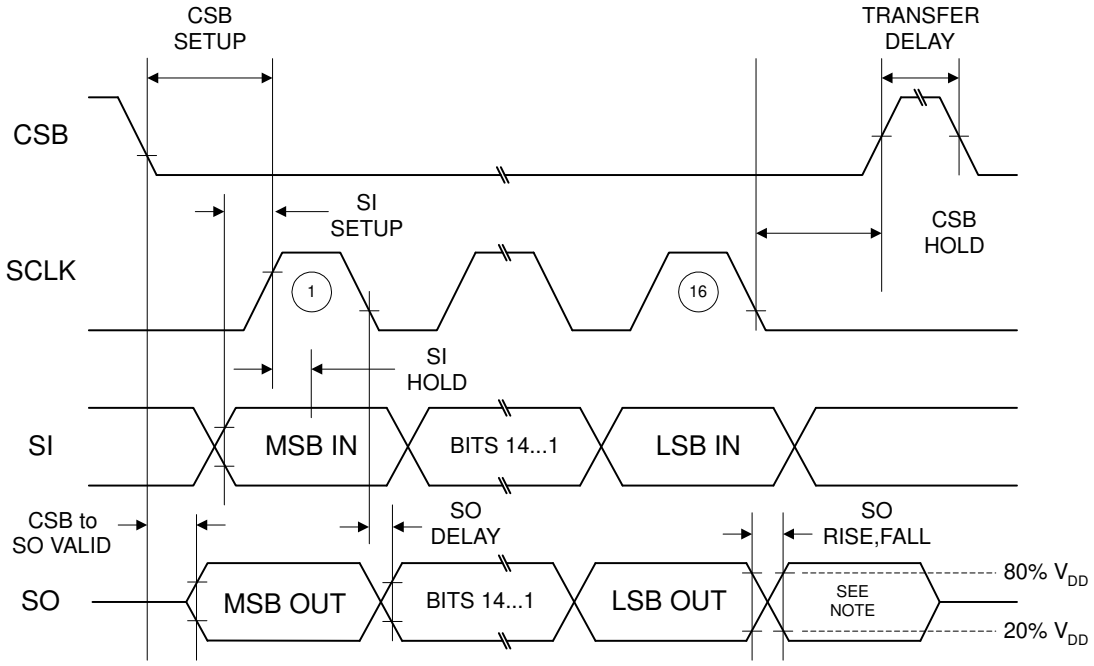


Figure 8. Fault Retry Timing Diagram



Note: Not defined but usually MSB of data just received.

Figure 9. SPI Timing Diagram

DETAILED OPERATING DESCRIPTION

General

The NCV7518 is a six channel general-purpose low-side pre-driver for controlling and protecting N-type logic level MOSFETs. Programmable fault detection and protection modes allow the device to accommodate a wide range of external MOSFETs and loads, providing flexible application solutions. Separate power supply pins are provided for low and high current paths to improve analog accuracy and digital signal integrity.

Power Up/Down Control

An internal Power-On Reset (POR) monitors V_{CC1} and causes all GAT_X outputs to be held low until sufficient voltage is available to allow proper control of the device. All internal registers are initialized to their defaults, status data is cleared, and the open-drain fault flag (FLTB) is disabled.

When V_{CC1} exceeds the POR threshold, the device is initialized and ready to accept input data. When V_{CC1} falls below the POR threshold during power down, FLTB is disabled and all GAT_X outputs are driven and held low until V_{CC1} falls below about 1.5 V.

RSTB and ENB Inputs

The active-low RSTB input with a resistive pull-down allows device reset by an external signal. When RSTB is brought low, all GAT_X outputs, the timer clock, the SPI, and the FLTB flag are disabled. All internal registers are initialized to their default states, status data is cleared, and the SPI and FLTB are enabled when RSTB goes high.

The active-low ENB input with resistive pull-up provides a global enable. ENB disables all GAT_X outputs and diagnostics, and resets the auto-retry timer when brought high. The SPI is enabled, fault data is not cleared and registers remain as programmed. Faulted outputs are re-enabled when ENB goes low.

SPI Communication

The NCV7518 is a 16-bit slave device. Communication between the host and the device may either be parallel via individual CSB addressing or daisy-chained through other devices using a compatible SPI protocol.

The active-low CSB chip select input has a pull-up resistor. The SI and SCLK inputs have pull-down resistors. The recommended idle state for SCLK is low. The tri-state SO line driver is powered via the V_{DD} and the V_{SS} pins, and can be supplied with either 3.3 V or 5 V.

The device employs odd parity, and frame error detection that requires integer multiples of 16 SCLK cycles during each CSB high-low-high cycle (valid communication frame.) A parity or frame error does not affect the FLTB flag.

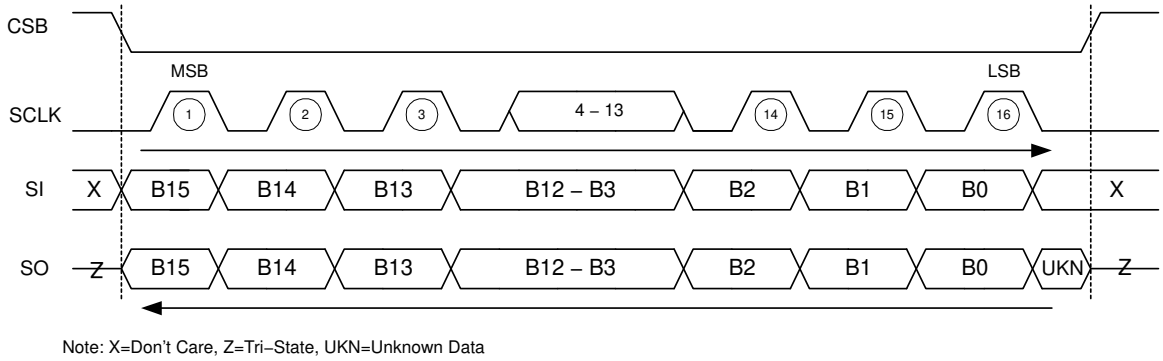
The host initiates communication when a selected device's CSB pin goes low. Output data is simultaneously sent MSB first from the SO pin while input data is received MSB first at the SI pin under synchronous control of the master's SCLK signal while CSB is held low (Figure 10). Output data changes on the falling edge of SCLK and is guaranteed valid before the next rising edge of SCLK. Input data received must be valid before the rising edge of SCLK.

When CSB goes low, frame error detection is initialized, output data is transferred to the SPI, and the FLTB flag is disabled and reset if previously set.

If a valid frame has been received when CSB goes high, the last multiple of 16 bits received is decoded into command data, and FLTB is re-enabled. The FLTB flag will be set if a fault is detected.

If a frame or parity error is detected when CSB goes high, new command data is ignored, and previous fault data remains latched and available for retrieval during the next valid frame. The FLTB flag will be set if a fault (not a frame or parity error) is detected.

The interaction between CSB and FLTB facilitates fault polling. When multiple NCV7518 devices are configured for parallel SPI access with individual CSB addressing, the device reporting a fault can be identified by pulsing each CSB in turn.



Note: X=Don't Care, Z=Tri–State, UKN=Unknown Data

Figure 10. SPI Communication Frame Format

Serial Data and Register Structure

The 16-bit data received by the NCV7518 is decoded into a 3-bit address, a 12-bit data word, and an odd parity bit (Figure 11). The upper three bits, beginning with the received MSB, are fully decoded to address one of eight registers. The valid register addresses are shown in Table 1. The input command structure is shown in Table 3. Each register is later described in detail.

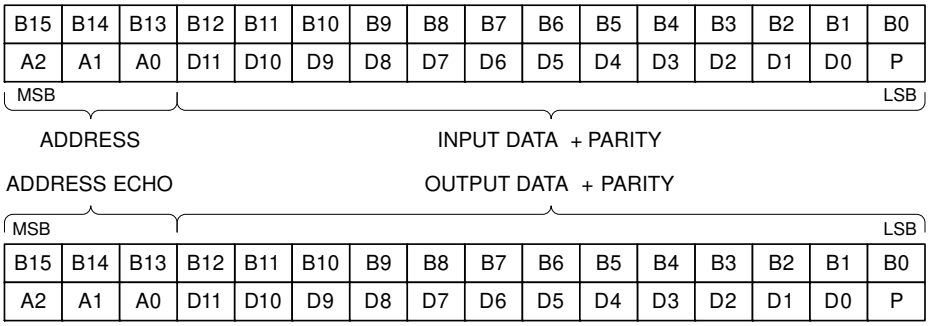


Figure 11. SPI Data Format

Table 1. VALID REGISTER ADDRESSES

Function	Type	Alias	A2	A1	A0
GATE & MODE SELECT	W	R0	0	0	0
DIAGNOSTIC PULSE	W	R1	0	0	1
DIAGNOSTIC CONFIG 1	W	R2	0	1	0
DIAGNOSTIC CONFIG 2	W	R3	0	1	1
STATUS CH2:0	R	R4	1	0	0
STATUS CH5:3	R	R5	1	0	1
REVISION INFO	R	R6	1	1	0
RESERVED	TEST	R7	1	1	1

The 16-bit data sent by the NCV7518 is an echo of the previously received 3-bit address with the remainder of the 12-bit data and parity bit formatted into one of four response types − an echo of the previously received input data, the diagnostic status information, the device revision information, or a transmission error (Table 2). The first response frame sent after reset (via POR or RSTB) is the device revision information.

Table 2. OUTPUT RESPONSE TYPES

ECHO RESPONSE															
A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
ADDRESS ECHO			INPUT DATA ECHO												?
DIAGNOSTIC STATUS RESPONSE															
1	0	0	0	0	ENB	CH2	CH1	CH0	CH2	CH1	CH0	CH2	CH1	CH0	?
1	0	1	0	0	ENB	CH5	CH4	CH3	CH5	CH4	CH3	CH5	CH4	CH3	?
						ST2			ST1			ST0			
DEVICE REVISION RESPONSE															
1	1	0	0	0	0	0	0	0	D5	D4	D3	D2	D1	D0	?
									DIE REVISION			MASK REVISION			
TRANSMISSION ERROR RESPONSE															
1	1	1	0	1	0	1	0	1	0	1	0	1	0	D0	P
PARITY ERROR														1	0
1	1	1	0	1	0	1	0	1	0	1	0	1	0	D0	P
FRAME ERROR														0	1

Table 3. INPUT COMMAND STRUCTURE OVERVIEW

ALIAS	3-BIT ADDR			12-BIT COMMAND INPUT DATA												ODD PARITY
R0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	0	0	0	M5	M4	M3	M2	M1	M0	G5	G4	G3	G2	G1	G0	?
GATE & MODE SELECT				1 = AUTO RETRY DEFAULT = LATCH OFF						1 = GATx ON DEFAULT = ALL OFF						
R1	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	0	0	1	F5	F4	F3	F2	F1	F0	N5	N4	N3	N2	N1	N0	?
DIAGNOSTIC PULSE				1 = DIAGNOSTIC OFF PULSE DEFAULT = 0						1 = DIAGNOSTIC ON PULSE DEFAULT = 0						
R2	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	0	1	0	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	?
DIAGNOSTIC CONFIG 1				%VFLTREF SELECT			TBLANK OFF		TBLANK ON		NOT USED		CHANNEL SELECT			
R3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	0	1	1	CH5	CH4	CH3	CH2	CH 1	CH0	CH5	CH 4	CH 3	CH 2	CH 1	CH 0	?
DIAGNOSTIC CONFIG 2				1 = ENABLE FAST CHARGE DEFAULT = DISABLE						1 = ENABLE DIAGNOSTIC DEFAULT = ENABLE						
				OPEN LOAD DIAGNOSTIC ENABLE/DISABLE												
R4	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	?
DIAGNOSTIC STATUS CH2:CH0						RETURN ENB STATUS; D[9] = 0 = ENABLED RETURN CH2:CH0 STATUS; DEFAULT D[8:0] = 1											
R5	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	?
DIAGNOSTIC STATUS CH5:CH3						RETURN ENB STATUS; D[9] = 0 = ENABLED RETURN CH5:CH3 STATUS; DEFAULT D[8:0] = 1											
R6	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	?
REVISION INFORMATION										RETURN REVISION INFORMATION						
R7	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	1	1	1	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	?
RESERVED				RESERVED FOR TEST MODE												

Gate & Mode Select – Register R0

Each GAT_X output is turned on/off serially by programming its respective G_X bit (Table 4). When parallel inputs $IN_X = 0$, setting $R0.G_X = 1$ causes the selected GAT_X output to drive its external MOSFET's gate to V_{CC2} (ON). Setting $R0.G_X = 0$ causes the selected GAT_X output to drive its external MOSFET's gate to V_{SS} (OFF.) Note that the actual state of the output depends on POR, RSTB, ENB and shorted load fault states ($SHRT_X$) as later defined by Equation 1. Default after reset is R0.D[11:0] = 0 (all channels latch-off mode, all outputs OFF.) R0 is an echo type response register.

The disable mode for shorted load (on-state) faults is controlled by each channel's respective M_X bit. Setting $R0.M_X = 0$ causes the selected GAT_X output to latch-off when a fault is detected. Setting $R0.M_X = 1$ causes the selected GAT_X output to auto-retry when a fault is detected.

Recovery from latch-off is performed for all channels by disabling then re-enabling the device via the ENB input. Recovery for selected channels is performed by reading the status registers (R4, R5) for the faulted channels then executing a diagnostic ON or OFF pulse for the desired channels.

When auto-retry is selected, input changes for turn-on time are ignored while the retry timer is active. Once active, the timer will run to completion of the programmed time. The output will follow the input at the end of the retry interval. The timer is reset when ENB = 1 or when the mode is changed to latch-off.

Table 4. GATE & MODE SELECT REGISTER

R0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	0	0	0	M5	M4	M3	M2	M1	M0	G5	G4	G3	G2	G1	G0	?
				1 = AUTO RETRY DEFAULT = LATCH OFF						1 = GATx ON DEFAULT = ALL OFF						

Diagnostic Pulse Select – Register R1

The NCV7518 has functionality to perform either on-state or off-state diagnostic pulses (Table 5) The function is provided for applications having loads normally in a continuous on or off state. The diagnostic pulse function is available for both latch-off and auto-retry modes. The pulse executes for the selected channel(s) on low-high transition on CSB. Default after reset is R1.D[11:0] = 0. R1 is an echo type response register.

Diagnostic pulses have priority and are not dependant on the input (IN_X, G_X) or the output (GAT_X) states. The pulse does not execute if: ENB =1 (device is disabled); both an ON and OFF pulse is simultaneously requested for the same channel; an ON or OFF pulse is requested and a SCB (shorted load) diagnostic code is present for the selected channels; an ON or OFF pulse is requested while a pulse is currently executing in the selected channels (i.e. a blanking timer is active); the selected channels are currently under auto-retry control (i.e. refresh timer is active).

When R1.F_X = 1, the diagnostic OFF pulse command is executed. The open load diagnostic is turned on if disabled (see Diagnostic Config 2 – R3), the output changes state for the programmed $t_{BL(OFF)}$ blanking period, and the diagnostic status is latched if of higher priority than the previous status. ICHG current is turned on if enabled via R3. The output assumes the currently commanded state at the end of the pulse.

When R1.N_X = 1, the diagnostic ON pulse command is executed. The output changes state for the programmed $t_{BL(ON)}$ blanking period, and the diagnostic status is latched if of higher priority than the previous status. The output assumes the currently commanded state at the end of the pulse. A flowchart for the diagnostic pulse is given in Figure 16.

Table 5. DIAGNOSTIC PULSE SELECT REGISTER

R1	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	0	0	1	F5	F4	F3	F2	F1	F0	N5	N4	N3	N2	N1	N0	?
				1 = DIAGNOSTIC OFF PULSE DEFAULT = 0						1 = DIAGNOSTIC ON PULSE DEFAULT = 0						

Diagnostic Config 1 – Register R2

The diagnostic Config 1 register programs the turn-on/off blanking time and shorted load fault detection references for each channel (Table 6) Bits R2.C[2:0] select which channels receive the configuration data (Table 7). Bits R2.C[8:5] select turn-on/off blanking time (Table 8). Bits R2.C[11:9] select the fault reference (Table 9). Default after reset is indicated by "(DEF)" in the tables. R2 is an echo type response register.

If a blanking timer is currently running when the register is changed, the new value is accepted but will not take effect until the next activation of the timer.

Table 6. DIAGNOSTIC CONFIG 1 REGISTER

R2	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	0	1	0	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	?
				%VFLTREF SELECT			TBLANK OFF		TBLANK ON		NOT USED		CHANNEL SELECT			

Table 7. CHANNEL SELECT

C2	C1	C0	CHANNEL SELECT
0	0	0	NONE
0	0	1	CHANNEL 0
0	1	0	CHANNEL 1
0	1	1	CHANNEL 2
1	0	0	CHANNEL 3
1	0	1	CHANNEL 4
1	1	0	CHANNEL 5
1	1	1	ALL (DEF)

Table 8. BLANKING TIME SELECT

C8	C7	C6	C5	C4	C3	TBLANK OFF	TBLANK ON
				X	X		
		0	0				6 μs
		0	1				12 μs
		1	0				24 μs (DEF)
		1	1				48 μs
0	0					55 μs	
0	1					81 μs	
1	0					162 μs (DEF)	
1	1					325 μs	

Table 9. FAULT REFERENCE SELECT

C11	C10	C9	%VFLTREF SELECT
0	0	0	25 (DEF)
0	0	1	40
0	1	0	50
0	1	1	60
1	0	0	70
1	0	1	80
1	1	0	90
1	1	1	100

Diagnostic Config 2 – Register R3

Off-state open load diagnostic currents for each channel can be enabled or disabled for LED loads. Short to GND diagnostic is unaffected. Fast charge current (ICHG) can be enabled or disabled for capacitive loads. Channels are selected by bit positions in the register (Table 10.) Open load status (OLF) information is suppressed when the diagnostic is turned off via R3. Open load diagnostic and OLF status is temporarily enabled when a diagnostic off pulse is executed via R1. Default after reset is R3.D[11:6] = 0 and R3.D[5:0] = 1. R3 is an echo type response register.

Table 10. DIAGNOSTIC CONFIG 2 REGISTER

R3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
	0	1	1	CH5	CH4	CH3	CH2	CH1	CH0	CH5	CH4	CH3	CH2	CH1	CH0	?
				1 = ENABLE FAST CHARGE DEFAULT = DISABLE						1 = ENABLE DIAGNOSTIC DEFAULT = ENABLE						
				OPEN LOAD DIAGNOSTIC ENABLE/DISABLE												

Diagnostic Status Registers – Register R4 & R5

Diagnostic status and ENB status information is returned when R4 or R5 is selected (Table 11) Diagnostic status information for each channel is 3-bit (ST2:0) priority encoded (Table 12). Bit D[9] returns the state of the ENB input e.g. D[9] = 0 when ENB = 0 (enabled). Default response after reset or SPI read is D[8:0] = 1 (“Diagnostic Not Complete”).

Table 11. DIAGNOSTIC STATUS REGISTERS

	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P	
R4	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	?	SI
	1	0	0	0	0	ENB	CH2	CH1	CH0	CH2	CH1	CH0	CH2	CH1	CH0	?	SO
R5	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	?	SI
	1	0	1	0	0	ENB	CH5	CH4	CH3	CH5	CH4	CH3	CH5	CH4	CH3	?	SO
							ST2			ST1			ST0				

Table 12. DIAGNOSTIC STATUS ENCODING

ST2	ST1	ST0	STATUS	PRIORITY
0	0	0	INVALID	–
0	0	1	SCB – SHORT TO BATTERY	1 HIGHEST
0	1	0	SCG – SHORT TO GROUND	2
0	1	1	OLF – OPEN LOAD	3 (Note)
1	0	0	Diagnostic Complete – No Fault	4
1	0	1	No SCB Fault – ON State	5
1	1	0	No SCG/OLF Fault – OFF State	6
1	1	1	Diagnostic Not Complete (DEFAULT)	7 LOWEST

NOTE: OLF status report is suppressed when open load diagnostic is turned off via Diagnostic Config 2 – register R3

Status is latched for the currently higher priority fault and is not demoted if a fault of lower priority occurs. The status registers are reset to “Diagnostic Not Complete” after reading the registers, or by asserting a reset via RSTB. Status registers are not affected by ENB.

Revision Information – Register R6

Device revision information is returned when R6 is selected (Table 13). Output bits D[11:6] are hard coded to 0, bits D[5:3] are hard coded with the die (silicon) revision, and bits D[2:0] are hard coded with the mask (interconnect) revision. The first response frame sent after reset is the device revision information. The revision encoding scheme is shown in Table 14.

Mask revision may be incremented when an interconnect revision is made. Die revision is incremented when a silicon revision is made. Mask revision is reset to “000” when a die revision is made.

Table 13. DEVICE REVISION INFORMATION

	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P	
R6	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	?	SI
	1	1	0	0	0	0	0	0	0	D5	D4	D3	D2	D1	D0	?	SO
										DIE REV			MASK REV				

Table 14. DEVICE REVISION ENCODING

D5	D4	D3		D2	D1	D0	
DIE			REV	MASK			REV
0	0	0	A	0	0	0	0
0	0	1	B	0	0	1	1
0	1	0	C	0	1	0	2
0	1	1	D	0	1	1	3
1	0	0	E	1	0	0	4
1	0	1	F	1	0	1	5
1	1	0	G	1	1	0	6
1	1	1	H	1	1	1	7

Reserved – Register R7

Register R7 is reserved for factory test use. Data sent to R7 is ignored. In normal operation, R7 is an echo type response register. In the event of a transmission error, R7 responds with either a parity or frame error on the next valid frame.

Table 15. TEST MODE REGISTER

	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P	
	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	?	SI
R7	ECHO			INPUT DATA ECHO												?	SO
	PARITY ERR			0	1	0	1	0	1	0	1	0	1	0	1	0	SO
	FRAME ERR			0	1	0	1	0	1	0	1	0	1	0	0	1	SO

Gate Driver Control and Enable

Each GAT_X output may be turned on by either its respective parallel IN_X input or the Gate & Mode Select register bits R0.G[5:0] via SPI communication. The device's RSTB reset and ENB enable inputs can be used to implement global control functions, such as system reset, over-voltage or input override by a watchdog controller.

The RSTB input has an internal pull-down resistor and the ENB input has an internal pull-up resistor. Each parallel input has an internal pull-down resistor. Parallel input is recommended when low frequency (≤ 10 kHz) PWM operation of the outputs is desired. Unused parallel inputs should be connected to GND.

When RSTB is brought low, all GAT_X outputs, the timer clock, the SPI, and the FLTB flag are disabled. All internal registers are initialized to their default states, status data is cleared, and the SPI and FLTB are enabled when RSTB goes high.

ENB disables all GAT_X outputs and diagnostics, and resets the auto-retry timer when brought high. The SPI is enabled, fault data is not cleared and registers remain as programmed. Faulted outputs are re-enabled when ENB goes low.

The IN_X input state and the G_X register bit data are logically combined with the internal (active low) power-on reset signal (POR), the RSTB and ENB input states, and the shorted load state (internal $SHRT_X$) to control the corresponding GAT_X output such that:

$$GAT_X = POR \cdot RSTB \cdot ENB \cdot SHRT_X \cdot (IN_x + G_X) \quad \text{(eq. 1)}$$

The GAT_X state truth table is given in Table 16.

Table 16. GATE DRIVER TRUTH TABLE

POR	RSTB	ENB	$SHRT_X$	IN_X	G_X	GAT_X
0	X	X	X	X	X	L
1	0	X	X	X	X	L
1	1	1	X	X	X	L
1	1	0	1	0	0	L
1	1	0	1	1	X	H
1	1	0	1	X	1	H
1	1	0	0	X	X	→L
1	1	0→1	X	X	G_X	→L
1	1	1→0	→1	0	G_X	→G_X
1	1→0	X	X	X	→0	→L

Gate Drivers

The non-inverting GAT_X drivers are symmetrical resistive switches (350 Ω typ.) to the VCC2 and VSS voltages. While the outputs are designed to provide symmetrical gate drive to an external MOSFET, load current switching symmetry is dependent on the characteristics of the external MOSFET and its load. Figure 12 shows the gate driver block diagram.

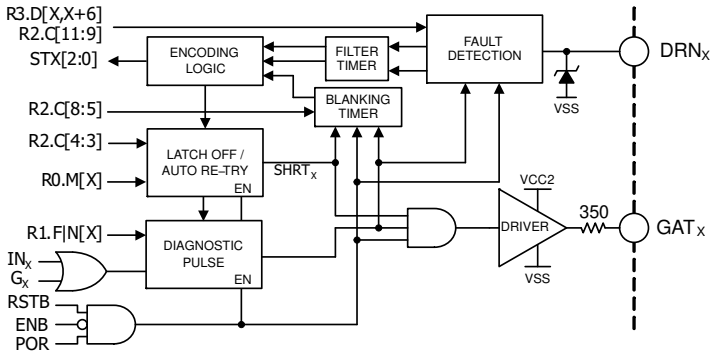


Figure 12. Gate Driver Channel

Blanking and Filter Timers

Blanking timers are used to allow drain feedback to stabilize after a channel is commanded to change states. Filter timers are used to suppress glitches while a channel is in a stable state.

A turn-on blanking timer is started when a channel is commanded on. Drain feedback is sampled after $t_{BL(ON)}$. A turn-off blanking timer is started when a channel is commanded off. Drain feedback is sampled after $t_{BL(OFF)}$.

A filter timer is started when a channel is in a stable state and a fault detection threshold associated with that state has been crossed. Drain feedback is sampled after $t_{FF(ON|OFF)}$. A filter timer may also be started while a blanking timer is active, so the blanking interval could be extended by the filter time.

Each channel has independent blanking and filter timers. The parameters for the $t_{FF(ON|OFF)}$ filter timer are the same for all channels. The turn-on/off blanking time for each channel can be selected via the Diagnostic Config 1 register bits R2.C[8:5] (Tables 6 and 8).

If a blanking timer is currently running when the register is changed, the new value is accepted but will not take effect until the next activation of the timer.

Blanking timers for all channels are started when both RSTB goes high and ENB goes low, when RSTB goes high while ENB is low, when ENB goes low while RSTB is high, or by POR.

Fault Diagnostics and Behavior

Each channel has independent fault diagnostics and employs blanking and filter timers to suppress false faults. An external MOSFET is monitored for fault conditions by connecting its drain to a channel's DRN_X feedback input through an optional external series resistor.

Shorted load (or short to V_{LOAD}) faults can be detected when a driver is on. Open load or short to GND faults can be detected when a driver is off.

On-state faults will initiate MOSFET protection behavior, set the FLTB flag and the respective channel's status bits in

the device's status registers. Off-state faults will simply set the FLTB flag and the channel's status bits.

Status information is retrieved by SPI read of registers R4 and R5 (Table 11). Status information for each channel is 3-bit priority encoded (Table 12). Shorted load fault has priority over open load and short to GND. Short to GND has priority over open load. Priority ensures that the most severe fault data is available at the next SPI read.

Status is latched for the currently higher priority fault and is not demoted if a fault of lower priority occurs. The status registers are reset to "Diagnostic Not Complete" after reading the registers, or by asserting a reset via RSTB. Status registers are not affected by ENB.

When either RSTB is low or ENB is high, diagnostics are disabled. When RSTB is high and ENB is low, open load diagnostics are enabled according to the state of the Diagnostic Config 2 register bits R3**.**D[5:0] (Table 10).

Diagnostic Pulse Mode

The NCV7518 has functionality to perform either on-state or off-state diagnostic pulses (Table 5). The function is provided for applications having loads normally in a continuous on or off state. The diagnostic pulse function is available for both latch-off and auto-retry modes. The pulse executes for the selected channel(s) on low-high transition on CSB.

Diagnostic pulses have priority and are not dependant on the input (IN_X, G_X) or the output (GAT_X) states. The pulse does not execute if: ENB =1 (device is disabled); both an ON and OFF pulse is simultaneously requested for the same channel; an ON or OFF pulse is requested and a SCB (shorted load) diagnostic code is present for the selected channels; an ON or OFF pulse is requested while a pulse is currently executing in the selected channels (i.e. a blanking timer is active); the selected channels are currently under auto-retry control (i.e. refresh timer is active).

When $R1.F_X = 1$, the diagnostic OFF pulse command is executed. The open load diagnostic is turned on if disabled (see Diagnostic Config 2 – R3), the output changes state for the programmed $t_{BL(OFF)}$ blanking period, and the diagnostic status is latched if of higher priority than the previous status. ICHG current is turned on if enabled via R3. The output assumes the currently commanded state at the end of the pulse.

When $R1.N_X = 1$, the diagnostic ON pulse command is executed. The output changes state for the programmed $t_{BL(ON)}$ blanking period, and the diagnostic status is latched if of higher priority than the previous status. The output assumes the currently commanded state at the end of the pulse. A flowchart for the diagnostic pulse is given in Figure 16.

Shorted Load Detection

An external reference voltage applied to the FLTREF input serves as a common reference for all channels (Figures 1 and 2). The FLTREF voltage should be within the range of 0.35 to 2.75 V and can be derived via a voltage divider between V_{CC1} and GND.

Shorted load detection thresholds can be programmed via SPI in eight increments that are ratiometric to the applied FLTREF voltage. Separate thresholds can be selected for each channel via the Diagnostic Config 1 register bits R2**.**C[11:9] (Tables 6 and 9).

A shorted load fault is detected when a channel's DRN_X feedback is greater than its selected fault reference after either the turn-on blanking or the filter has timed out.

Shorted Load Fault Disable and Recovery

Shorted load fault disable mode for each channel is individually SPI programmable via the device's Gate & Mode select register bits R0**.**M[5:0] (Table 4).

When latch-off mode (default) is selected, the corresponding GAT_X output is latched off upon detection of a fault. Recovery from latch-off is performed for all channels by disabling then re-enabling the device via the ENB input. Recovery for selected channels is performed by reading the status registers (R4, R5) for the faulted channels then executing a diagnostic ON or OFF pulse for the desired channels.

When auto-retry mode is selected the corresponding GAT_X output is turned off upon detection of a fault for the duration of the fault retry time (t_{FR}). When auto-retry is selected, input changes for turn-on blanking time are ignored while the retry timer is active. Once active, the timer will run to completion of the programmed time. The output will follow the input at the end of the retry interval. The timer is reset when ENB = 1 or when the mode is changed to latch-off.

The output is automatically turned back on (if still commanded on) when the retry time ends. The channel's DRN_X feedback is re-sampled after the turn-on blanking time. The output will automatically be turned off if a fault is again detected. This behavior will continue for as long as the channel is commanded on and the fault persists.

In either mode, a fault may exist at turn-on or may occur some time afterward. To be detected, the fault must exist longer than either $t_{BL(ON)}$ at turn-on or longer than $t_{FF(ON)}$ some time after turn-on. The length of time that a MOSFET stays on during a shorted load fault is thus limited to either $t_{BL(ON)}$ or $t_{FF(ON)}$.

Recovery Retry Time

A global retry timer is used for auto-retry timing. The first faulted channel triggers the timer and the full retry time is guaranteed for that channel. An additional faulted channel may initially retry immediately after its turn-on blanking time, but subsequent retries will have the full retry time.

If all channels become faulted, they will become synchronized to the global retry timer.

Open Load and Short to GND Detection

A window comparator with references and bias currents proportional to V_{LOAD} is used to detect open load or short to GND faults when a channel is off. Each channel's DRN_X feedback is compared to the references after either the turn-off blanking or the filter has timed out. Figure 13 shows the DRNX bias and fault detection zones.

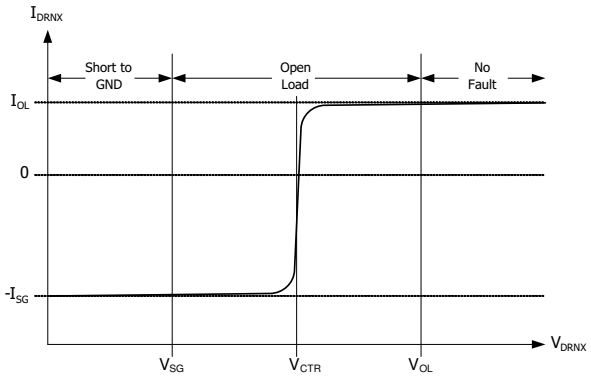


Figure 13. DRN_X Bias and Fault Detection Zones

No fault is detected if the feedback voltage at DRN_X is greater than the V_{OL} open load reference. If the feedback is less than the V_{SG} short to GND reference, a short to GND fault is detected. If the feedback is less than V_{OL} and greater than V_{SG}, an open load fault is detected.

When either RSTB is low or ENB is high, diagnostics are disabled. When RSTB is high and ENB is low, off-state diagnostics are enabled according to the content of the Diagnostic Config 2 register bits R3.D[11:0] (Tables 10 and 17.)

Table 17. OPEN LOAD DIAGNOSTIC CONTROL (CH0 shown)

D6	D0	ICHG CURRENT	OPEN LOAD DIAGNOSTIC	
X	0		OFF	
X	1		ON	(DEF)
0	X	OFF		(DEF)
1	X	ON		

Figure 14 shows the simplified detection circuitry. Bias currents I_{SG} and I_{OL} are applied to a bridge along with bias voltage V_{CTR}. Transient fast charge current I_{CHG} is supplied to help charge any capacitance present at the DRNx node to suppress a false short to GND fault.

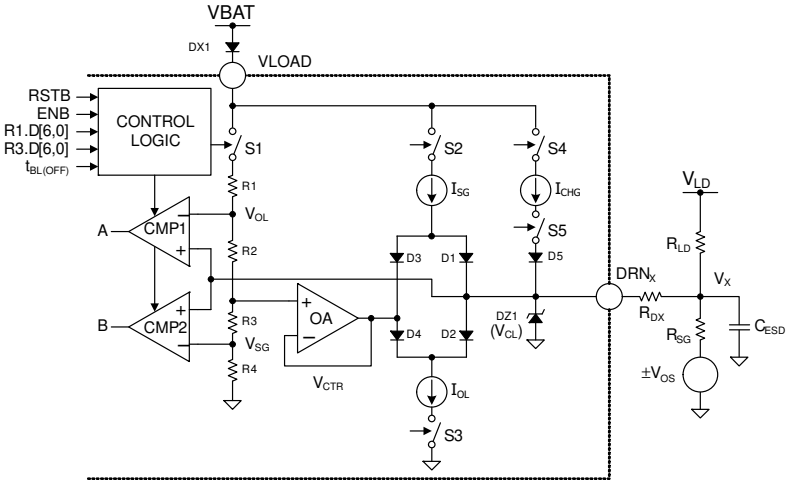


Figure 14. Short to GND/Open-Load Detection

The transient current is started when a channel's turn-off blanking time is started and terminated either when the DRNx voltage reaches V_{CTR} or when the turn-off blanking time $t_{BL(OFF)}$ expires. V_{DRNX} will remain at V_{CTR} if an open load truly exists, otherwise the capacitance can continue to charge via R_{LD}.

When a channel is off and V_{LD} and R_{LD} are present, R_{SG} is absent, and $V_{DRNX} >> V_{CTR}$, bias current I_{OL} is supplied from V_{LD} to ground through resistors R_{LD} and optional R_{DX}, and bridge diode D2. Bias current I_{SG} is supplied from V_{LOAD} to V_{CTR} through D3. No fault is detected if the feedback voltage (V_{LD} minus the total voltage drop caused by I_{OL} and the resistance in the path) is greater than V_{OL}.

When R_{SG} and either V_{LD} or R_{LD} are absent, the bridge will self-bias so that V_{DRNX} will settle to about V_{CTR}. An open load fault can be detected since the feedback is between V_{SG} and V_{OL}.

Short to GND detection can tolerate up to a ±1.0 V offset (V_{OS}) between the NCV7518's GND and the short. When R_{SG} is present and $V_{DRNX} << V_{CTR}$, bias current I_{SG} is supplied from V_{LOAD} to V_{OS} through D1, and the R_{SG} and optional R_{DX} resistances. Bias current I_{OL} is supplied from V_{CTR} to ground through D4.

When V_{LD} and R_{LD} are present, a voltage divider between V_{LD} and V_{OS} is formed by R_{LD} and R_{SG}. A "soft" short to

GND may be detected in this case depending on the ratio of R_{LD} and R_{SG} and the values of R_{DX}, V_{LD}, and V_{OS}.

Optional R_{DX} resistor is used when voltages greater than the 60 V minimum clamp voltage or down to −1 V are expected at the DRNx inputs. Note that the comparators see a voltage drop or rise due to the R_{DX} resistance and the bias currents. This produces an error in the comparison of feedback voltage at the comparator inputs to the actual node voltage V_X.

Several equations for choosing R_{DX} and for predicting open load or short to GND resistances, and a discussion of the dynamic behavior of the short to GND/ open load diagnostic are provided in the "Application Guidelines" section of this data sheet.

Fault Flag (FLTB)

The open-drain active-low fault flag output can be used to provide immediate fault notification to a host controller. Fault detection from all channels is logically ORed to the flag (Figure 15) The FLTB outputs from several devices can be wire-ORed to a common pull-up resistor connected to the controller's 3.3 or 5 V V_{DD} supply.

When RSTB and CSB are high, and ENB is low, the flag is set (low) when any channel detects any fault. The flag is reset (hi-Z) and disabled during POR, when either RSTB or CSB is low, or when ENB is high. See Table 18 for details.

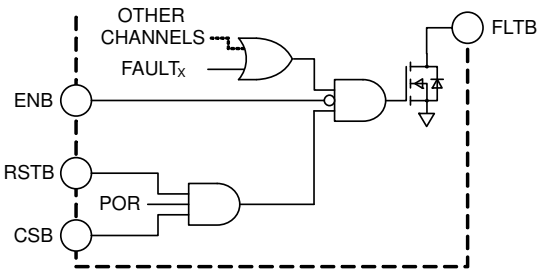


Figure 15. FLTB Flag Logic

The interaction between CSB and FLTB facilitates fault polling. When multiple NCV7518 devices are configured for parallel SPI access with individual CSB addressing, the device reporting a fault can be identified by pulsing each CSB in turn.

Fault Detection and Capture

Each channel of the NCV7518 is capable of detecting shorted load faults when the channel is on, and short to ground or open load faults when the channel is off. Each fault type is priority encoded into 3-bit per channel fault data (Table 12.) Shorted load fault data has priority over open load and short to GND data. Short to GND data has priority over open load data. Priority ensures that the most severe fault data is available at the next SPI read.

A drain feedback input for each channel compares the voltage at the drain of the channel's external MOSFET to several internal reference voltages. Separate detection references are used to distinguish the three fault types. Blanking and filter timers are used respectively to allow for output state transition settling and for glitch suppression.

When enabled and configured, each channel's drain feedback input is continuously compared to references appropriate to the channel's input state to detect faults, but the comparison result is only latched at the end of either a blanking or filter timer event.

Blanking timers for all channels are started when both RSTB goes high and ENB goes low, when RSTB goes high while ENB is low, when ENB goes low while RSTB is high, or by POR. A single channel's blanking timer is triggered when its input state changes. If the comparison of the feedback to a reference indicates an abnormal condition when the blanking time ends, a fault has been detected and the fault data is latched into the channel's status register.

A channel's filter timer is triggered when its drain feedback comparison state changes. If the change indicates an abnormal condition when the filter time ends, a fault has been detected and the fault data is latched into the channel's status register.

Thus, a state change of the inputs (POR, RSTB, ENB, IN_X or G_X) or a state change of an individual channel's feedback (DRN_X) comparison must occur for a timer to be triggered and a detected fault to be captured.

Fault Capture, SPI Communication, and SPI Frame Error Detection

The NCV7518 latches a fault when it is detected, and parity and frame error detection will not allow any register to accept data if an invalid frame occurred.

The fault capture, parity, and frame error detection strategies combine to ensure that intermittent faults can be captured and identified, and that the device cannot be inadvertently re-programmed by a communication error.

When a fault has been detected, status information is latched into a channel's status register if of higher priority than current status, and the FLTB flag is set. The register holds the status data and ignores subsequent lower priority status data for that channel.

Current status information is transferred from the selected status register into the SPI shift register at the start of the SPI frame following the read status request. This ensures that status updates continue during inter-frame latency between the status request and delivery. The FLTB flag is reset when CSB goes low.

The selected status register is cleared when CSB goes high at the end of the SPI frame only if a valid frame has occurred; otherwise the register retains status information until a valid read frame occurs. The FLTB flag will be set if a fault is still present.

Status registers and the FLTB flag can also be cleared by toggling RSTB H→L→H. A full I/O truth table is given in Table 18.

Status Priority Encoding

Shorted load (SCB) faults can be detected when a driver is ON. Open load (OLF) or short to GND (SCG) faults can

be detected when a driver is OFF. Status memory is priority encoded in a 3-bit per driver format (Table 12).

Status memory will be encoded “Diagnostic Not Complete” during a blanking period unless a fault of higher priority has previously been encoded. Status memory will be encoded “Diagnostic Not Complete” (cleared) for the selected status register at the end of a valid SPI frame.

“Diagnostic Complete – No Fault” will be encoded when BOTH on-state AND off-state diagnostics have been completed unless a fault of higher priority has previously been encoded. A diagnostic cycle may start from either an off-state or an on-state.

When a diagnostic cycle starts from an off-state and no fault is detected, “No SCG/OLF Fault” will be encoded unless a fault of higher priority has previously been encoded. Otherwise, “OLF” or “SCG” will be encoded unless a fault of higher priority has previously been encoded. If the cycle continues to an on-state and no fault is detected, “Diagnostic Complete – No Fault” will be encoded. Otherwise, “SCB” will be encoded.

When a diagnostic cycle starts from an on-state and no fault is detected, “No SCB Fault” will be encoded unless a fault of higher priority has previously been encoded. Otherwise, “SCB” will be encoded. If the cycle continues to an off-state and no fault is detected, “Diagnostic Complete – No Fault” will be encoded unless a fault of higher priority has previously been encoded. Otherwise, “OLF” or “SCG” will be encoded unless a fault of higher priority has previously been encoded.

Status is latched for the currently higher priority fault and is not demoted if a fault of lower priority occurs. The status registers are reset to “Diagnostic Not Complete” after reading the registers, or by asserting a reset via RSTB. Status registers are not affected by ENB.

A Statechart diagram of the diagnostic status encoding is given in Figure 17 and additional clarification is given in “Appendix A – Diagnostic and Protection Behavior Tutorial”.

VLOAD Undervoltage Detection

Undervoltage detection is used to suppress off-state diagnostics when VLOAD falls below the specified VLDUV operating voltage. This ensures that potentially incorrect diagnostic status is not captured. On-state diagnostics continue to operate normally and status information is updated appropriately for an off-to-on input transition during undervoltage.

Previous status information and FLTB are unchanged when entering or leaving undervoltage. Upon a read of the status registers during undervoltage, the status is changed to “Diagnostic Not Complete” and will remain as such for channels in an off-state during the entire undervoltage interval. Status information and FLTB are updated appropriately if a channel changes from off to on during the interval.

When VLOAD returns to its normal operating range, a channel’s $t_{BL(OFF)}$ blanking timer is started if the channel was in an off state. Status information is updated appropriately after the $t_{BL(OFF)}$ blanking interval, or after the $t_{FF(OFF)}$ filter interval if the filter has been activated.

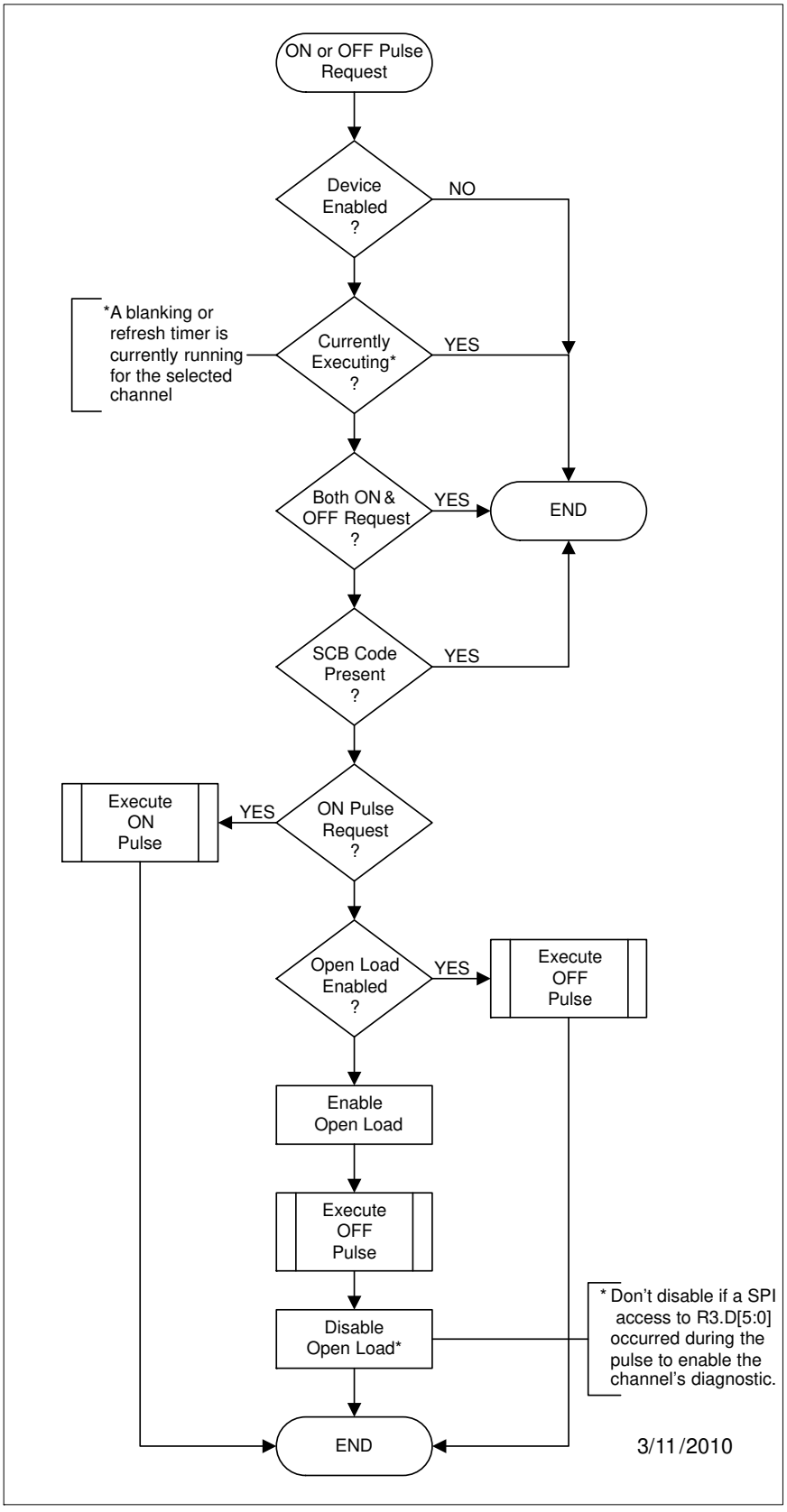


Figure 16. Pulse Mode Diagnostic Flowchart

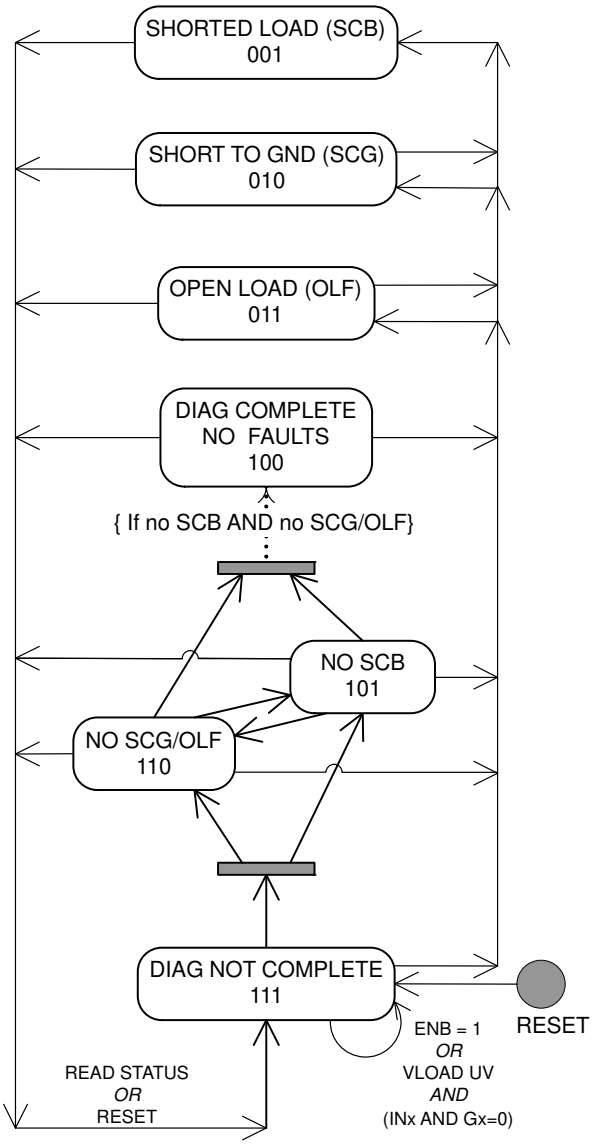


Figure 17. Diagnostic Status Encoding Statechart

Table 18. I/O TRUTH TABLE

Inputs							Outputs*			
POR	**RSTB**	**ENB**	**CSB**	**IN_X**	**G_X**	**DRN_X**	**GAT_X**	**FLTB**	**ST[2:0]**	**COMMENT**
0	X	X	X	X	→0	X	→L	→Z	→111	POR RESET
1	0	X	X	X	X	X	L	Z	111	RSTB
1	1	1	X	X	G_X	X	L	Z	ST[2:0]	ENB
1	1→0	0	X	X	→0	X	→L	→Z	→111	RSTB RESET
1	1	0→1	X	X	G_X	X	→L	→Z	ST[2:0]	ENB DISABLE
1	1	0	X	0	0	> V_{OL}	L	Z	ST[2:0]	FLTB RESET
1	1	0	1	0	0	V_{SG} < V < V_{OL}	L	L	→ 011	FLTB SET – OLF
1	1	0	1→0	0	0	V_{SG} < V < V_{OL}	L	L→Z	011	FLTB RESET
1	1	0	0→1	0	0	V_{SG} < V < V_{OL}	L	Z→L	011	FLTB SET
1	1	0	1	0	0	< V_{SG}	L	L	→ 010	FLTB SET – SCG
1	1	0	1→0	0	0	< V_{SG}	L	L→Z	010	FLTB RESET
1	1	0	0→1	0	0	< V_{SG}	L	Z→L	010	FLTB SET
1	1	0	X	1	X	< V_{FLTREF}	H	Z	ST[2:0]	FLTB RESET
1	1	0	1	1	X	> V_{FLTREF}	L	L	→ 001	FLTB SET – SCB
1	1	0	1→0	1	X	> V_{FLTREF}	L	L→Z	001	FLTB RESET
1	1	0	0→1	1	X	> V_{FLTREF}	L	Z→L	001	FLTB SET
1	1	0	1	X	1	< V_{FLTREF}	H	Z	ST[2:0]	FLTB RESET
1	1	0	1	X	1	> V_{FLTREF}	L	L	→ 001	FLTB SET – SCB
1	1	0	1→0	X	1	> V_{FLTREF}	L	L→Z	001	FLTB RESET
1	1	0	0→1	X	1	> V_{FLTREF}	L	Z→L	001	FLTB SET

*Output states after blanking and filter timers end and when channel is set to latch-off mode.