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NCV78763

Power Ballast and Dual LED Driver for Automotive Front Lighting 2nd Generation

The NCV78763 is a single−chip and high efficient smart Power ballast and Dual LED DRIVER designed for automotive front lighting applications like high beam, low beam, daytime running light (DRL), turn indicator, fog light, static cornering and so on.

The NCV78763 is a best fit for high current LEDs and provides a complete solution to drive two strings up to 60 V, by means of two internal independent buck switch channel outputs, with a minimum of external components. For each individual LED channel, the output current and voltage can be customized according to the application requirements. An on−chip diagnostic feature for automotive front lighting is provided, easing the safety monitoring from the microcontroller. The device integrates a current−mode voltage booster controller, realizing a unique input current filter with a limited BOM.

When more than two LED channels are required on one module, then two, three or more NCV78763 devices can be combined, with the possibility for the booster circuits to operate in multiphase−mode. This helps to further optimize the filtering effect of the booster circuit and allows a cost effective dimensioning for mid to high power LED systems.

Due to the SPI programmability, one single hardware setup can support multiple system configurations for a flexible platform solution approach.

Features

- Single Chip Boost−Buck Solution
- Two LED Strings up to 60 V
- High Current Capability up to 1.6 A DC per Output
- High Overall System Efficiency
- Minimum of External Components
- Active Input Filter with Low Current Ripple from Battery
- Integrated Switched Mode Buck Current Regulator
- Integrated Boost Current−mode Controller
- Programmable Input Current Limitation
- Average Current Regulation Through the LEDs
- High Operating Frequencies to Reduce Inductor Sizes
- Integrated PWM Dimming with Wide Frequency Range
- Low EMC Emission for LED switching and dimming
- SPI Interface for Dynamic Control of System Parameters
- These are Pb−Free Devices

Typical Applications

- Front Lighting High Beam and Low Beam
- Day time Running Light (DRL)
- Position or Park light
- Turn Indicator
- Fog Light and Static Cornering

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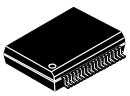
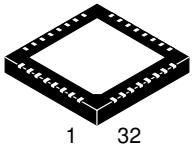
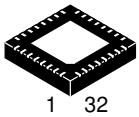


SSOP36 EP
CASE 940AB

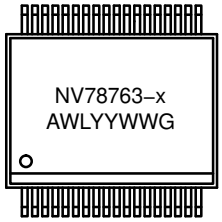


QFN32 7x7
CASE 485J

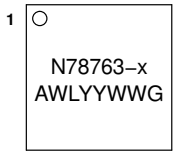


QFN32
CASE 488AM

MARKING DIAGRAMS



SSOP36



QFN32

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 46 of this data sheet.

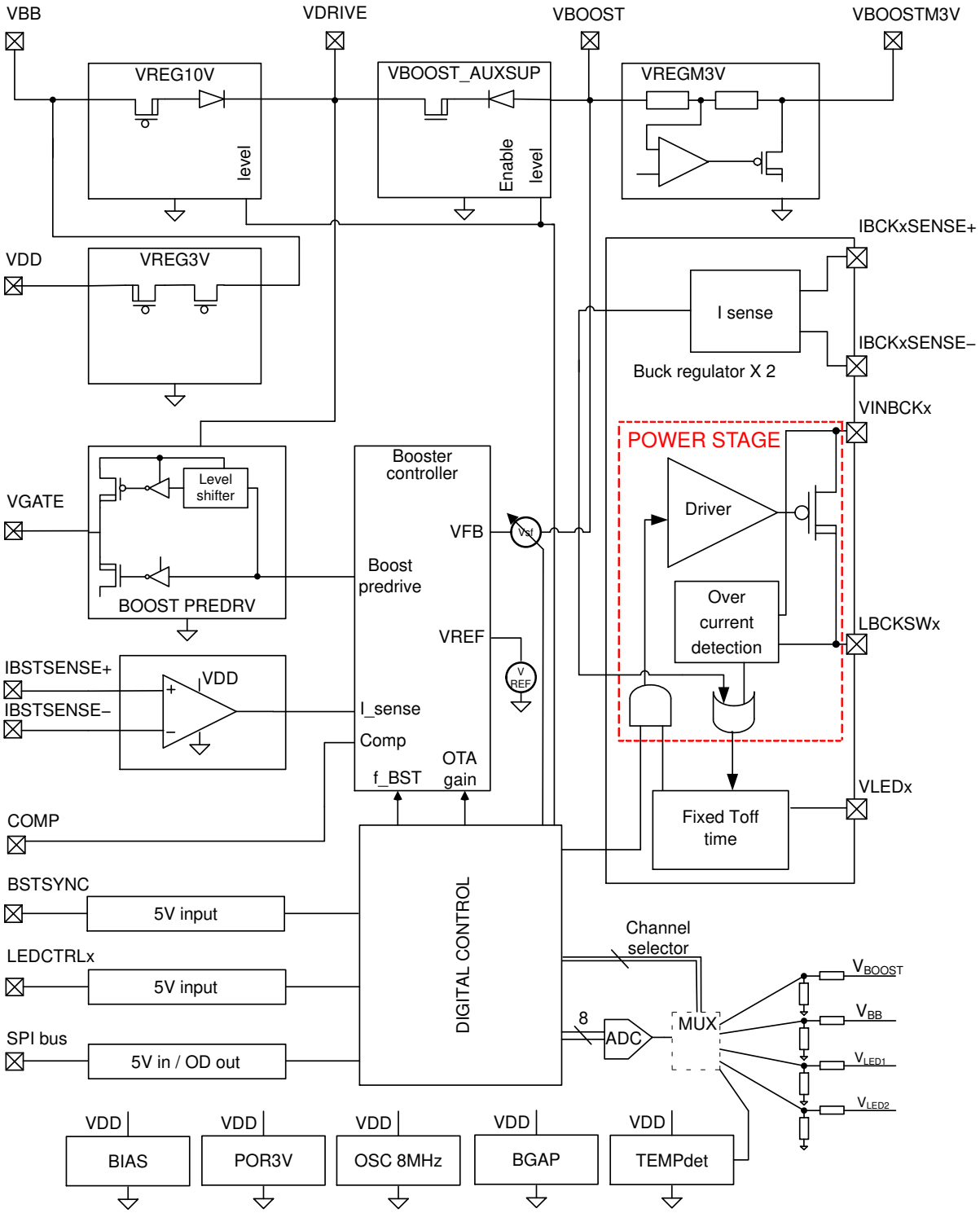


Figure 1. Internal Block Diagram

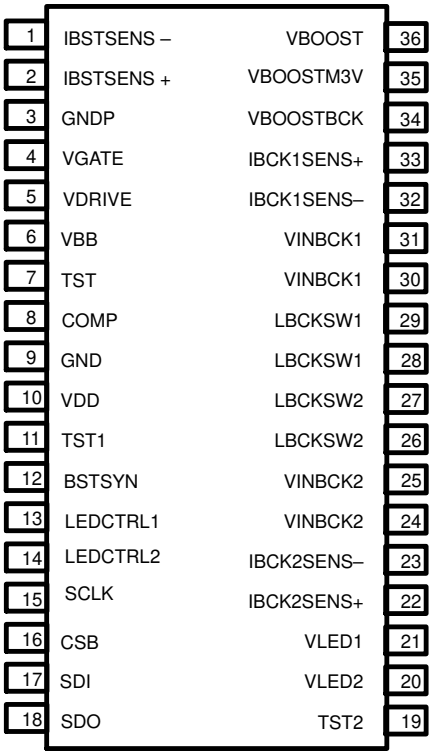


Figure 2. Pin Connections (SSOP36 EP)

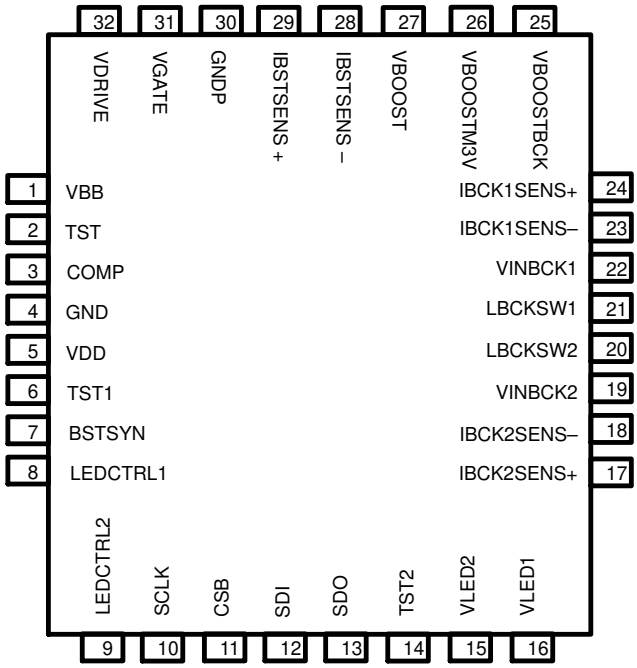


Figure 3. Pin Connections (QFN32)

Table 1. PIN DESCRIPTION

Pin No. SSOP36−EP	Pin No. QFN32	Pin Name	Function	I/O Type
1	28	IBSTSENSE−	Battery current negative feedback input	LV in/out
2	29	IBSTSENSE+	Battery current positive feedback input	LV in/out
3	30	GNDP	Power ground	Ground
4	31	VGATE	Booster MOSFET gate pre−driver	MV out
5	32	VDRIVE	10V supply	MV supply
6	1	VBB	Battery supply	HV supply
7	2	TST	Internal function. To be tied to GND.	LV in/out
8	3	COMP	Compensation for the Boost regulator	LV in/out
9	4	GND	Ground	Ground
10	5	VDD	3V logic supply	LV supply
11	6	TST1	Internal function. To be tied to GND.	LV in/out
12	7	BSTSYN	External clock for the boost regulator	MV in
13	8	LEDCTRL1	LED string 1 enable	MV in
14	9	LEDCTRL2	LED string 2 enable	MV in
15	10	SCLK	SPI clock	MV in
16	11	CSB	SPI chip select (chip select bar)	MV in
17	12	SDI	SPI data input	MV in
18	13	SDO	SPI data output	MV open−drain
19	14	TST2	Internal function. To be tied to GND.	LV in/out
20	15	VLED2	LED string 2 forward voltage input	HV in
21	16	VLED1	LED string 1 forward voltage input	HV in
22	17	IBCK2SENSE+	Buck 2 positive sense input	HV in
23	18	IBCK2SENSE−	Buck 2 negative sense input	HV in
24	19	VINBCK2	Buck 2 high voltage supply	HV in
25	X	VINBCK2	Buck 2 high voltage supply	HV in
26	20	LBCKSW2	Buck 2 switch output	HV out
27	X	LBCKSW2	Buck 2 switch output	HV out
28	21	LBCKSW1	Buck 1 switch output	HV out
29	X	LBCKSW1	Buck 1 switch output	HV out
30	22	VINBCK1	Buck 1 high voltage supply	HV in
31	X	VINBCK1	Buck 1 high voltage supply	HV in
32	23	IBCK1SENSE−	Buck 1 negative sense input	HV in
33	24	IBCK1SENSE+	Buck 1 positive sense input	HV in
34	25	VBOOSTBCK	High voltage for the BUCK switches	HV supply
35	26	VBOOSTM3V	VBOOST−3V regulator output	HV out (supply)
36	27	VBOOST	Boost voltage feedback input	HV in

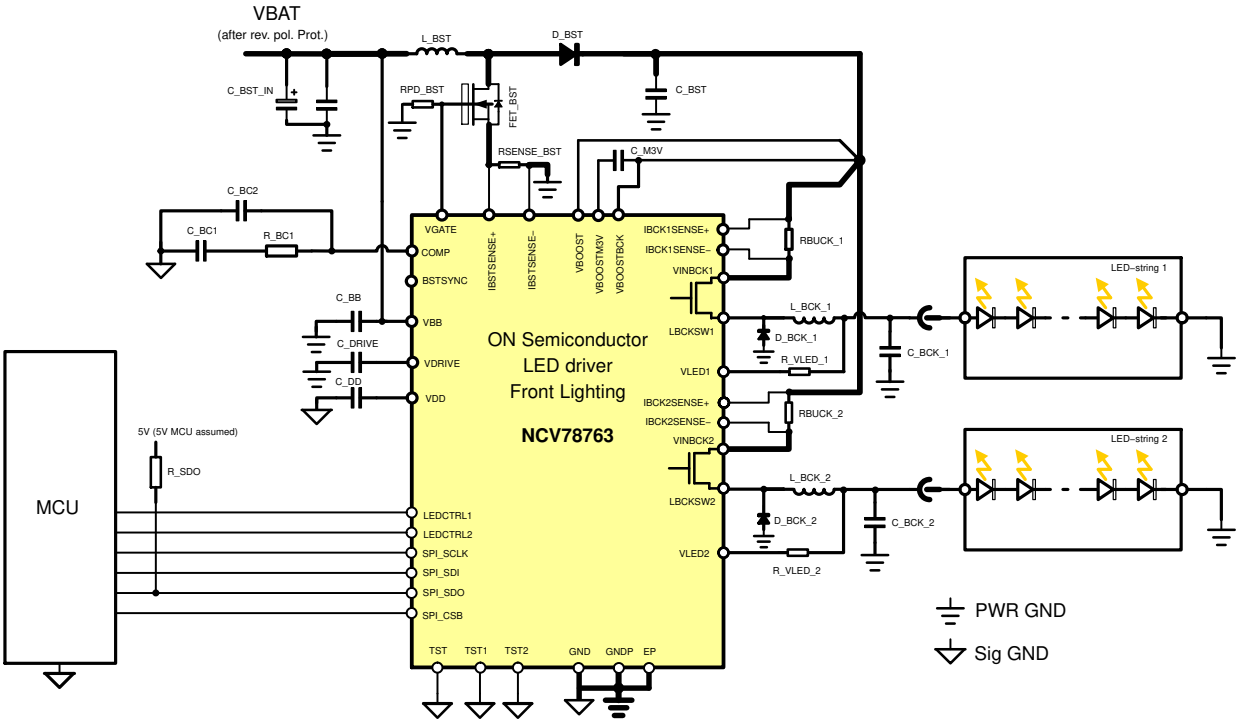


Figure 4. NCV78763 Application Diagram

Note A: as reported in the application diagram, the device pins TST, TST2 & TST1 must be connected to the signal ground GND.
Note B: external capacitors or RC may be added to these SPI lines for stable communication in case of application noise. The selection of these components must be done so that the resulting waveforms are respecting the limits reported in Table 19.
Note C: recommended values for the external MOSFET pull down resistor RPD_BST range from 10 kΩ to 33 kΩ.
Note D: the minimum value for the LED feedback resistors R_VLED_1 and R_VLED_2 is 1 kΩ.

Table 2. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Battery Supply voltage (Note 1)	V_{BB}	−0.3	60	V
LED supply voltage (Note 2)	V_{BOOST}	−0.3	68	V
Logic Supply voltage (Note 3)	V_{DD}	−0.3	3.6	V
MOSFET Gate driver supply voltage (Note 4)	V_{DRIVE}	−0.3	12	V
Input current sense voltage pins	IBSTSENSE+, IBSTSENSE−	−1.0	12	V
Medium voltage IO pins (Note 5)	IOMV	−0.3	7.0	V
Relative voltage IO pins (Note 6)	ΔV_IO	VBOOSTM3V	VBOOSTBCK	V
Buck switch low side (Note 7)	LBCKSW1, LBCKSW2	−2.0	VBOOSTBCK	V
Current into or out of the VLED pin	$I_{VLEDpin}$	−30	30	mA
Series resistor on the VLED pin	R_{VLEDx}	1		kΩ
Storage Temperature (Note 8)	T_{strg}	−50	150	°C
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 9)	T_{SLD}		260	°C
Electrostatic discharge on component level (Note 10)	V_{ESD}	−2	+2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Absolute maximum rating for pin VBB.
2. Absolute maximum rating for pins: VBOOST, VBOOSTM3V, IBCK1SENSE+, IBCK1SENSE−, VINBCK1, VLED1, IBCK2SENSE+, IBCK2SENSE−, VINBCK2, VLED2.
3. Absolute maximum rating for pins: VDD, TEST1, TEST2, COMP.
4. Absolute maximum rating for pins: VDRIVE, VGATE.
5. Absolute maximum rating for pins: SCLK, CSB, SDI, SDO, LEDCTRL1, LEDCTRL2, BSTSYNC. The device tolerates 5 V coming from the external logics (MCU) when in off state.
6. Relative maximum rating for pins: VINBCK1, VINBCK2, IBCK1SENSE+, IBCK2SENSE+, IBCK1SENSE−, IBCK2SENSE−.
7. Requirement: V(VINBCKx − LBCKSWx) < 70 V.
8. For limited time up to 100 hours, otherwise the max. storage temperature < 85°C.
9. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
10. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
    ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
    Latch−up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78

Table 3. RECOMMENDED OPERATING RANGES

The recommended operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the device outside the operating ranges described in this section is not warranted. Operating outside the recommended operating ranges for extended periods of time may affect device reliability. A mission profile (Note 11) is a substantial part of the operation conditions; hence the Customer must contact ON Semiconductor in order to mutually agree in writing on the allowed missions profile(s) in the application.

Characteristic	Symbol	Min	Max	Unit
Battery Supply voltage	V_{BB}	4	40	V
Gate driver supply current (Note 12)	I_{DRIVE}		40	mA
Functional operating junction temperature (Note 13)	T_{JF}	−45	155	°C
Parametric operating junction temperature range	T_{JP}	−40	150	°C
Buck switch output current peak	$I_{LBUCKpeak}$		1.9	A

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

11. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating junction temperature range. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.
12. $I_{DRIVE} = Q_{Tgate\ x}\ F_{BOOST}$ (external MOSFET total gate charge multiplied by booster driving frequency).
13. The circuit functionality is not guaranteed outside the functional operating junction temperature range. The maximum functional operating range can be limited by thermal shutdown "Tsd" (ADC_Tsd, see Table 10). Also please note that the device is verified on bench for operation up to 170°C but that the production test guarantees 155°C only.

Table 4. THERMAL RESISTANCE

Characteristic	Package	Symbol	Value	Unit
Thermal resistance package to Exposed Pad (Note 14)	SSOP36−EP	θJcbot	3.5	°C/W
Thermal resistance package to Exposed Pad (Note 14)	QFN32 7x7	θJcbot	3.4	°C/W
Thermal resistance package to Exposed Pad (Note 14)	QFN32 5x5	θJcbot	3.4	°C/W

14. Includes also typical solder thickness under the Exposed Pad (EP).

ELECTRICAL CHARACTERISTICS NOTE: Unless differently specified, all device Min and Max parameters boundaries are given for the full supply operating ranges and junction temperature (T_{JP}) range (−40°C; +150°C).

Table 5. VBB: BATTERY SUPPLY INPUT

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Nominal Operating Supply Range	V_{BB}		5		40	V
Device Current Consumption	I_{BB_0}	buck regulators off, gate drive off, outputs unloaded			8	mA

Table 6. VDRIVE: SUPPLY FOR BOOSTER MOSFET GATE DRIVE CIRCUIT

Characteristic	Symbol	Conditions		Min	Typ	Max	Unit
VDRIVE reg. voltage from VBB (Note 15)	$V_{DRV\_BB\_15}$	$V_{BB} - V_{DRIVE} > 1.65$ V @I_{DRIVE} = 25 mA	VDRIVE_ SETPOINT[3:0] = 1111	9.7	10.1	10.7	V
	$V_{DRV\_BB\_00}$	$V_{BB} - V_{DRIVE} > 1.65$ V @I_{DRIVE} = 25 mA	VDRIVE_ SETPOINT[3:0] = 0000	4.8	5	5.3	V
VDRIVE from VBB increase per code (Note 15)	ΔV_{DRV_BB}	Linear increase, 4Bits			0.34		V
VDRIVE reg. voltage from VBOOST (Note 15)	$V_{DRV\_BST\_15}$	$V_{BOOST} - V_{DRIVE} > 3$ V @I_{DRIVE} = 40 mA	VDRIVE_SETPOINT[3:0] = 1111	9.5	10.1	10.7	V
	$V_{DRV\_BST\_00}$	$V_{BOOST} - V_{DRIVE} > 3$ V @I_{DRIVE} = 40 mA	VDRIVE_SETPOINT[3:0] = 0000	4.7	5	5.3	V
VDRIVE from VBOOST increase per code (Note 15)	Δ_{VDRV_BST}	Linear increase, 4 Bits			0.34		V
VDRIVE Output current limitation from VBB input	$V_{DRV\_BB\_IL}$			40		400	mA
VDRIVE Output current limitation from VBOOST input	$V_{DRV\_BB\_IL}$			40		200	mA
VDRIVE decoupling capacitor	C_{VDRIVE}				470		nF
VDRIVE decoupling capacitor ESR	C_{VDRIVE_ESR}					100	mΩ

15. The VDRIVE voltage setpoint is in the same range if the current is either provided by VBB or VBOOST pin. The voltage headroom between VBB and VDRIVE or VDRIVE and VBOOST needs to be sufficient. For what concerns VDRIVE from VBB, in case of 25 mA current, the worst case headroom is 1.65V. The VBOOST_AUX regulator can be enabled by SPI (bit VDRIVE_BST_EN[0]).

Table 7. VDD: 3V LOW VOLTAGE ANALOG AND DIGITAL SUPPLY

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VBB to VDD switch disconnection	V_{BB_LOW}		3.65		3.9	V
VDD regulator output voltage	V_{DD}	V_{BB} > 4 V	3.15		3.4	V
DC total current consumption including output	V_{DD_IOUT}	V_{BB} > 4 V			15	mA
DC current limitation	V_{DD_ILIM}	V_{BB} > 4 V	15		240	mA
VDD external decoupling cap.	C_{VDD}		0.3	0.47	2.2	μF
VDD ext. decoupling cap. ESR	C_{VDD_ESR}				200	mΩ
POR Toggle level on VDD rising	POR_{3V_H}		2.7		3.05	V
POR Toggle level on VDD falling	POR_{3V_L}		2.45		2.8	V
POR Hysteresis	POR_{3V_HYST}			0.2		V

Table 8. VBOOSTM3: HIGH SIDE MOSFETS AUXILIARY SUPPLY

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VBSTM3 regulator output voltage	V_{BSTM3}		–3.6	–3.3	–3.0	V
VBSTM3 DC output current consumption	V_{BSTM3_IOUT}			5		mA
VBSTM3 Output current limitation	V_{BSTM3_ILIM}				200	mA
VBSTM3 external decoupling capacitor	C_{VBSTM3}		0.3	0.47	2.2	μF
VBSTM3 external decoupling cap. ESR	C_{VBSTM3_ESR}				200	mΩ

Table 9. OSC8M: SYSTEM OSCILLATOR CLOCK

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
System oscillator frequency	FOSC8M	After device factory trimming	7.1	8.0	8.9	MHz

Table 10. ADC FOR MEASURING VBOOST, VBB, VLED1, VLED2, VTEMP

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
ADC Resolution	ADC_{RES}			8		Bits
Integral Nonlinearity (INL)	ADC_{INL}		–1.5		+1.5	LSB
Differential Nonlinearity (DNL)	ADC_{DNL}		–2.0		+2.0	LSB
Full path gain error for measurements via VBB, VLEDx, VBOOST	$ADC_{GAINERR}$		–3.25		3.25	%
Offset at output of ADC	ADC_{OFFSET}		–2		2	LSB
Time for 1 SAR conversion	ADC_{CONV_TIME}			8		μs

Table 10. ADC FOR MEASURING VBOOST, VBB, VLED1, VLED2, VTEMP (continued)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
ADC full scale for VBB measurement	ADC_{FS_VBB}			39.7		V
ADC full scale for VLED	ADC_{FS_VLED}			69.5		V
ADC full scale for Vboost	ADC_{FS_VBST}			69.5		V
ADC internal temperature measurement for thermal shutdown	ADC_{TSD}		163	169	175	°C
VLED input impedance	$VLED_{R\_IN}$		255		710	kΩ

Table 11. BOOSTER CONTROLLER – VOLTAGE REGULATION PARAMETERS

Characteristic	Symbol	Conditions	SPI Setting	Min	Typ	Max	Unit
Booster overvoltage shutdown (Note 16)	BST_OV_07	ΔV to the reg. level, DC level	[BOOST_OV_SD = 111]	5.3	5.8	6.3	V
	BST_OV_06	ΔV to the reg. level, DC level	[BOOST_OV_SD = 110]	4.3	4.85	5.3	V
	BST_OV_05	ΔV to the reg. level, DC level	[BOOST_OV_SD = 101]	3.4	3.9	4.3	V
	BST_OV_04	ΔV to the reg. level, DC level	[BOOST_OV_SD = 100]	2.4	2.9	3.3	V
	BST_OV_03	ΔV to the reg. level, DC level	[BOOST_OV_SD = 011]	1.9	2.4	2.8	V
	BST_OV_02	ΔV to the reg. level, DC level	[BOOST_OV_SD = 010]	1.5	2	2.3	V
	BST_OV_01	ΔV to the reg. level, DC level	[BOOST_OV_SD = 001]	1.2	1.5	1.8	V
	BST_OV_00	ΔV to the reg. level, DC level	[BOOST_OV_SD = 000]	0.6	1	1.3	V
Booster overvoltage shutdown increase per code	ΔBST_OV	Linear increase, 2 bits, DC level			0.5/1	0.6/1.2	V
Booster overvoltage re−activation	BST_RA_3	ΔV to the VBOOST reg. overvoltage protection, DC level	[BOOST_OV_REACT = 11]	−1.8	−1.4	−1	V
Booster overvoltage re−activation	BST_RA_0	ΔV to the VBOOST reg. overvoltage protection, DC level	[BOOST_OV_REACT = 00]		0		V
Booster overvoltage re−activation decrease per code	ΔBST_RA	Linear decrease, 2 bits, DC level		−0.6	−0.5		V
Booster regulation setpoint voltage	BST_REG_127	DC level	[BOOST_VSETPOINT = 1111111]	62.8	64.1	66	V
	BST_REG_001	DC level	[BOOST_VSETPOINT = 0000001]	14.4	15	15.6	V
	BST_REG_000	DC level	[BOOST_VSETPOINT = 0000000]	10.5	11	11.5	V
Booster regulation setpoint increase step per code	ΔBST_REG	Linear increase, 7 bits			0.39	0.55	V

Table 11. BOOSTER CONTROLLER – VOLTAGE REGULATION PARAMETERS

Characteristic	Symbol	Conditions	SPI Setting	Min	Typ	Max	Unit
Booster Error Amplifier (EA) Trans−conductance Gain G_m	$EA_{\_Gm\_3}$	Seen from VBOOST pin input, DC value	[BOOST_OTA_GAIN = 11]	63	90	117	μS
	$EA_{\_Gm\_2}$	Seen from VBOOST pin input, DC value	[BOOST_OTA_GAIN = 10]	42	60	78	μS
	$EA_{\_Gm\_1}$	Seen from VBOOST pin input, DC value	[BOOST_OTA_GAIN = 01]	21	30	39	μS
	$EA_{\_Gm\_0}$	Seen from VBOOST pin input, High impedance tri−state	[BOOST_OTA_GAIN = 00]		0		μS
EA max output current (positive/source)	$EA_{\_Iout\_pos\_max\_03}$	$EA_{\_Gm\_03}$ is set	[BOOST_OTA_GAIN = 11]	150	180		μA
	$EA_{\_Iout\_pos\_max\_02}$	$EA_{\_Gm\_02}$ is set	[BOOST_OTA_GAIN = 10]	100	120		μA
	$EA_{\_Iout\_pos\_max\_01}$	$EA_{\_Gm\_01}$ is set	[BOOST_OTA_GAIN = 01]	50	60		μA
EA max output current (negative/sink)	$EA_{\_Iout\_neg\_max\_03}$	$EA_{\_Gm\_03}$ is set	[BOOST_OTA_GAIN = 11]		−180	−150	μA
	$EA_{\_Iout\_neg\_max\_02}$	$EA_{\_Gm\_02}$ is set	[BOOST_OTA_GAIN = 10]		−120	−100	μA
	$EA_{\_Iout\_neg\_max\_01}$	$EA_{\_Gm\_01}$ is set	[BOOST_OTA_GAIN = 01]		−60	−50	μA
EA max output leakage current in tri−state	$EA_{\_Iout\_leak}$	$EA_{\_Gm\_00}$ is set (EA disabled, high impedance tri−state)	[BOOST_OTA_GAIN = 00]	−1		1	μA
EA equivalent output resistance	$EA_{\_ROUT}$			0.7		2.9	MΩ
EA max output voltage (at VCOMP pin)	$COMP_{\_CLH3}$	(BST_SLPCTRL_3 or BST_SLPCTRL_2) & (BST_VLIMTH_3 or BST_VLIMTH_2)	[BOOST_SLP_CTRL = 1x] & [BOOST_VLIMTH = 1x]	2.1	2.26		V
	$COMP_{\_CLH2}$	BST_SLPCTRL_3 or BST_SLPCTRL_2) & (BST_VLIMTH_1 or BST_VLIMTH_0)	[BOOST_SLP_CTRL = 1x] & [BOOST_VLIMTH = x1]	1.8	1.98		V
	$COMP_{\_CLH1}$	BST_SLPCTRL_1 or BST_SLPCTRL_0) & (BST_VLIMTH_3 or BST_VLIMTH_2)	[BOOST_SLP_CTRL = x1] & [BOOST_VLIMTH = 1x]	1.5	1.64		V
	$COMP_{\_CLH0}$	BST_SLPCTRL_1 or BST_SLPCTRL_0) & (BST_VLIMTH_1 or BST_VLIMTH_0)	[BOOST_SLP_CTRL = x1] & [BOOST_VLIMTH = x1]	1.2	1.35		V
EA min output voltage (at VCOMP pin)	$COMP_{\_CLL}$					0.4	V
Division factor of VCOMP voltage towards the Current comparator input	$COMP_{\_DIV}$				7		
Voltage shift (offset) on VCOMP on Current comparator input	$COMP_{\_VSF}$				0.5		V
Booster skip cycle for low currents (Note 17)	BST_SKCL_3		[BOOST_SKCL = 11]		0.7 or 0.8		V
	BST_SKCL_2		[BOOST_SKCL = 10]		0.625 or 0.7		V
	BST_SKCL_1		[BOOST_SKCL = 01]		0.55 or 0.6		V

Table 11. BOOSTER CONTROLLER – VOLTAGE REGULATION PARAMETERS

Characteristic	Symbol	Conditions	SPI Setting	Min	Typ	Max	Unit
VGATE comparator to start BST_TOFF time	$BST_{VGATE\_THR\_1}$		[VBOOST_VGATE_THR = 1]		1.2		V
	$BST_{VGATE\_THR\_0}$		[VBOOST_VGATE_THR = 0]		0.4		V
Booster PWM frequency (when from internal generation)	BST_{FREQ_31}	FOSC8M / 38	[BOOST_FREQ = 11111]	187	210	234	kHz
	BST_{FREQ_01}	FOSC8M / 8	[BOOST_FREQ = 00001]	890	1000	1110	kHz
	BST_{FREQ_00}	PWM clock disabled	[BOOST_FREQ = 00000]		0		kHz
Booster PWM freq. increase per code	ΔBST_{FREQ}	Nonlinear increase, 5 bits			5–112		kHz
Booster minimum OFF time (Note 18)	$BST_{TOFF\_MIN\_3}$		[VBOOST_TOFFMIN = 11]	100	155	210	ns
	$BST_{TOFF\_MIN\_2}$		[VBOOST_TOFFMIN = 10]	140	195	250	ns
	$BST_{TOFF\_MIN\_1}$		[VBOOST_TOFFMIN = 01]	30	75	120	ns
	$BST_{TOFF\_MIN\_0}$		[VBOOST_TOFFMIN = 00]	70	115	160	ns
Booster minimum ON time (Note 18)	$BST_{TON\_MIN\_3}$		[VBOOST_TONMIN = 11]	235	300	365	ns
	$BST_{TON\_MIN\_2}$		[VBOOST_TONMIN = 10]	200	260	320	ns
	$BST_{TON\_MIN\_1}$		[VBOOST_TONMIN = 01]	150	200	250	ns
	$BST_{TON\_MIN\_0}$		[VBOOST_TONMIN = 00]	100	150	200	ns

16. The following condition must always be respected: BST_REG_XX + BST_OV_X < 68 V.
17. The higher levels indicated in the cells are valid for BST_VLIMTH_2 and BST_VLIMTH_3 selection (BOOST_VLIMTH<1> = 1).
18. Rise and fall time of the VGATE is not included.

Table 12. BOOSTER CONTROLLER – CURRENT REGULATION PARAMETERS

Characteristic	Symbol	Conditions	SPI setting	Min	Typ	Max	Unit
Current comparator for Imax detection	BST_{VLIMTH_3}		[BOOST_VLIMTH = 11]	95	100	105	mV
	BST_{VLIMTH_2}		[BOOST_VLIMTH = 10]	75	80	85	mV
	BST_{VLIMTH_1}		[BOOST_VLIMTH = 01]	57	62.5	67	mV
	BST_{VLIMTH_0}		[BOOST_VLIMTH = 00]	45	50	55	mV
Current comparator for VBOOST regulation, offset voltage	BST_{OFFS}			–5	0	5	mV
Booster slope compensation	$BST_{SLPCTRL\_3}$		[BOOST_SLPCTRL = 11]		20		mV/ μs
	$BST_{SLPCTRL\_2}$		[BOOST_SLPCTRL = 10]		10		mV/ μs
	$BST_{SLPCTRL\_1}$		[BOOST_SLPCTRL = 01]		5		mV/ μs
	$BST_{SLPCTRL\_0}$	(no slope control)	[BOOST_SLPCTRL = 00]		0		mV/ μs
Booster Current Sense voltage common mode range	CMVSENSE			–0.1		1	V

Table 13. BOOSTER CONTROLLER – MOSFET GATE DRIVER

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
High–side switch impedance	RON_{HI}			2.5	4	Ω
Low–side switch impedance	RON_{LO}			2.5	4	Ω

Table 14. BUCK REGULATOR – INTERNAL SWITCHES CHARACTERISTICS

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Buck switch On resistance	$R_{DS(on)}$	At room–temperature, I(VINBCKx) pin = 1.5 A, (VBOOST–VINBCKx) = 0.2 V			0.65	Ω
	$R_{DS(on)\_hot}$	At Tj = 150°C, I(VINBCKx) pin = 1.5 A, (VBOOST–VINBCKx) = 0.2 V			0.9	Ω

Table 14. BUCK REGULATOR – INTERNAL SWITCHES CHARACTERISTICS

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Buck Overcurrent detection	OCD		1.9		3	A
Buck Switching slope (ON phase)	Trise			3		V/ns
Buck Switching slope (OFF phase)	Tfall			2		V/ns

Table 15. BUCK REGULATOR – CURRENT REGULATION PARAMETERS

Characteristic	Symbol	Conditions		Min	Typ	Max	Unit
Buck current sense threshold voltage	VTHR_255		[BUCKx_VTHR = 11111111]		412		mV
Buck current sense threshold voltage	VTHR_000		[BUCKx_VTHR = 00000000]		31.5		mV
Buck current sense threshold voltage increase per code	ΔVTHR	exponential increase, 7.5 bits equivalent, DC level			1.013	1.5	%
Buck threshold voltage temperature stability	$VTHR_{TEMP}$	Without chopper function		–1.5 & –2		+1.5 & +2	% & mV / 100°C
Buck threshold voltage accuracy (Note 21)	$VTHR_{ERR}$	Without chopper function		–3 & –6		+3 & +6	% & mV
Buck TOFFxVLED constant setting for shortest OFF time	$T_{OFF\_VLED\_15}$		[BUCKx_TOFFVLED = 1111]		10		µs V
Buck TOFFxVLED constant setting for longest OFF time	$T_{OFF\_VLED\_00}$		[BUCKx_TOFFVLED = 0000]		50		µs V
Buck OFF time relative error	$BCK_{\_TOFF\_ERR\_REL}$	T_{OFF} xVLED @VLED > 2 V & T_{OFF} > 0.35 µs		–10	0	10	%
Buck OFF time absolute error	$BCK_{\_TOFF\_ERR\_ABS}$	T_{OFF} xVLED @VLED > 2 V & $T_{OFF} \le$ 0.35 µs		–35	0	35	ns
Buck OFF time setting decrease per code	ΔTC	exponential increase, 4 bits, DC level			11.33		%
Detection level for low VLED voltages	$VLED_{\_LMT}$			1.62	1.8	1.98	V
Buck ON too long time detection (OPEN LOAD)	$BCK_{\_TON\_OPEN}$			44.3	50	55.7	µs
Buck minimum ON time mask in regulation (Note 20)	$BCK_{\_TON\_MIN}$			50		250	ns
Buck OFF time for short circuit detected on VLEDx	$BCK_{\_TOFF\_SHORT}$	VLEDx < $VLED_{\_LMT}$		63		90	µs
Delay from BUCK ISENS comparator input to BUCK switch going OFF (Note 21)	$BCK_{\_CMP\_DEL}$	ISENS comparator over–drive ramp > 1 mV/10 ns			70		ns

19. Without use of buck chopper function (for sufficient coil current ripple, see buck section in the datasheet). With the buck chopper function, the offset is reduced to a level lower than ±|3 mV|.
20. The buck ISENSE comparator is active at the end of this mask time.
21. BCK_CMP_DEL < 120 ns, guaranteed by laboratory measurement, not tested in production.

Table 16. 5V TOLERANT DIGITAL INPUTS (SCLK, CSB, SDI, LEDCTRL1, LEDCTRL2, BSTSYNC)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
High−level input voltage	VINHI		2			V
Low−level input voltage	VINLO				0.8	V
Input digital in leakage current (Note 22)	R_{PULL}		40		160	kΩ
LEDCTRLx to PWM dimming propagation delay	$BUCKx_{\_SW\_DEL}$		3.6	4	4.9	μs

22. Pull down resistor ($R_{pulldown}$) for LEDCTRLx, BSTSYNC, SDI and SCLK, pull up resistor (R_{pullup}) for CSB to VDD.

Table 17. 5V TOLERANT OPEN−DRAIN DIGITAL OUTPUT (SDO)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Low−voltage output voltage	VOUTLO	I_{out} = −10 mA (current flows into the pin)			0.4	V
Equivalent output resistance	$R_{DS(on)}$	Low−side switch		20	40	Ω
SDO pin leakage current	$SDO_{\_ILEAK}$				2	μA
SDO pin capacitance (Note 23)	$SDO_{\_C}$			10		pF
CLK to SDO propagation delay (Note 24)	$SDO_{\_DL}$	Low−side switch activation/deactivation time			320	ns

23. Guaranteed by bench measurement, not tested in production.
24. Values valid for 1 kΩ external pull−up connected to 5 V and 100 pF to GND, when in case of falling edge the voltage on the SDO pin goes below 0.5 V. This delay is internal to the chip and does not include the RC charge at pin level when the output goes to high impedance.

Table 18. 3V TOLERANT DIGITAL PINS (TST1, TST2)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
High−level input voltage	VINHI		2			V
Low−level input voltage	VINLO				0.8	V
Input leakage current TST1 pin	$TST1_{\_Rpulldown}$	Internal pull−down resistance	19	32	47	kΩ
Input leakage current TST2 pin	$TST2_{\_Rpulldown}$	Internal pull−down resistance	1.6	4	5.9	kΩ

Table 19. SPI INTERFACE

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
CSB setup time	t_{CSS}		500			ns
CSB hold time	t_{CSH}		250			ns
SCLK low time	t_{WL}		500			ns
SCLK high time	t_{WH}		500			ns
Data−in (DIN) setup time	t_{SU}		250			ns
Data−in (DIN) hold time	t_{H}		275			ns
SDO disable time	t_{DIS}		110		320	ns
SDO valid for high lo low transition	t_{SDO_HL}				320	ns
SDO valid for low lo high transition (Note 25)	t_{SDO_LH}				320 + t(RC)	ns
SDO hold time	t_{HO}		110			ns
CSB high time	t_{CS}		1000			ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
25. Time depends on the SDO load and pull−up resistor.

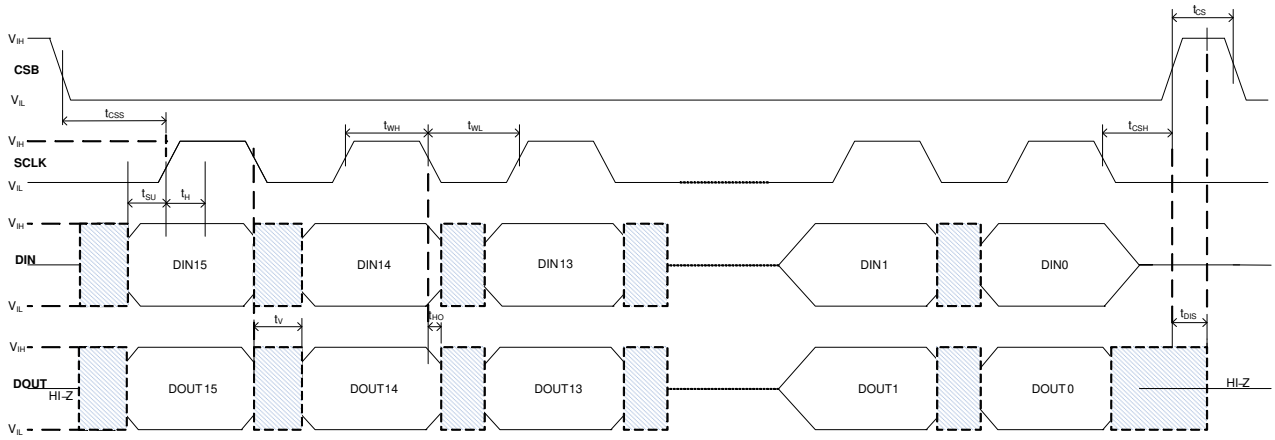


Figure 5. NCV78763 SPI Communication Timing

TYPICAL CHARACTERISTICS

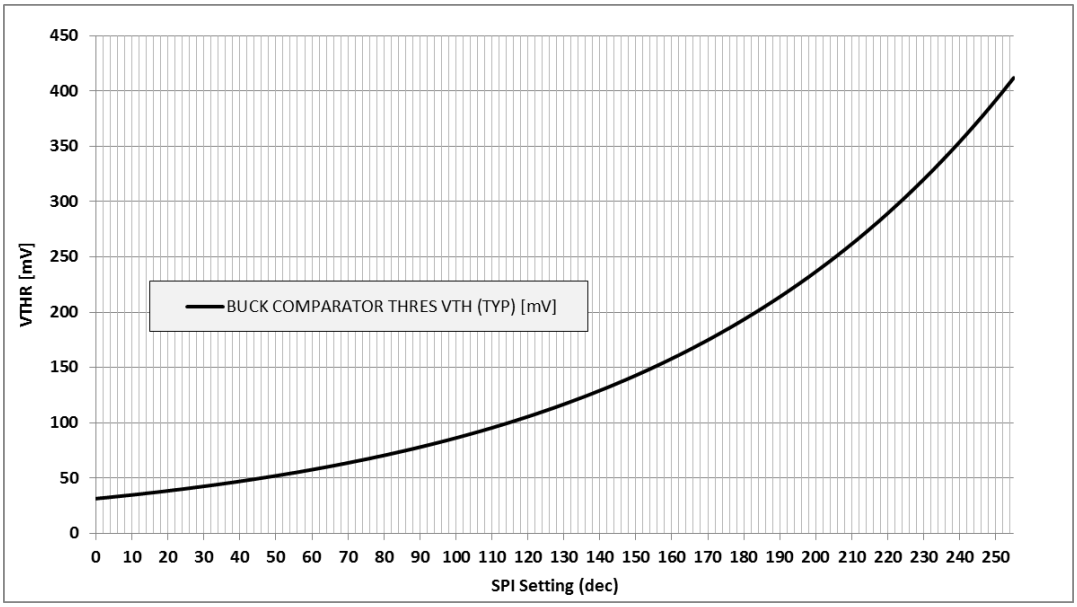


Figure 6. Buck Peak Comparator Threshold (Note 26)

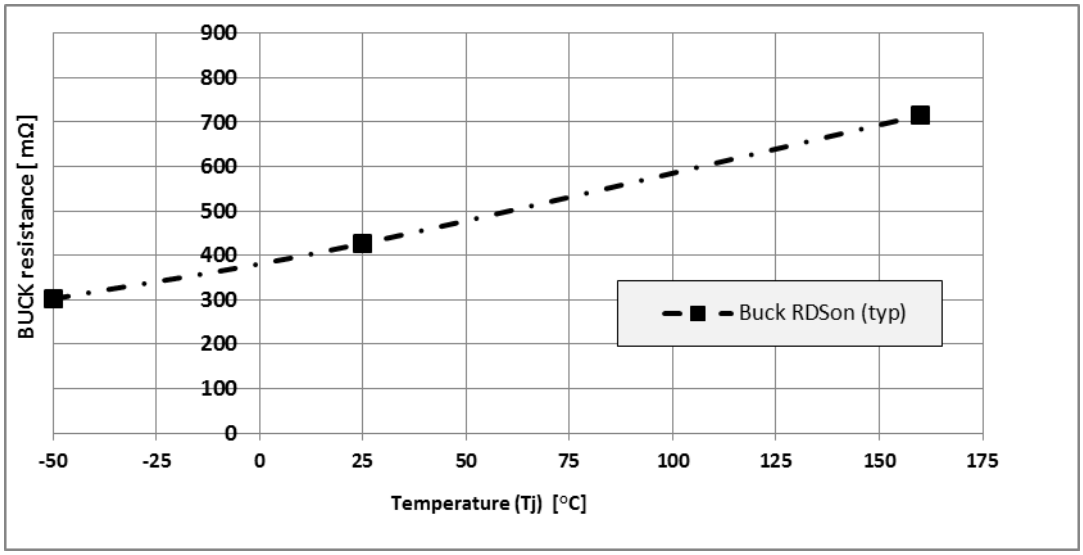


Figure 7. Buck MOSFET Typical $R_{DS(on)}$ Over Silicon Junction Temperature

26. Curve obtained by applying the typical exponential increase from the min value VTHR_000. Please see Table 15 for details.

DETAILED OPERATING AND PIN DESCRIPTION

SUPPLY CONCEPT IN GENERAL

Low operating voltages become more and more required due to the growing use of start stop systems. In order to respond to this necessity, the NCV78763 is designed to support power−up starting from V_{BB} = 5 V.

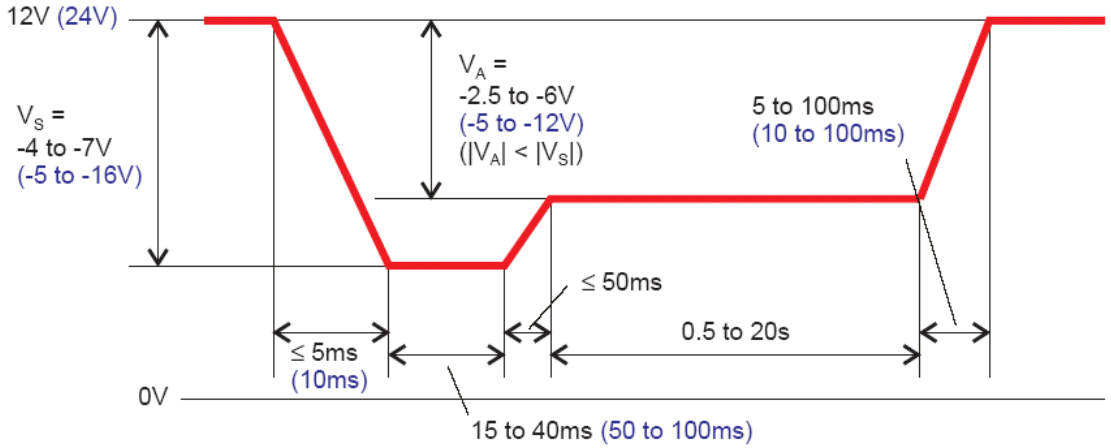


Figure 8. Cranking Pulse (ISO7637−1): System has to be Fully Functional (Grade A) from Vs = 5 V to 28 V

VDRIVE Supply

The VDRIVE supply voltage represents the power for the complete the BOOST PREDRV block, which generates the VGATE, used to switch the booster MOSFET. The voltage is programmable via SPI in 16 different values (register VDRIVE_SETPOINT[3:0], ranging from a minimum of 5 V typical to 10 V typical: see Table 6). This feature allows having the best switching losses vs. resistive losses trade off, according to the MOSFET selection in the application, also versus the minimum required battery voltage. The lowest settings can be exploited to drive logic gate drive MOSFETs. In order to support low VBB battery voltages and long crank pulse drops, the VDRIVE supply can take its energy from the source with the highest output voltage, either from (refer to Figure 1):

- the VREG10V supply, which derives its energy from the VBB input.
- the VBOOST_AUXSUP, which gets its energy from the VBOOST path. In order to enable this condition the bit VDRIVE_BST_EN[0] = 1. It is highly recommended to enable this function at module running mode in order to insure proper MOSFET gate drive even in case of large battery drop transients.

Under normal operating conditions, when the voltage headroom between VBB and VREG10V is sufficient, the gate driver energy is entirely supplied via the VBB path. In case the VBOOST_AUX regulator is enabled, it will start to draw part of the required current starting as from when the headroom reduces below the minimum requirement, then linearly increasing, until bearing 100% of the IDRIVE current when the VBB drops close or below the VDRIVE target and still enough energy can be supplied by the booster circuit. Please note that the full device functionality is not guaranteed for VBB voltages lower than 4 V and that for very low voltages a reset will be generated (see Table 7).

Note: powering the device via the VBOOST_AUXSUP will produce an extra power dissipation linked to the related linear drop (VBOOST − VBOOST_AUXSUP), which must be taken into account during the thermal design.

VDD Supply

The VDD supply is the low voltage digital and analog supply for the chip and derives energy from VBB. Due to the low dropout regulator design, VDD is guaranteed already from low VBB voltages. The Power−On−Reset circuit (POR) monitors the VDD voltage and the VBB voltage to control the out−of−reset and reset entering state: an internal switch disconnects the VDD regulator from the VBB input as its voltage drops below the admitted threshold VBB_LOW (Table 7); this originates a VDD discharge that will result in a device reset either if the voltage falls below the PORL level or in general, if due to the drop, the VDD regulation target cannot be kept for more than typically 100 µs. At power-up, the chip will exit from reset state when VBB > VBB_LOW and VDD > PORH.

VBOOSTM3V Supply

The VBOOSTM3V is the high side auxiliary supply for the gate drive of the buck regulators' integrated high−side P−MOSFET switches. This supply receives energy directly from the VBOOST pin.

INTERNAL CLOCK GENERATION − OSC8M

An internal RC clock named OSC8M is used to run all the digital functions in the chip. The clock is trimmed in the factory prior to delivery. Its accuracy is guaranteed under full operating conditions and is independent from external component selection (refer to Table 9 for details).

ADC

General

The built−in analog to digital converter (ADC) is an 8−bit capacitor based successive approximation register (SAR). This embedded peripheral can be used to provide the following measurements to the external Micro Controller Unit (MCU):

- V_{BOOST} voltage: sampled at the VBOOST pin;
- V_{BB} voltage (linked to the battery line);
- $VLED1_{ON}$, $VLED2_{ON}$ voltages;
- VLED1 and VLED2 voltages;
- VTEMP measurement (chip temperature).

The internal NCV78763 ADC state machine samples all the above channels automatically, taking care for setting the analog MUX and storing the converted values in memory. The external MCU can readout all ADC measured values via the SPI interface, in order to take application specific decisions. Please note that none of the MCU SPI commands interfere with the internal ADC state machine sample and conversion operations: the MCU will always get the last available data at the moment of the register read.

The state machine sampling and conversion scheme is represented in the figure below.

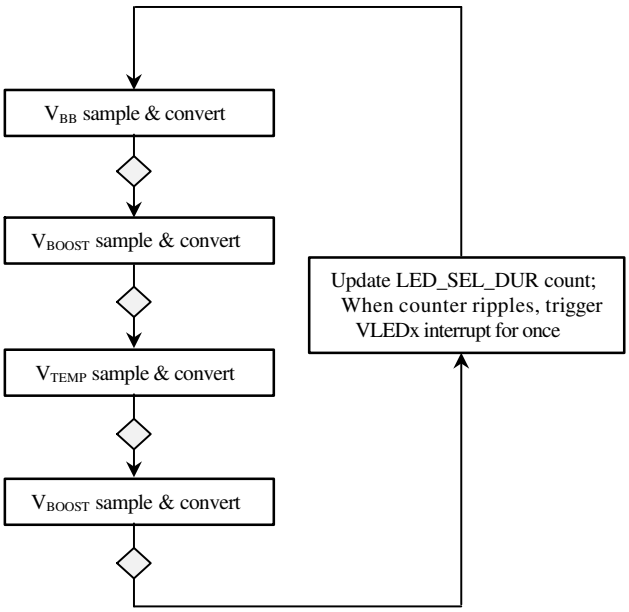


Figure 9. ADC Sample and Conversion Main Sequence

Referring to the figure above, the typical rate for a full SAR plus digital conversion per channel is 8 μs (Table 10). For instance, each new V_{BOOST} ADC converted sample occurs at 16 μs typical rate, whereas for both the V_{BB} and V_{TEMP} channel the sampling rate is typically 32 μs, that is to say a complete cycle of the depicted sequence. This time is referred to as T_{ADC_SEQ}.

If the SPI setting LED_SEL_DUR[8:0] is not zero, then interrupts for the VLEDx measurements are allowed at the points marked with a rhombus, with a minimum cadence corresponding to the number of the elapsed ADC sequences (forced interrupt). In formulas:

$$T_{VLEDx\_INT\_forced} = LED\_SEL\_DUR[8:0] \times T_{ADC\_SEQ}$$

In general, prior to the forced interrupt status, the $VLEDx_{ON}$ ADC interrupts are generated when a falling edge on the control line for the buck channel "x" is detected by the device. In case of *external dimming*, this interrupt start signal corresponds to the LEDCTRLx falling edge together with a controlled phase delay (Table 16). When in *internal dimming*, the phase delay is also internally created, in relation with the falling edge of the dimming signal. The purpose of the phase delay is to allow completion the ongoing ADC conversion before starting the one linked to the VLEDx interrupt: if at the moment of the conversion LEDCTRLx pin is logic high, then the updated registers are VLEDxON[7:0] and VLEDx[7:0]; otherwise, if LEDCTRLx pin is logic low, the only register refreshed is VLEDx[7:0]. This mechanism is handled automatically by the NCV78763 logic without need of intervention from the user, thus drastically reducing the MCU cycles and embedded firmware and CPU cycles overhead that would be otherwise required.

To avoid loss of data linked to the ADC main sequence, one LED channel is served at a time also when interrupt requests from both channels are received in a row and a full sequence is required to go through to enable a new interrupt VLEDx. In addition, possible conflicts are solved by using a defined priority (channel pre−selection). Out of reset, the default selection is given to channel "1". Then an internal flag keeps priority tracking, toggling at each time between channels pre−selection. Therefore, up to two dimming periods will be required to obtain a full measurement update of the two channels. This not considered however a limitation, as typical periods for dimming signals are in the order of 1 ms period, thus allowing very fast failure detection.

A flow chart referring to the ADC interrupts is also displayed (Figure 10).

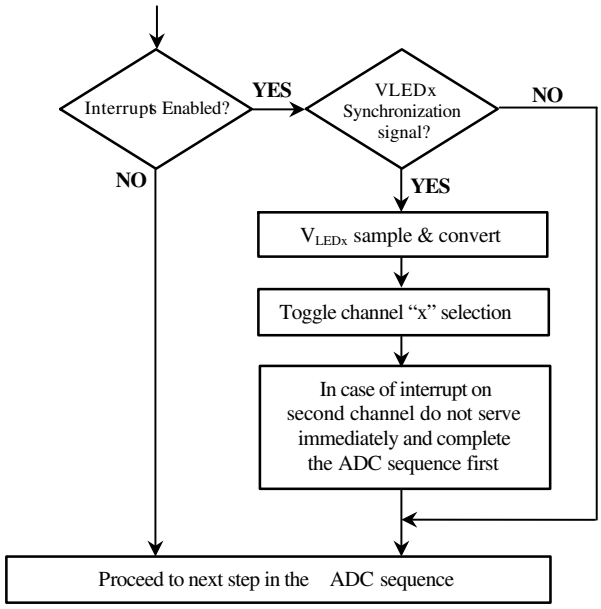


Figure 10. ADC VLEDx Interrupt Sequence

All NCV78763 ADC registers data integrity is protected by ODD parity on the bit 8 (that is to say the 9th bit if counting from the LSbit named "0"). Please refer to the SPI map section for further details.

Battery voltage ADC: V_{BB}

The battery voltage is sampled making use of the device supply V_{BB} pin. The (8−bit) conversion ratio is 40/255 (V/dec) = 0.157 (V/dec) typical. The converted value can be found in the SPI register VBB[7:0], with ODD parity protection bit in VBB[8]. The external MCU can make use of the measured VBB value to monitor the status of the module supply, for instance for a power de−rating algorithm.

Boost voltage ADC: V_{BOOST}

This measure refers to the boost voltage at the VBOOST pin, with an 8 bit conversion ratio of 70/255 (V/dec) = 0.274 (V/dec) typical, inside the SPI register VBOOST[7:0]. This measurement can be used by the MCU for diagnostics and booster control loop monitoring. The measurement is protected by parity (ODD) in bit VBOOST[8].

Device Temperature ADC: V_{TEMP}

By means of the VTEMP measurement, the MCU can monitor the device junction temperature (T_J) over time. The conversion formula is:

$$T_J = (VTEMP[7:0](dec) - 20)[^\circ C]$$

VTEMP[7:0] is the value read out directly from the related 8bit−SPI register (please refer to the SPI map). The value is also used internally by the device to for the *thermal warning* and *thermal shutdown* functions. More details on these two can be found in the dedicated sections in this document. The parity protection (ODD) is found on bit VTEMP[8].

LED String Voltages ADC: V_{LEDx}, V_{LEDxON}

The voltage at the pins VLEDx (1, 2) is measured. Their conversion ratio is 70/255 (V/dec) = 0.274 (V/dec) typical. This information, found in registers VLEDxON[7:0] and VLEDx[7:0], can be used by the MCU to infer about the LED string status. For example, individual shorted LEDs, or dedicated Open string and short to GND or short to battery algorithms. As for the other ADC registers, the values are protected by ODD parity, respectively in VLEDxON[8] and VLEDx[8].

Please note that in the case of constant LEDCTRLx inputs and no dimming (in other words dimming duty cycle equals to 0% or 100%) the VLEDx interrupt is forced with a rate equal to $T_{VLEDx\_INT\_forced}$, given in the ADC general section. This feature can be exploited by MCU embedded algorithm diagnostics to read the LED channels voltage even when in OFF state, before module outputs activation (module startup pre−check).

BOOSTER REGULATOR

General

The NCV78763 features one common booster stage for the two high−current integrated buck current regulators. In addition, optional external buck regulators, belonging to other NCV78x63 devices, can be cascaded to the same boost voltage source as exemplified in the picture below.

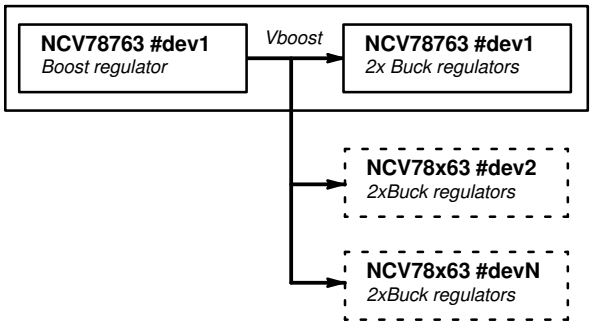


Figure 11. Cascading Multiple NCV78x63 Buck Channels on a Common Boost Voltage Source

The booster stage provides the required voltage source for the LED string voltages out of the available battery voltage. Moreover, it filters out the variations in the battery input current in case of LED strings PWM dimming.

For nominal loads, the boost controller will regulate in *continuous mode* of operation, thus maximizing the system power efficiency at the same time having the lowest possible input ripple current (with “continuous mode” it is meant that the supply current does not go to zero while the load is activated). Only in case of very low loads or low dimming duty cycle values, *discontinuous mode* can occur: this means the supply current can swing from zero when the load is off, to the required peak value when the load is on, while keeping the required input average current through the cycle. In such situations, the total efficiency ratio may be lower than the theoretical optimal. However, as also the total losses will at the same time be lower, there will be no impact on the thermal design.

On top of the cascaded configuration shown in the previous figure, the booster can be operated in *multi−phase mode* by combining more NCV78763 in the application. More details about the multiphase mode can be found in the dedicated section.

Booster Regulation Principles

The NCV78763 features a *current−mode* voltage controller, which regulates the V_{BOOST} line used by the buck converters. The regulation loop principle is shown in the following picture. The loop compares the reference voltage ($V_{BOOST\_SETPOINT}$) with the actual measured voltage at the V_{BOOST} pin, thus generating an error signal which is treated internally by the error trans−conductance amplifier (block A1). This amplifier transforms the error voltage into current by means of the trans−conductance gain G_m. The amplifier’s output current is then fed into the external compensation network impedance (A2), so that it originates a voltage at the V_{COMP} pin, this last used as a reference by the current control block (B).

The current controller regulates the duty cycle as a consequence of the V_{COMP} reference, the sensed inductor peak current via the external resistor R_{SENSE} and the slope compensation used. The power converter (block C) represents the circuit formed by the boost converter externals (inductor, capacitors, MOSFET and forward diode). The load power (usually the LED power going via the buck converters) is applied to the converter.

The controlled variable is the boost voltage, measured directly at the device VBOOST pin with a unity gain feedback (block F). The picture highlights as block G all the elements contained inside the device. The regulation parameters are flexibly set by a series of SPI commands indicated in Tables 11 and 12. A detailed internal boost controller block diagram is presented in the next section.

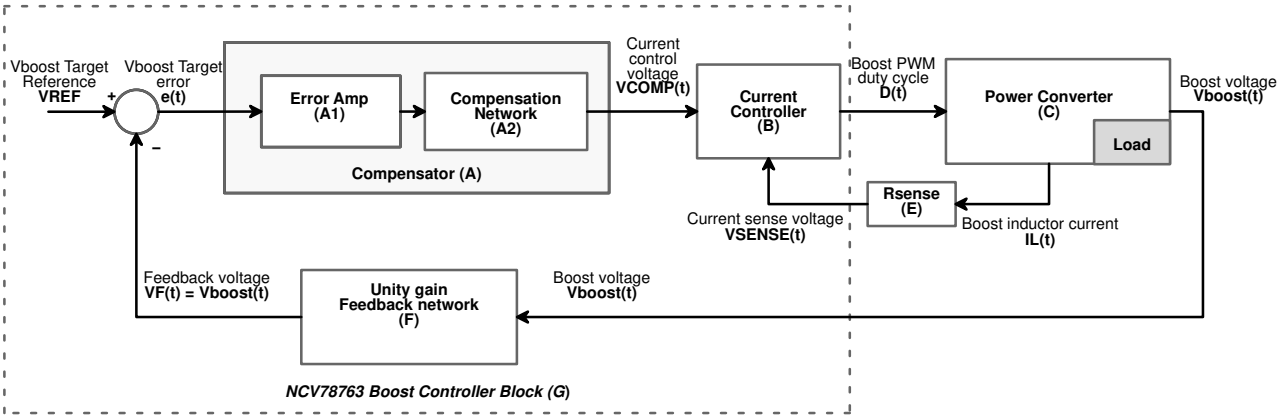


Figure 12. NCV78763 Boost Control Loop – Principle Block Diagram

Boost Controller Detailed Internal Block Diagram

A detailed NCV78763 boost controller block diagram is provided in this section. The main signals involved are indicated, with a particular highlight on the SPI programmable parameters.

The blocks referring to the principle block diagram are also indicated. In addition, the *protection specific* blocks can be found (see dedicated sections for details).

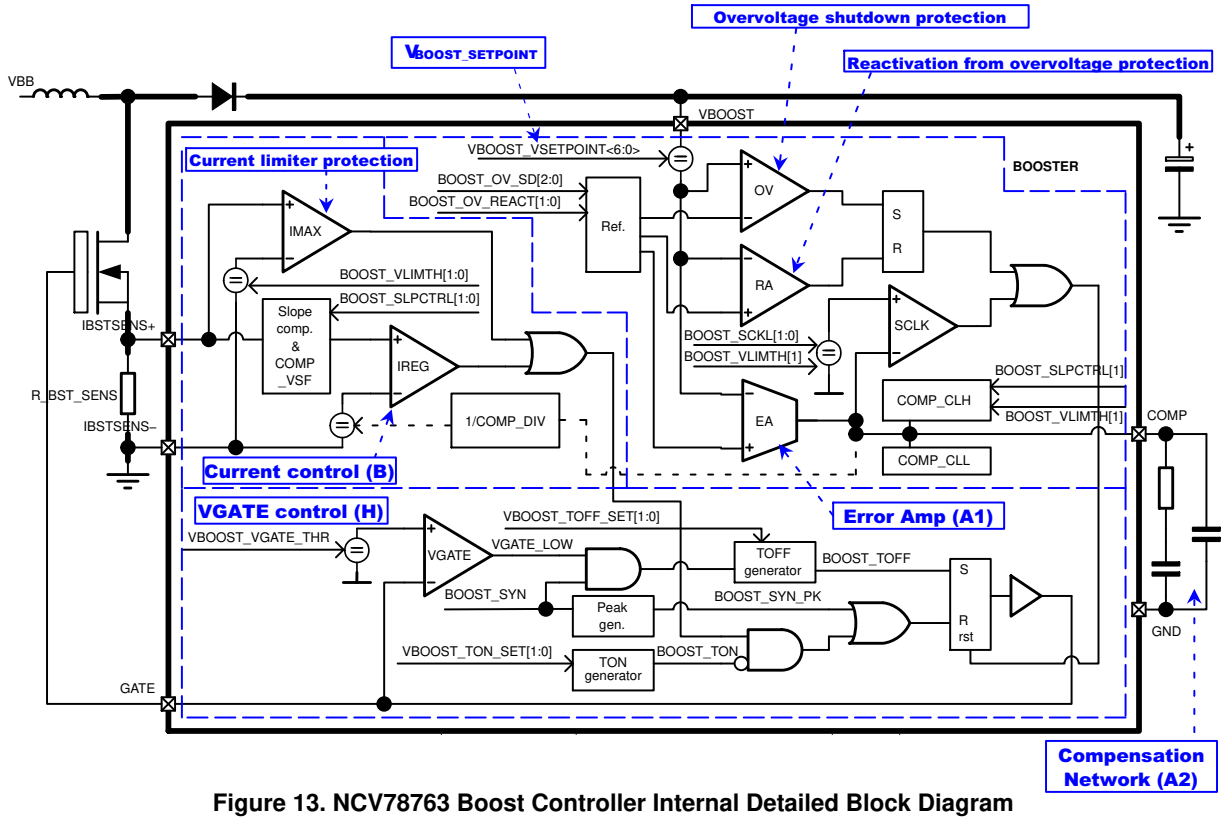


Figure 13. NCV78763 Boost Controller Internal Detailed Block Diagram

Booster Regulator Setpoint ($V_{BOOST\_SETPOINT}$)

The booster voltage V_{BOOST} is regulated around the target programmable by the 7−bit SPI setting VBOOST_SETPOINT[6:0], ranging from a minimum of 11 V to a maximum of typical 64.1 V (please refer to Table 11 for details). Due to the step−up only characteristic of any boost converter, the boost voltage cannot obviously be lower than the supply battery voltage provided. Therefore a target of 11 V would be used only for systems that require the activation of the booster in case of battery drops below the nominal level.

At power−up, the booster is disabled and the setpoint is per default the minimum (all zeroes).

Booster Overvoltage Shutdown Protection

An integrated comparator monitors V_{BOOST} in order to protect the external booster components and the led driver device from overvoltage. When the voltage rises above the threshold defined by the sum of the $V_{BOOST\_SETPOINT}$ (VBOOST_SETPOINT[6:0]) and the overvoltage shutdown value (BOOST_OV_SD[2:0]), the MOSFET gate is switched−off at least for the current PWM cycle and at the same time, the boost overvoltage flag in the status register will be set (BOOST_OV = 1), together with the BOOST_STATUS flag equals to zero. The PWM runs again as from the moment the V_{BOOST} will fall below the reactivation hysteresis defined by the BOOST_OV_REACT[1:0] SPI parameter. Therefore, depending on the voltage drop and the PWM frequency, it might be that more than one cycle will be skipped. A graphical interpretation of the protection levels is given in the figure below, followed by a summary table (Table 20).

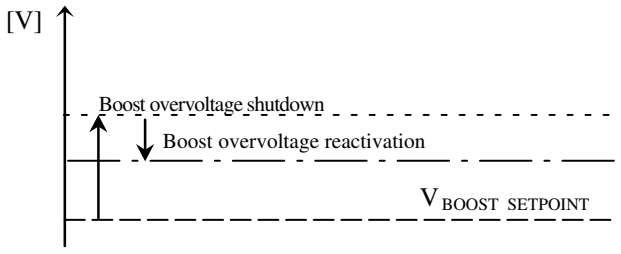


Figure 14. Booster Voltage Protection Levels with Respect to the Setpoint

Table 20. NCV78763 BOOST CONTROLLER OVERVOLTAGE PROTECTION LEVELS AND RELATED SPI DIAGNOSTICS

ID	Description	PWM VGATE Condition	SPI FLAGS	
			BOOST_STATUS	BOOST_OV
A	$V_{BOOST} < V_{BOOST\_SETPOINT}$	Normal (not disabled)	1	0
B	$V_{BOOST} > V_{BOOST\_SETPOINT}$ + BOOST_OV_SD	Disabled until case “C”	0	1 (latched)
C	$V_{BOOST} < V_{BOOST\_SETPOINT}$ + BOOST_OV_SD BOOST_OV_REACT	Re−enables the PWM, normal mode resumed if from case “B”	1	1
				(latched, if read in this condition it will go back to “0”)

After POR, the BOOST_OV flag may be set at first read out. Please note that the booster overvoltage detection is also active when Booster is OFF (booster disabled by SPI related bit). Please note that the tolerances of the booster setpoint level and the booster overvoltage and reactivation are given in Table 11.

Booster Current Regulation Loop

The peak−current level of the booster is set by the voltage of the compensation pin COMP (output of the trans−conductance error amplifier, “block B” of Figure 13). This reference voltage is fed to the current comparator through a divider by 7 and compared to the voltage V_{SENSE} on the external sense resistor R_{SENSE}, connected to the pins IBSTSENSE+ and IBSTSENSE−. The sense voltage is created by the booster inductor coil current when the MOSFET is switched on and is summed up to an additional offset of +0.5 V (see $COMP\_{VSF}$ in Table 11) and on top of that a slope compensation ramp voltage is added. The slope compensation is programmable by SPI via the setting (BOOST_SLP_CTRL[1:0]) and can also be disabled. Due to the offset, current can start to flow in the circuit as $V_{COMP} > COMP\_{VSF}$.

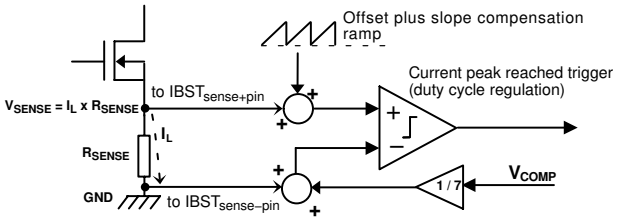


Figure 15. Booster Peak Current Regulator Involved in Current Control Loop

The maximum booster peak−current is limited by a dedicated comparator, presented in the next section.

Booster Current Limitation Protection

On top of the normal current regulation loop comparator, an additional comparator clamps the maximum physical current that can flow in the booster input circuit while the MOSFET is driven. The aim is to protect all the external components involved (boost inductor from saturation, boost diode and boost MOSFET from overcurrent, etc…). The protection is active PWM cycle−by−cycle and switches off the MOSFET GATE as V_{SENSE} reaches its maximum threshold V_{SENSE_MAX} defined by the BST_VLIMTH[1:0] register (see IMAX comparator in Figure 13 and Table 12 for more details). Therefore, the maximum allowed peak current will be defined by the ratio $I_{PEAK\_MAX} = V_{SENSE\_MAX} / R_{SENSE}$. The maximum current must be set in order to allow the total desired booster power for the lowest battery voltage. Warning: setting the current limit too low may generate unwanted system behavior as uncontrolled de−rating of the LED light due to insufficient power.

Booster PWM Frequency and Disable

The NCV78763 allows a flexible set of the booster PWM frequency. Two modes are available: internal generation or external drive, selectable by SPI bit setting BOOST_SRC[0]. In either case, the booster must be enabled via the dedicated SPI bit to allow PWM generation (BOOST_EN = 1). When BOOST_EN = 0, the peripheral is off and the GATE drive is disabled. Please note that the error amplifier is not shut off automatically and to avoid voltage generation on the VCOMP pin the G_m gain must be put to zero as well.

Booster PWM Internal Generation

This mode activated by BOOST_SRC = 0, creates the PWM frequency starting from the internal clock FOSC8M. A fine selection of frequencies is enabled by the register BOOST_FREQ[4:0], ranging from typical 210 kHz to typical 1 MHz (Table 11). The frequency generation is disabled by selecting the value “zero”; this is also the POR default value.

Booster PWM External Generation

When BOOST_SRC = 1, the booster PWM external generation mode is selected and the frequency is taken directly from the BOOST_SYNC device pin. There is no actual limitation in the resolution, apart from the system clock for the sampling and a debounce of two clock cycles on the signal edges. The gate PWM is synchronized with either the rising or falling edge of the external signal depending on the BOOST_SRCINV bit value. The default POR value is “0” and corresponds to synchronization to the

rising flank. BOOST_SRCINV equals “1” selects falling edge synchronization.

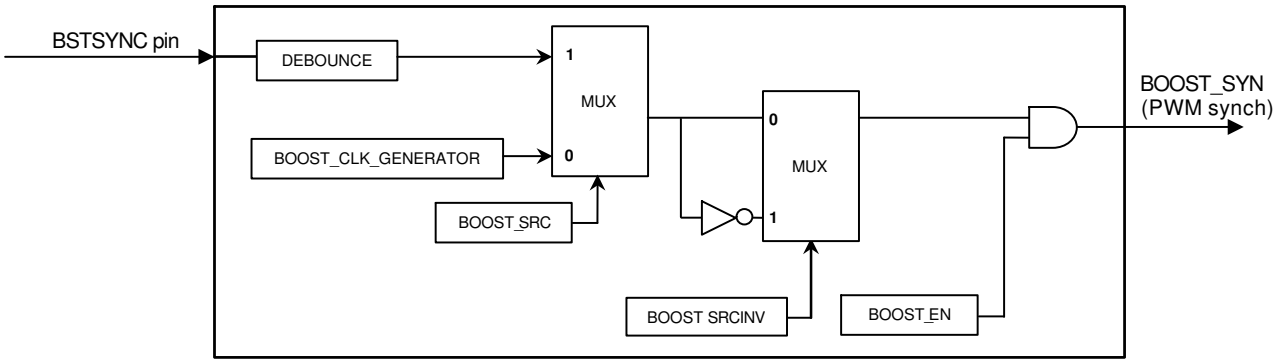


Figure 16. NCV78763 Booster Frequency Generation Block

Booster PWM Min TOFF and Min TON protection

As additional protection, the PWM duty cycle is constrained between a minimum and a maximum, defined per means of two parameters available in the device. The PWM *minimum on−time* is programmable via BOOST_TONMIN[1:0]: its purpose is to guarantee a minimum activation interval for the booster MOSFET GATE, to insure full drive of the component and avoiding switching in the linear region. Please note that this does not imply that the PWM is always running even when not required by the control loop, but means that whenever the MOSFET should be activated, then its on time would be at least the one specified. At the contrary When no duty cycle at all is required, then it will be zero.

The PWM *minimum off−time* is set via the parameter BOOST_TOFFMIN[1:0]: this parameter is limiting the maximum duty cycle that can be used in the regulation loop for a defined period T_{PWM}:

$$Duty_{MAX} = \frac{\left(T_{PWM} - T_{OFFMIN}\right)}{T_{PWM}}$$

The main aim of a maximum duty cycle is preventing MOSFET shoot−through in cases the (transient) duty cycle would get too close to 100% of the MOSFET real switch−off characteristics. In addition, as a secondary effect, a limit on the duty cycle may also be exploited to minimize the inrush current when the load is activated.

Warning: a wrong setting of the duty cycle constraints may result in unwanted system behavior. In particular, a too big T_{OFFMIN} may prevent the system to regulate the V_{BOOST} with low battery voltages (V_{BAT}). This can be explained by the simplified formula for booster *steady state continuous mode*:

$$V_{BOOST} \cong \frac{V_{BAT}}{(1 - Duty)} \Leftrightarrow Duty \cong \frac{V_{BOOST} - V_{BAT}}{V_{BOOST}}$$

So in order to reach a desired V_{BOOST} for a defined supply voltage, a certain duty cycle must be guaranteed.

Booster Compensator Model

A linear model of the booster controller compensator (block “A” Figure 13) is provided in this section. The protection mechanisms around are not taken into account. A type “2” network is taken into account at the VCOMP pin. The equivalent circuit is shown below:

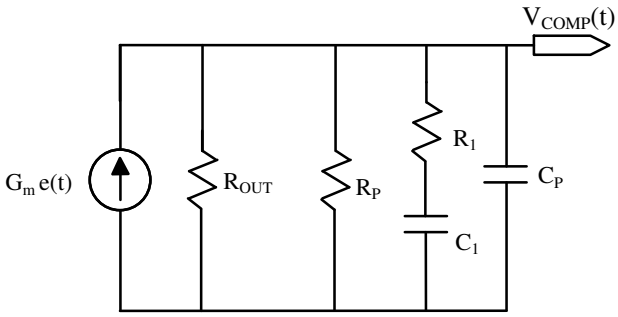


Figure 17. Booster Compensator Circuit with Type “2” Network

In the Figure, e(t) represents the control error, equals to the difference $V_{BOOST\_SETPOINT}(t) - V_{BOOST}(t)$. “$G_m$” is the trans−conductance error amplifier gain, while “R_{OUT}” is the amplifier internal output resistance. The values of these two parameters can be found in Table 11 in this datasheet.

By solving the circuit in Laplace domain the following error to V_{COMP} transfer function is obtained:

$$H_{COMP}(s) = \frac{V_{COMP}(s)}{e(s)} = G_{COMP}\frac{\left(1 + \tau_1 s\right)}{\left(1 + \left(\tau_P + \tau_{1P}\right)s + \left(\tau_1 + \tau_P\right)s^2\right)}$$

The explanation of the parameters stated in the equation above follows:

$$\begin{cases} G_{COMP} = G_m R_T \\ R_T = \dfrac{R_P}{R_P + R_{OUT}} \\ \tau_1 = R_1 C_1 \\ \tau_P = R_P C_P \\ \tau_{1P} = \left(R_1 + R_T\right)C_1 \end{cases}$$

This transfer function model can be used for closed loop stability calculations.

Booster PWM skip cycles

In case of light booster load, it may be useful to reduce the number of effective PWM cycles in order to get a decrease of the input current inrush bursts and a less oscillating boost voltage. This can be obtained by using the “skip cycles” feature, programmable by SPI via BOOST_SKCL[1:0] (see Table 11 and SPI map). BOOST_SKCL[1:0] = ‘00’ means skip cycle disabled.

The selection defines the VCOMP voltage threshold below which the PWM is stopped, thus avoiding V_{BOOST} oscillations in a larger voltage window.

Booster Monophase or Multiphase Mode Principles

The NCV78763 booster can be operated in two main modes: *single phase* (N = 1), or “*multiphase*” (N ≥ 2).

In single phase mode, a unique NCV78763 booster is used, in the configuration shown in the standard application diagram (Figure 4).

In multiphase mode, more NCV78763 boosters can be connected together to the same V_{BOOST} node, sharing the boost capacitor block. Multiphase mode shows to be a cost effective solution in case of mid to high power systems, where bigger external BOM components would be required to bear the total power in one phase only with the same performances and total board size. In particular, the boost inductor could become a critical item for very high power levels, to guarantee the required minimum saturation current and RMS heating current.

Another advantage is the benefit from EMC point of view, due to the reduction in ripple current per phase and ripple voltage on the module input capacitor and boost capacitor. The picture below shows the (very) ideal case of 50% duty cycle, the ripple of the total module current (I_{Lmp_sum} = I_{L1mp} + I_{L2mp}) is reduced to zero. The equivalent single phase current (I_{Lsp}) is provided as a graphical comparison.

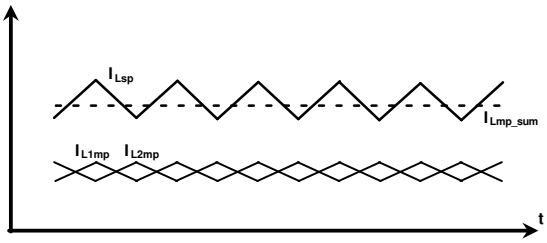


Figure 18. Booster Single Phase vs. Multiphase Example (N = 2)

Booster Multiphase Diagram and Programming

This section describes the steps both from hardware and SPI programming point of view to operate in multiphase mode. For hardware point of view, it is assumed that in multiphase mode (N boosters), each stage has the same external components. In particular, the values of the sense resistors have to match as much as possible to have a balanced current sharing. The following features have to be considered as well:

1. The compensation pin (COMP) of all boosters is connected together to the same compensation network, to equalize the power distribution of each booster. For the best noise rejection, the compensation network area has to be surrounded by the GND plane. Please refer to the PCB Layout recommendations section for more general advices.
2. To synchronize the MOSFET gate PWM clock and needed phase shifts, the boosters must use the external clock generation (BSTSYNC), generated by the board MCU or external logic, according to the user−defined control strategy. The generic number of lines needed is “N” equivalent to the number of stages. Please note that in case of a bi−phase system (N = 2) and an electrical phase shift of 180°, it is possible to use only one external clock line, exploiting the integrated NCV78763 features: the slave device shall have BOOST_SRCINV bit to “1” (clock polarity internal inversion active), whereas the master device will keep the BOOST_SRCINV bit to “0” (= no inversion, default).
3. Only the master booster error amplifier OTA must be active, while the other (slave) boosters must have all their own OTA block disabled (BOOST_OTA_GAIN[1:0] = ‘00’). For each of the devices in the chain, the register BOOST_MULTI_MD[1:0] must be kept to zero, default (‘00’)
4. In order to let the slave device(s) detect locally the boost over-voltage condition thus disabling the correspondent phase, the slave(s) must have the same (or higher) booster overvoltage shutdown level of the master device (see also section “Booster overvoltage shutdown protection” for more details on the protection mechanism and threshold). The MCU shall monitor the BOOST_OV flags to insure that all devices are properly operating in the application.

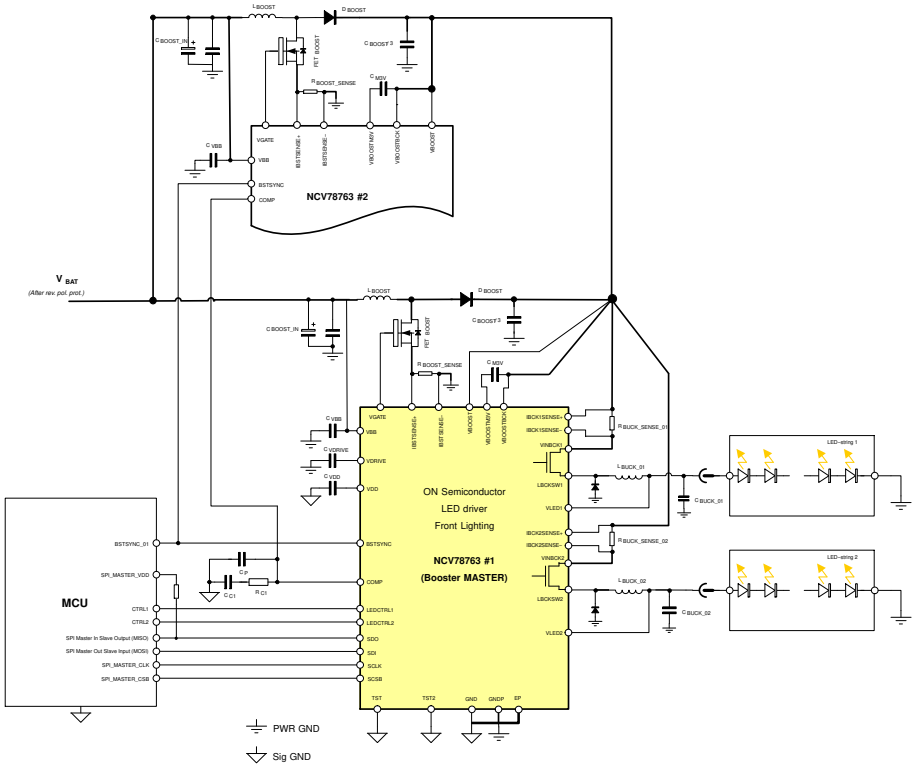


Figure 19. Booster Bi−phase Application Diagram (N = 2)

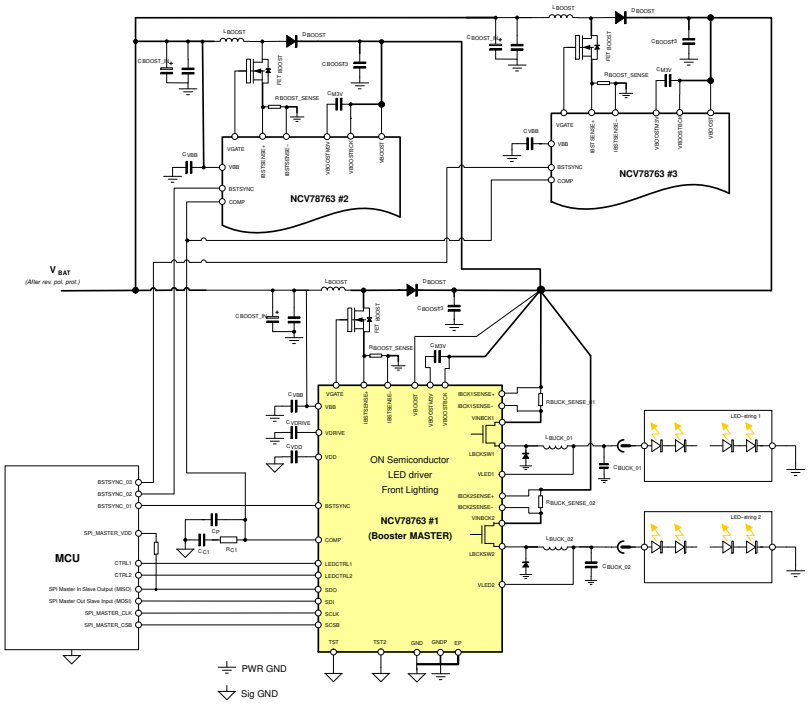


Figure 20. Booster Three−Phase Application Diagram (N = 3)

Booster Enable Control

The NCV78763 booster can be enabled/disabled directly by SPI via the bit BOOST_EN[0]. The enable signal is the transition from “0” to “1”; the disable function is vice−versa. The status of the physical activation is contained in the flag BOOST_STATUS: whenever the booster is running, the value of the flag is one, otherwise zero. It might in fact happen that despite the user *wanted* activation, the booster is stopped by the device in two main cases:

a. Whenever the boost overvoltage detection triggers in the control loop. The booster is automatically activated when the voltage falls below the hysteresis (Figure 14).