Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NCV8163

250 mA, Ultra-Low Noise and High PSRR LDO Regulator for RF and Analog Circuits

ON Semiconductor®

www.onsemi.com

The NCV8163 is a next generation of high PSRR, ultra−low noise LDO capable of supplying 250 mA output current. Designed to meet the requirements of RF and sensitive analog circuits, the NCV8163 device provides ultra−low noise, high PSRR and low quiescent current. The device also offer excellent load/line transients. The NCV8163 is designed to work with a 1 μF input and a 1 μF output ceramic capacitor. It is available in XDFN4 0.65P, 1 mm x 1 mm and TSOP−5 packages.

Features

- Operating Input Voltage Range: 2.2 V to 5.5 V
- Available in Fixed Voltage Option: 1.2 V to 5.3 V
- ±2% Accuracy Over Load/Temperature
- Ultra Low Quiescent Current Typ. 12 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 80 mV at 250 mA @ 3.3 V
- Ultra High PSRR: Typ. 92 dB at 20 mA, f = 1 kHz
- Ultra Low Noise: 6.5 μV_{RMS}
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in XDFN4 1 mm x 1 mm x 0.4 mm and TSOP−5 Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; Grade 1 AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- ADAS, Infotainment & Cluster, and Telematics
- General Purpose Automotive & Industrial
- Building & Factory Automation, Smart Meters

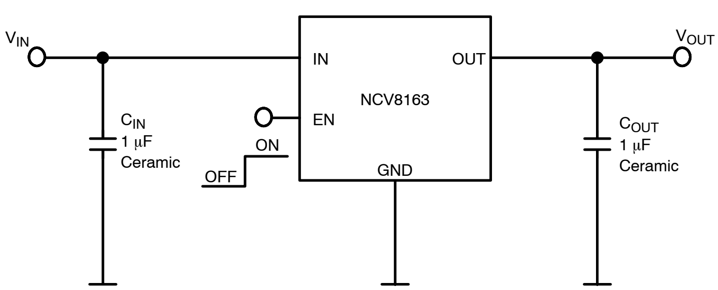
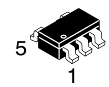
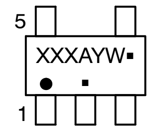


Figure 1. Typical Application Schematics

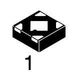
MARKING DIAGRAMS



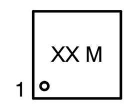
TSOP−5
CASE 483



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

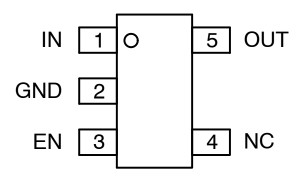


XDFN4
CASE 711AJ

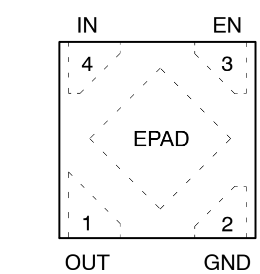


XX = Specific Device Code
M = Date Code

PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 14 of this data sheet.

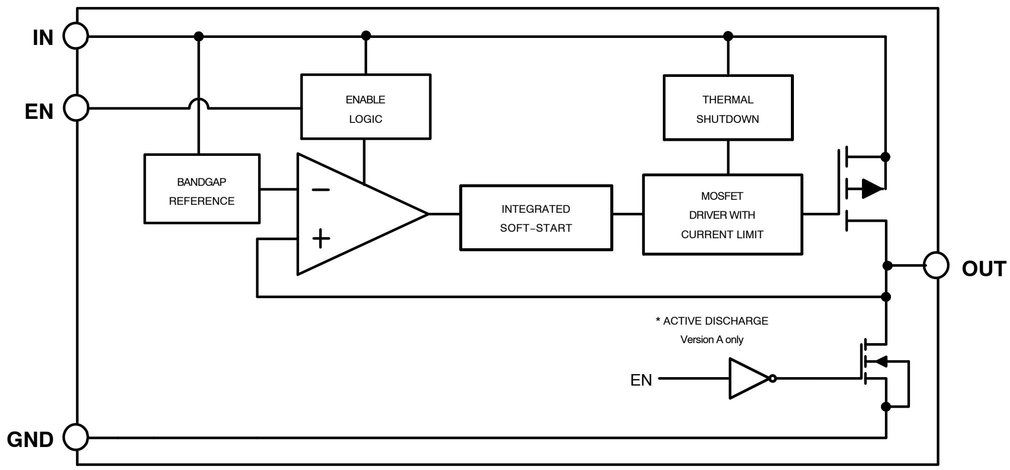


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. TSOP−5	Pin No. XDFN4	Pin Name	Description
1	4	IN	Input voltage supply pin
5	1	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor.
3	3	EN	Chip enable: Applying V_{EN} < 0.4 V disables the regulator, Pulling V_{EN} > 1.2 V enables the LDO.
2	2	GND	Common ground connection
4	–	N/C	Not connected. This pin can be tied to ground to improve thermal dissipation.
–	EP	EPAD	Exposed Pad. Exposed pad can be tied to ground plane for better power dissipation.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3, max. 6 V	V
Chip Enable Input	V_{CE}	−0.3 to 6 V	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   ESD Charged Device Model tested per EIA/JESD22−C101, Field Induced Charge Model
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	2.2	5.5	V
Junction Temperature	T_J	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN4 (Note 3), Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	198.1	°C/W
Thermal Characteristics, TSOP−5 (Note 3), Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	218	°C/W

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7

ELECTRICAL CHARACTERISTICS −40°C ≤ T_J ≤ 125°C; V_{IN} = $V_{OUT(NOM)}$ + 1 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 μF, unless otherwise noted. V_{EN} = 1.2 V. Typical values are at T_J = +25°C (Note 4).

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	2.2		5.5	V
Output Voltage Accuracy	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V		V_{OUT}	−2		+2	%
	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V (for V_{OUT} < 1.8 V)		V_{OUT}	−3		+3	%
Line Regulation	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 5.5 V		$Line_{Reg}$		0.02		%/V
Load Regulation	I_{OUT} = 1 mA to 250 mA	XDFN4	$Load_{Reg}$		0.001	0.005	%/mA
		TSOP−5			0.008	0.015	
Dropout Voltage (Note 5)	I_{OUT} = 250 mA XDFN4 package	$V_{OUT(NOM)}$ = 1.8 V	V_{DO}		180	250	mV
		$V_{OUT(NOM)}$ = 2.8 V			95	160	
		$V_{OUT(NOM)}$ = 3.0 V			90	155	
		$V_{OUT(NOM)}$ = 3.3 V			80	145	
Dropout Voltage (Note 5)	I_{OUT} = 250 mA TSOP−5 package	$V_{OUT(NOM)}$ = 1.8 V	V_{DO}		205	280	mV
		$V_{OUT(NOM)}$ = 2.8 V			120	190	
		$V_{OUT(NOM)}$ = 3.0 V			115	185	
		$V_{OUT(NOM)}$ = 3.3 V			105	175	
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	250	700		mA
Short Circuit Current	V_{OUT} = 0 V		I_{SC}		690		
Quiescent Current	I_{OUT} = 0 mA		I_Q		12	20	μA
Shutdown Current	V_{EN} ≤ 0.4 V, V_{IN} = 4.8 V		I_{DIS}		0.01	1	μA
EN Pin Threshold Voltage	EN Input Voltage "H"		V_{ENH}	1.2			V
	EN Input Voltage "L"		V_{ENL}			0.4	
EN Pull Down Current	V_{EN} = 4.8 V		I_{EN}		0.2	0.5	μA
Turn−On Time	C_{OUT} = 1 μF, From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$				120		μs
Power Supply Rejection Ratio	I_{OUT} = 20 mA	f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz	PSRR		91 92 85 60		dB
Output Voltage Noise	f = 10 Hz to 100 kHz	I_{OUT} = 1 mA I_{OUT} = 250 mA	V_N		8.0 6.5		μV_{RMS}
Thermal Shutdown Threshold	Temperature rising		T_{SDH}		160		°C
	Temperature falling		T_{SDL}		140		°C
Active Output Discharge Resistance	V_{EN} < 0.4 V, Version A only		R_{DIS}		280		Ω
Line Transient (Note 6)	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 1.6 V) in 30 μs, I_{OUT} = 1 mA		$Tran_{LINE}$	−1			mV
	V_{IN} = ($V_{OUT(NOM)}$ + 1.6 V) to ($V_{OUT(NOM)}$ + 1 V) in 30 μs, I_{OUT} = 1 mA					+1	
Load Transient (Note 6)	I_{OUT} = 1 mA to 200 mA in 10 μs		$Tran_{LOAD}$	−40			mV
	I_{OUT} = 200 mA to 1 mA in 10 μs					+40	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 100 mV below $V_{OUT(NOM)}$.
6. Guaranteed by design.

TYPICAL CHARACTERISTICS

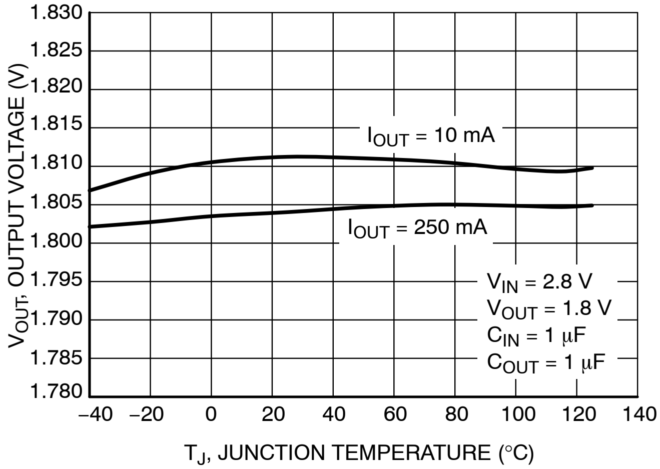


Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.8 V – XDFN Package

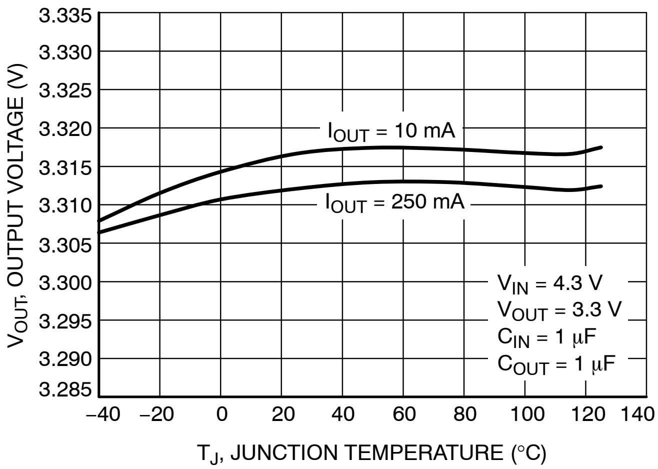


Figure 4. Output Voltage vs. Temperature – V_{OUT} = 3.3 V – XDFN Package

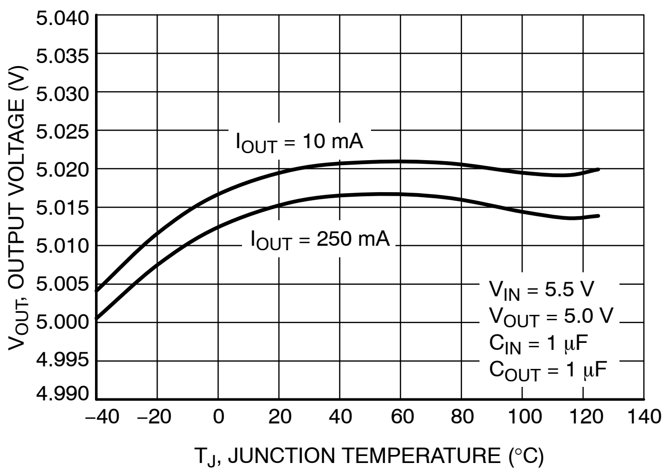


Figure 5. Output Voltage vs. Temperature – V_{OUT} = 5.0 V – XDFN Package

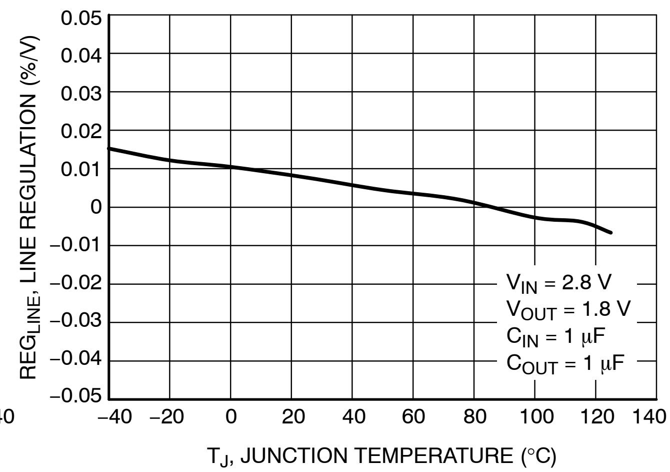


Figure 6. Line Regulation vs. Temperature – V_{OUT} = 1.8 V

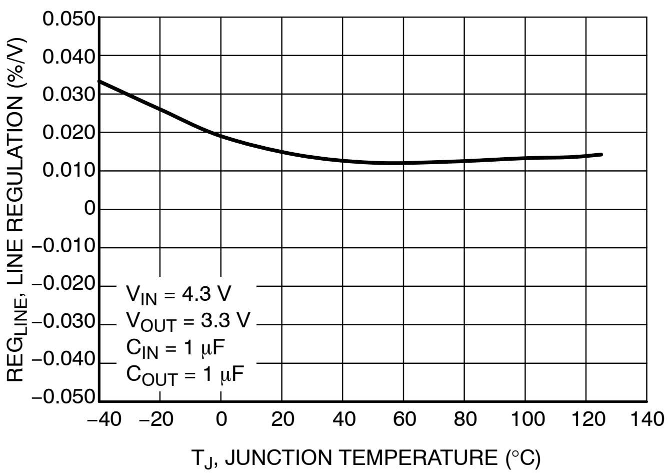


Figure 7. Line Regulation vs. Temperature – V_{OUT} = 3.3 V

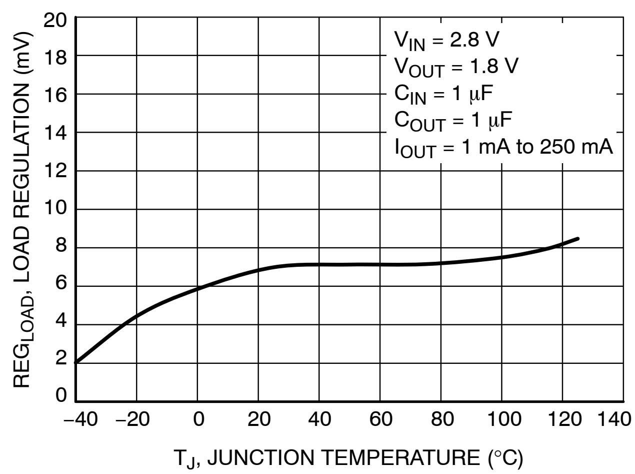


Figure 8. Load Regulation vs. Temperature – V_{OUT} = 1.8 V

TYPICAL CHARACTERISTICS

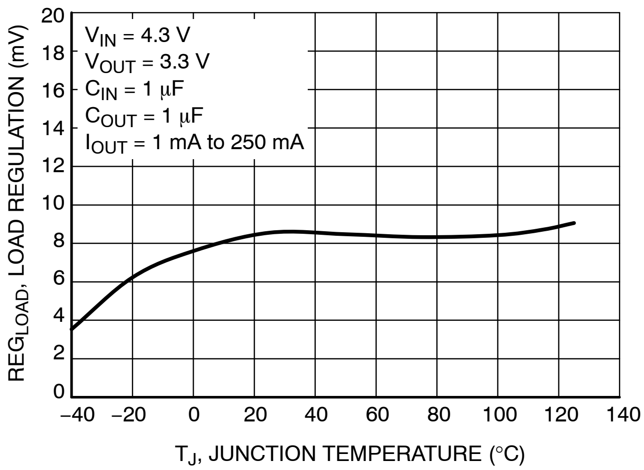


Figure 9. Load Regulation vs. Temperature – V_{OUT} = 3.3 V

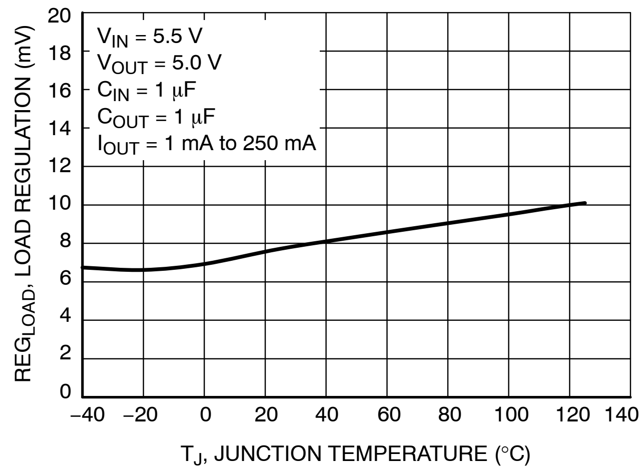


Figure 10. Load Regulation vs. Temperature – V_{OUT} = 5.0 V

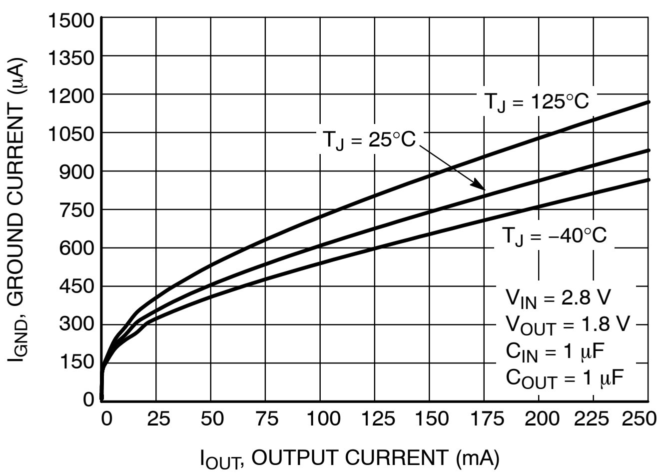


Figure 11. Ground Current vs. Load Current – V_{OUT} = 1.8 V

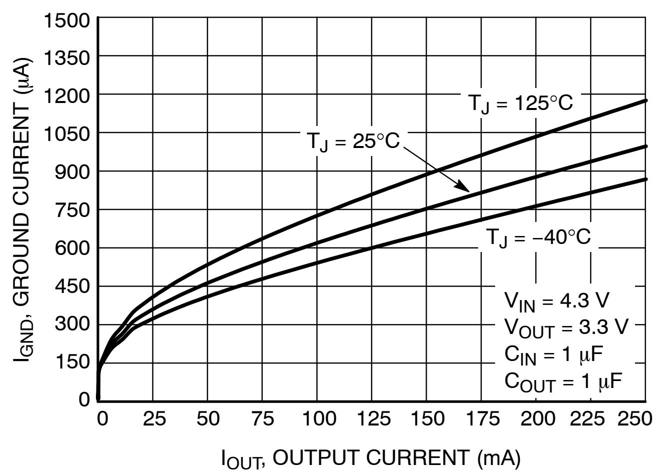


Figure 12. Ground Current vs. Load Current – V_{OUT} = 3.3 V

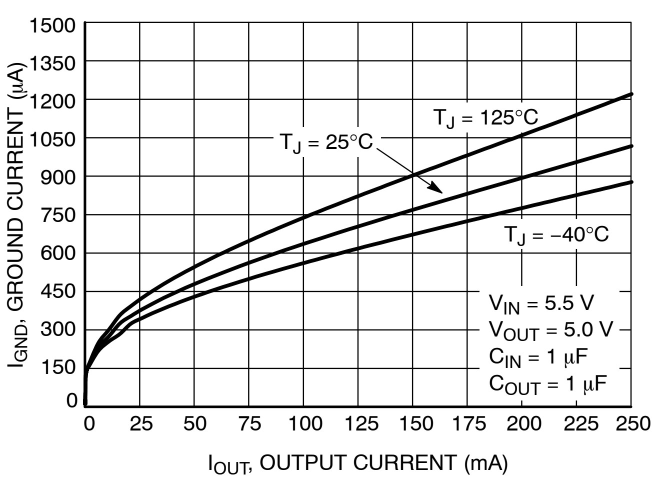


Figure 13. Ground Current vs. Load Current – V_{OUT} = 5.0 V

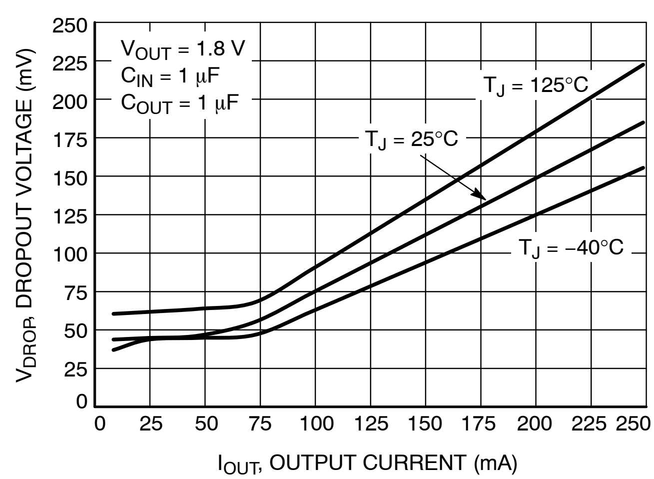


Figure 14. Dropout Voltage vs. Load Current – V_{OUT} = 1.8 V – XDFN4 Package

TYPICAL CHARACTERISTICS

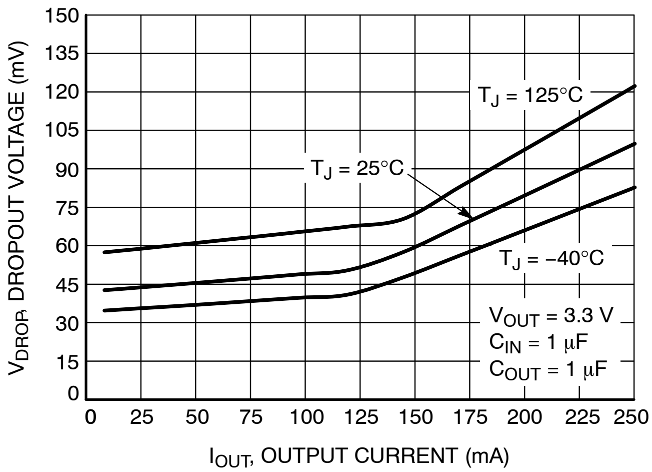


Figure 15. Dropout Voltage vs. Load Current – V_{OUT} = 3.3 V – XDFN4 Package

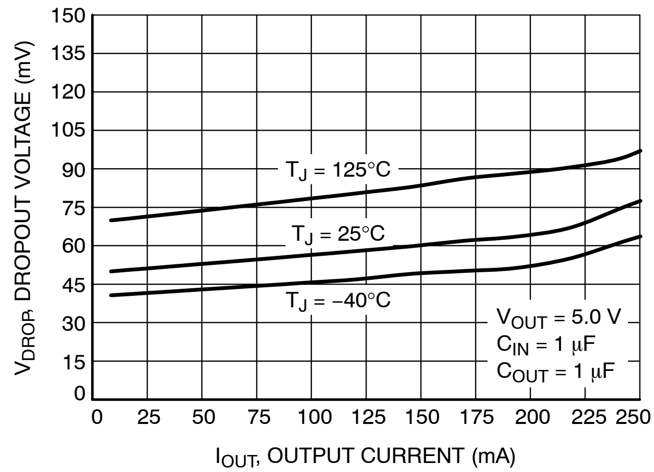


Figure 16. Dropout Voltage vs. Load Current – V_{OUT} = 5.0 V – XDFN4 Package

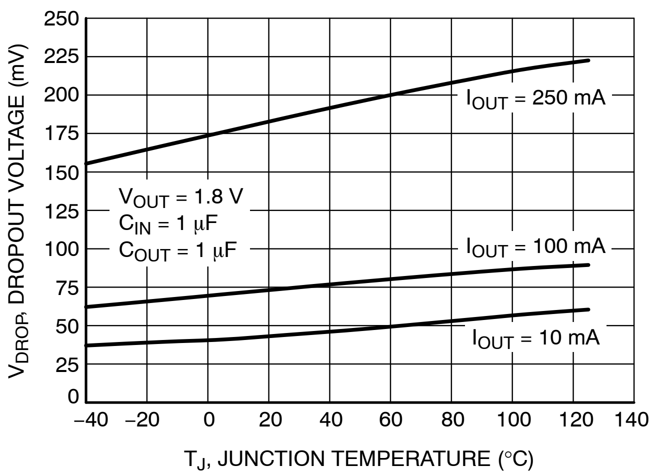


Figure 17. Dropout Voltage vs. Temperature – V_{OUT} = 1.8 V – XDFN4 Package

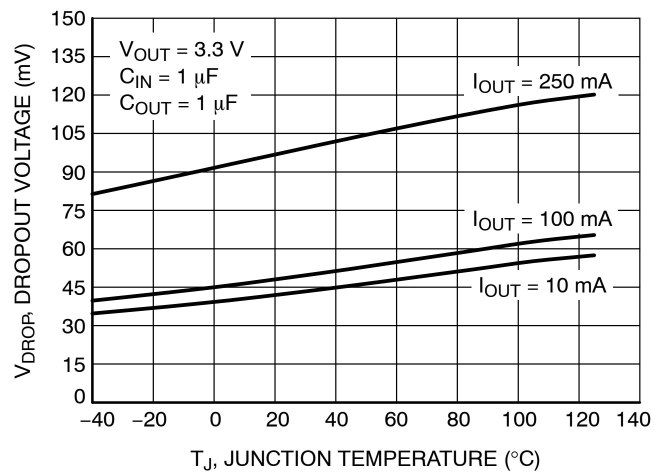


Figure 18. Dropout Voltage vs. Temperature – V_{OUT} = 3.3 V – XDFN4 Package

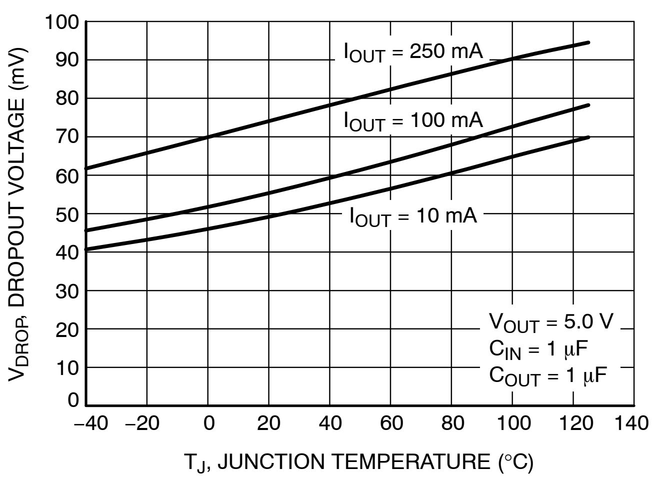


Figure 19. Dropout Voltage vs. Temperature – V_{OUT} = 5.0 V – XDFN4 Package

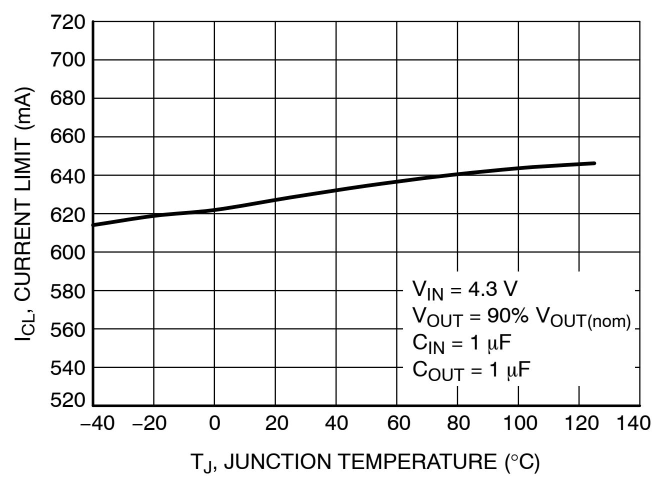


Figure 20. Current Limit vs. Temperature

TYPICAL CHARACTERISTICS

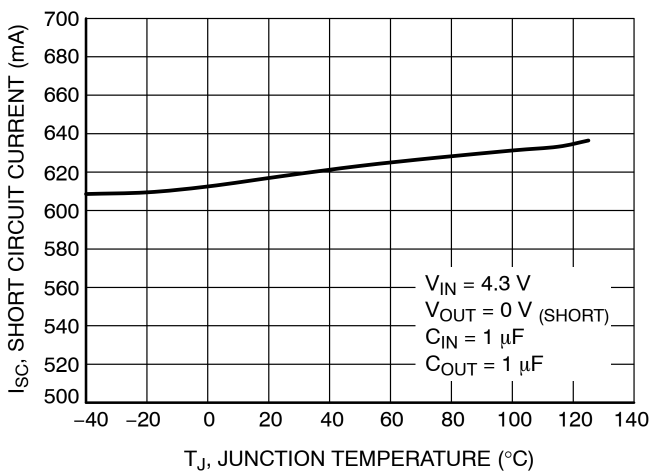


Figure 21. Short Circuit Current vs. Temperature

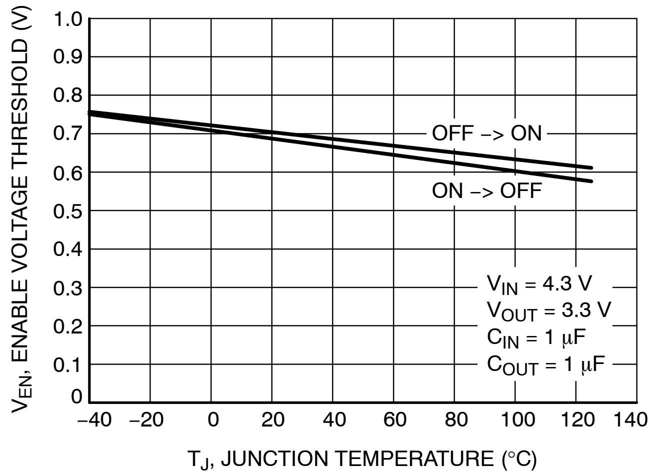


Figure 22. Enable Thresholds Voltage

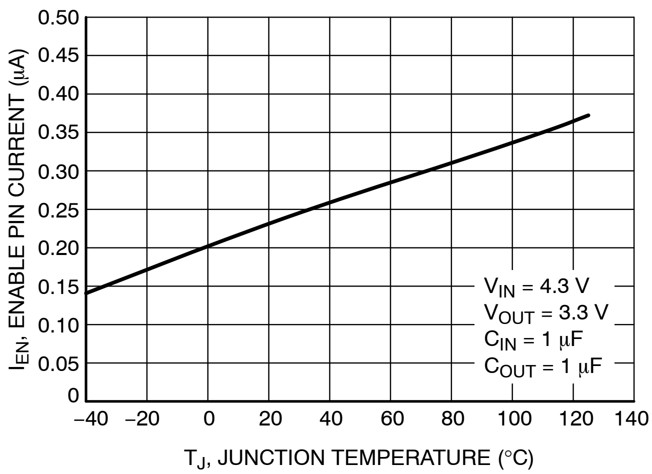


Figure 23. Current to Enable Pin vs. Temperature

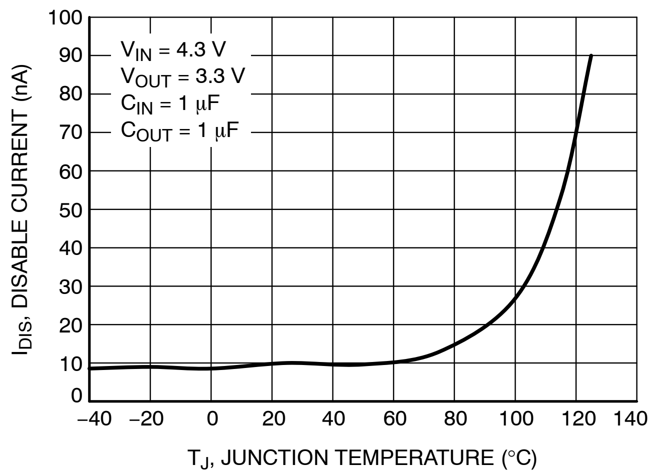


Figure 24. Disable Current vs. Temperature

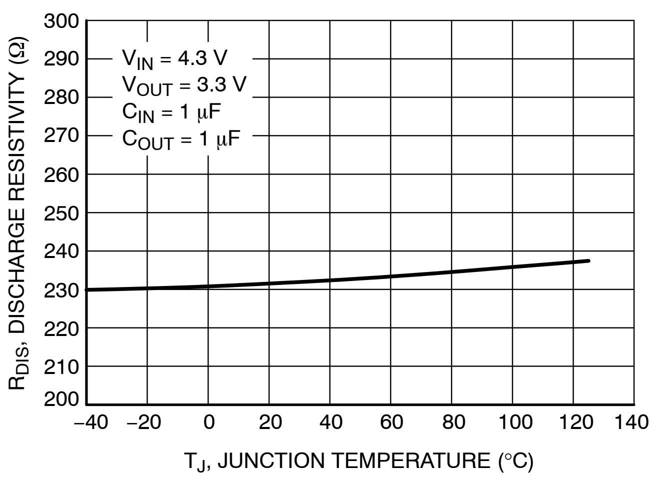


Figure 25. Discharge Resistance vs. Temperature

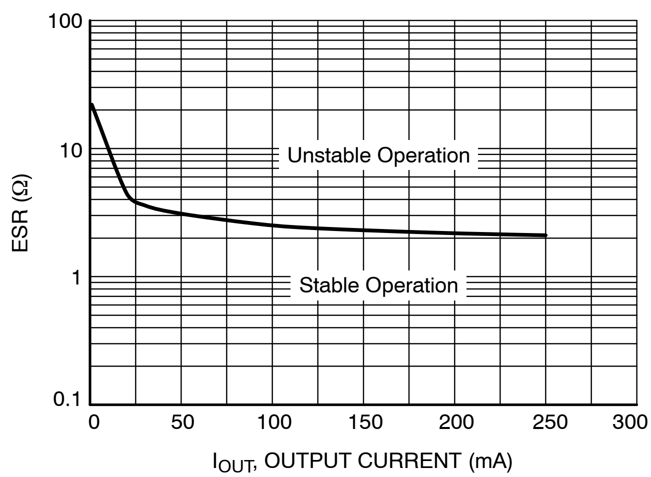
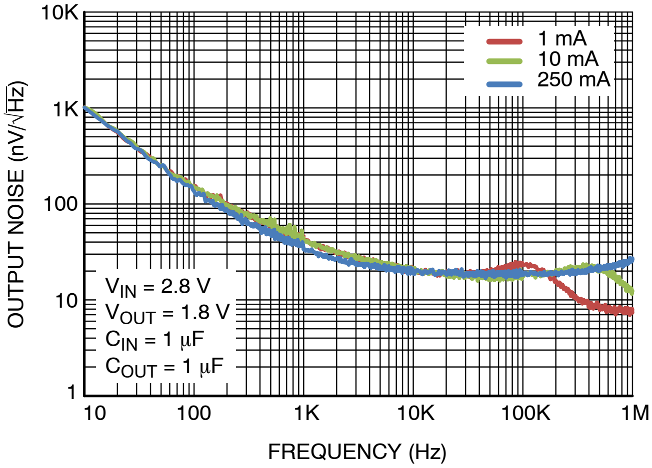


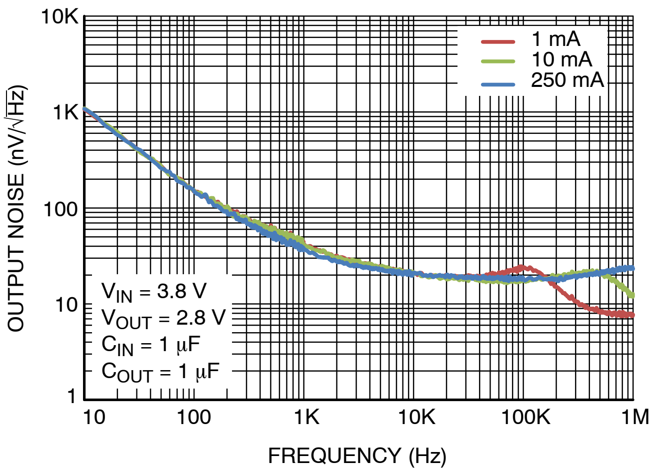
Figure 26. Maximum C_{OUT} ESR Value vs. Load Current

TYPICAL CHARACTERISTICS



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	7.73	6.99
10 mA	7.12	6.26
250 mA	7.11	6.33

Figure 27. Output Voltage Noise Spectral Density – V_{OUT} = 1.8 V



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	7.9	7.07
10 mA	7.19	6.25
250 mA	7.29	6.38

Figure 28. Output Voltage Noise Spectral Density – V_{OUT} = 2.8 V

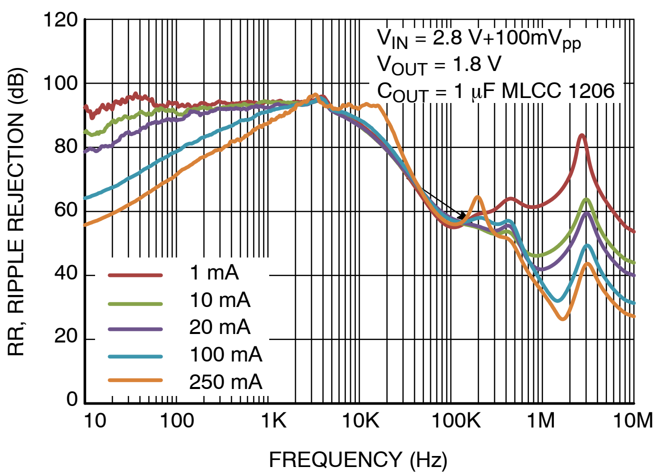


Figure 29. Power Supply Rejection Ratio – V_{OUT} = 1.8 V

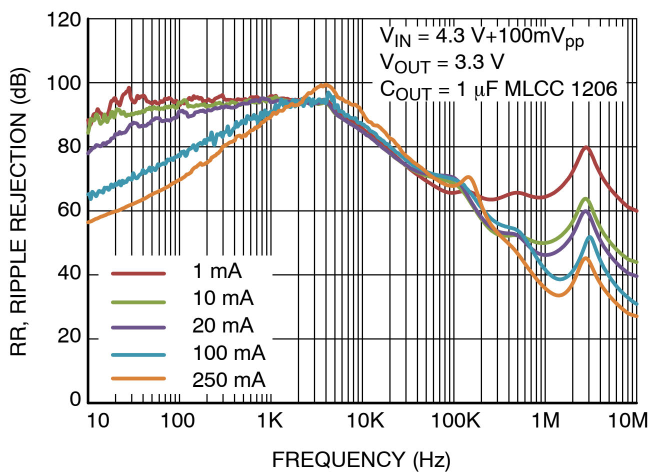


Figure 30. Power Supply Rejection Ratio – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

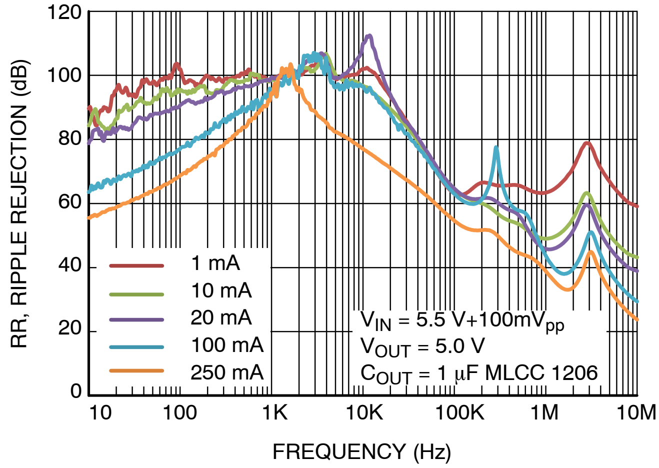


Figure 31. Power Supply Rejection Ratio – V_{OUT} = 5.0 V

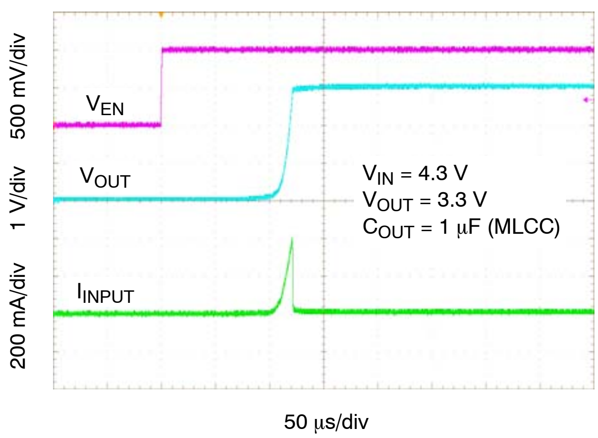


Figure 32. Enable Turn−on Response – C_{OUT} = 1 μF, I_{OUT} = 10 mA

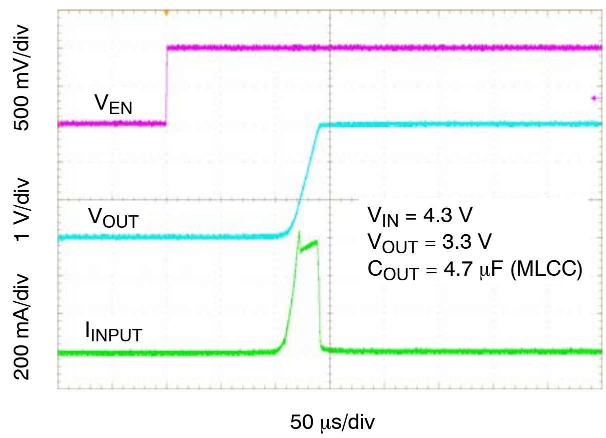


Figure 33. Enable Turn−on Response – C_{OUT} = 4.7 μF, I_{OUT} = 10 mA

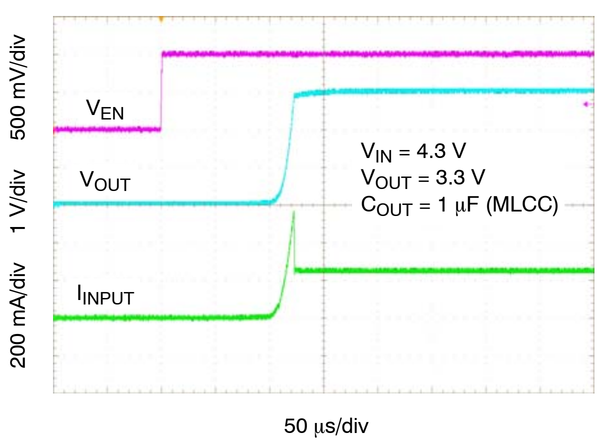


Figure 34. Enable Turn−on Response – C_{OUT} = 1 μF, I_{OUT} = 250 mA

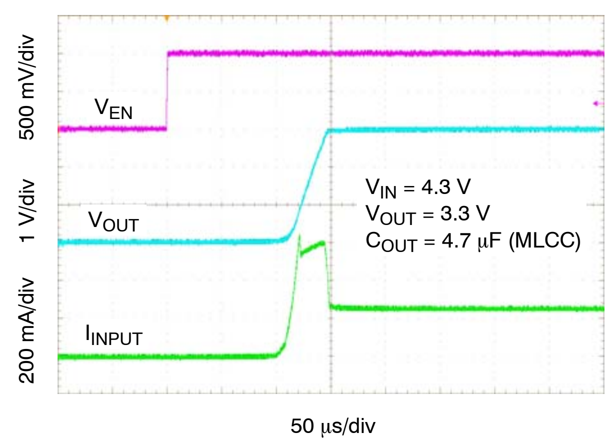


Figure 35. Enable Turn−on Response – C_{OUT} = 4.7 μF, I_{OUT} = 250 mA

TYPICAL CHARACTERISTICS

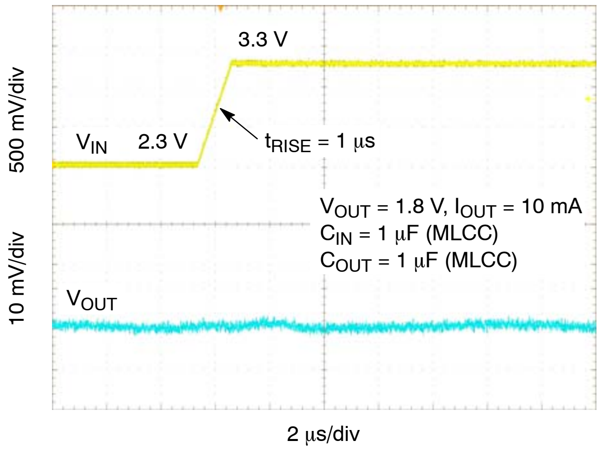


Figure 36. Line Transient Response – I_{OUT} = 10 mA

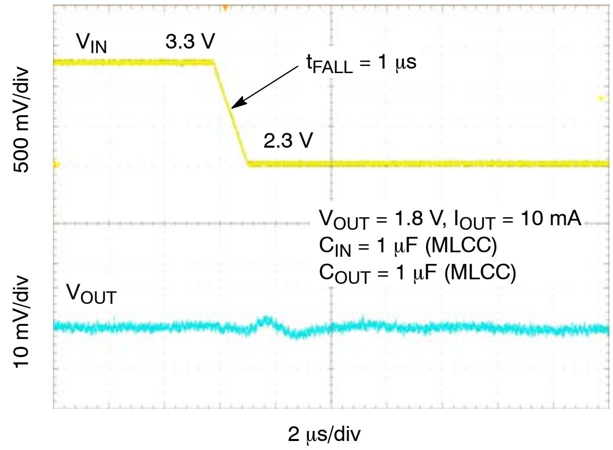


Figure 37. Line Transient Response – I_{OUT} = 10 mA

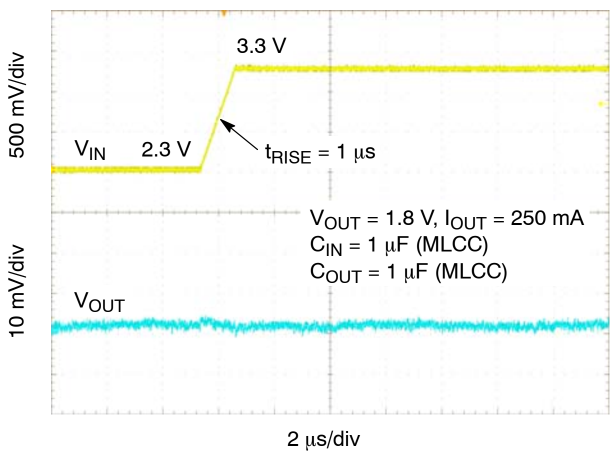


Figure 38. Line Transient Response – I_{OUT} = 250 mA

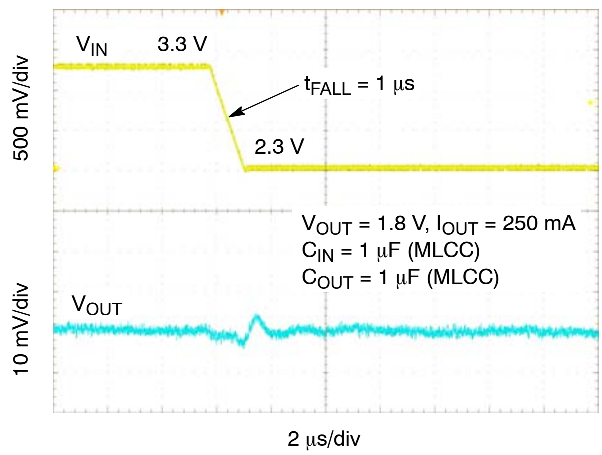


Figure 39. Line Transient Response – I_{OUT} = 250 mA

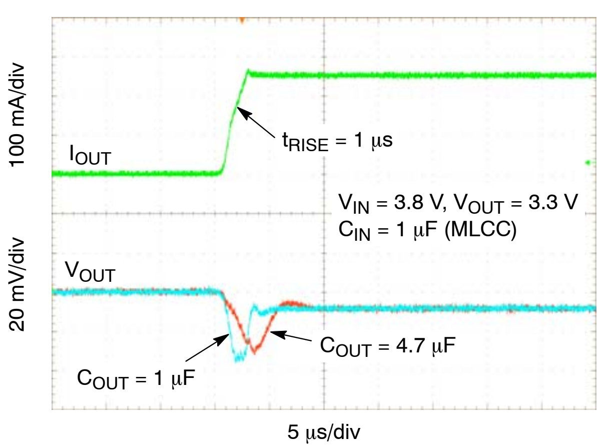


Figure 40. Load Transient Response – 1 mA to 250 mA

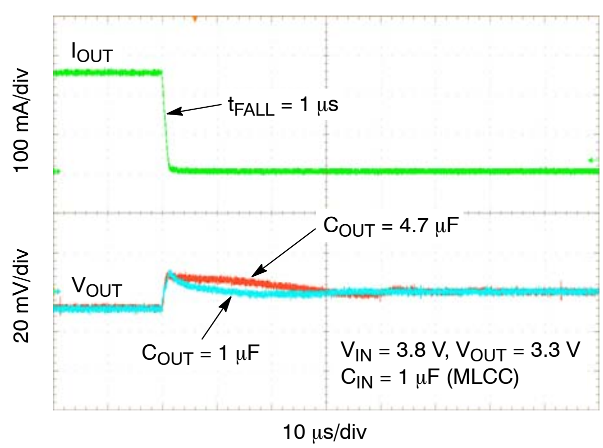


Figure 41. Load Transient Response – 250 mA to 1 mA

TYPICAL CHARACTERISTICS

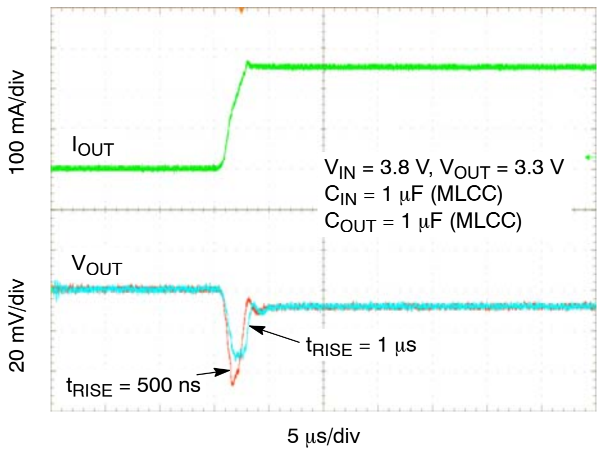


Figure 42. Load Transient Response – 1 mA to 250 mA

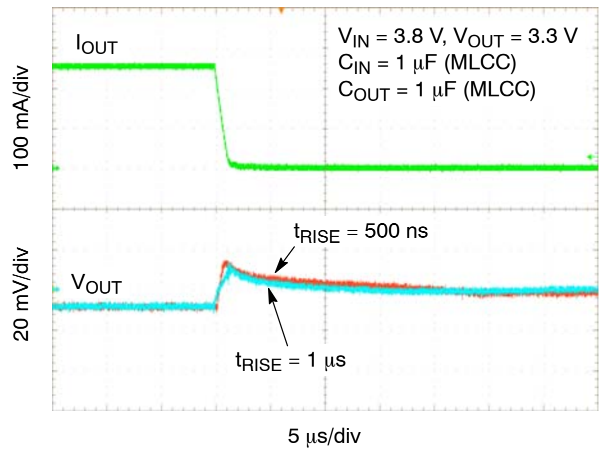


Figure 43. Load Transient Response – 250 mA to 1 mA

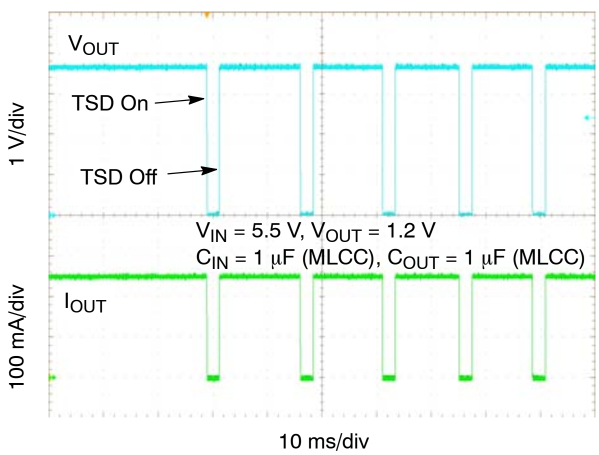


Figure 44. Overheating Protection – TSD

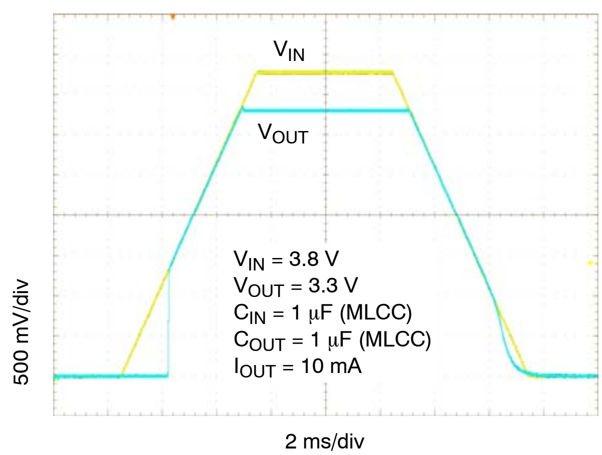


Figure 45. Turn−on/off – Slow Rising V_{IN}

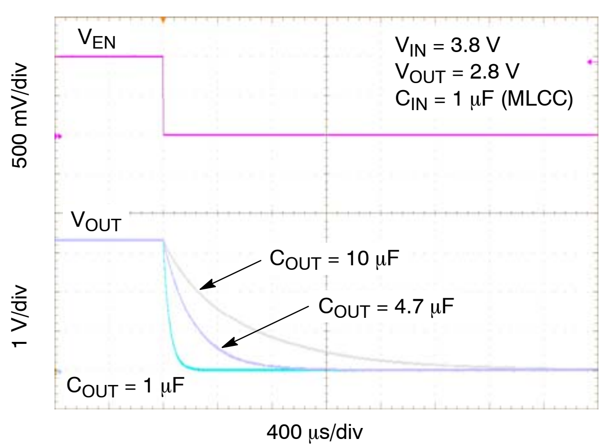


Figure 46. Enable Turn−off – Various Output Capacitors

APPLICATIONS INFORMATION

General

The NCV8163 is an ultra−low noise 250 mA low dropout regulator designed to meet the requirements of RF applications and high performance analog circuits. The NCV8163 device provides very high PSRR and excellent dynamic response. In connection with low quiescent current this device is well suitable for battery powered application such as cell phones, tablets and other. The NCV8163 is fully protected in case of current overload, output short circuit and overheating.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Decoupling (C_{OUT})

The NCV8163 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCV8163 is designed to remain stable with minimum effective capacitance of 0.7 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer Figure 47.

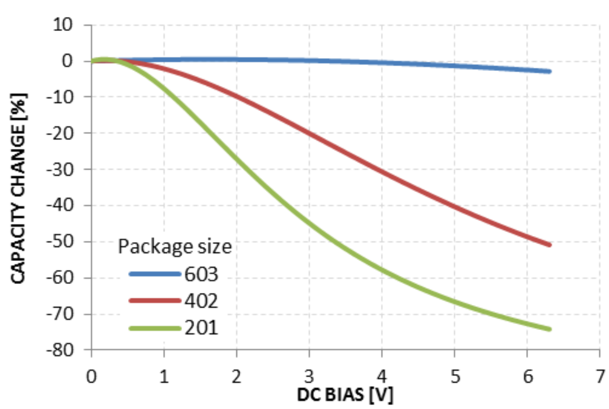


Figure 47. Capacity vs DC Bias Voltage

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 2 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCV8163 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 280 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >1.2 V the device is guaranteed to be enabled. The NCV8163 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 200 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 700 mA. The NCV8163 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 690 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCV8163 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCV8163 can handle is given by:

$$P_{D(MAX)} = \frac{[125°C - T_A]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCV8163 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

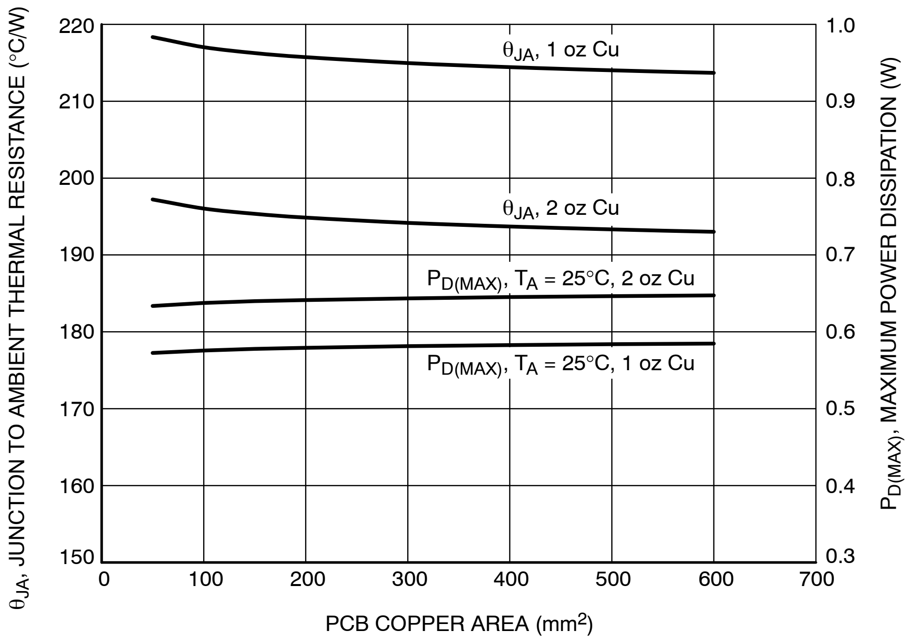


Figure 48. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area − XDFN4

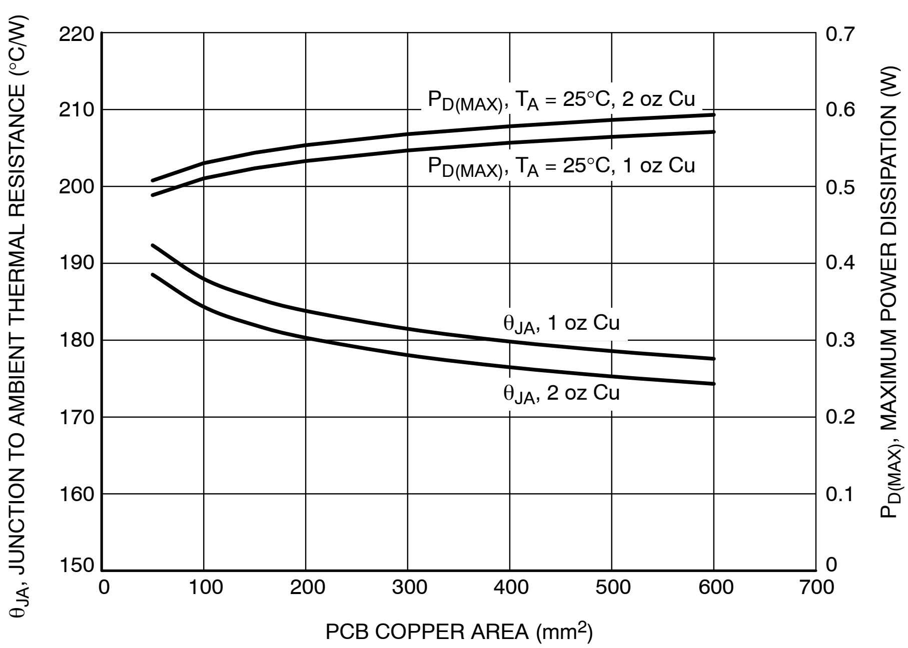


Figure 49. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area − TSOP−5

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCV8163 features very high Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors with appropriate capacity. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad can be tied to the GND pin for improvement power dissipation and lower device temperature.

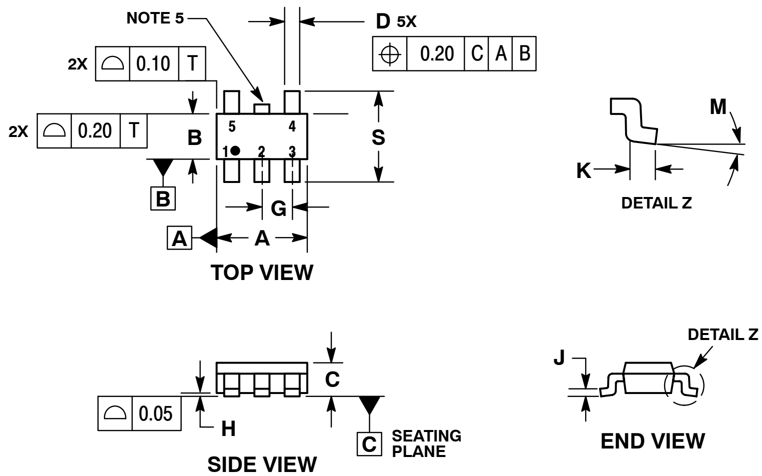
ORDERING INFORMATION

Device	Voltage Option	Marking	Description	Package	Shipping†
NCV8163AMX120TBG	1.2 V	ME	250 mA, Active Discharge	XDFN4 CASE 711AJ (Pb-Free)	3000 / Tape & Reel
NCV8163AMX150TBG	1.5 V	MV			
NCV8163AMX180TBG	1.8 V	MA			
NCV8163AMX250TBG	2.5 V	MU			
NCV8163AMX270TBG	2.7 V	MX			
NCV8163AMX280TBG	2.8 V	MM			
NCV8163AMX300TBG	3.0 V	MJ			
NCV8163AMX330TBG	3.3 V	MK			
NCV8163AMX400TBG	4.0 V	MY			
NCV8163ASN120T1G	1.2 V	MKE	250 mA, Active Discharge	TSOP−5 CASE 483 (Pb-Free)	3000 / Tape & Reel
NCV8163ASN180T1G	1.8 V	KAA			
NCV8163ASN270T1G	2.7 V	KAK			
NCV8163ASN280T1G	2.8 V	KAE			
NCV8163ASN300T1G	3.0 V	KAF			
NCV8163ASN330T1G	3.3 V	KAG			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

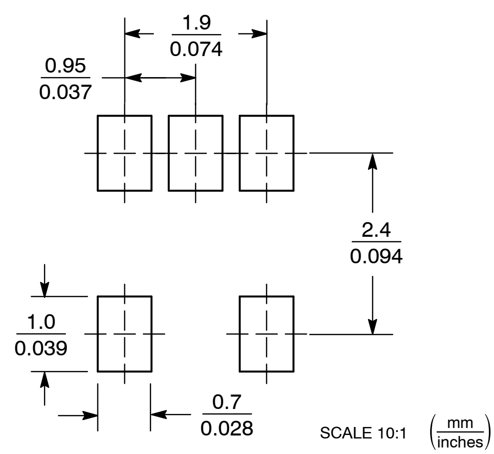
TSOP−5
CASE 483
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

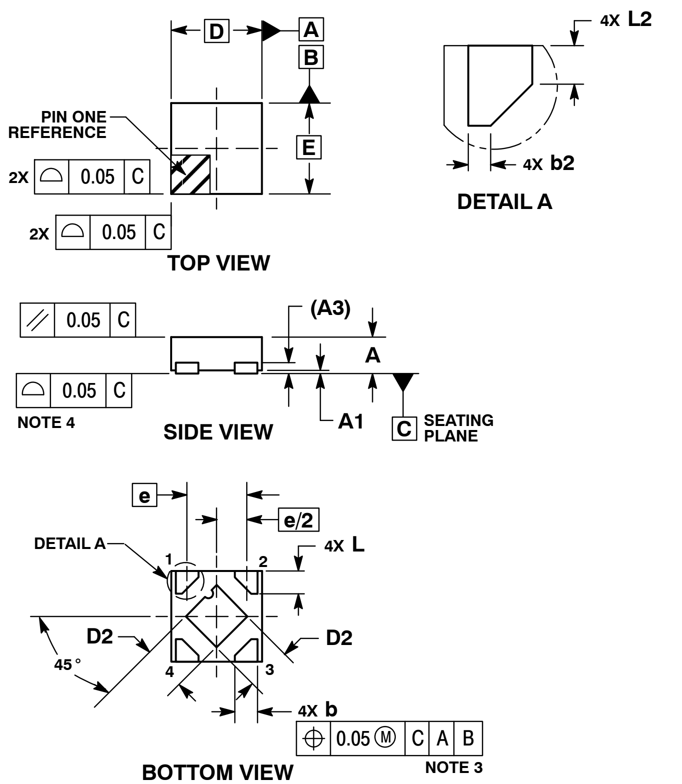
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

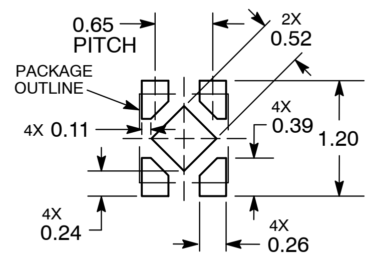
XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.33	0.43
A1	0.00	0.05
A3	0.10 REF	
b	0.15	0.25
b2	0.02	0.12
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.07	0.17

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative