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FAIRCHILD SEMICONDUCTOR

May 2002

NDC7003P

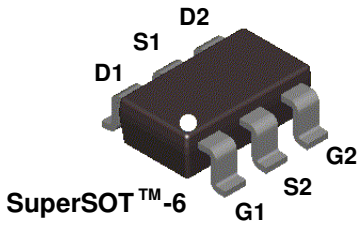
Dual P-Channel PowerTrench® MOSFET

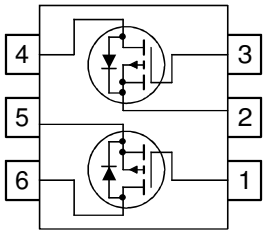
General Description

These dual P-Channel Enhancement Mode Power Field Effect Transistors are produced using Fairchild's proprietary Trench Technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

- –0.34A, –60 V. $R_{DS(ON)}$ = 5 Ω @ V_{GS} = –10 V
  $R_{DS(ON)}$ = 7 Ω @ V_{GS} = –4.5 V
- Low gate charge
- Fast switching speed
- High performance trench technology for low $R_{DS(ON)}$
- SuperSOT™ -6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick)





Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	–0.34	A
	– Pulsed		–1	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.96	W
		(Note 1b)	0.9	
		(Note 1c)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.03P	NDC7003P	7''	8mm	3000 units

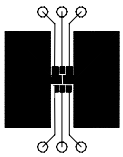
Electrical Characteristics

T_A = 25°C unless otherwise noted

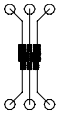
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		–57		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –48 V, V_{GS} = 0 V			–1	μA
I_{GSS}	Gate–Body Leakage,	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–1	–1.9	–3.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		3.2		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –0.34 A V_{GS} = –4.5 V, I_D = –0.25 A V_{GS}= –10 V,I_D = –0.34 A, T_J=125°C		1.2 1.5 1.9	5 7.5 10	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = –10 V V_{DS} = –10 V	–1			A
g_{FS}	Forward Transconductance	V_{DS} = –10 V, I_D = –0.34 A		700		mS
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –25 V, V_{GS} = 0 V, f = 1.0 MHz		66		pF
C_{oss}	Output Capacitance			13		pF
C_{rss}	Reverse Transfer Capacitance			6		pF
R_G	Gate Resistance	V_{GS} = 15mV, f = 1.0 MHz		11.2		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –25 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		3.2	6.4	ns
t_r	Turn–On Rise Time			10	20	ns
$t_{d(off)}$	Turn–Off Delay Time			8	16	ns
t_f	Turn–Off Fall Time			1	2	ns
Q_g	Total Gate Charge	V_{DS} = –25 V, I_D = –0.34 A, V_{GS} = –10 V		1.6	2.2	nC
Q_{gs}	Gate–Source Charge			0.3		nC
Q_{gd}	Gate–Drain Charge			0.3		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–0.34	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –0.34 A(Note 2)		–0.8	–1.4	V

Notes:

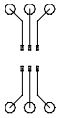
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 130 °C/W when mounted on a 0.125 in^2 pad of 2 oz. copper.



b) 140°C/W when mounted on a .005 in^2 pad of 2 oz copper



c) 180°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics

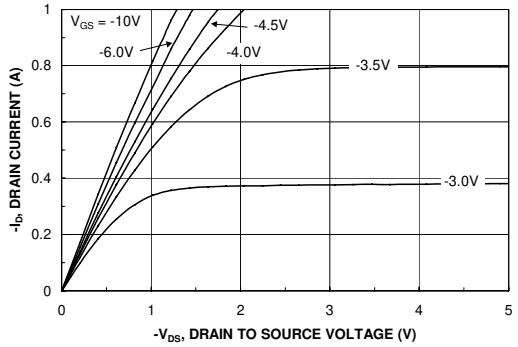


Figure 1. On-Region Characteristics.

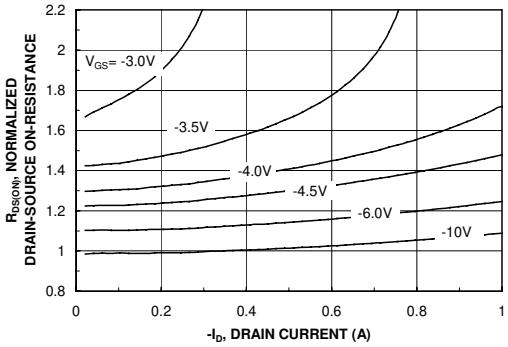


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

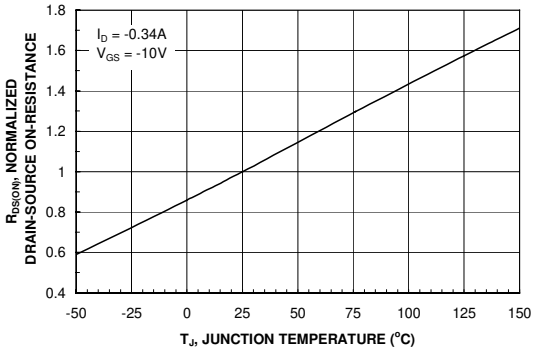


Figure 3. On-Resistance Variation with Temperature.

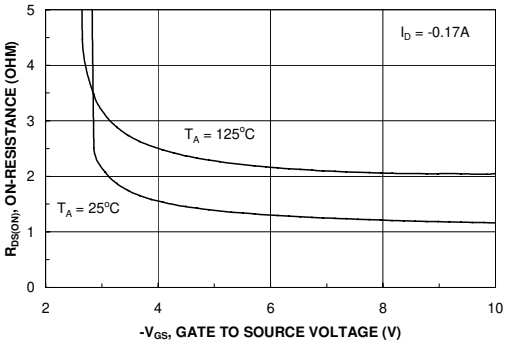


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

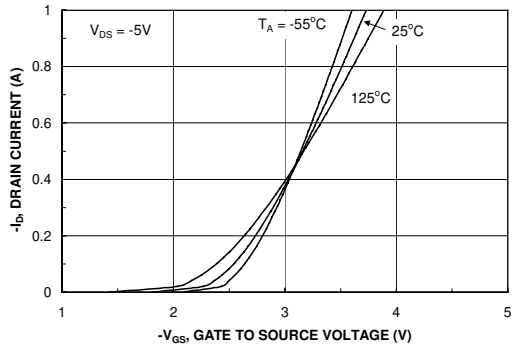


Figure 5. Transfer Characteristics.

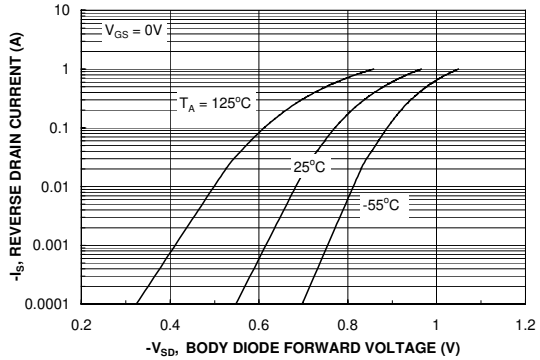


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

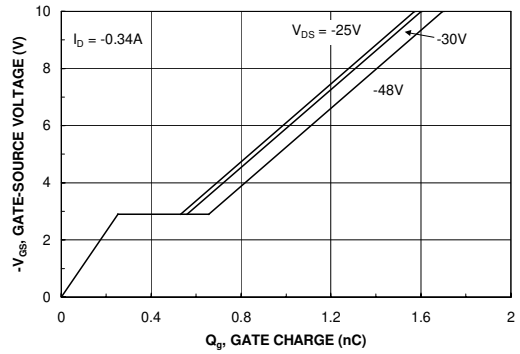


Figure 7. Gate Charge Characteristics.

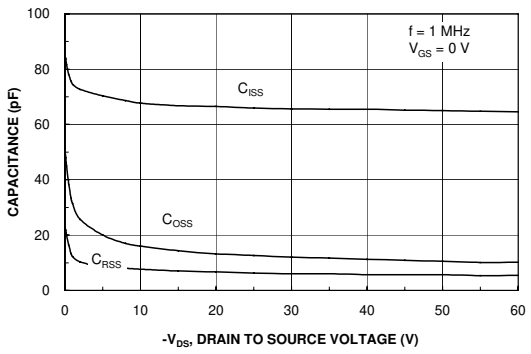


Figure 8. Capacitance Characteristics.

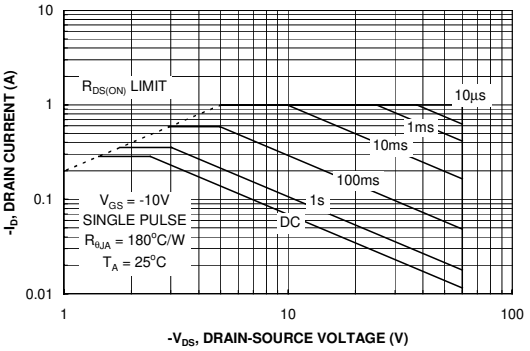


Figure 9. Maximum Safe Operating Area.

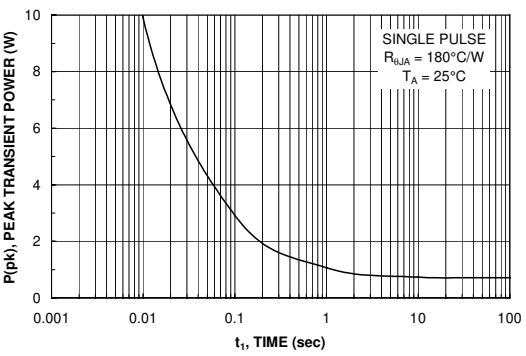


Figure 10. Single Pulse Maximum Power Dissipation.

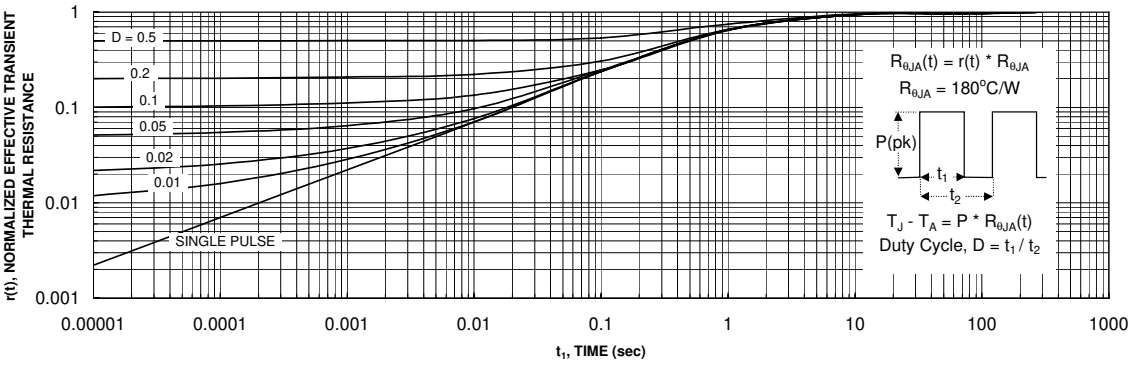


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient themal response will change depending on the circuit board design.

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