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**SERIES:** NDM2Z-25 | **DESCRIPTION:** AUTO COMPENSATED, DIGITAL DC-DC POL CONVERTER

**GENERAL CHARACTERISTICS**

- 4.5~14 V input range
- 0.6~3.3 V programmable output
- voltage tracking
- voltage margining
- active current sharing
- *Snapshot*™ parametric capture
- voltage/current/temperature monitoring
- synchronization and phase spreading
- remote differential voltage sense
- programmable soft start and soft stop
- fault management

**FEATURES**

- pin and function compatible with Architects of Modern Power™ product standards
- compact package, horizontal: 25.7 x 13.8 x 8.2 mm
- compact package, vertical: 26.3 x 7.6 x 15.60 mm
- 25 A output
- high efficiency
- auto compensation
- SMBus interface
- PMBus™ Compatible



MODEL	input voltage	output voltage	output current	output wattage
	(Vdc)	(Vdc)	max (A)	max (W)
NDM2Z-25	4.5~14	0.6~3.3	25	82.5

**PART NUMBER KEY**

**NDM2Z-25 X - X - XXX**

Base Number

Module Orientation and Pin Style:  
 HS = horizontal, surface mount  
 HT = horizontal, through hole mount  
 V = vertical

Pin Configuration:  
 A = Both functions present, 4.0 mm pin length (V)  
 B = Both functions present, 5.5 mm pin length (V)  
 P = Power Good (H)  
 V = Voltage Track (H)

Firmware Configuration:  
 000~ZZZ

Example part number: **NDM2Z-25V-A-001**

vertical module  
 4.0 mm pin length  
 firmware configuration 001

\* HS and HT modules are delivered on tape and reel  
 \* V modules are delivered in trays

## ABSOLUTE MAXIMUM RATINGS

parameter	conditions/description	min	typ	max	units
operating temperature (see thermal consideration section) ( $T_{P1}$ )		-40		125	°C
storage temperature ( $T_S$ )		-40		125	°C
input voltage (see operating information section for input and output voltage relations)( $V_I$ )		-0.3		16	V
logic I/O voltage	CTRL, SA0, SA1, SALERT, SCL, SDA, VSET, SYNC, DDC, PG	-0.3		6.5	V
ground voltage differential	-S, PREF, GND	-0.3		0.3	V
analog pin voltage	$V_{Or}$ , +S, VTRK	-0.3		6.5	V

Notes: Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

## Configuration File

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the default configuration file, unless otherwise specified. The default configuration file is designed to fit most application needs with focus on high efficiency. If different characteristics are required it is possible to change the configuration file to optimize certain performance characteristics. Note that current sharing operation requires changed configuration file.

## PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL

$T_{P1} = -30$  to  $+95$  °C,  $V_I = 4.5$  to  $14$  V,  $V_I > V_O + 1.0$  V

Typical values given at:  $T_{P1} = +25$  °C,  $V_I = 12.0$  V, max  $I_{Or}$ , unless otherwise specified under conditions.

External  $C_{IN} = 470$   $\mu$ F/10 m $\Omega$ ,  $C_{OUT} = 470$   $\mu$ F/10 m $\Omega$ . See Operating Information section for selection of capacitor types.

Sense pins are connected to the output pins.

parameter	conditions/description	min	typ	max	units
input voltage rise time ( $V_I$ )	monotonic			2.4	V/ms
output voltage without pin-strap ( $V_O$ )			1.2		V
output voltage adjustment range ( $V_O$ )		0.60		3.3	V
output voltage adjustment including margining ( $V_O$ )	see note 17	0.54		3.63	V
output voltage set-point resolution ( $V_O$ )			$\pm 0.025$		%FS
output voltage accuracy ( $V_O$ )	including line, load, temp see note 14	-1		1	%
	current sharing operation see note 15	-2		2	%
internal resistance +S/-S to VOUT/GND ( $V_O$ )			47		$\Omega$
line regulation ( $V_O$ )	$V_O = 0.6$ V		2		mV
	$V_O = 1.0$ V		2		mV
	$V_O = 1.8$ V		2		mV
	$V_O = 3.3$ V		3		mV
load regulation ( $V_O$ ) $I_O = 0 \sim 100\%$	$V_O = 0.6$ V		2		mV
	$V_O = 1.0$ V		2		mV
	$V_O = 1.8$ V		2		mV
	$V_O = 3.3$ V		3		mV
output ripple & noise ( $V_{osc}$ ) $C_O = 470$ $\mu$ F (minimum external capacitance) see note 11	$V_O = 0.6$ V		20		mVp-p
	$V_O = 1.0$ V		30		mVp-p
	$V_O = 1.8$ V		40		mVp-p
	$V_O = 3.3$ V		60		mVp-p

**PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL (CONTINUED)**

parameter	conditions/description	min	typ	max	units
output current ( $I_o$ )		0		25	A
static input current at max $I_o$ ( $I_s$ )	$V_o = 0.6 V$		1.58		A
	$V_o = 1.0 V$		2.43		A
	$V_o = 1.8 V$		4.13		A
	$V_o = 3.3 V$		7.32		A
current limit threshold ( $I_{lim}$ )		27		37.5	A
short circuit current ( $I_{SC}$ )	RMS, hiccup mode, see note 3	$V_o = 0.6 V$	8		A
		$V_o = 1.0 V$	6		A
		$V_o = 1.8 V$	5		A
		$V_o = 3.3 V$	4		A
efficiency ( $\eta$ )	50% of max $I_o$	$V_o = 0.6 V$	84.4		%
		$V_o = 1.0 V$	89.4		%
		$V_o = 1.8 V$	93.1		%
		$V_o = 3.3 V$	95.2		%
	max $I_o$	$V_o = 0.6 V$	79.2		%
		$V_o = 1.0 V$	85.7		%
		$V_o = 1.8 V$	90.8		%
		$V_o = 3.3 V$	93.9		%
power dissipation at max $I_o$ ( $P_d$ )	$V_o = 0.6 V$		3.93		W
	$V_o = 1.0 V$		4.17		W
	$V_o = 1.8 V$		4.55		W
	$V_o = 3.3 V$		5.34		W
input idling power (no load) ( $P_{ii}$ )	default configuration: continues conduction mode, CCM	$V_o = 0.6 V$	0.56		W
		$V_o = 1.0 V$	0.57		W
		$V_o = 1.8 V$	0.67		W
		$V_o = 3.3 V$	0.92		W
input standby power ( $P_{CTRL}$ )	turned off with CTRL-pin		170		mW
internal input capacitance ( $C_i$ )			70		$\mu F$
internal output capacitance ( $C_o$ )			200		$\mu F$
total external output capacitance ( $C_{OUT}$ )	see note 9	300		15,000	$\mu F$
ESR range of capacitors (per single capacitor) ( $C_{OUT}$ )	see note 9	5		30	m $\Omega$
load transient peak voltage deviation (L to H/H to L) load step 25-75-25% of max $I_o$ ( $V_{tr1}$ )	default configuration di/dt = 2 A/ $\mu s$ $C_o = 470 \mu F$ (minimum external capacitance) see note 12	$V_o = 0.6 V$	95		mV
		$V_o = 1.0 V$	105		mV
		$V_o = 1.8 V$	115		mV
		$V_o = 3.3 V$	168		mV
load transient recovery time note 5 (L to H/H to L) load step 25-75-25% of max $I_o$ ( $t_{tr1}$ )	default configuration di/dt = 2 A/ $\mu s$ $C_o = 470 \mu F$ (minimum external capacitance) see note 12	$V_o = 0.6 V$	74		$\mu s$
		$V_o = 1.0 V$	85		$\mu s$
		$V_o = 1.8 V$	122		$\mu s$
		$V_o = 3.3 V$	140		$\mu s$
switching frequency ( $f_s$ )			320		kHz
switching frequency range ( $f_s$ )	PMBus configurable		200-640		kHz
switching frequency set-point accuracy ( $f_s$ )		-5		5	%
control circuit PWM duty cycle		5		95	%
minimum sync pulse width		150			ns
input clock frequency drift tolerance	external clock source	-13		13	%

**PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL (CONTINUED)**

parameter	conditions/description	min	typ	max	units
input under voltage lockout, UVLO	UVLO threshold		3.85		V
	UVLO threshold range	PMBus configurable	3.85-14		V
	set point accuracy		-150	150	mV
	UVLO hysteresis		0.35		V
	UVLO hysteresis range	PMBus configurable	0-10.15		V
	delay			2.5	µs
	fault response	see note 3			automatic restart, 70 ms
input over voltage protection, IOVP	IOVP threshold		16		V
	IOVP threshold range	PMBus configurable	4.2-16		V
	set point accuracy		-150	150	mV
	IOVP hysteresis		1		V
	IOVP hysteresis range	PMBus configurable	0-11.8		V
	delay			2.5	µs
	fault response	see note 3			automatic restart, 70 ms
power good, PG, see note 2	PG threshold		90		%V <sub>o</sub>
	PG hysteresis		5		%V <sub>o</sub>
	PG delay		direct after DLC		ms
	PG delay range	PMBus configurable	0-500		s
output voltage over/under voltage protection, OVP/UVP	UVP threshold		85		%V <sub>o</sub>
	UVP threshold range	PMBus configurable	0-100		%V <sub>o</sub>
	UVP hysteresis		5		%V <sub>o</sub>
	OVP threshold		115		%V <sub>o</sub>
	OVP threshold range	PMBus configurable	100-115		%V <sub>o</sub>
	UVP/OVP response time			25	µs
	UVP/OVP response time range	PMBus configurable		5-60	µs
fault response	see note 3			automatic restart, 70 ms	
over current protection, OCP	OCP threshold		32		A
	OCP threshold range	PMBus configurable	0-32		A
	protection delay	see note 4	32		T <sub>sw</sub>
	protection delay range	PMBus configurable	1-32		T <sub>sw</sub>
	fault response	see note 3			automatic restart, 70 ms
over temperature protection, OTP at P2 see note 8	OTP threshold		120		°C
	OTP threshold range	PMBus configurable	-40	125	°C
	OTP hysteresis		25		°C
	OTP hysteresis range	PMBus configurable	0-165		°C
	fault response	see note 3			automatic restart, 240 ms

**PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL (CONTINUED)**

parameter	conditions/description	min	typ	max	units
logic input low threshold( $V_{IL}$ )	SYNC, SA0, SA1, SCL, SDA, DDC, CTRL, VSET			0.8	V
logic input high threshold ( $V_{IH}$ )		2			V
logic input low sink current( $I_{TL}$ )	CTRL			0.6	mA
logic output low signal level ( $V_{OL}$ )	SYNC, SCL, SDA, SALERT, DDC, PG			0.4	V
logic output high signal level ( $V_{OH}$ )		2.25			V
logic output low sink current ( $I_{OL}$ )				4	mA
logic output high source current ( $I_{OH}$ )				2	mA
setup time, SMBus( $t_{SET}$ )	see note 1	300			ns
hold time, SMBus( $t_{hold}$ )	see note 1	250			ns
bus free time, SMBus( $t_{free}$ )	see note 1	2			ms
internal capacitance on logic pins ( $C_p$ )			10		pF
initialization time	see note 10		40		ms
	delay duration	see note 16	10		ms
output voltage delay time see note 6	delay duration range	PMBus configurable	5-500,000		ms
	delay accuracy turn-on		-0.25/+4		ms
	delay accuracy turn-off		-0.25/+4		ms
output voltage ramp time see note 13	ramp duration		10		ms
	ramp duration range	PMBus configurable	0-200		ms
	ramp time accuracy	current sharing operation	100		$\mu$ s
VTRK input bias current	$V_{VTRK} = 5.5$ V		110	200	$\mu$ A
	100% tracking, see note 7	-100		100	mV
VTRK tracking ramp accuracy ( $V_o - V_{VTRK}$ )	current sharing operation 2 phases, 100% tracking $V_o = 1.0$ V, 10 ms ramp		$\pm 100$		mV
	100% Tracking	-1		1	%
VTRK regulation accuracy ( $V_o - V_{VTRK}$ )	current sharing operation 100% Tracking	-2		2	%
	steady state operation		Max 2 x READ_IOUT monitoring accuracy		
current difference between products in a current sharing group	ramp-up		2		A
	number of products in a current sharing group			7	
monitoring accuracy	READ_VIN vs $V_I$		3		%
	READ_VOUT vs $V_o$		1		%
	READ_IOUT vs $I_o$	$I_o = 0-20$ A, $T_{p1} = 0$ to $+95$ °C $V_I = 4.5-14$ V, $V_o = 1.0$ V		$\pm 1.7$	A
	READ_IOUT vs $I_o$	$I_o = 0-20$ A, $T_{p1} = 0$ to $+95$ °C $V_I = 4.5-14$ V, $V_o = 0.6-3.3$ V		$\pm 3$	A

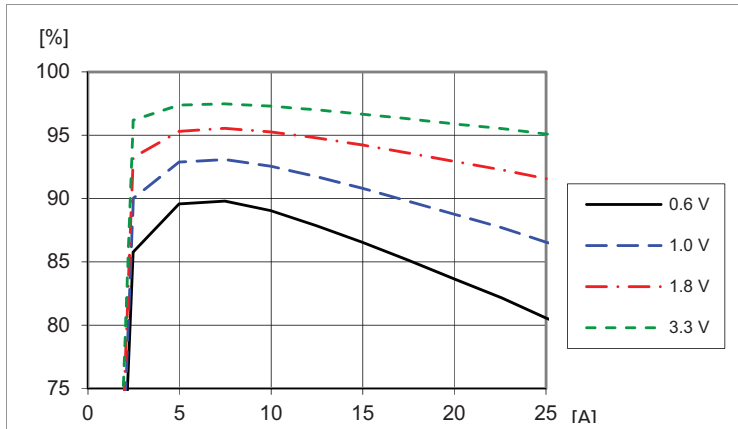
## PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL (CONTINUED)

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- Notes:
- 1: See section I<sup>2</sup>C/SMBus Setup and Hold Times – Definitions.
  - 2: Monitorable over PMBus Interface.
  - 3: Automatic restart ~70 or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart.
  - 4:  $T_{sw}$  is the switching period.
  - 5: Within +/-3% of VO
  - 6: See section Soft-start Power Up.
  - 7: Tracking functionality is designed to follow a VTRK signal with slew rate < 2.4 V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.
  - 8: See section Over Temperature Protection (OTP).
  - 9: See section External Capacitors.
  - 10: See section Initialization Procedure.
  - 11: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.
  - 12: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.
  - 13: Time for reaching 100% of nominal Vout.
  - 14: For Vout < 1.0 V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus.
  - 15: Accuracy here means deviation from ideal output voltage level given by configured droop and actual load. Includes line, load and temperature variations.
  - 16: For current sharing the Output Voltage Delay Time must be reconfigured to minimum 15 ms.
  - 17: For steady state operation above 1.05 x 3.3 V, please contact your local CUI sales representative.

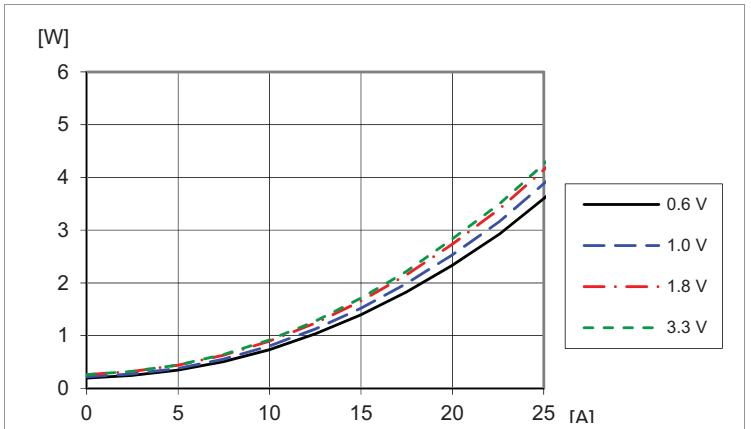
## TYPICAL CHARACTERISTICS, HORIZONTAL (CONTINUED)

Efficiency vs. Output Current,  $V_I = 5\text{ V}$



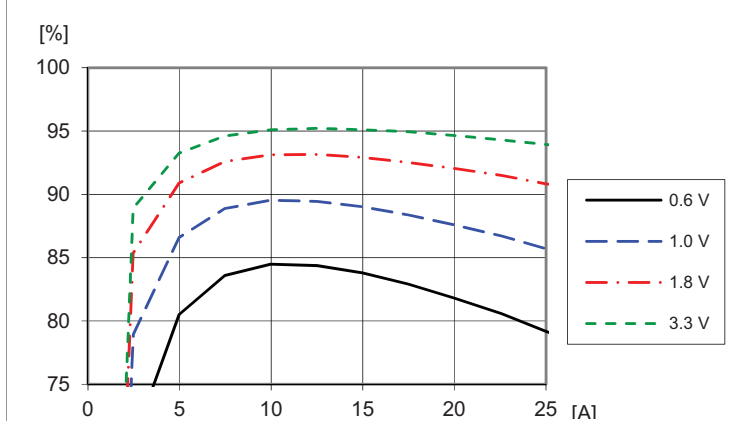
Efficiency vs. load current and output voltage:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 5\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .

Power Dissipation vs. Output Current,  $V_I = 5\text{ V}$



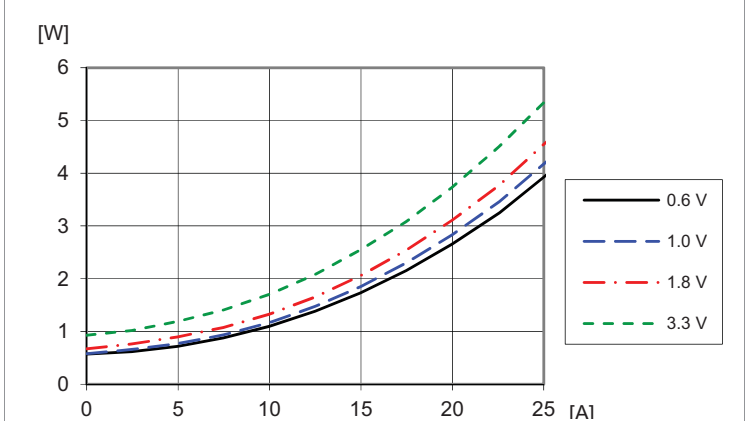
Dissipated power vs. load current and output voltage:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 5\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .

Efficiency vs. Output Current,  $V_I = 12\text{ V}$



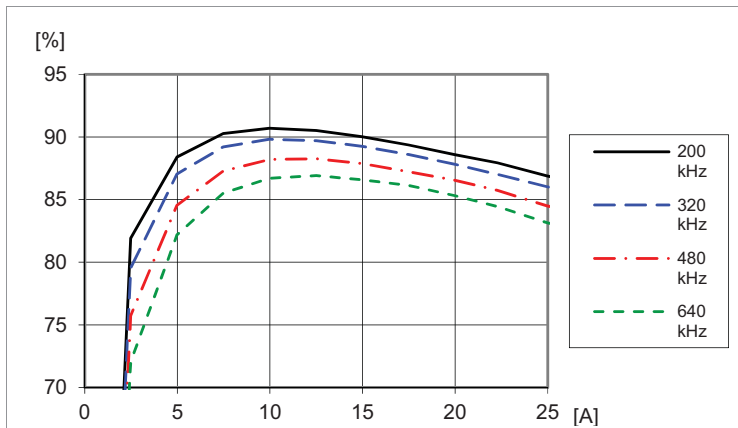
Efficiency vs. load current and output voltage at  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .

Power Dissipation vs. Output Current,  $V_I = 12\text{ V}$



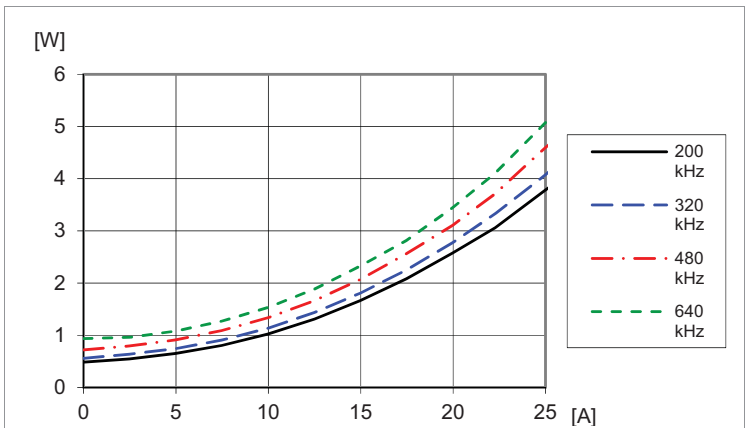
Dissipated power vs. load current and output voltage:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .  
 Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency

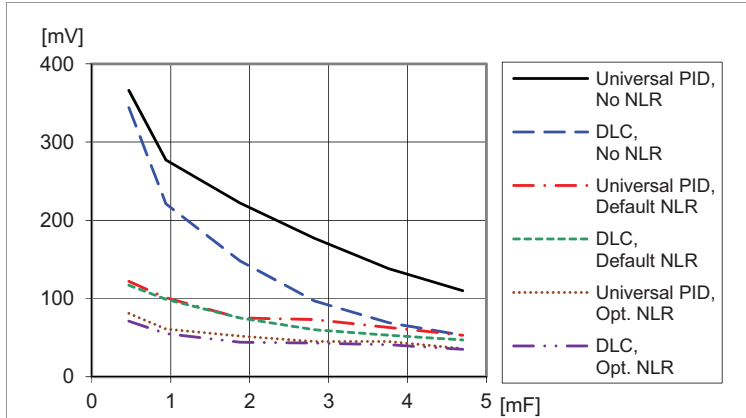


Dissipated power vs. load current and switch frequency at  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .  
 Default configuration except changed frequency



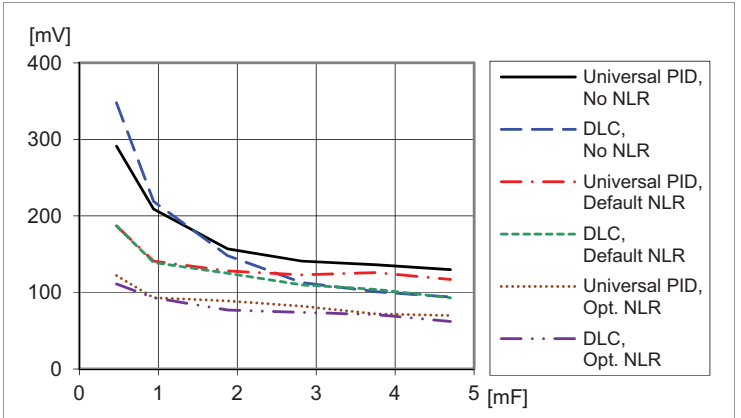
## TYPICAL CHARACTERISTICS, HORIZONTAL (CONTINUED)

Load Transient vs. External Capacitance,  $V_O = 1.0\text{ V}$



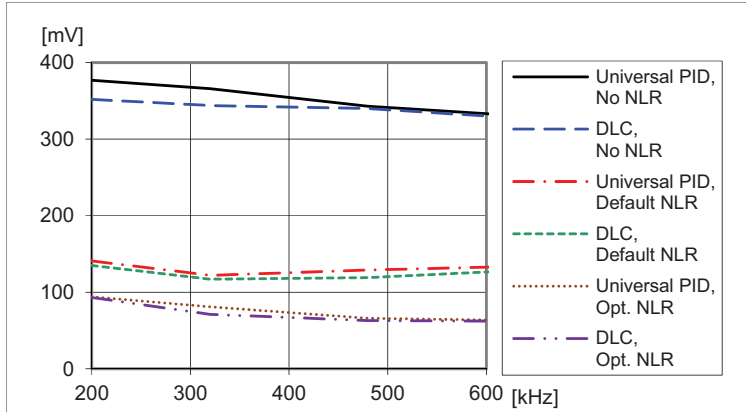
Load transient peak voltage deviation vs. external capacitance. Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with  $470\ \mu\text{F}/10\ \text{m}\Omega$ .  $T_{P1} = +25\ ^\circ\text{C}$ ,  $V_I = 12\ \text{V}$ ,  $V_O = 1.0\ \text{V}$ ,  $f_{sw} = 320\ \text{kHz}$ ,  $di/dt = 2\ \text{A}/\mu\text{s}$

Load Transient vs. External Capacitance,  $V_O = 3.3\ \text{V}$



Load transient peak voltage deviation vs. external capacitance. Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with  $470\ \mu\text{F}/10\ \text{m}\Omega$ .  $T_{P1} = +25\ ^\circ\text{C}$ ,  $V_I = 12\ \text{V}$ ,  $V_O = 3.3\ \text{V}$ ,  $f_{sw} = 320\ \text{kHz}$ ,  $di/dt = 2\ \text{A}/\mu\text{s}$

Load transient vs. Switch Frequency

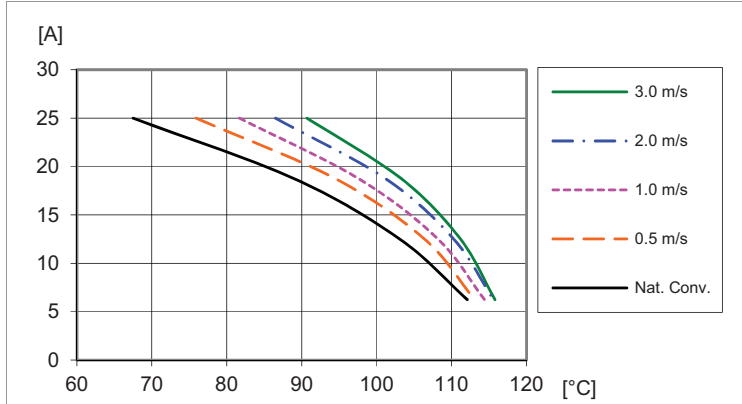


Load transient peak voltage deviation vs. frequency. Step-change (6.25-18.75-6.25 A).  $T_{P1} = +25\ ^\circ\text{C}$ .  $V_I = 12\ \text{V}$ ,  $V_O = 1.0\ \text{V}$ ,  $C_O = 470\ \mu\text{F}/10\ \text{m}\Omega$

Note: For Universal PID, see section Dynamic Loop Compensation (DLC).

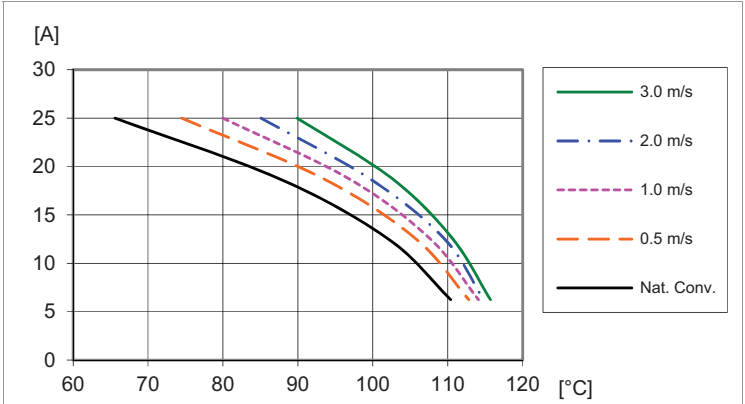
## TYPICAL CHARACTERISTICS, HORIZONTAL (CONTINUED)

### Output Current Derating, $V_O = 0.6 V$



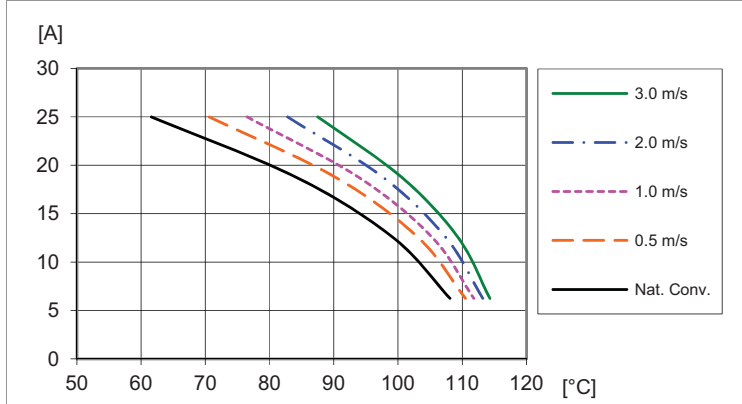
Available load current vs. ambient air temperature and airflow at  $V_O = 0.6 V$ ,  $V_I = 12 V$ . See Thermal Consideration section.

### Output Current Derating, $V_O = 1.0 V$



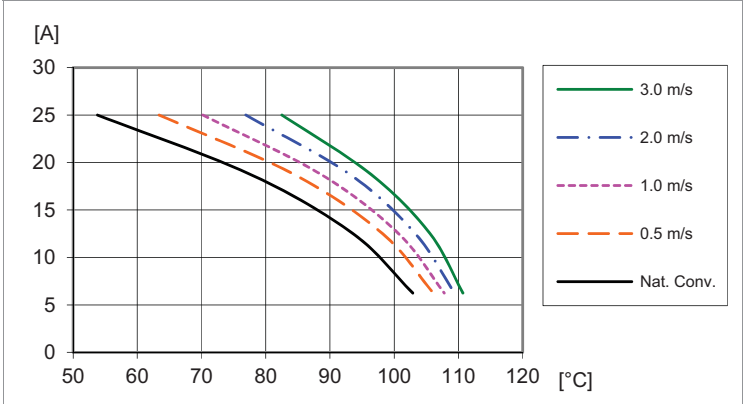
Available load current vs. ambient air temperature and airflow at  $V_O = 1.0 V$ ,  $V_I = 12 V$ . See Thermal Consideration section.

### Output Current Derating, $V_O = 1.8 V$



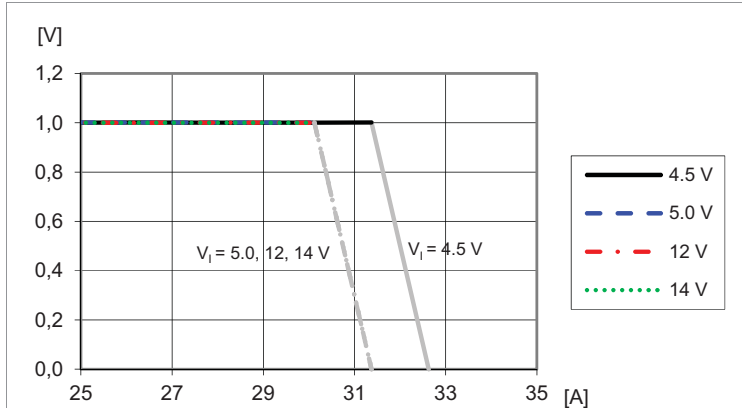
Available load current vs. ambient air temperature and airflow at  $V_O = 1.8 V$ ,  $V_I = 12 V$ . See Thermal Consideration section.

### Output Current Derating, $V_O = 3.3 V$



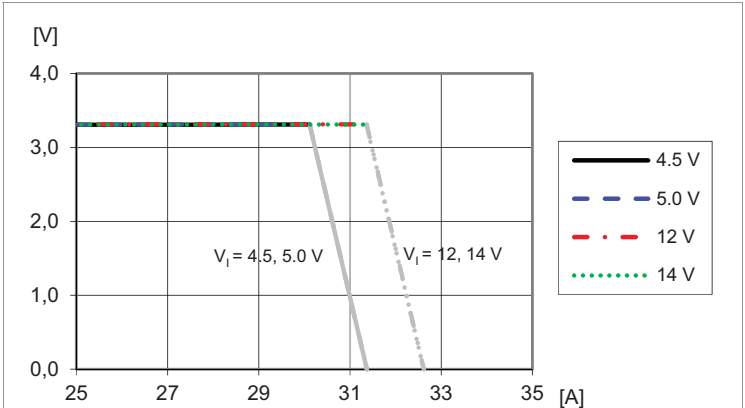
Available load current vs. ambient air temperature and airflow at  $V_O = 3.3 V$ ,  $V_I = 12 V$ . See Thermal Consideration section.

### Current Limit Characteristics, $V_O = 1.0 V$



Output voltage vs. load current at  $T_{P1} = +25 ^\circ C$ ,  $V_O = 1.0 V$ . Note: Output enters hiccup mode at current limit.

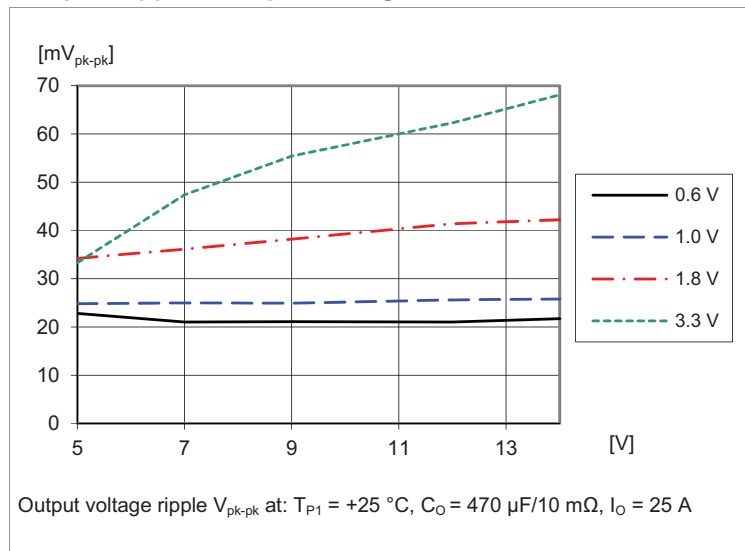
### Current Limit Characteristics, $V_O = 3.3 V$



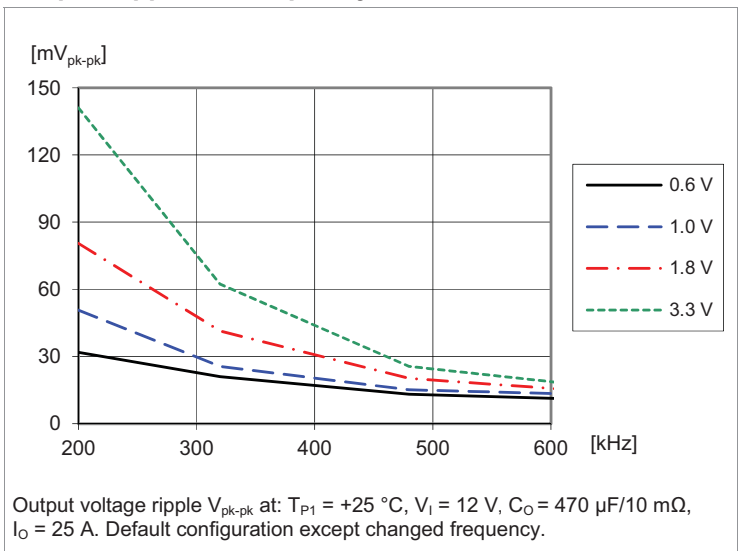
Output voltage vs. load current at  $T_{P1} = +25 ^\circ C$ ,  $V_O = 3.3 V$ . Note: Output enters hiccup mode at current limit.

## TYPICAL CHARACTERISTICS, HORIZONTAL (CONTINUED)

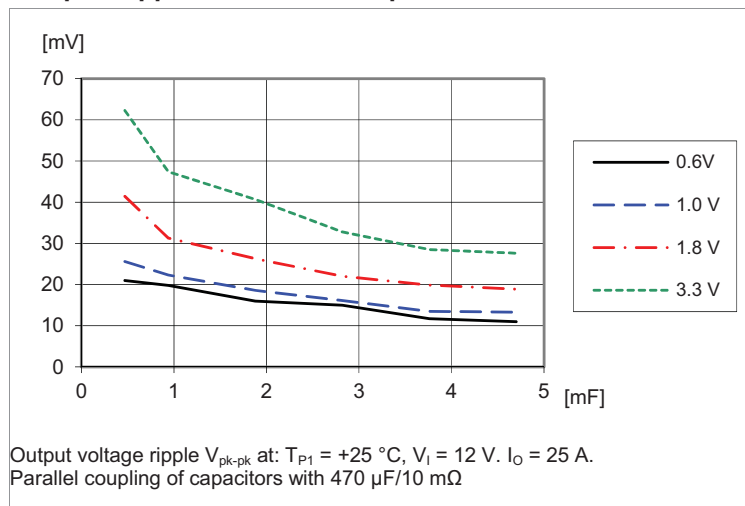
### Output Ripple vs. Input Voltage



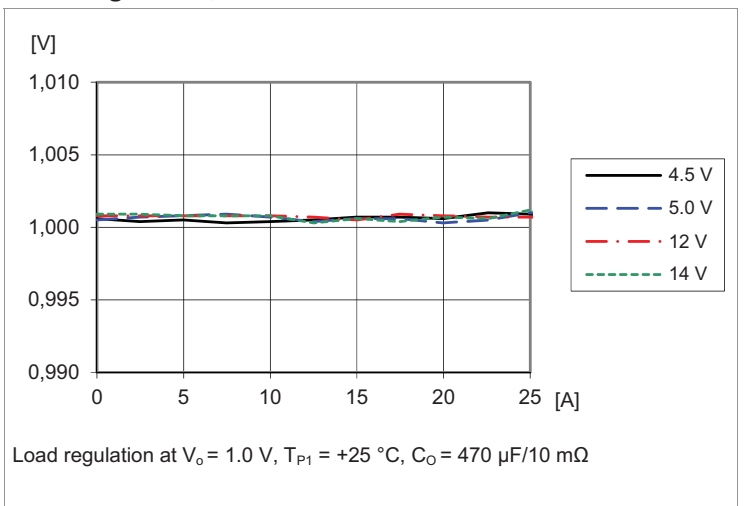
### Output Ripple vs. Frequency



### Output Ripple vs. External Capacitance

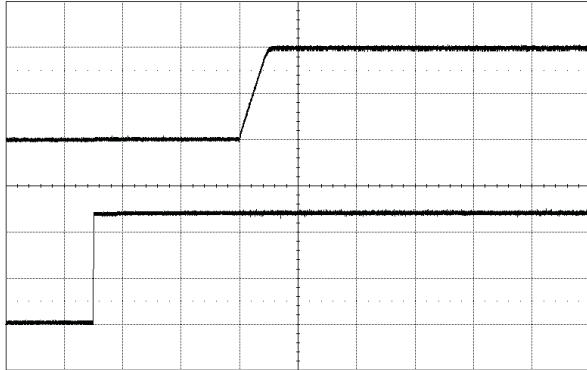


### Load regulation, $V_O = 1.0\text{ V}$



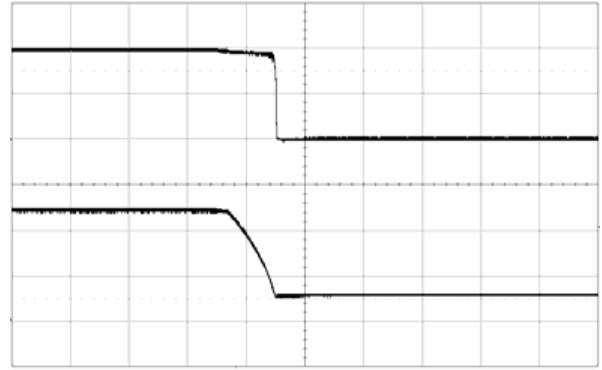
## TYPICAL CHARACTERISTICS, HORIZONTAL (CONTINUED)

### Start-up by input source



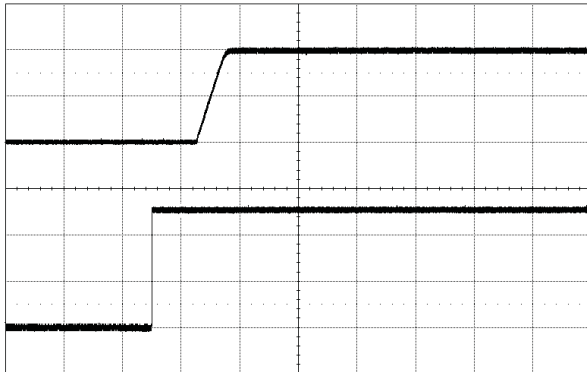
Start-up enabled by connecting  $V_I$  at:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$   
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ ,  $I_O = 25\text{ A}$   
 Top trace: output voltage (0.5 V/div.).  
 Bottom trace: input voltage (5 V/div.).  
 Time scale: (20 ms/div.).

### Shut-down by input source



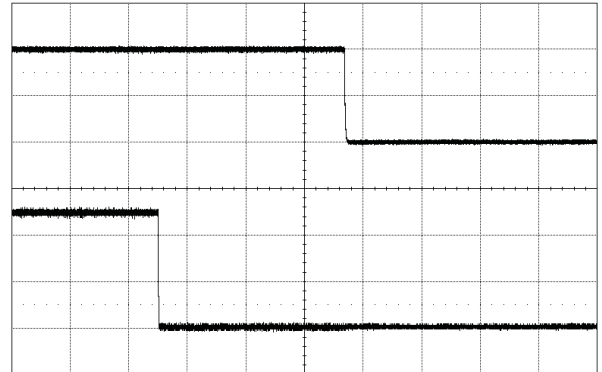
Shut-down enabled by disconnecting  $V_I$  at:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$   
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ ,  $I_O = 25\text{ A}$   
 Top trace: output voltage (0.5 V/div.).  
 Bottom trace: input voltage (5 V/div.).  
 Time scale: (2 ms/div.).

### Start-up by CTRL signal



Start-up by enabling CTRL signal at:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$   
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ ,  $I_O = 25\text{ A}$   
 Top trace: output voltage (0.5 V/div.).  
 Bottom trace: CTRL signal (2 V/div.).  
 Time scale: (20 ms/div.).

### Shut-down by CTRL signal



Shut-down enabled by disconnecting  $V_I$  at:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$   
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ ,  $I_O = 25\text{ A}$   
 Top trace: output voltage (0.5 V/div.).  
 Bottom trace: CTRL signal (2 V/div.).  
 Time scale: (2 ms/div.).

**PRODUCT ELECTRICAL SPECIFICATION, VERTICAL**

$T_{p1} = -30$  to  $+95$  °C,  $V_I = 4.5$  to  $14$  V,  $V_I > V_O + 1.0$  V

Typical values given at:  $T_{p1} = +25$  °C,  $V_I = 12.0$  V, max  $I_O$ , unless otherwise specified under conditions.

External  $C_{IN} = 470$   $\mu$ F/10 m $\Omega$ ,  $C_{OUT} = 470$   $\mu$ F/10 m $\Omega$ . See Operating Information section for selection of capacitor types.

Sense pins are connected to the output pins.

parameter	conditions/description	min	typ	max	units
input voltage rise time ( $V_I$ )	monotonic			2.4	V/ms
output voltage without pin-strap ( $V_O$ )			1.2		V
output voltage adjustment range ( $V_O$ )		0.60		3.3	V
output voltage adjustment including margining ( $V_O$ )	see note 17	0.54		3.63	V
output voltage set-point resolution ( $V_O$ )			$\pm 0.025$		%FS
output voltage accuracy ( $V_O$ )	including line, load, temp see note 14	-1		1	%
	current sharing operation see note 15	-2		2	%
internal resistance +S/-S to VOUT/GND ( $V_O$ )			47		$\Omega$
line regulation ( $V_O$ )	$V_O = 0.6$ V		2		mV
	$V_O = 1.0$ V		2		mV
	$V_O = 1.8$ V		2		mV
	$V_O = 3.3$ V		3		mV
load regulation ( $V_O$ ) $I_O = 0 \sim 100\%$	$V_O = 0.6$ V		2		mV
	$V_O = 1.0$ V		2		mV
	$V_O = 1.8$ V		2		mV
	$V_O = 3.3$ V		3		mV
output ripple & noise ( $V_{oac}$ ) $C_O = 470$ $\mu$ F (minimum external capacitance) see note 11	$V_O = 0.6$ V		20		mVp-p
	$V_O = 1.0$ V		30		mVp-p
	$V_O = 1.8$ V		40		mVp-p
	$V_O = 3.3$ V		60		mVp-p
output current ( $I_O$ )		0		20	A
static input current at max $I_O$ ( $I_S$ )	$V_O = 0.6$ V		1.61		A
	$V_O = 1.0$ V		2.46		A
	$V_O = 1.8$ V		4.17		A
	$V_O = 3.3$ V		7.35		A
current limit threshold ( $I_{lim}$ )		27		37.5	A
short circuit current ( $I_{SC}$ )	RMS, hiccup mode, see note 3	$V_O = 0.6$ V	8		A
		$V_O = 1.0$ V	6		A
		$V_O = 1.8$ V	5		A
		$V_O = 3.3$ V	4		A
efficiency ( $\eta$ )	50% of max $I_O$	$V_O = 0.6$ V	83.6		%
		$V_O = 1.0$ V	89		%
		$V_O = 1.8$ V	92.8		%
		$V_O = 3.3$ V	95.1		%
	max $I_O$	$V_O = 0.6$ V	77.4		%
		$V_O = 1.0$ V	84.6		%
		$V_O = 1.8$ V	90		%
		$V_O = 3.3$ V	93.5		%
power dissipation at max $I_O$ ( $P_d$ )	$V_O = 0.6$ V		4.37		W
	$V_O = 1.0$ V		4.54		W
	$V_O = 1.8$ V		5.01		W
	$V_O = 3.3$ V		5.77		W
input idling power (no load) ( $P_{ii}$ )	default configuration: continues conduction mode, CCM	$V_O = 0.6$ V	0.56		W
		$V_O = 1.0$ V	0.57		W
		$V_O = 1.8$ V	0.67		W
		$V_O = 3.3$ V	0.92		W

**PRODUCT ELECTRICAL SPECIFICATION, VERTICAL (CONTINUED)**

parameter	conditions/description	min	typ	max	units
input standby power ( $P_{CTRL}$ )	turned off with CTRL-pin default configuration: monitoring enabled, precise timing enabled		170		mW
internal input capacitance ( $C_i$ )			70		$\mu$ F
internal output capacitance ( $C_o$ )			200		$\mu$ F
total external output capacitance ( $C_{OUT}$ )	see note 9	300		15,000	$\mu$ F
ESR range of capacitors (per single capacitor) ( $C_{OUT}$ )	see note 9	5		30	m $\Omega$
load transient peak voltage deviation (L to H/H to L) load step 25-75-25% of max $I_o(V_{tr1})$	default configuration di/dt = 2 A/ $\mu$ s $C_o$ = 470 $\mu$ F (minimum external capacitance) see note 12	$V_o$ = 0.6 V $V_o$ = 1.0 V $V_o$ = 1.8 V $V_o$ = 3.3 V	115 122 143 174		mV mV mV mV
load transient recovery time note 5 (L to H/H to L) load step 25-75-25% of max $I_o(t_{tr1})$	default configuration di/dt = 2 A/ $\mu$ s $C_o$ = 470 $\mu$ F (minimum external capacitance) see note 12	$V_o$ = 0.6 V $V_o$ = 1.0 V $V_o$ = 1.8 V $V_o$ = 3.3 V	60 65 115 130		$\mu$ s $\mu$ s $\mu$ s $\mu$ s
switching frequency ( $f_s$ )			320		kHz
switching frequency range ( $f_s$ )	PMBus configurable		200-640		kHz
switching frequency set-point accuracy ( $f_s$ )		-5		5	%
control circuit PWM duty cycle		5		95	%
minimum sync pulse width		150			ns
input clock frequency drift tolerance	external clock source	-13		13	%
input under voltage lockout, UVLO	UVLO threshold		3.85		V
	UVLO threshold range	PMBus configurable	3.85-14		V
	set point accuracy		-150	150	mV
	UVLO hysteresis		0.35		V
	UVLO hysteresis range	PMBus configurable	0-10.15		V
	delay		2.5		$\mu$ s
	fault response	see note 3		automatic restart, 70 ms	
input over voltage protection, IOVP	IOVP threshold		16		V
	IOVP threshold range	PMBus configurable	4.2-16		V
	set point accuracy		-150	150	mV
	IOVP hysteresis		1		V
	IOVP hysteresis range	PMBus configurable	0-11.8		V
	delay		2.5		$\mu$ s
	fault response	see note 3		automatic restart, 70 ms	
power good, PG, see note 2	PG threshold		90		% $V_o$
	PG hysteresis		5		% $V_o$
	PG delay		direct after DLC		ms
	PG delay range	PMBus configurable	0-500		s

**PRODUCT ELECTRICAL SPECIFICATION, VERTICAL (CONTINUED)**

parameter	conditions/description	min	typ	max	units
output voltage over/under voltage protection, OVP/UV	UVP threshold		85		%V <sub>o</sub>
	UVP threshold range	PMBus configurable	0-100		%V <sub>o</sub>
	UVP hysteresis		5		%V <sub>o</sub>
	OVP threshold		115		%V <sub>o</sub>
	OVP threshold range	PMBus configurable	100-115		%V <sub>o</sub>
	UVP/OVP response time		25		μs
	UVP/OVP response time range	PMBus configurable	5-60		μs
	fault response	see note 3			
over current protection, OCP	OCP threshold		32		A
	OCP threshold range	PMBus configurable	0-32		A
	protection delay	see note 4	32		T <sub>sw</sub>
	protection delay range	PMBus configurable	1-32		T <sub>sw</sub>
	fault response	see note 3			
over temperature protection, OTP at P2 see note 8	OTP threshold		120		°C
	OTP threshold range	PMBus configurable	-40	125	°C
	OTP hysteresis		25		°C
	OTP hysteresis range	PMBus configurable	0-165		°C
	fault response	see note 3			
logic input low threshold(V <sub>IL</sub> )	SYNC, SA0, SA1, SCL, SDA, DDC, CTRL, VSET			0.8	V
logic input high threshold (V <sub>IH</sub> )		2			V
logic input low sink current(I <sub>IL</sub> )	CTRL			0.6	mA
logic output low signal level (V <sub>OL</sub> )	SYNC, SCL, SDA, SALERT, DDC, PG			0.4	V
logic output high signal level (V <sub>OH</sub> )		2.25			V
logic output low sink current (I <sub>OL</sub> )				4	mA
logic output high source current (I <sub>OH</sub> )				2	mA
setup time, SMBus(t <sub>SET</sub> )		see note 1	300		
hold time, SMBus(t <sub>hold</sub> )	see note 1	250			ns
bus free time, SMBus(t <sub>free</sub> )	see note 1	2			ms
internal capacitance on logic pins (C <sub>p</sub> )			10		pF
initialization time	see note 10		40		ms
output voltage delay time see note 6	delay duration	see note 16	10		ms
	delay duration range	PMBus configurable	5-500,000		ms
	delay accuracy turn-on		-0.25/+4		ms
	delay accuracy turn-off		-0.25/+4		ms
output voltage ramp time see note 13	ramp duration		10		ms
	ramp duration range	PMBus configurable	0-200		ms
			100		μs
	ramp time accuracy	current sharing operation	20		%

**PRODUCT ELECTRICAL SPECIFICATION, VERTICAL (CONTINUED)**

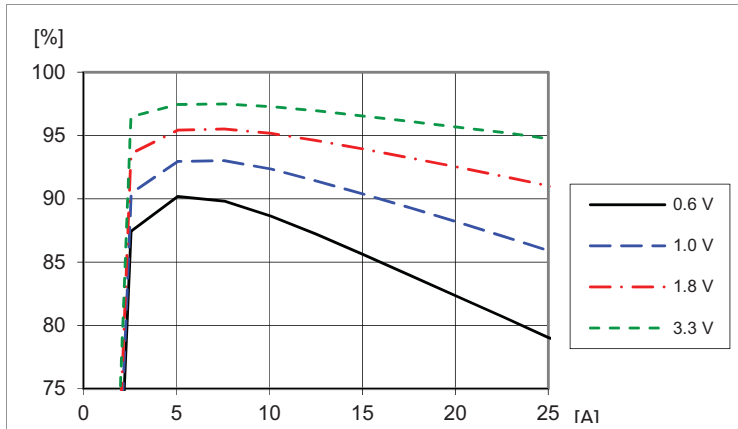
parameter	conditions/description	min	typ	max	units
VTRK input bias current	$V_{VTRK} = 5.5\text{ V}$		110	200	$\mu\text{A}$
VTRK tracking ramp accuracy ( $V_o - V_{VTRK}$ )	100% tracking, see note 7	-100		100	mV
	current sharing operation 2 phases, 100% tracking $V_o = 1.0\text{ V}$ , 10 ms ramp		$\pm 100$		mV
VTRK regulation accuracy ( $V_o - V_{VTRK}$ )	100% Tracking	-1		1	%
	current sharing operation 100% Tracking	-2		2	%
current difference between products in a current sharing group	steady state operation	Max 2 x READ_IOUT monitoring accuracy			
	ramp-up		2		A
number of products in a current sharing group				7	
	READ_VIN vs $V_I$		3		%
	READ_VOUT vs $V_o$		1		%
monitoring accuracy	READ_IOUT vs $I_o$	$I_o = 0-20\text{ A}$ , $T_{P1} = 0\text{ to }+95\text{ }^\circ\text{C}$ $V_I = 4.5-14\text{ V}$ , $V_o = 1.0\text{ V}$	$\pm 1.7$		A
	READ_IOUT vs $I_o$	$I_o = 0-20\text{ A}$ , $T_{P1} = 0\text{ to }+95\text{ }^\circ\text{C}$ $V_I = 4.5-14\text{ V}$ , $V_o = 0.6-3.3\text{ V}$	$\pm 3$		A

- Notes:
- 1: See section I<sup>2</sup>C/SMBus Setup and Hold Times – Definitions.
  - 2: Monitorable over PMBus Interface.
  - 3: Automatic restart ~70 or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart.
  - 4:  $T_{sw}$  is the switching period.
  - 5: Within +/-3% of VO
  - 6: See section Soft-start Power Up.
  - 7: Tracking functionality is designed to follow a VTRK signal with slew rate < 2.4 V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.
  - 8: See section Over Temperature Protection (OTP).
  - 9: See section External Capacitors.
  - 10: See section Initialization Procedure.
  - 11: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.
  - 12: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.
  - 13: Time for reaching 100% of nominal Vout.
  - 14: For Vout < 1.0 V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus.
  - 15: Accuracy here means deviation from ideal output voltage level given by configured droop and actual load. Includes line, load and temperature variations.
  - 16: For current sharing the Output Voltage Delay Time must be reconfigured to minimum 15 ms.
  - 17: For steady state operation above 1.05 x 3.3 V, please contact your local CUI sales representative.



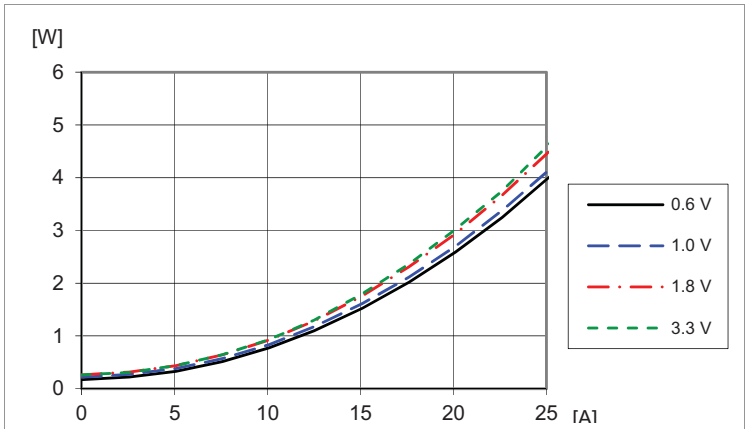
## TYPICAL CHARACTERISTICS, VERTICAL (CONTINUED)

Efficiency vs. Output Current,  $V_I = 5\text{ V}$



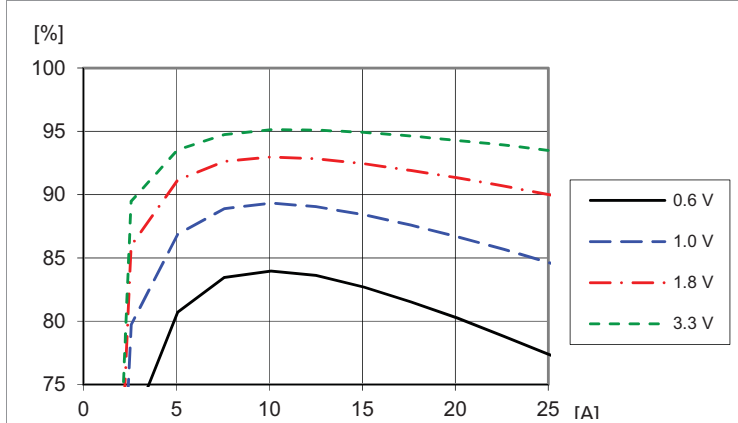
Efficiency vs. load current and output voltage:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 5\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .

Power Dissipation vs. Output Current,  $V_I = 5\text{ V}$



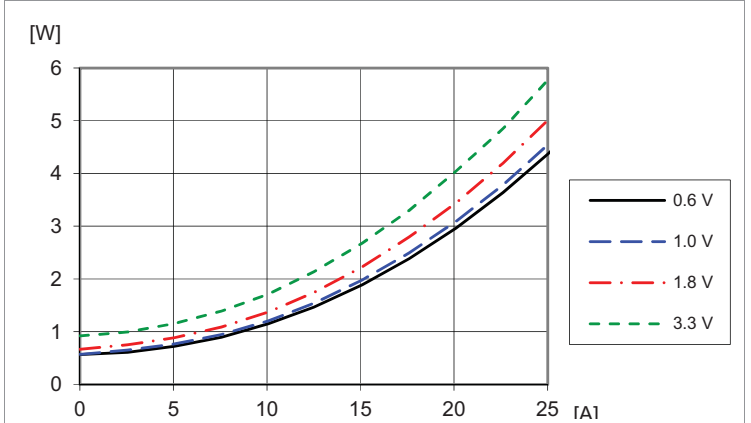
Dissipated power vs. load current and output voltage:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 5\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .

Efficiency vs. Output Current,  $V_I = 12\text{ V}$



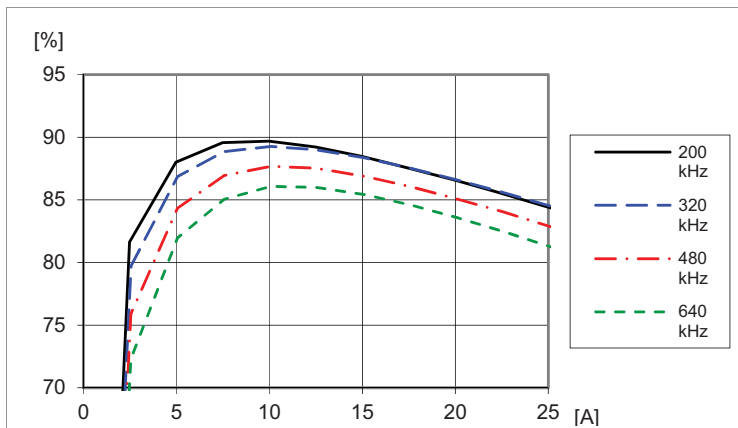
Efficiency vs. load current and output voltage at  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .

Power Dissipation vs. Output Current,  $V_I = 12\text{ V}$



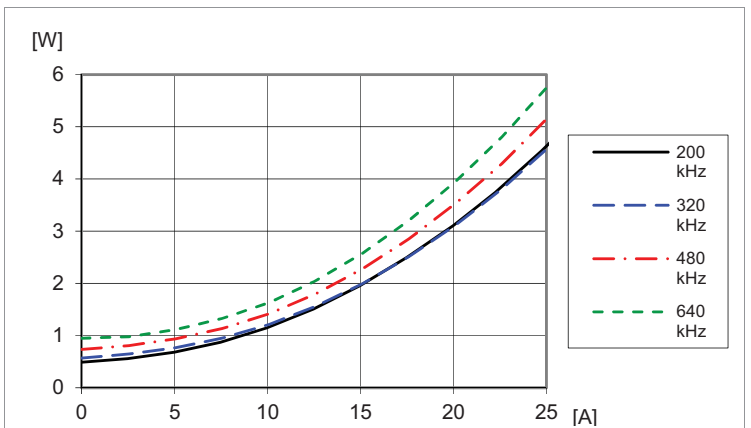
Dissipated power vs. load current and output voltage:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .  
 Default configuration except changed frequency

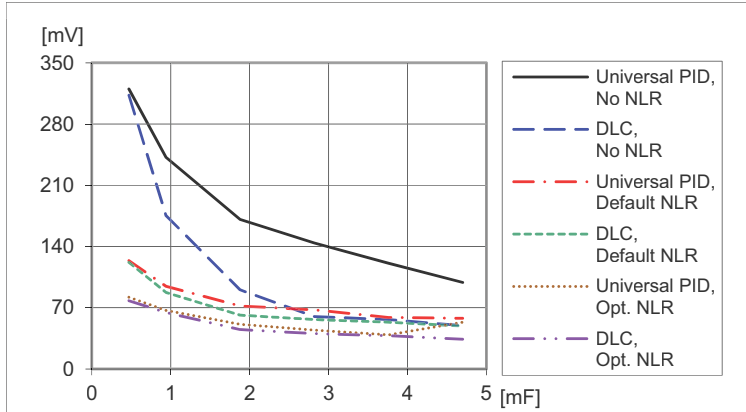
Power Dissipation vs. Output Current and Switching frequency



Dissipated power vs. load current and switch frequency at  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ .  
 Default configuration except changed frequency

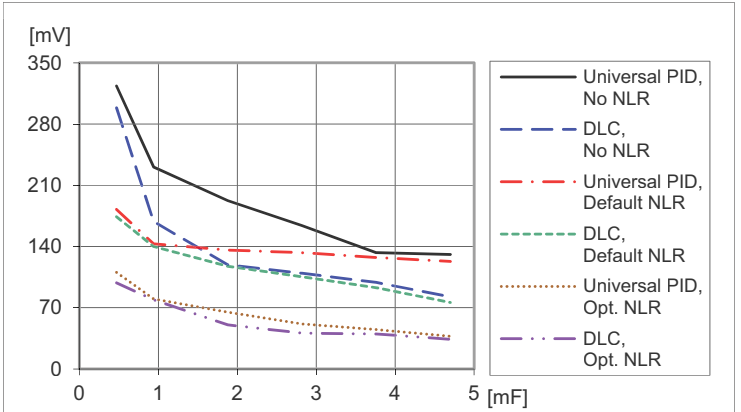
## TYPICAL CHARACTERISTICS, VERTICAL (CONTINUED)

Load Transient vs. External Capacitance,  $V_O = 1.0\text{ V}$



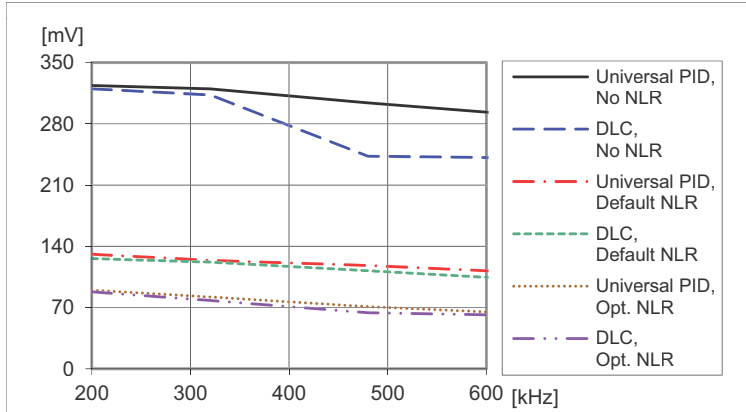
Load transient peak voltage deviation vs. external capacitance. Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with 470  $\mu\text{F}/10\text{ m}\Omega$ ,  $T_{P1} = +25\text{ }^\circ\text{C}$ .  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $di/dt = 2\text{ A}/\mu\text{s}$

Load Transient vs. External Capacitance,  $V_O = 3.3\text{ V}$



Load transient peak voltage deviation vs. external capacitance. Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with 470  $\mu\text{F}/10\text{ m}\Omega$ ,  $T_{P1} = +25\text{ }^\circ\text{C}$ .  $V_I = 12\text{ V}$ ,  $V_O = 3.3\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $di/dt = 2\text{ A}/\mu\text{s}$

Load transient vs. Switch Frequency

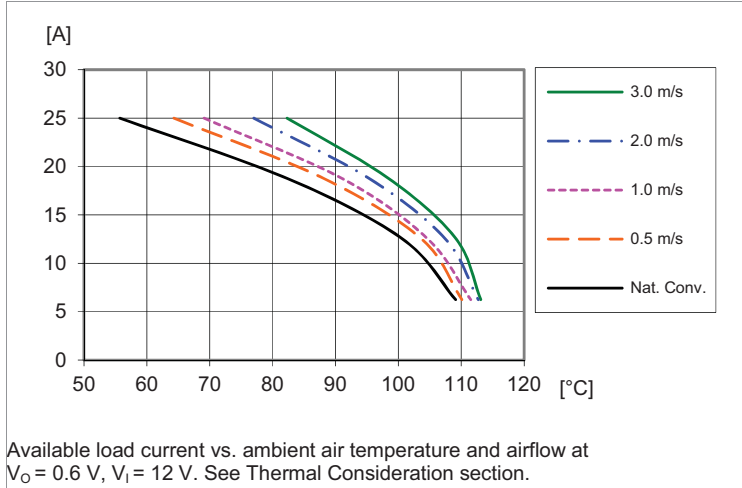


Load transient peak voltage deviation vs. frequency. Step-change (6.25-18.75-6.25 A).  $T_{P1} = +25\text{ }^\circ\text{C}$ .  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$

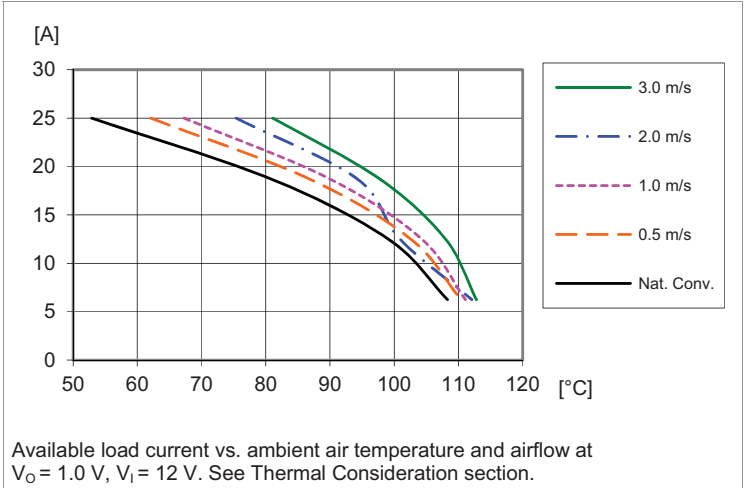
Note: For Universal PID, see section Dynamic Loop Compensation (DLC).

## TYPICAL CHARACTERISTICS, VERTICAL (CONTINUED)

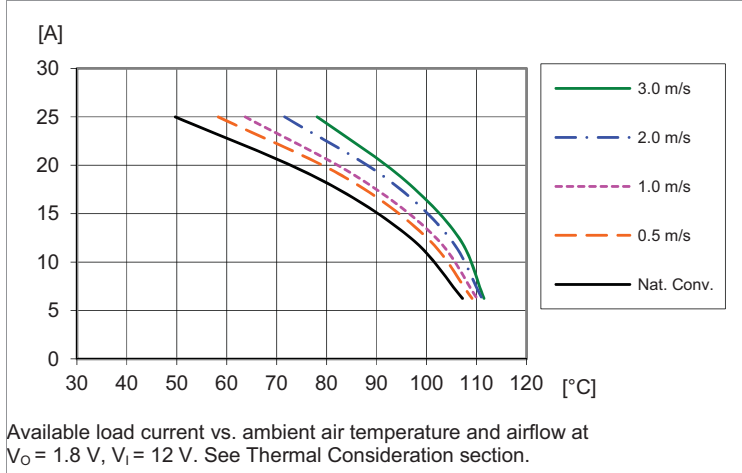
### Output Current Derating, $V_O = 0.6\text{ V}$



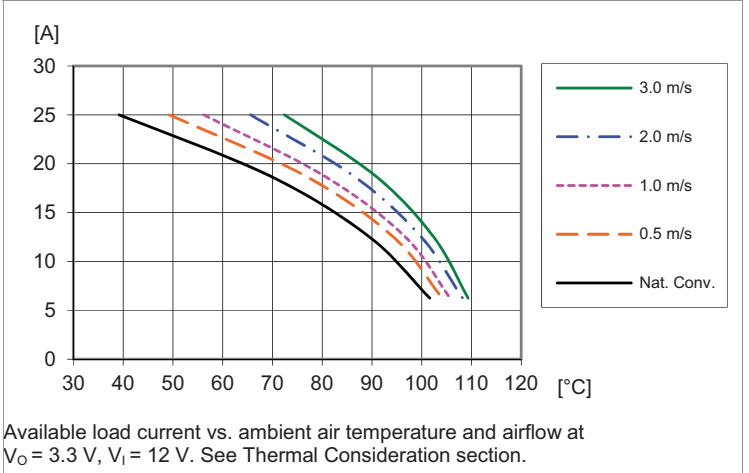
### Output Current Derating, $V_O = 1.0\text{ V}$



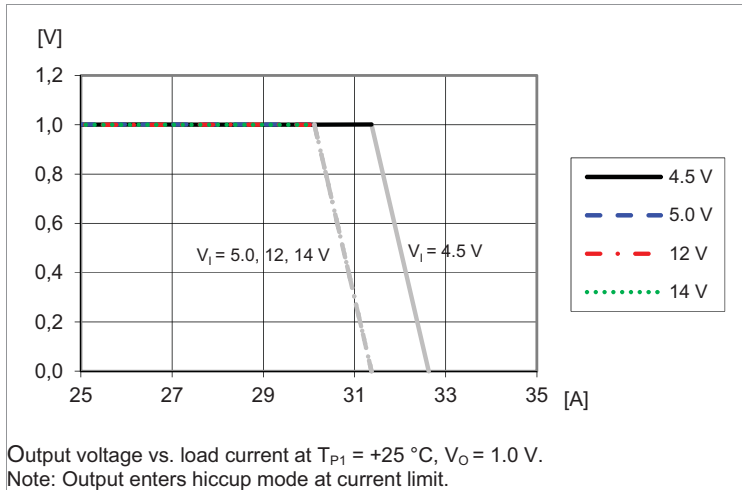
### Output Current Derating, $V_O = 1.8\text{ V}$



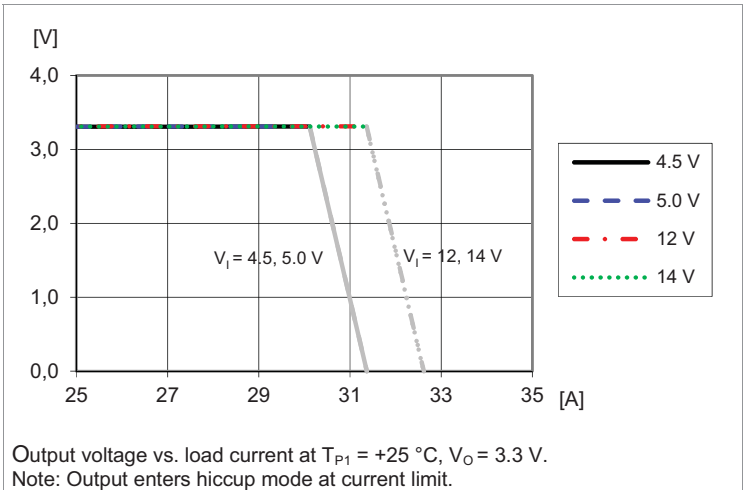
### Output Current Derating, $V_O = 3.3\text{ V}$



### Current Limit Characteristics, $V_O = 1.0\text{ V}$

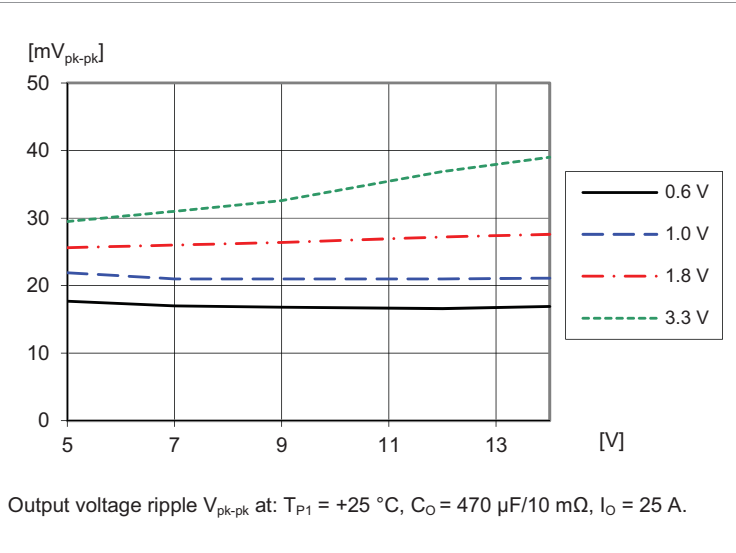


### Current Limit Characteristics, $V_O = 3.3\text{ V}$

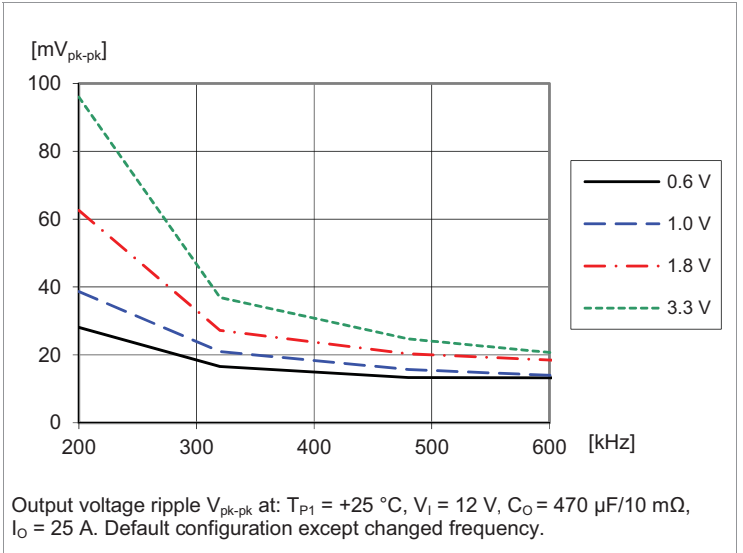


## TYPICAL CHARACTERISTICS, VERTICAL (CONTINUED)

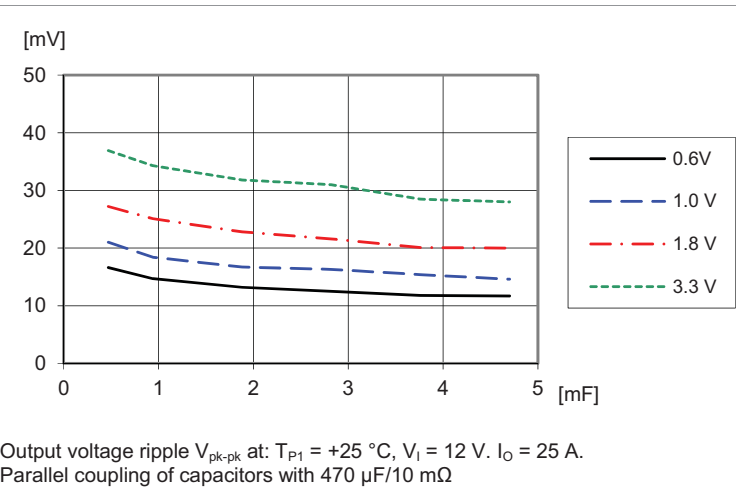
Output Ripple vs. Input Voltage



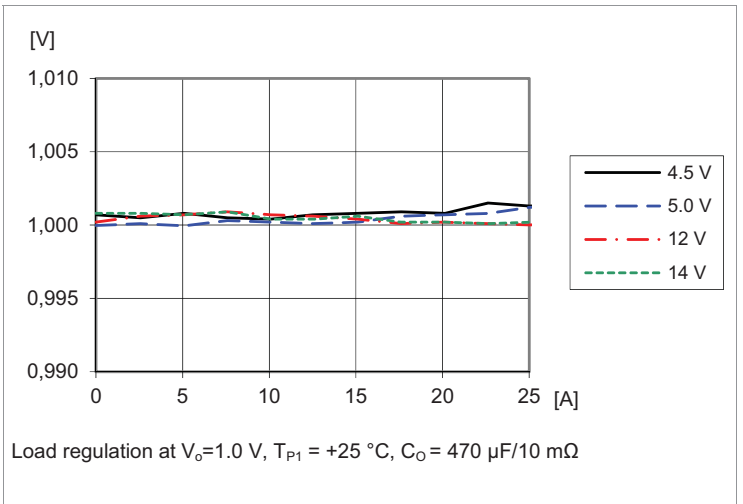
Output Ripple vs. Frequency



Output Ripple vs. External Capacitance

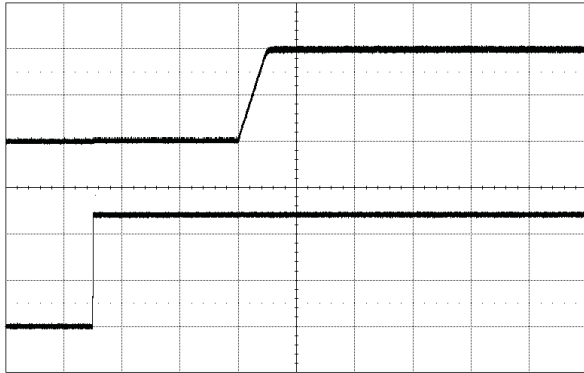


Load regulation,  $V_O = 1.0\text{ V}$



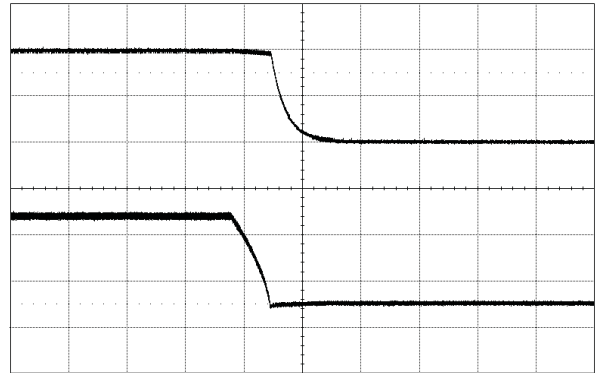
## TYPICAL CHARACTERISTICS, VERTICAL (CONTINUED)

### Start-up by input source



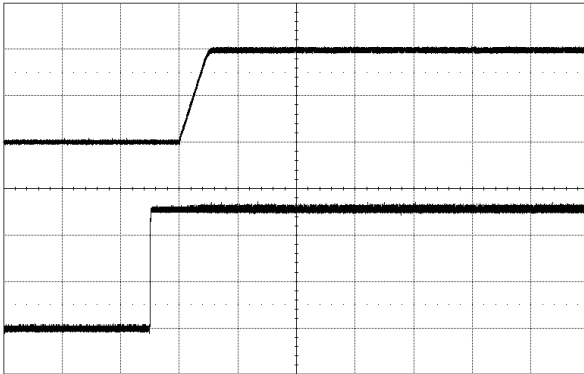
Start-up enabled by connecting  $V_I$  at:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$   
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ ,  $I_O = 25\text{ A}$   
 Top trace: output voltage (0.5 V/div.).  
 Bottom trace: input voltage (5 V/div.).  
 Time scale: (20 ms/div.).

### Shut-down by input source



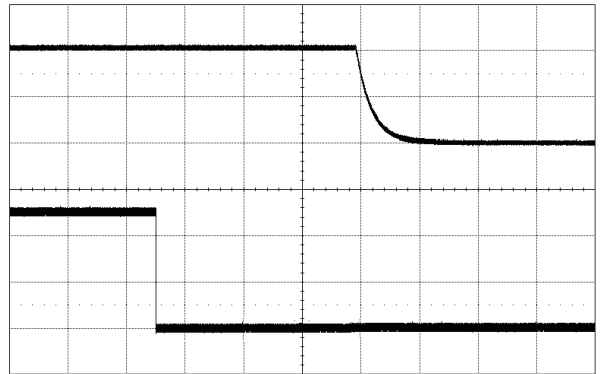
Shut-down enabled by disconnecting  $V_I$  at:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$   
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ ,  $I_O = 25\text{ A}$   
 Top trace: output voltage (0.5 V/div.).  
 Bottom trace: input voltage (5 V/div.).  
 Time scale: (2 ms/div.).

### Start-up by CTRL signal



Start-up by enabling CTRL signal at:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$   
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ ,  $I_O = 25\text{ A}$   
 Top trace: output voltage (0.5 V/div.).  
 Bottom trace: CTRL signal (2 V/div.).  
 Time scale: (20 ms/div.).

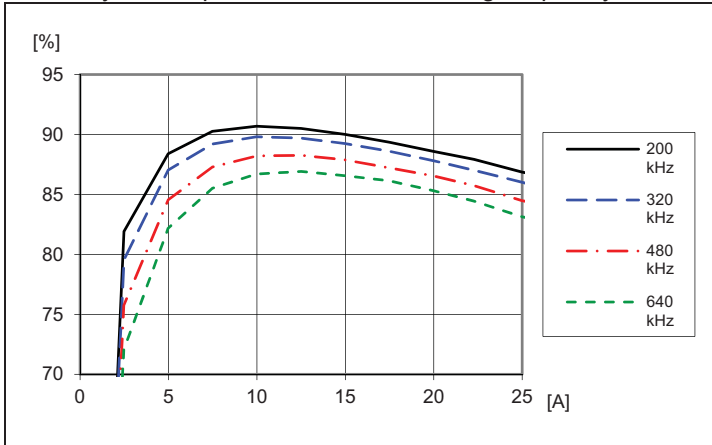
### Shut-down by CTRL signal



Shut-down enabled by disconnecting  $V_I$  at:  
 $T_{P1} = +25\text{ }^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$   
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$ ,  $I_O = 25\text{ A}$   
 Top trace: output voltage (0.5 V/div.).  
 Bottom trace: CTRL signal (2 V/div.).  
 Time scale: (2 ms/div.).

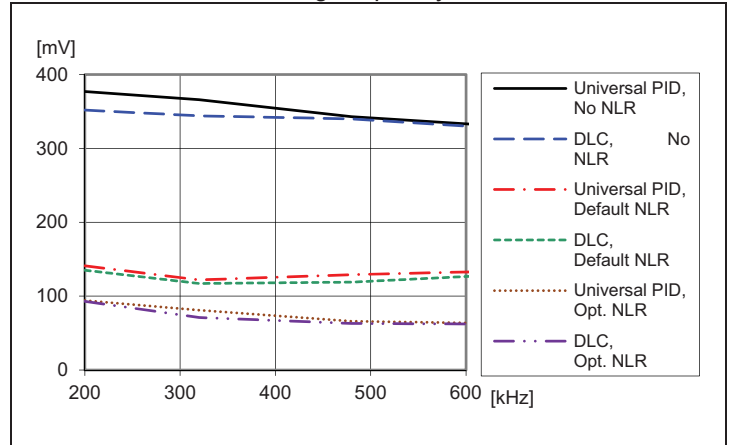
## TYPICAL CHARACTERISTICS

Efficiency vs. Output Current and Switching frequency



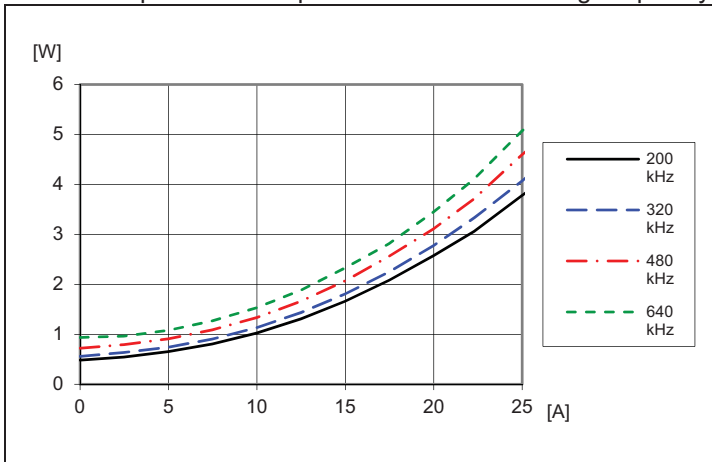
Efficiency vs. load current and switching frequency at  $T_{P1} = +25^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $C_O = 470\ \mu\text{F}/10\text{ m}\Omega$ . Default configuration except changed frequency

Load transient vs. Switching frequency



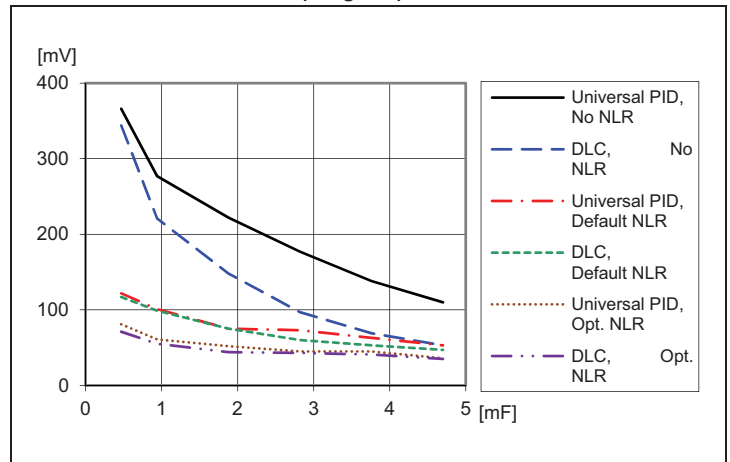
Load transient peak voltage deviation vs. frequency. Step-change (6.25-18.75-6.25 A).  $T_{P1} = +25^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $C_O = 470\ \mu\text{F}/10\text{ m}\Omega$

Power Dissipation vs. Output Current and Switching frequency



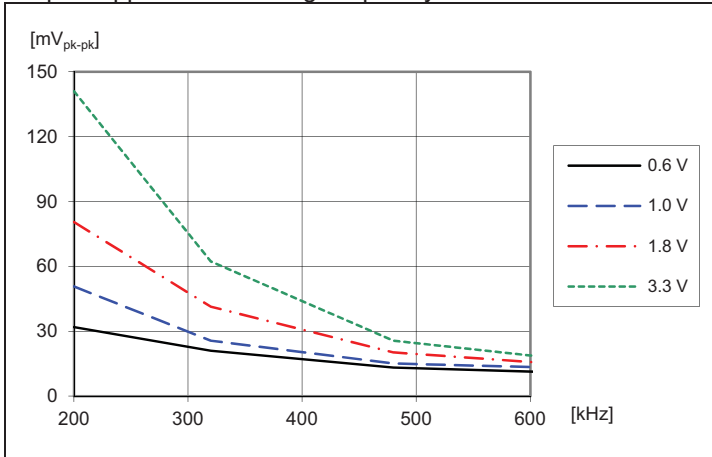
Dissipated power vs. load current and switching frequency at  $T_{P1} = +25^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $C_O = 470\ \mu\text{F}/10\text{ m}\Omega$ . Default configuration except changed frequency

Load Transient vs. Decoupling Capacitance,  $V_O = 1.0\text{ V}$



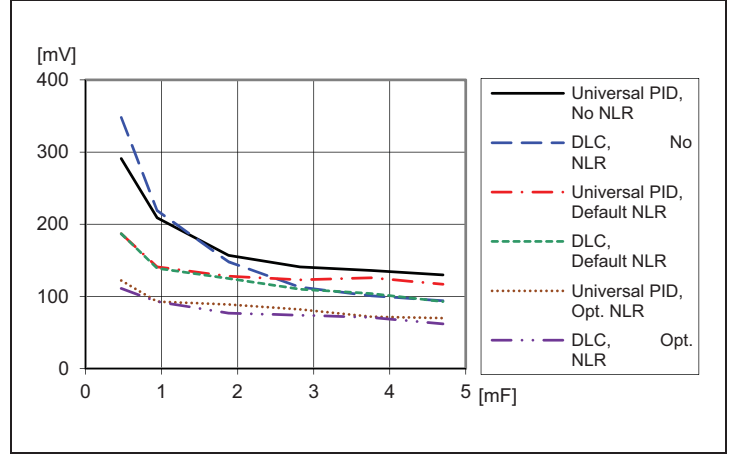
Load transient peak voltage deviation vs. decoupling capacitance. Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with  $470\ \mu\text{F}/10\text{ m}\Omega$ ,  $T_{P1} = +25^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 1.0\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $di/dt = 2\text{ A}/\mu\text{s}$

Output Ripple vs. Switching frequency



Output voltage ripple  $V_{pk-pk}$  at:  $T_{P1} = +25^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $C_O = 470\ \mu\text{F}/10\text{ m}\Omega$ ,  $I_O = 25\text{ A}$  resistive load. Default configuration except changed frequency.

Load Transient vs. Decoupling Capacitance,  $V_O = 3.3\text{ V}$

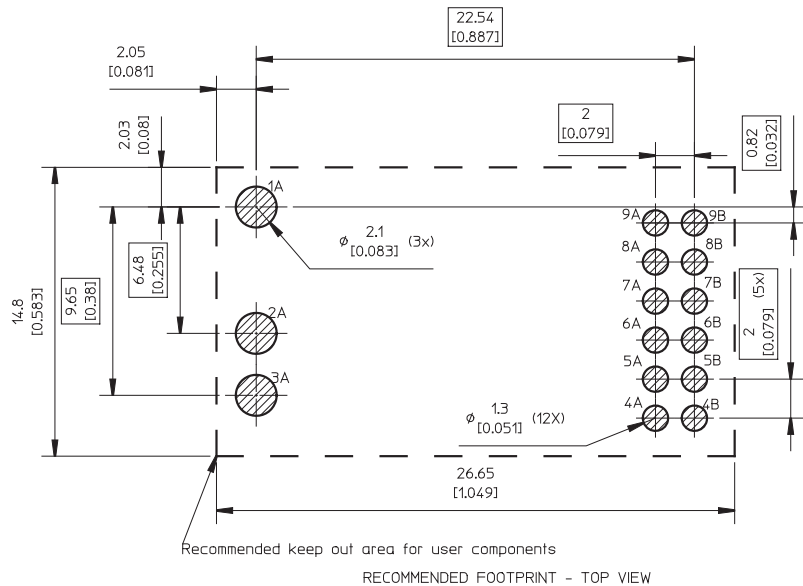
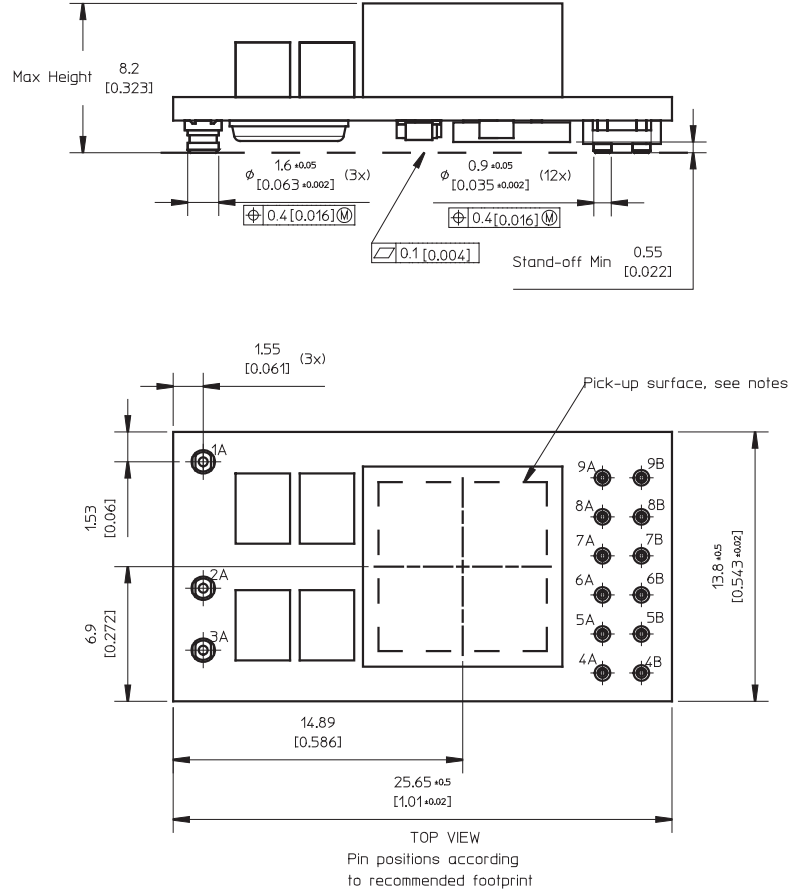


Load transient peak voltage deviation vs. decoupling capacitance. Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with  $470\ \mu\text{F}/10\text{ m}\Omega$ ,  $T_{P1} = +25^\circ\text{C}$ ,  $V_I = 12\text{ V}$ ,  $V_O = 3.3\text{ V}$ ,  $f_{sw} = 320\text{ kHz}$ ,  $di/dt = 2\text{ A}/\mu\text{s}$

## MECHANICAL DRAWING (HORIZONTAL, SURFACE MOUNT)

units: mm [inches]  
 tolerance unless specified:  
 X.X ±0.50 [0.02]  
 X.XX ±0.25 [0.01]  
 (not applied on footprint or typical values)

PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A	VIN	Copper Alloy	Min 0.1 μm Au over 1~3 μm Ni
2A	GND		
3A	VOUT		
4A	VTRK/PG	Brass	Min 0.1 μm Au over 2 μm Ni
4B	PREF		
5A	+S		
5B	-S		
6A	SA0		
6B	DDC		
7A	SCL		
7B	SDA		
8A	VSET		
8B	SYNC		
9A	SALRT		
9B	CTRL		



## MECHANICAL DRAWING (HORIZONTAL, THROUGH HOLE MOUNT)

units: mm [inches]

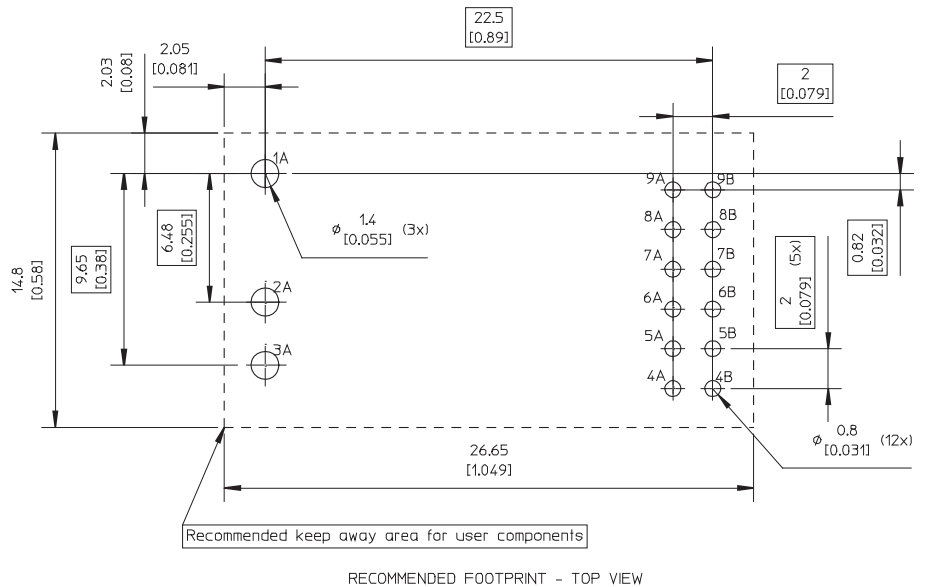
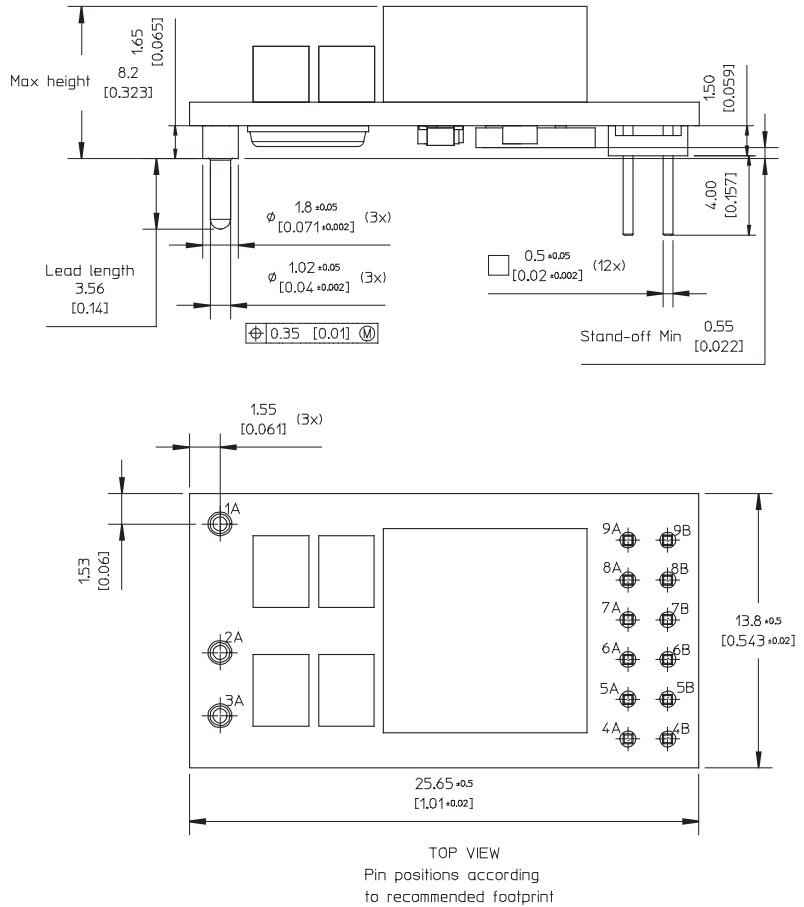
tolerance unless specified:

X.X ±0.50 [0.02]

X.XX ±0.25 [0.01]

(not applied on footprint or typical values)

PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A	VIN	Copper Alloy	Min 8~13 μm matte tin over 2.5~5 μm Ni
2A	GND		
3A	VOUT		
4A	VTRK/PG	Brass	Min 0.2 μm Au over 1.27 μm Ni
4B	PREF		
5A	+S		
5B	-S		
6A	SA0		
6B	DDC		
7A	SCL		
7B	SDA		
8A	VSET		
8B	SYNC		
9A	SALRT		
9B	CTRL		





## MECHANICAL DRAWING (VERTICAL, THROUGH HOLE MOUNT)

units: mm [inches]

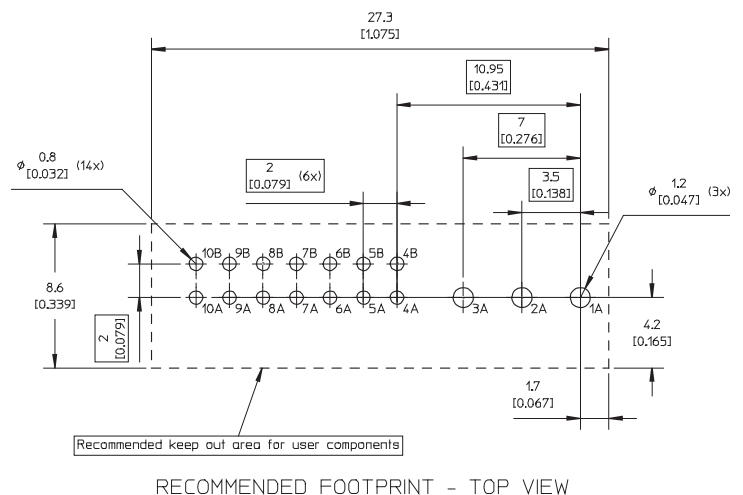
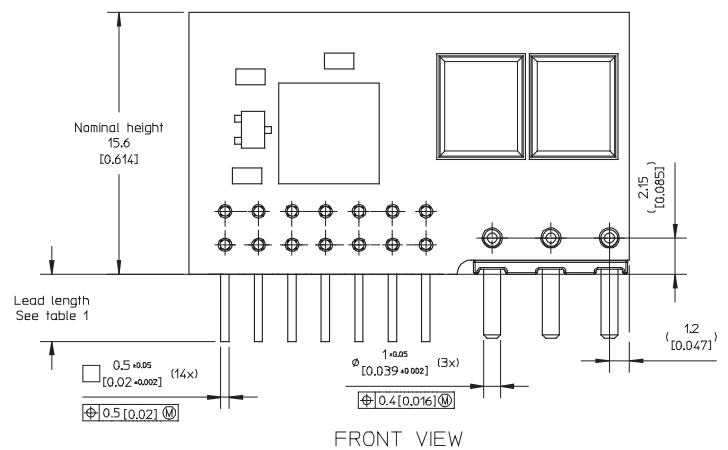
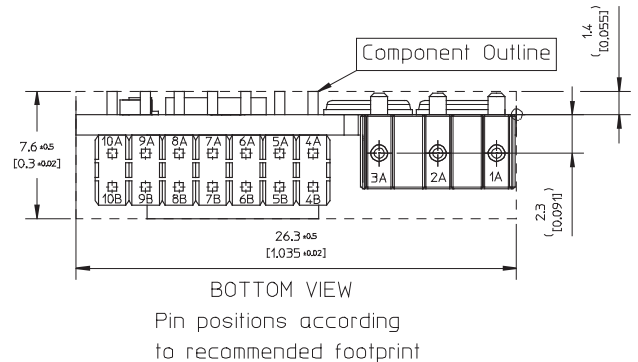
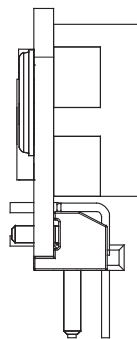
tolerance unless specified:

X.X ±0.50 [0.02]

X.XX ±0.25 [0.01]

(not applied on footprint or typical values)

PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A	VIN	Copper Alloy	Min 0.1 µm Au over 1~3 µm Ni
2A	GND		
3A	VOUT		
4A	+S		Min 0.1 µm Au over 1 µm Ni
4B	-S		
5A	VSET		
5B	VTRK		
6A	SALRT		
6B	SDA		
7A	SCL		
7B	SA1		
8A	SA0		
8B	SYNC		
9A	PG		
9B	CTRL		
10A	DDC		
10B	PREF		



## OPERATING INFORMATION

The NDM2Z-25 modules are available in different configurations; not all pins and functions are supported by each configuration. This document describes all pins and functions.

The Novum Z Products PMBus Commands application note defines the available PMBus™ commands.

## REQUIRED CONFIGURATIONS

### NDM2Z-25 Module Pins

Each NDM2Z-25 module should have a resistor placed between VSET and PREF to set the output voltage of the module. The maximum output voltage which can be configured by PMBus commands can never exceed 110% of the voltage set by the VSET pin. The SMBus address of each module is set by either pin-strap configuration or resistor value associated with the SA0 and SA1 pins. More information regarding setting the SMBus address for a module can be found in the section titled "SMBus".

### PCB Layout

Good performance of any point of load voltage regulator module can only be achieved with careful PCB layout considerations. Ground planes or very wide traces should be used for power and ground routing. Input capacitors should be placed close to the input voltage pins of the module and output capacitors should be placed close to the load. The module should also be placed as close as possible to the load.

## INPUT AND OUTPUT CAPACITORS

### Input Capacitors

Input capacitors are recommended to be used with the NDM2Z-25 module in order to minimize input voltage ripple. A 330  $\mu$ F POSCAP or electrolytic and 3x 22  $\mu$ F ceramic capacitors should be placed as close as possible to the input pins of the module. Additional input capacitors may be used if less input voltage ripple is desired.

### Output Capacitors

Output capacitors are recommended to be used with the NDM2Z-25 module in order to improve transient response and minimize output voltage ripple. A 330  $\mu$ F POSCAP or electrolytic and 3x 22  $\mu$ F ceramic capacitors should be placed as close as possible to the load. Additional output capacitors may be used to further improve the output voltage characteristics.

## POWER CONVERSION AND MANAGEMENT

### Power Conversion Overview

The NDM2Z-25 module has several features to enable high power conversion efficiency. Non-linear loop response (NLR) improves the response time and reduces the output deviation as a result of load transients. The incorporation of DFM enhances the performance of CUI modules over that available from conventional analog POL offerings.

### Power Management Overview

The NDM2Z-25 module incorporates a wide range of power management features. All power management functions can be configured via the SMBus interface. The NDM2Z-25 can monitor and report many characteristics of the module including input voltage, output voltage, output current and internal temperature. Additionally, the NDM2Z-25 includes circuit protection features that protect the module and load from damage due to system faults. Monitoring parameters can also be configured to provide alerts for specific conditions. The ability of CUI modules to digitally control, configure and monitor OS features provides significant benefits over traditional analog POL products.

## CONFIGURING THE MODULE

### Pin Settings

Pins SA0 and SA1 are used to set the SMBus address of the NDM2Z-25 module. Details of this feature are discussed in the section titled "SMBus". Pin SYNC is used to synchronize the switching clock of the module to an external clock source. More information regarding synchronization can be found in the section titled "SWITCHING FREQUENCY AND SYNCHRONIZATION".

Pin VSET is used to configure the output voltage of the module. The voltage established by the VSET pin limits the maximum output voltage that can be configured by SMBus commands.

The SA0, SA1, SYNC and VSET pin configurations are read by the module when power is applied or whenever a SMBus RESTORE command is issued.

The CTRL pin is active high and can be used to enable the module. Internal connections on the module will drive the CTRL pin high if it is left floating.

Pins +S and -S are used for remote voltage sensing of the output voltage.