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FAIRCHILD
SEMICONDUCTOR TM

February 1996

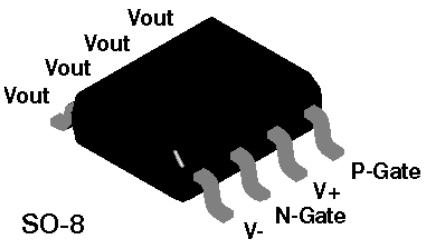
NDS8852H
Complementary MOSFET Half Bridge

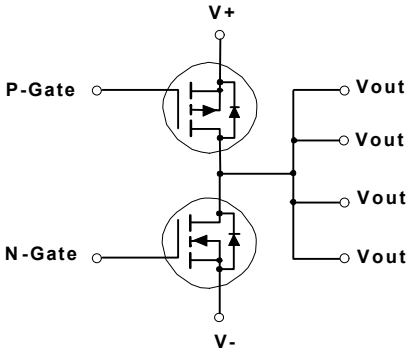
General Description

These Complementary MOSFET half bridge devices are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage half bridge applications or CMOS applications when both gates are connected together.

Features

- N-Channel 4.3A, 30V, $R_{DS(ON)}$=0.08Ω @ V_{GS}=10V.
  P-Channel -3.4A, -30V, $R_{DS(ON)}$=0.13Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Matched pair for equal input capacitance and power capability .





Absolute Maximum Ratings

T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		20	-20	V
I_D	Drain Current - Continuous	(Note 1a & 2)	4.3	-3.4	A
	- Pulsed		15	-10	
P_D	Maximum Power Dissipation	(Note 1a)	2.5		W
	(Single Device)	(Note 1b)	1.2		
		(Note 1c)	1		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Single Device)	(Note 1a)	50		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Single Device)	(Note 1)	25		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	N-Ch			2	µA
		T_J = 55°C				25	µA
		V_{DS} = -24 V, V_{GS} = 0 V	P-Ch			-2	µA
		T_J = 55°C				-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 3)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.7	2.8	V
		T_J = 125°C		0.7	1.2	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-1.6	-2.8	
		T_J = 125°C		-0.85	-1.25	-2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.4 A	N-Ch		0.06	0.08	Ω
		T_J = 125°C			0.08	0.13	
		V_{GS} = 4.5 V, I_D = 2.8 A			0.08	0.11	
		V_{GS} = -10 V, I_D = -3.4 A	P-Ch		0.11	0.13	
		T_J = 125°C			0.15	0.21	
		V_{GS} = -4.5 V, I_D = -2.8 A			0.17	0.2	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	10			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-10			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3.4 A	N-Ch		6		S
		V_{DS} = -15 V, I_D = -3.4 A	P-Ch		4		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		300		pF
			P-Ch		330		
C_{oss}	Output Capacitance		N-Ch		190		pF
		P-Channel V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		190		
C_{rss}	Reverse Transfer Capacitance		N-Ch		70		pF
			P-Ch		70		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 3)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		10	15	ns
			P-Ch		9	40	
t_r	Turn - On Rise Time		N-Ch		13	20	ns
		P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	P-Ch		21	40	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		21	50	ns
			P-Ch		21	90	
t_f	Turn - Off Fall Time		N-Ch		5	50	ns
			P-Ch		8	50	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 3.4 A, V_{GS} = 10 V	N-Ch		9.5	27	nC
			P-Ch		10	25	
Q_{gs}	Gate-Source Charge	P-Channel V_{DS} = -10 V, I_D = -3.4 A, V_{GS} = -10 V	N-Ch		1.5		
			P-Ch		1.6		
Q_{gd}	Gate-Drain Charge		N-Ch		2.6		
			P-Ch		2.7		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			2.1	A
			P-Ch			-2.1	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)	N-Ch		0.8	1.2	V
		V_{GS} = 0 V, I_S = -2.1 A (Note 2)	P-Ch		-0.8	-1.2	
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0 V, I_F = 2.1 A, dI_F/dt = 100 A/µs	N-Ch			100	ns
		P-Channel V_{GS} = 0 V, I_F = -2.1 A, dI_F/dt = 100 A/µs	P-Ch			100	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

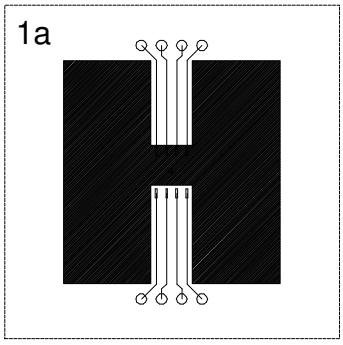
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

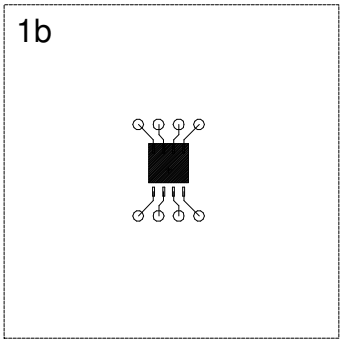
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

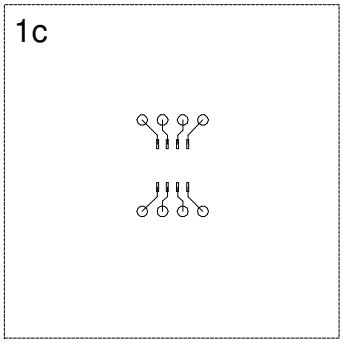
a. 50°C/W when mounted on a 1 in^2 pad of 2oz cpper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz cpper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz cpper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

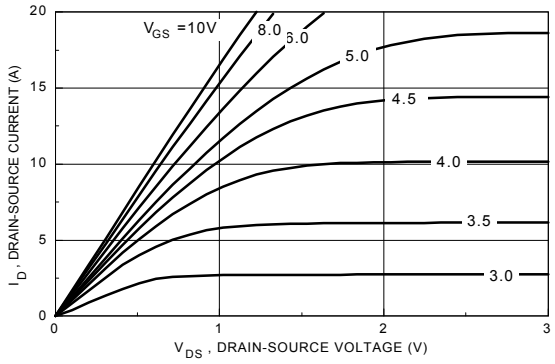


Figure 1. N-Channel On-Region Characteristics.

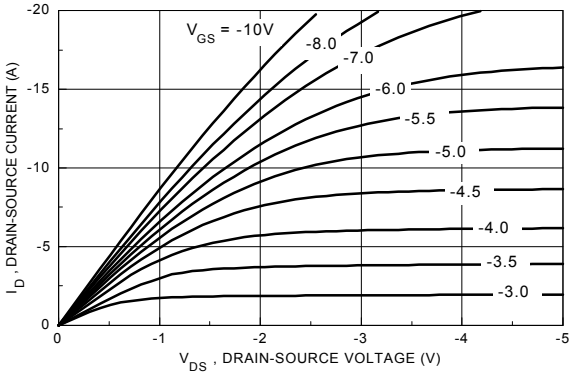


Figure 2. P-Channel On-Region Characteristics.

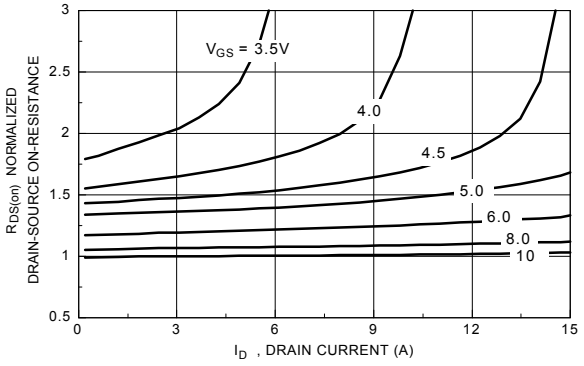


Figure 3. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

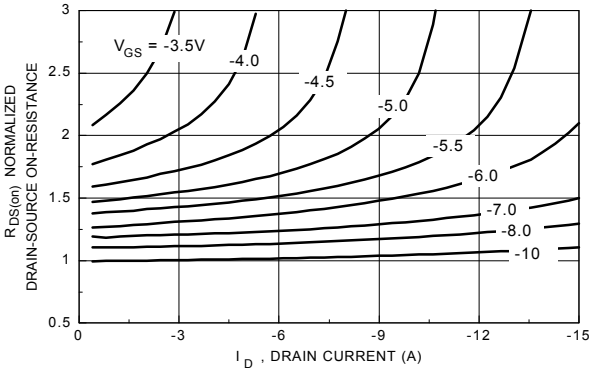


Figure 4. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

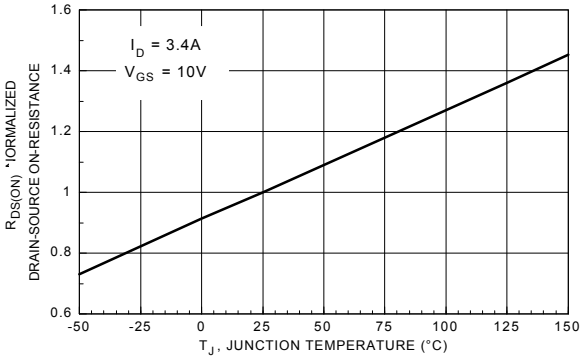


Figure 5. N-Channel On-Resistance Variation with Temperature.

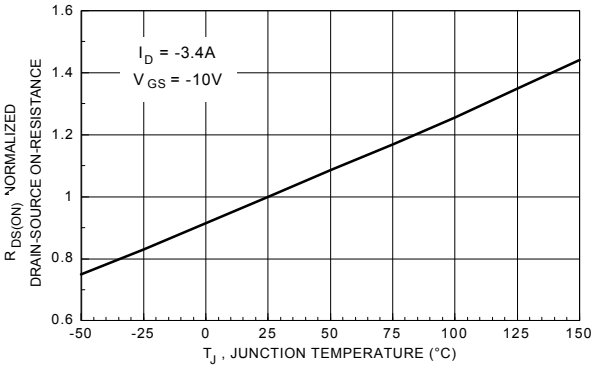


Figure 6. P-Channel On-Resistance Variation with Temperature.

Typical Electrical Characteristics

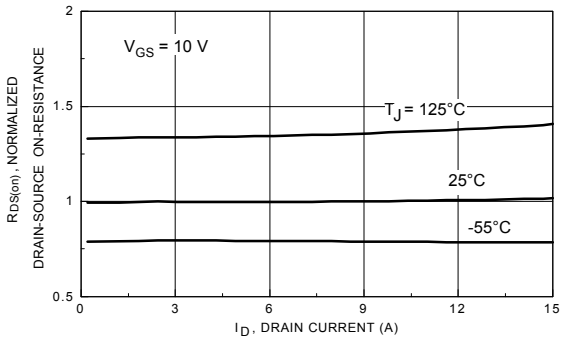


Figure 7. N-Channel On-Resistance Variation with Drain Current and Temperature.

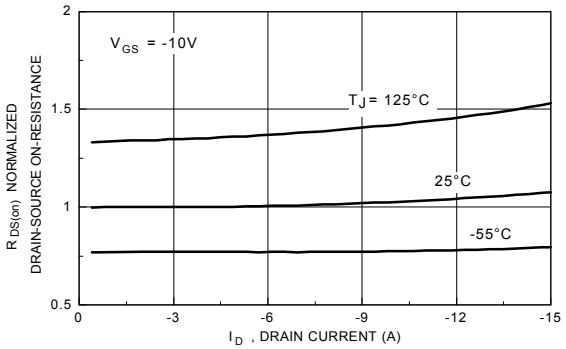


Figure 8. P-Channel On-Resistance Variation with Drain Current and Temperature.

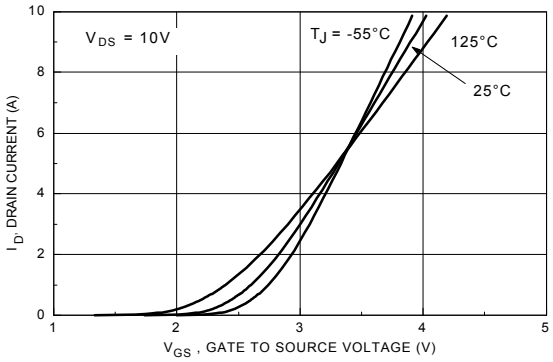


Figure 9. N-Channel Transfer Characteristics.

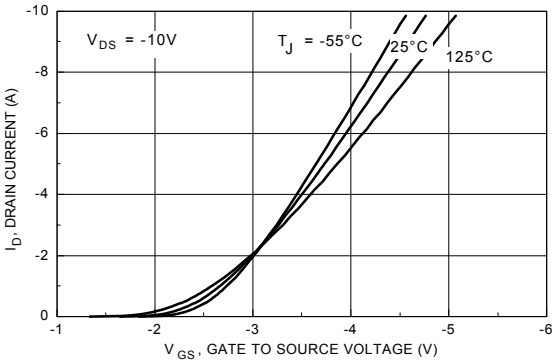


Figure 10. P-Channel Transfer Characteristics.

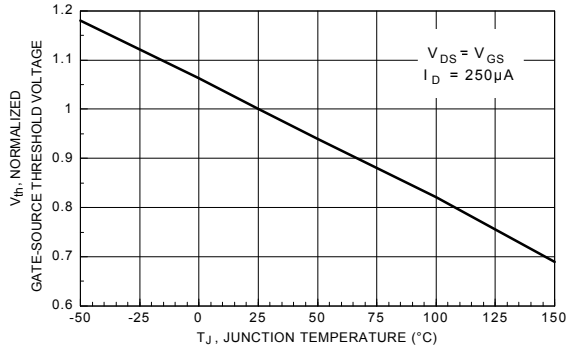


Figure 11. N-Channel Gate Threshold Variation with Temperature.

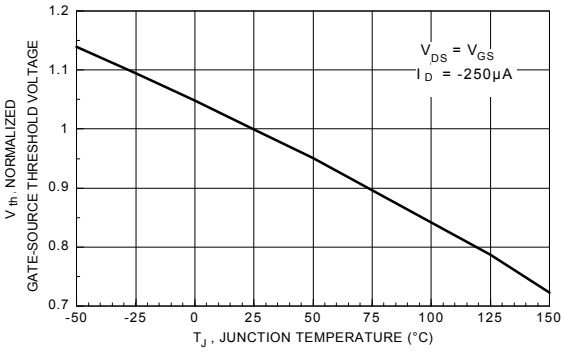


Figure 12. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

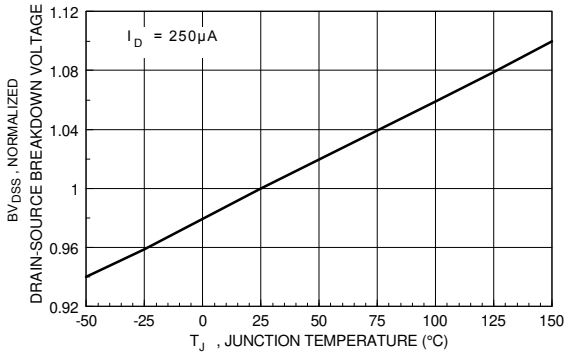


Figure 13. N-Channel Breakdown Voltage Variation with Temperature.

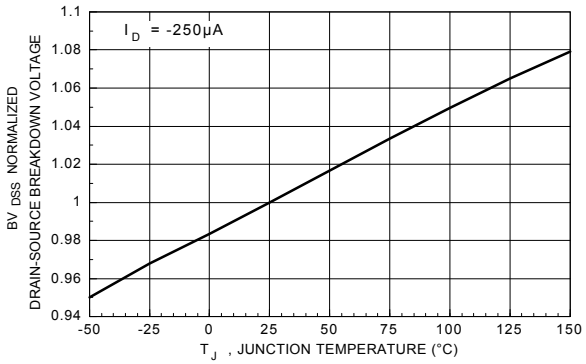


Figure 14. P-Channel Breakdown Voltage Variation with Temperature.

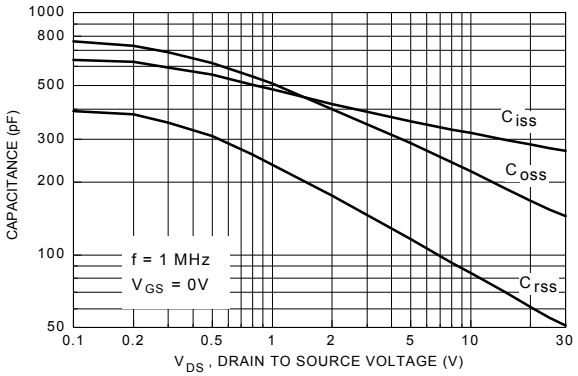


Figure 15. N-Channel Capacitance Characteristics.

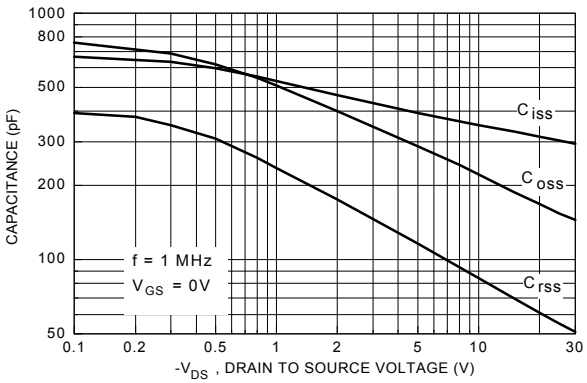


Figure 16. P-Channel Capacitance Characteristics.

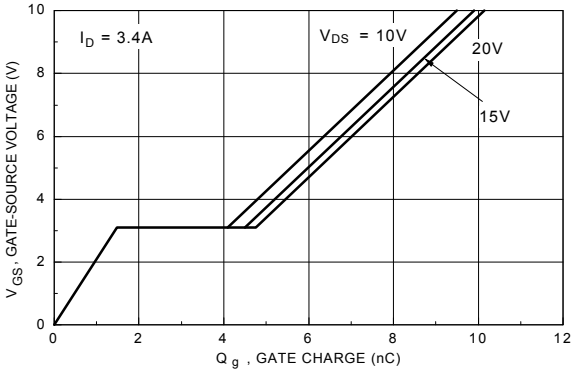


Figure 17. N-Channel Gate Charge Characteristics.

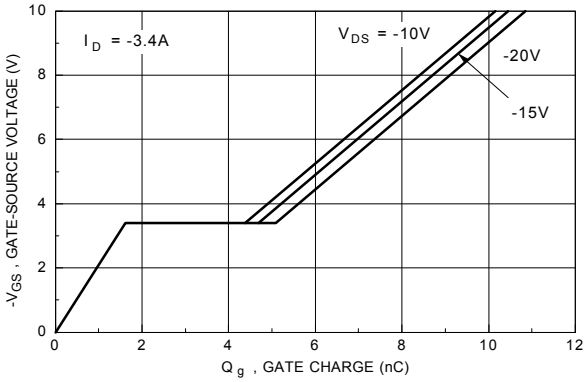


Figure 18. P-Channel Gate Charge Characteristics.

Typical Electrical and Thermal Characteristics

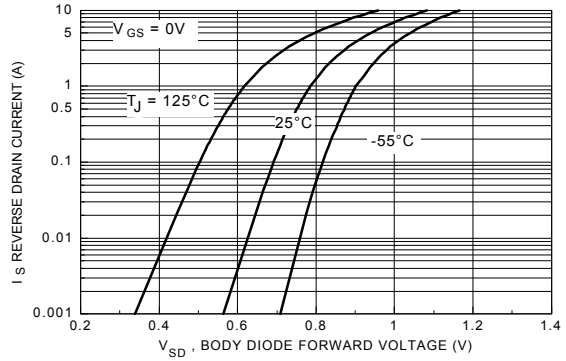


Figure 19. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

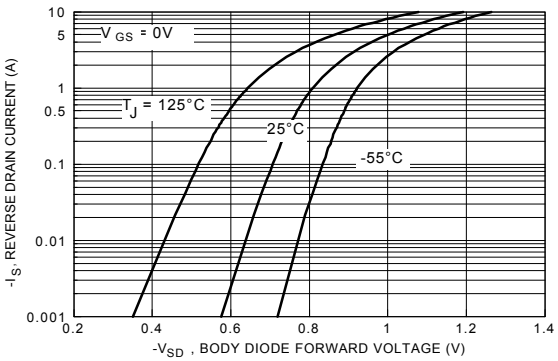


Figure 20. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

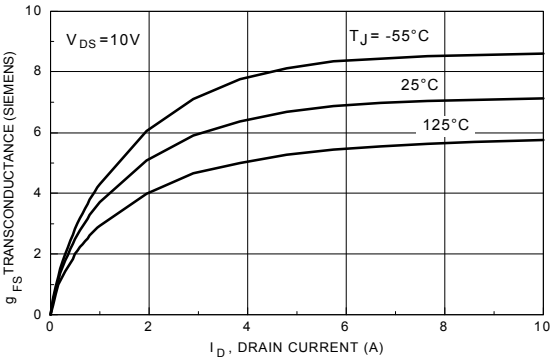


Figure 21. N-Channel Transconductance Variation with Drain Current and Temperature.

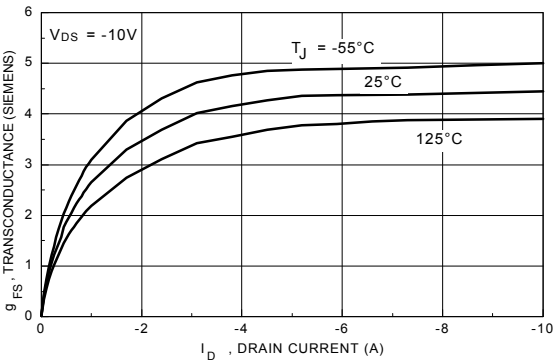


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

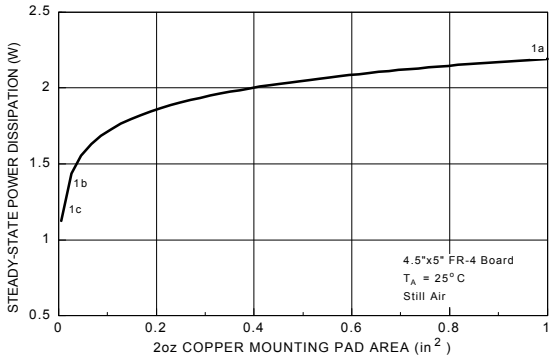


Figure 23. SO-8 Single Device DC Power Dissipation versus Copper Mounting Pad Area.

Typical Thermal Characteristics

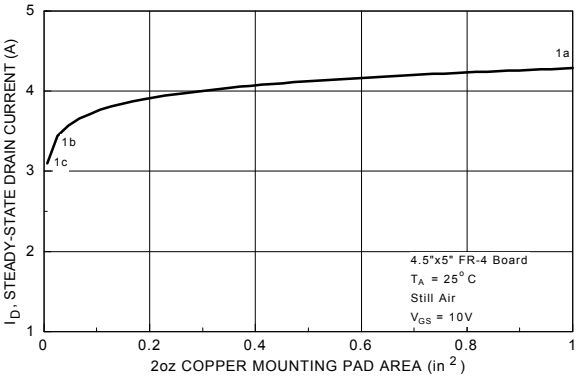


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

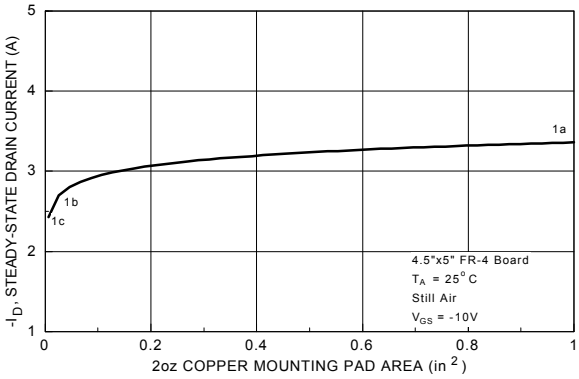


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

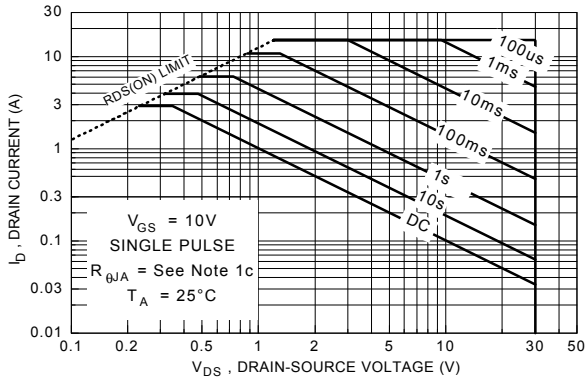


Figure 26. N-Ch Maximum Safe Operating Area.

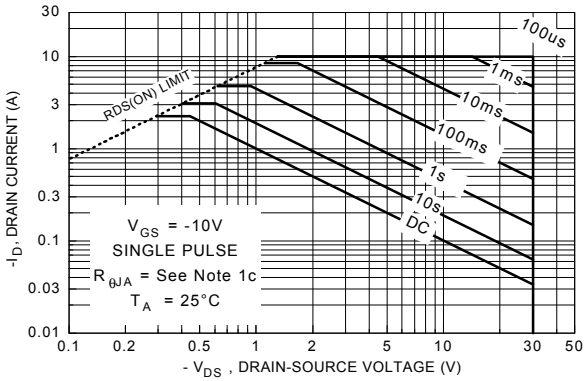


Figure 27. P-Ch Maximum Safe Operating Area.

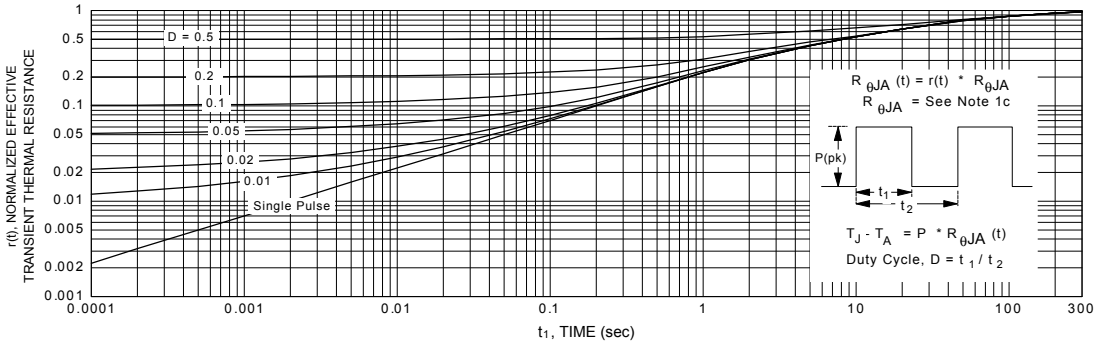


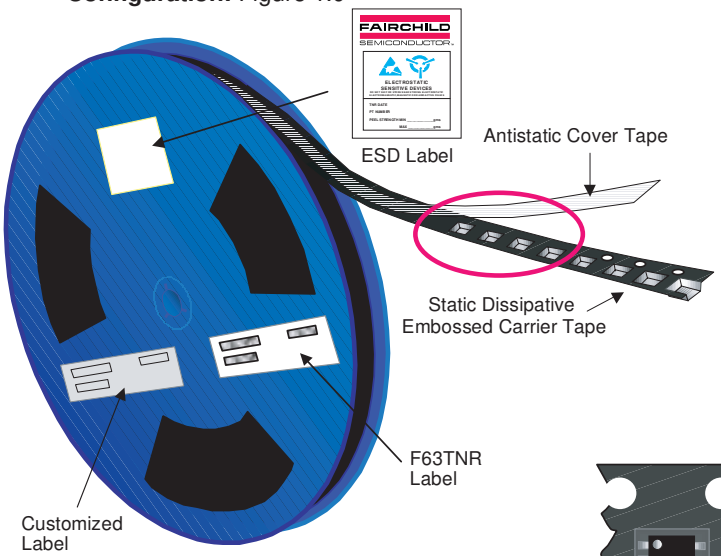
Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

SO-8 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

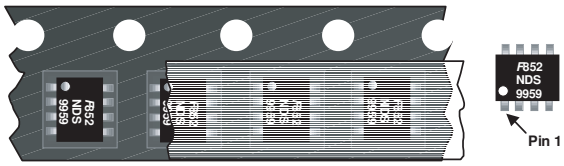
SOIC(8lds) Packaging Configuration: Figure 1.0



Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

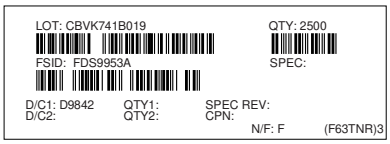
These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

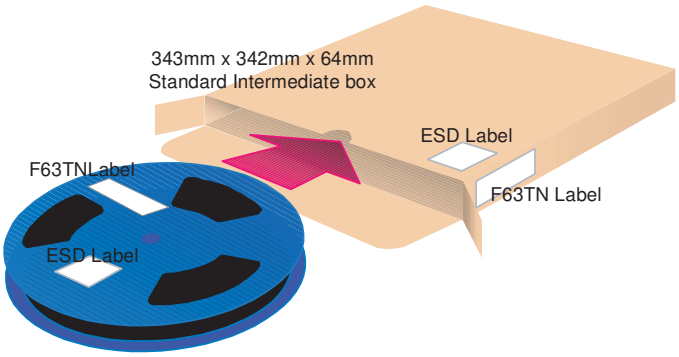


SOIC-8 Unit Orientation

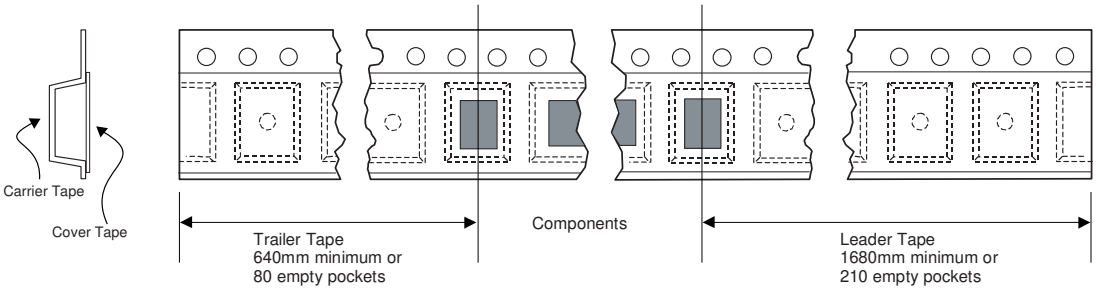
SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	TNR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47
Max qty per Box	5,000	30,000	8,000	1,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				

F63TNR Label sample



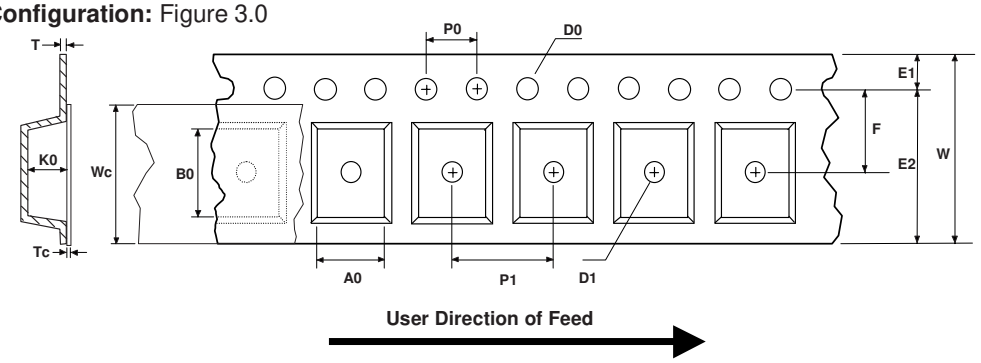


SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



SO-8 Tape and Reel Data and Package Dimensions, continued

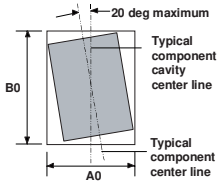
SOIC(8lds) Embossed Carrier Tape
Configuration: Figure 3.0



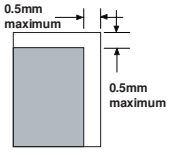
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation

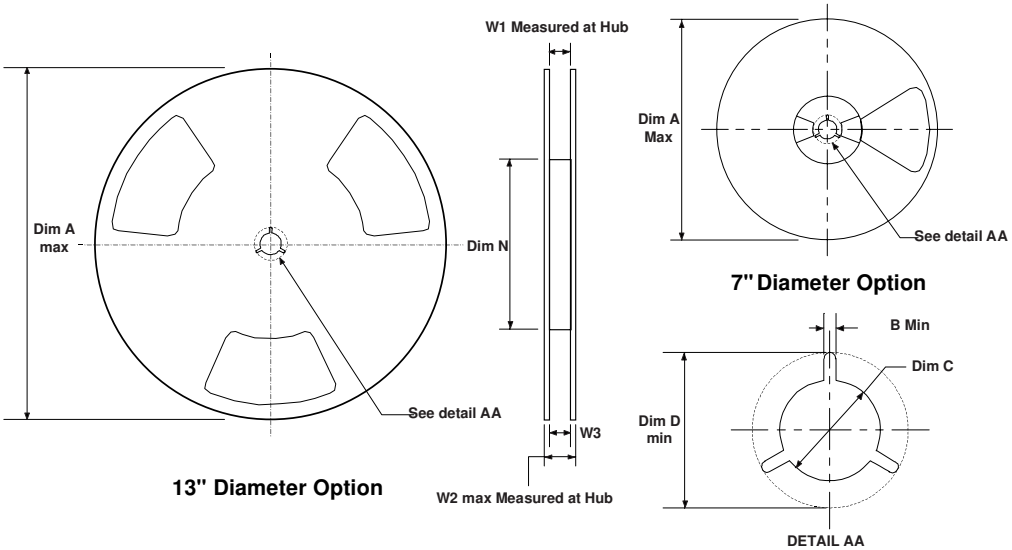


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

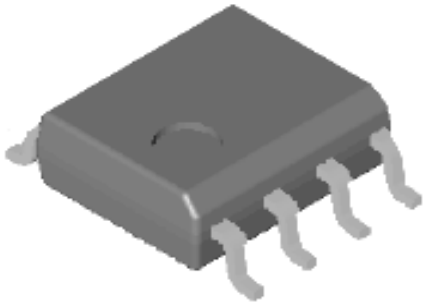
SOIC(8lds) Reel Configuration: Figure 4.0

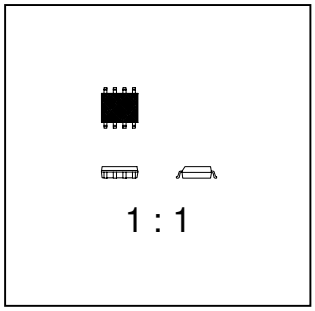


Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4

SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC-8 (FS PKG Code S1)

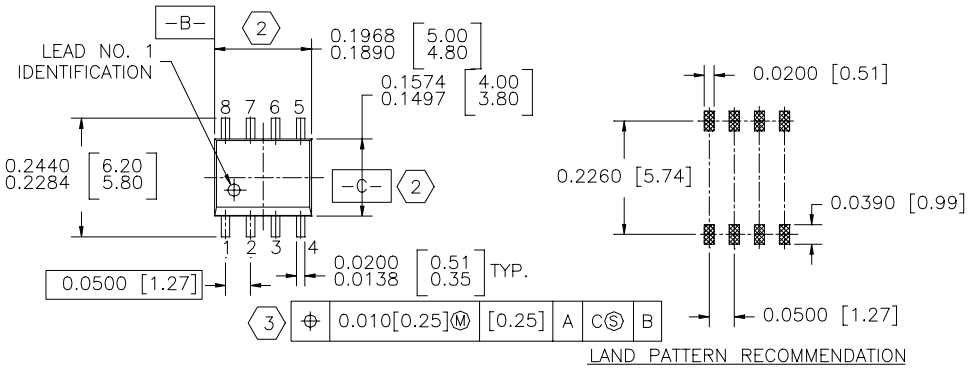


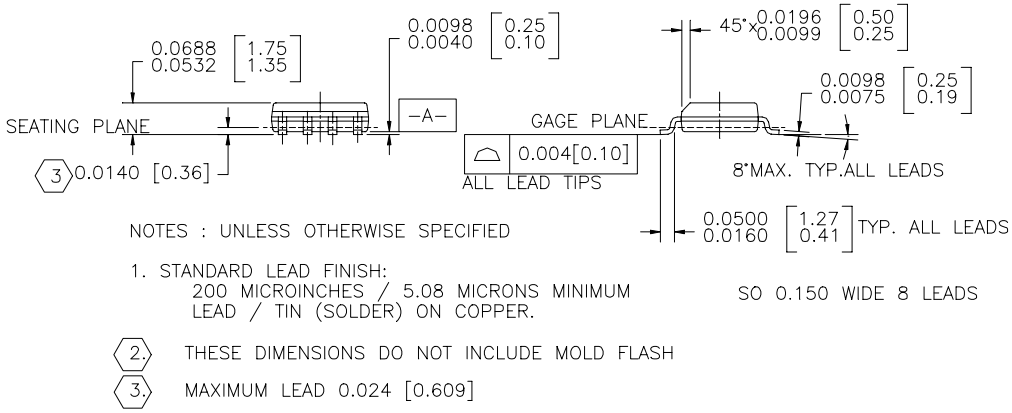


Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774





NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   200 MICROINCHES / 5.08 MICRONS MINIMUM
   LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

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POP™
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