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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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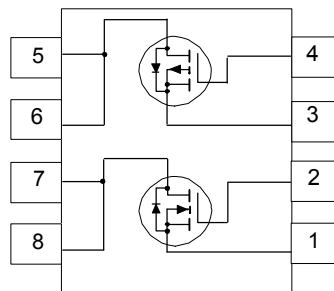
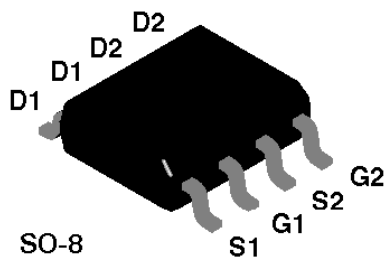
NDS9952A Dual N & P-Channel Enhancement Mode Field Effect Transistor

General Description

These dual N- and P-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.7A, 30V, $R_{DS(ON)}=0.08\Omega @ V_{GS}=10V$.
P-Channel -2.9A, -30V, $R_{DS(ON)}=0.13\Omega @ V_{GS}=-10V$.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	30	-30	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Note 1a)	± 3.7	± 2.9	A
	- Pulsed	± 15	± 10	
P_D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	N-Ch	30			V
		$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	P-Ch	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$	N-Ch			2	μA
		$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$	P-Ch			-2	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	N-Ch	1	1.7	2.8	V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	P-Ch	-1	-1.6	-2.8	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.0\text{ A}$ $T_J = 125^\circ\text{C}$	N-Ch		0.06	0.08	Ω
					0.08	0.13	
		$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$ $T_J = 125^\circ\text{C}$			0.08	0.11	
		$V_{GS} = -10\text{ V}, I_D = -1.0\text{ A}$ $T_J = 125^\circ\text{C}$	P-Ch		0.11	0.13	
					0.15	0.21	
		$V_{GS} = -4.5\text{ V}, I_D = -0.5\text{ A}$ $T_J = 125^\circ\text{C}$			0.17	0.2	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	N-Ch	15			A
		$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	P-Ch	-10			
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 3.7\text{ A}$	N-Ch		6		S
		$V_{DS} = -15\text{ V}, I_D = -2.9\text{ A}$	P-Ch		4		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch		320		μF
			P-Ch		350		
C_{oss}	Output Capacitance	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch		225		μF
			P-Ch		260		
C_{rss}	Reverse Transfer Capacitance		N-Ch		85		μF
			P-Ch		100		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
t _{D(on)}	Turn - On Delay Time	N-Channel V _{DD} = 10 V, I _D = 1 A, V _{GEN} = 10 V, R _{GEN} = 6 Ω	N-Ch		10	15	ns
			P-Ch		9	40	
t _r	Turn - On Rise Time	P-Channel V _{DD} = -10 V, I _D = -1 A, V _{GEN} = -10 V, R _{GEN} = 6 Ω	N-Ch		13	20	ns
			P-Ch		21	40	
t _{D(off)}	Turn - Off Delay Time		N-Ch		21	50	ns
				P-Ch		21	
t _f	Turn - Off Fall Time	N-Ch		5	50	ns	
			P-Ch		8		50
Q _g	Total Gate Charge	N-Channel V _{DS} = 10 V, I _D = 3.7 A, V _{GS} = 10 V	N-Ch		9.5	27	nC
			P-Ch		10	25	
Q _{gs}	Gate-Source Charge	P-Channel V _{DS} = -10 V, I _D = -2.9 A, V _{GS} = -10 V	N-Ch		1.5		nC
			P-Ch		1.6		
Q _{gd}	Gate-Drain Charge	N-Ch		3.3		nC	
			P-Ch		3.4		

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.2	A
			P-Ch			-1.2	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.25 A (Note 2)	N-Ch		0.8	1.3	V
		V _{GS} = 0 V, I _S = -1.25 A (Note 2)	P-Ch		-0.8	-1.3	
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _F = 1.25 A, dI _F /dt = 100 A/μs	N-Ch			75	ns
		V _{GS} = 0 V, I _F = -1.25 A, dI _F /dt = 100 A/μs	P-Ch			100	

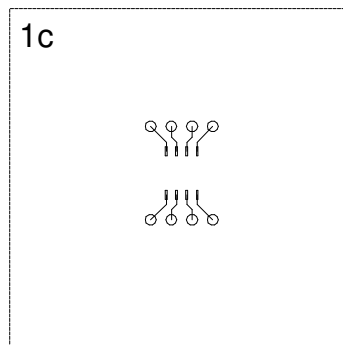
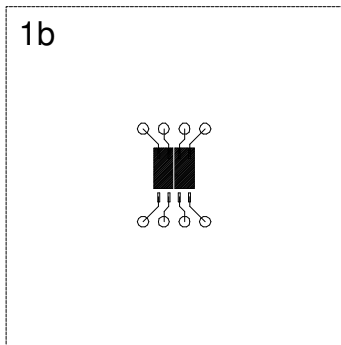
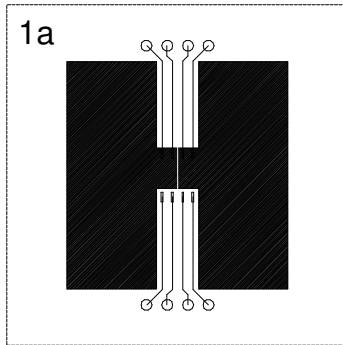
Notes:

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta J} k(t)} = \frac{T_J - T_A}{R_{\theta J} \alpha R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} \theta_{TJ}$$

Typical R_{θJA} for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 78°C/W when mounted on a 0.5 in² pad of 2oz copper.
- 125°C/W when mounted on a 0.02 in² pad of 2oz copper.
- 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

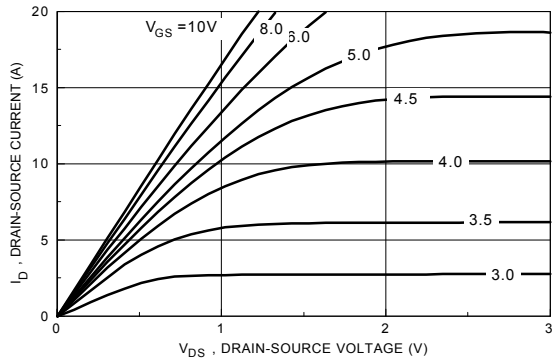


Figure 1. N-Channel On-Region Characteristics.

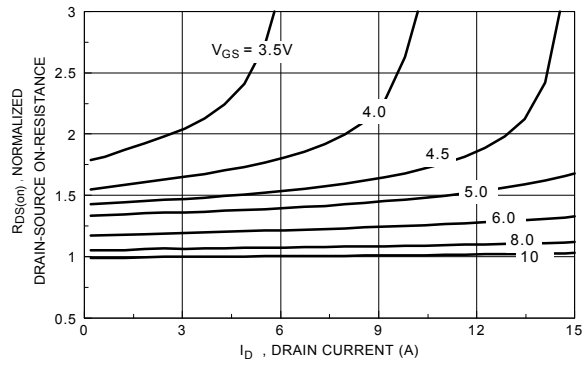


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

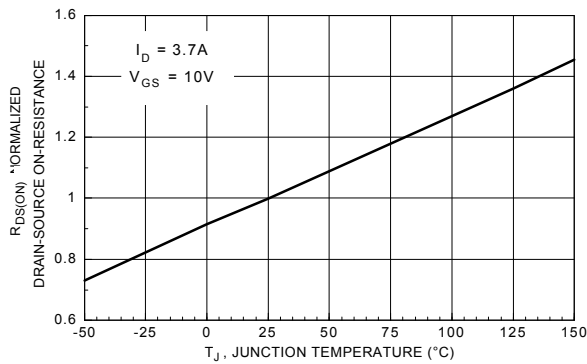


Figure 3. N-Channel On-Resistance Variation with Temperature.

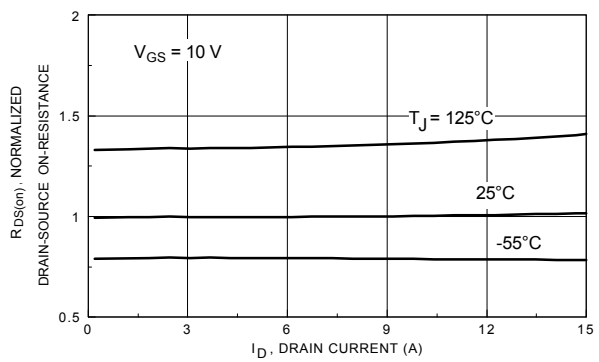


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

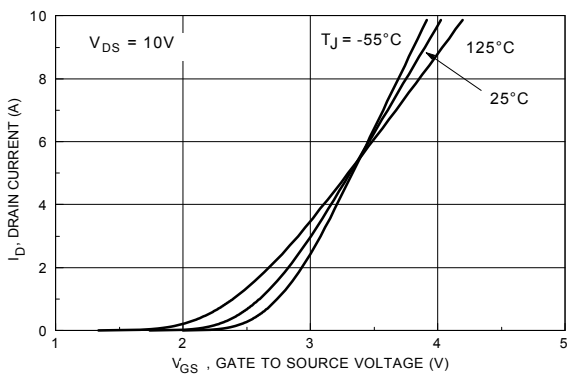


Figure 5. N-Channel Transfer Characteristics.

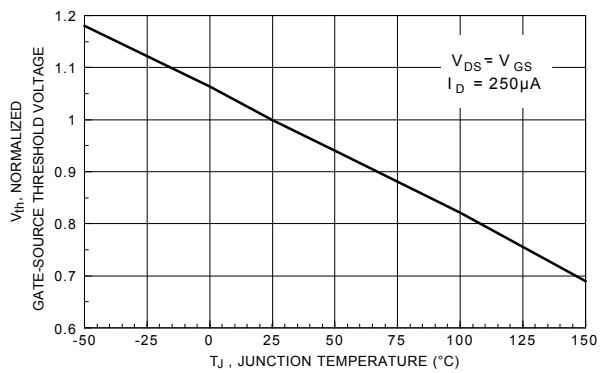


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

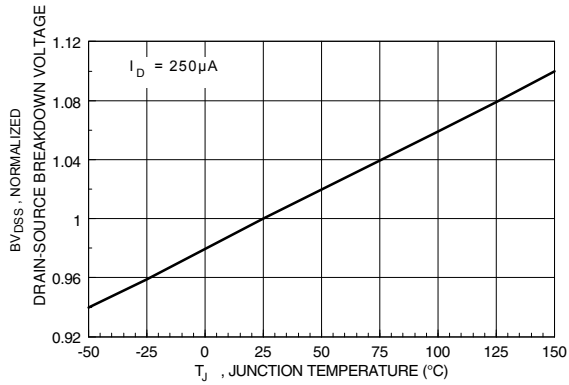


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

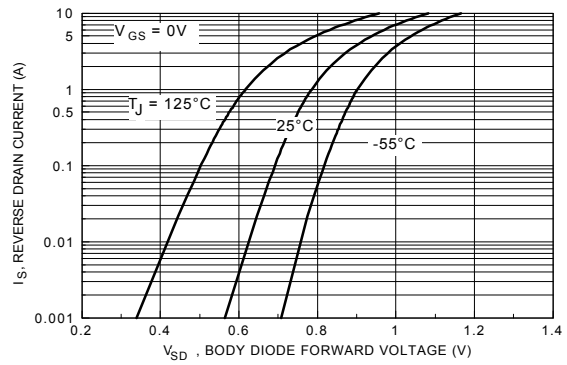


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

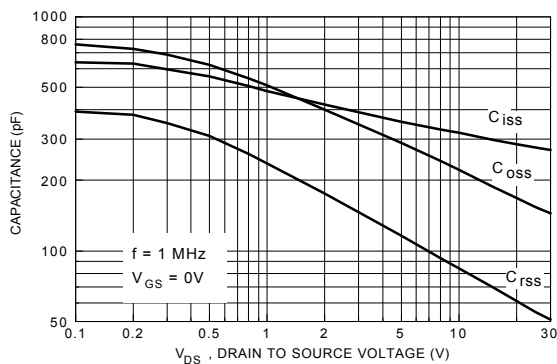


Figure 9. N-Channel Capacitance Characteristics.

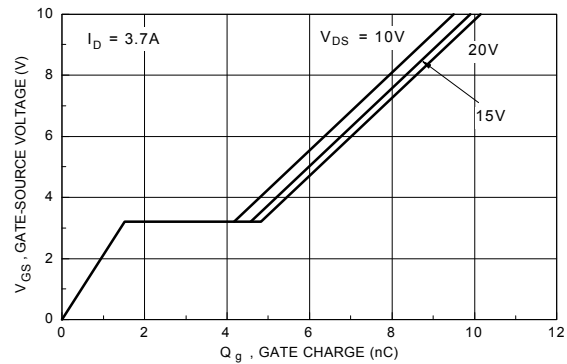


Figure 10. N-Channel Gate Charge Characteristics.

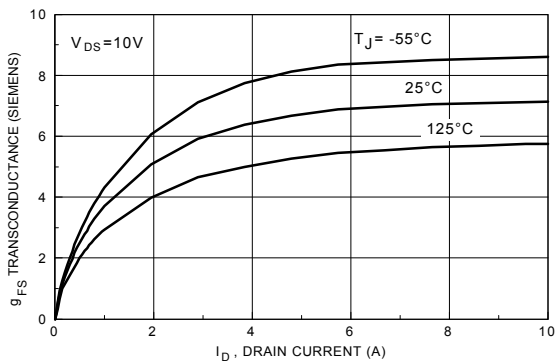


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

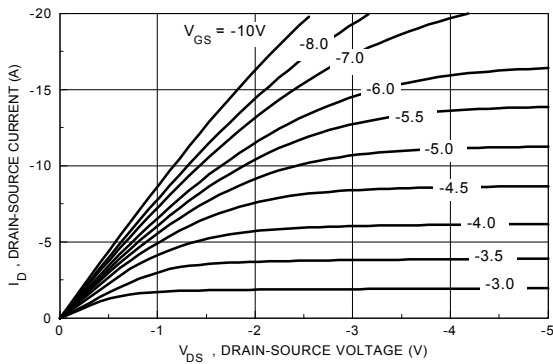


Figure 12. P-Channel On-Region Characteristics.

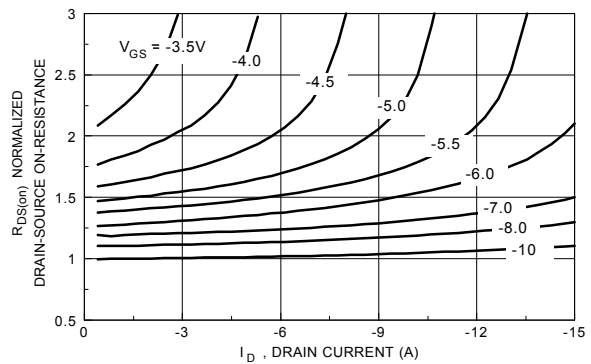


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

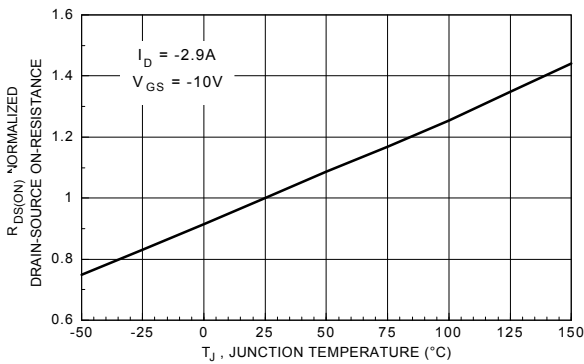


Figure 14. P-Channel On-Resistance Variation with Temperature.

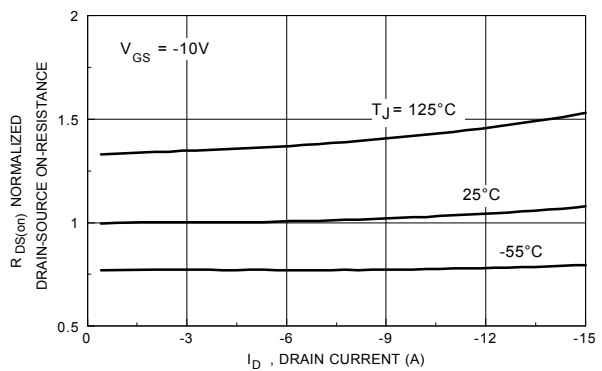


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

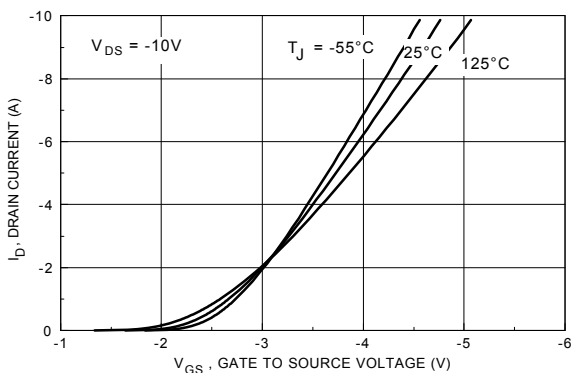


Figure 16. P-Channel Transfer Characteristics.

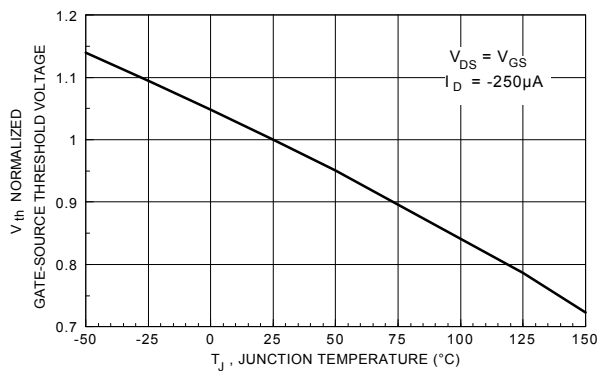


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

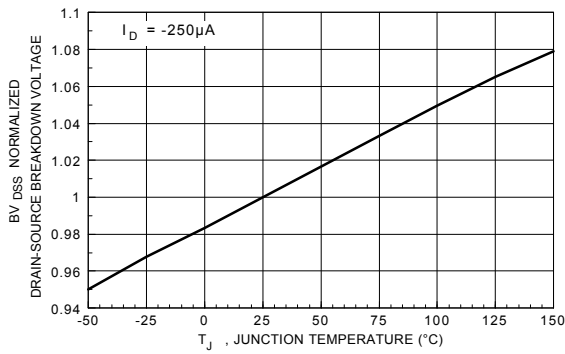


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

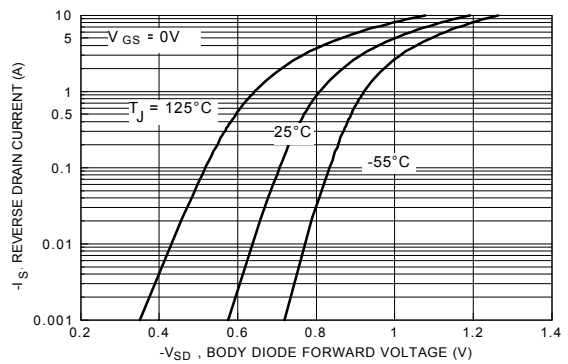


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

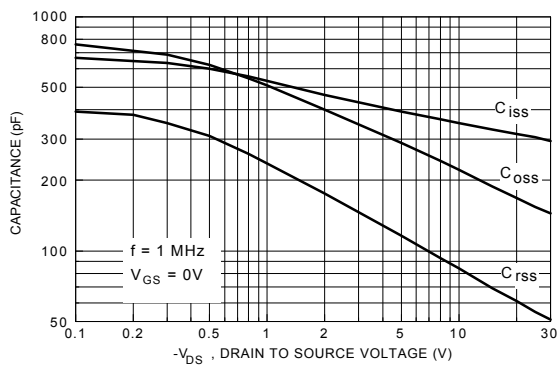


Figure 20. P-Channel Capacitance Characteristics.

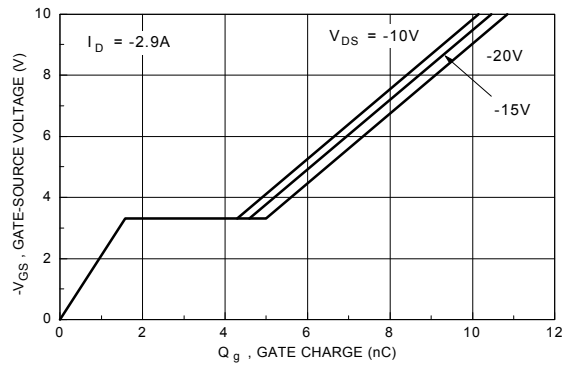


Figure 21. P-Channel Gate Charge Characteristics.

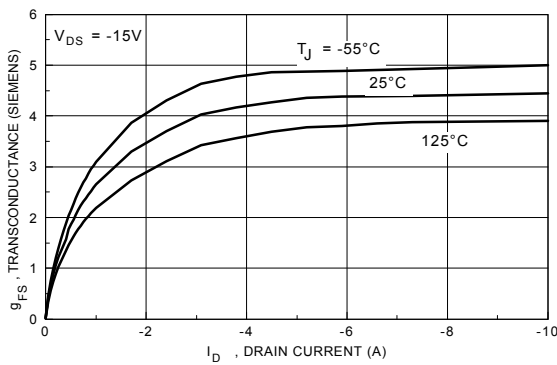


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics: N & P-Channel

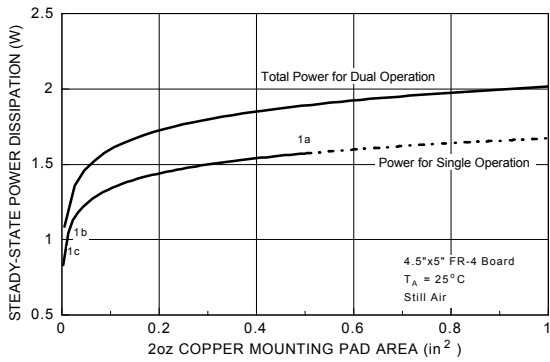


Figure 23. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

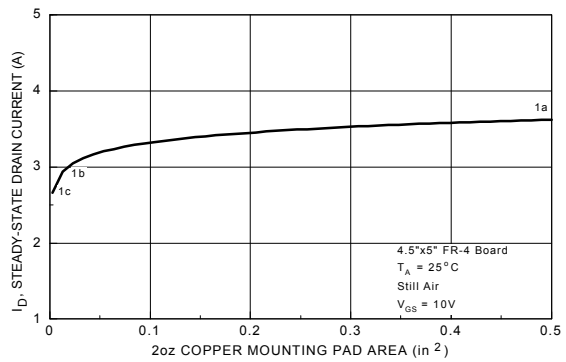


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

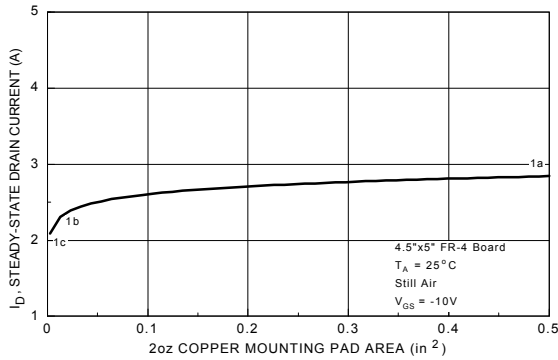


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

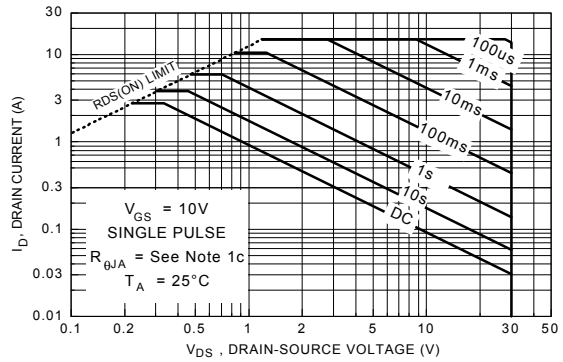


Figure 26. N-Channel Maximum Safe Operating Area.

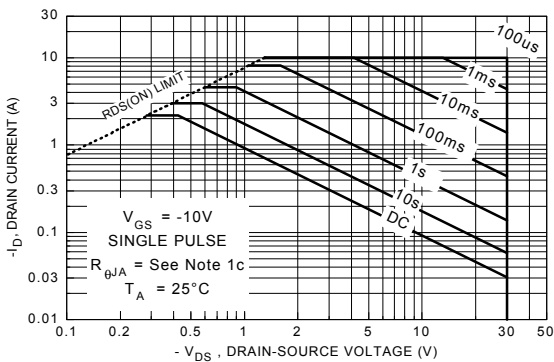


Figure 27. P-Channel Maximum Safe Operating Area.

Typical Thermal Characteristics: N & P-Channel

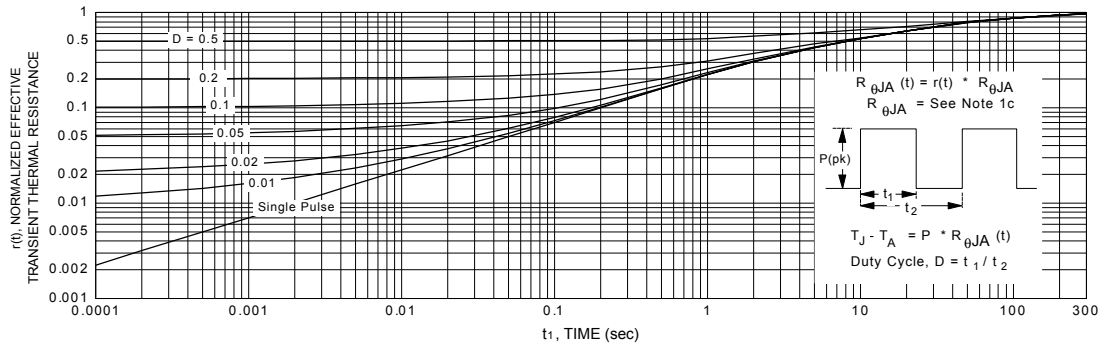


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

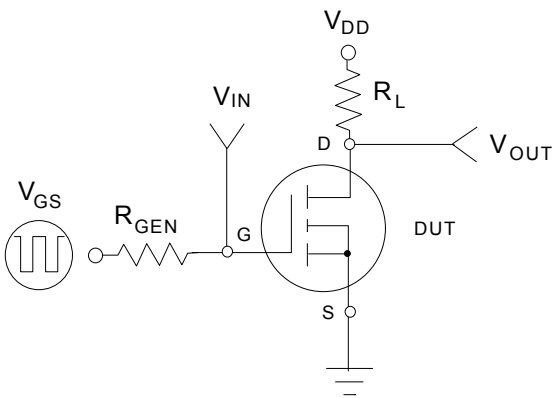


Figure 29. N or P-Channel Switching Test Circuit.

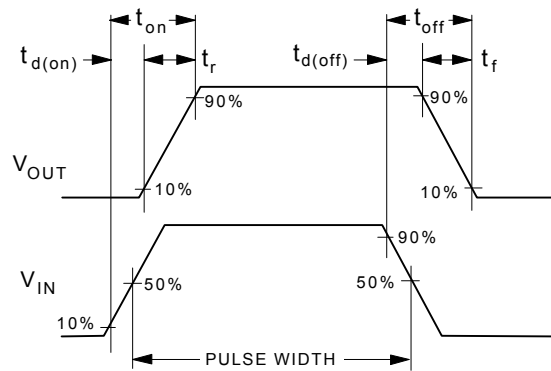


Figure 30. N or P-Channel Switching Waveforms.

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