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DATA SHEET

NE57811

Advanced DDR memory termination power with shutdown

Product data
Supersedes data of 2002 Jul 16

2003 Apr 02

Philips
Semiconductors

PHILIPS

Advanced DDR memory termination power with shutdown

NE57811

DESCRIPTION

The NE57811 is designed to provide power for termination of a Double Data Rate (DDR) SDRAM memory bus. It significantly reduces parts count, board space, and overall system cost compared to previous solutions.

The NE57811 DDR termination regulator maintains an output voltage (DDR reference bus voltage) that is one-half that of the RAM supply voltage. It is capable of providing up to ±3.5 A for sustained periods. Overcurrent limiting protects the NE57811 from inrush currents at start-up, and overtemperature shutdown protects the device in extreme temperature situations.

The SPAK-5 (SOT756) package is thermally robust for flexibility of thermal design. Because the NE57811 is a linear regulator, no external inductors or switching FETs are necessary. Fast response to load changes reduces the need for output capacitors.

FEATURES

- Fast transient response time
- Overtemperature protection
- Overcurrent protection
- Commercial (0 °C to +70 °C) temperature range
- Reduced need for external components (switching FETs, inductors, decoupling capacitors)
- Internal divider maintains termination voltage at $^1/_2$ memory supply voltage
- Reference out for other memory and control components
- Shutdown pin that may be used to put the device into low power mode
- Compatible with DDR-I (V_{DD} = 2.5 V) or DDR-II (V_{DD} = 1.8 V) SDRAM systems

APPLICATIONS

- Desktop microcomputer systems
- Workstations
- Servers
- Game machines
- Set top boxes
- Embedded systems
- Digital video recorders

SIMPLIFIED SYSTEM DIAGRAM

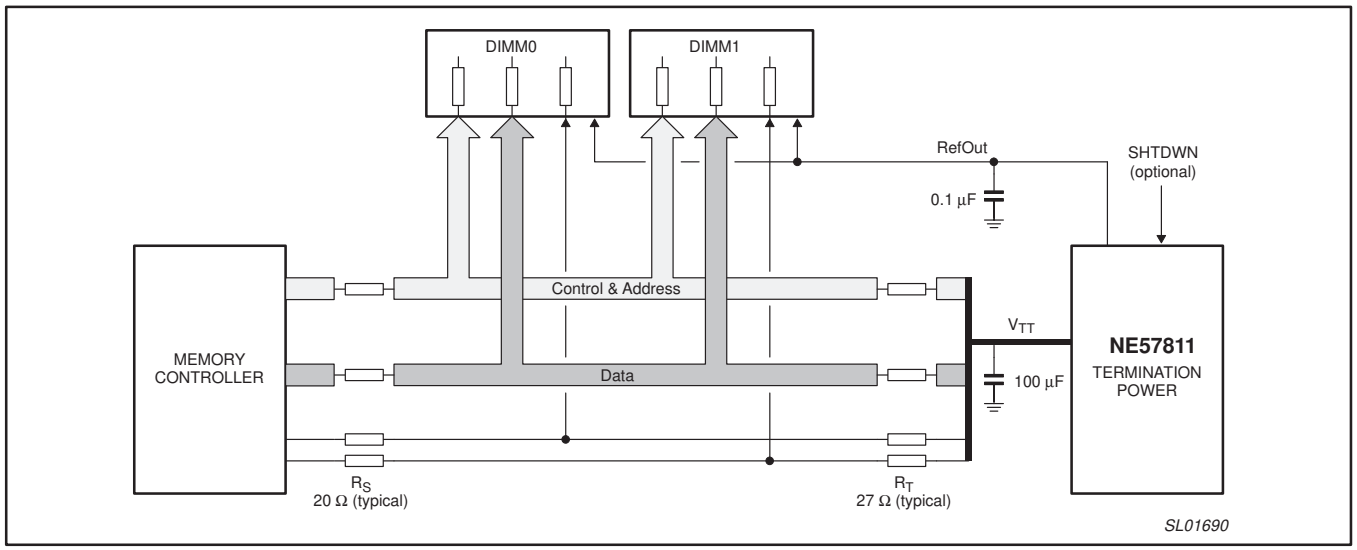


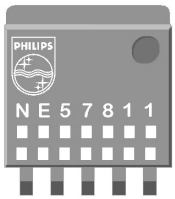
Figure 1. Simplified system diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE
	NAME	DESCRIPTION	VERSION	
NE57811S	SPAK-5	plastic single-ended surface mounted package; 5 leads	SOT756	0 °C to +70 °C

Part number marking

The package is marked with the part number under the logo. The second line indicates wafer lot number. The first four characters of the third line contain a date code. The remaining characters are manufacturing codes.



PIN CONFIGURATION

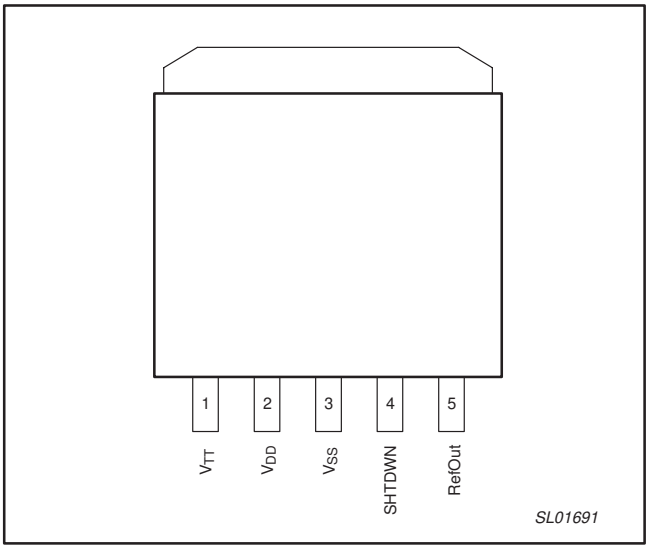


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	V_{TT}	Regulated terminator voltage
2	V_{DD}	Power supply
3	V_{SS}	Circuit ground (Note 1)
4	SHTDWN	Shutdown
5	RefOut	Reference voltage out

NOTE:

1. The thermal backside pad connects electrically to V_{SS} internally and provides enhancement to thermal conductivity, but it should not be used as the primary connection to ground. Device specifications apply to use of the V_{SS} pin as the connection to ground.

MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	V_{DD} to V_{SS} voltage	–0.3	–	+3.6	V
T_{amb}	Operating ambient temperature	0	–	+70	°C
T_{stg}	Storage temperature	–40	–	+165	°C
T_j	Junction temperature	–	–	160	°C
$R_{th(j-a)}$	Thermal resistance, junction to ambient	–	16.5	–	°C/W
P_D	Power dissipation (Note 1)	–	–	3.3	W

NOTE:

1. Tested on a minimum footprint on a four-layer PCB per JEDEC specification JESD51-7.

ELECTRICAL CHARACTERISTICS

T_{amb} = 0 °C to +70 °C, V_{DD} = 2.5 V; I_{TT} = –3.5 A to +3.5 A, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{TT}	Output voltage		–	$V_{DD}/2$	–	V
V_{ACC}	Output voltage accuracy (Note 4)	I_{TT} = 0 A	–15	–	+15	mV
V_{DD}	Supply voltage		1.6	–	3.6	V
$I_{Q(op)}$	Supply current	I_{TT} = 0 A	–	14	30	mA
$I_{Q(SD)}$	Standby quiescent current	Standby asserted	–	1.2	1.35	mA
I_{TT}	Output current	V_{DD} = 2.5 V ≤ V_{DD} ≤ 3.6 V	–3.5	–	+3.5	A
		V_{DD} = 1.6 V	–2.5	–	+2.5	A
ΔV_{TT}	Load regulation	I_{TT} = ±1.0 A	–	±6	–	mV
		I_{TT} = ±3.5 A	–18	–	+18	mV
C_{LOAD}	Load capacitance (Note 2)	Stable operation	–	100	–	µF
Reference Out						
RefOut	Voltage reference out (Note 3)	IrefOut = 0 A; source or sink	–15	$V_{DD}/2$	+15	mV
IrefOut	Reference Out current max		2.2	3	–	mA
C_{LOAD}	Load capacitance	Stable operation	0.1	–	–	µF
Power Stage						
I_{lim}	Current limit		3.6	4.5	5.6	A
T_{lim}	Temperature shutdown		–	+150	–	°C
	Temperature shutdown hysteresis		–	20	–	°C

NOTES:
1. Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
2. Ceramic capacitors only. Low ESR electrolytic capacitors are not necessary.
3. RefOut voltage referenced to $^1/_2$ V_{DD}.
4. $V_{ACC} = V_{TT} - V_{DD}/2$.

TYPICAL PERFORMANCE CURVES

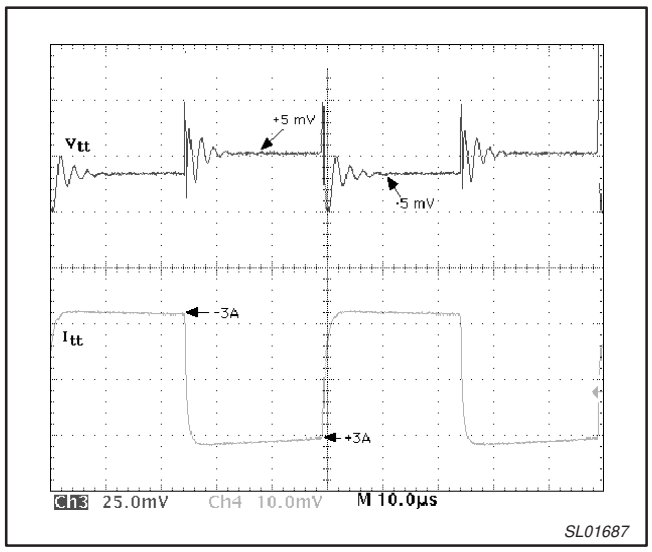


Figure 3. V_{TT} transient response (output filter 50 µF ceramic)

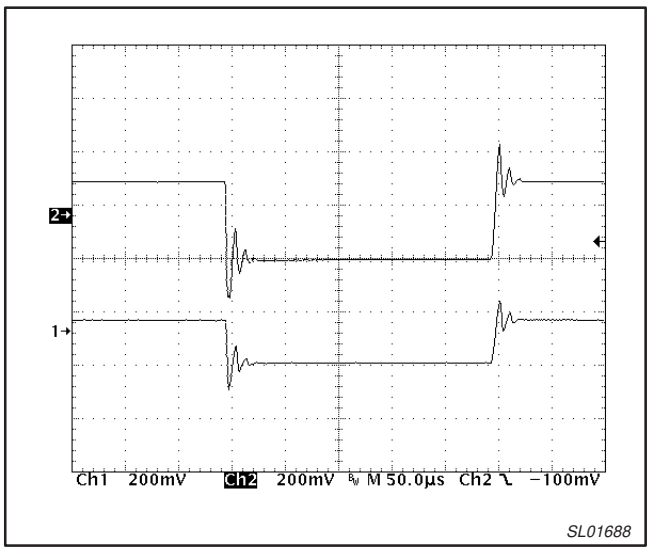


Figure 4. V_{DD}-to-V_{TT} response (output filter 50 µF ceramic)

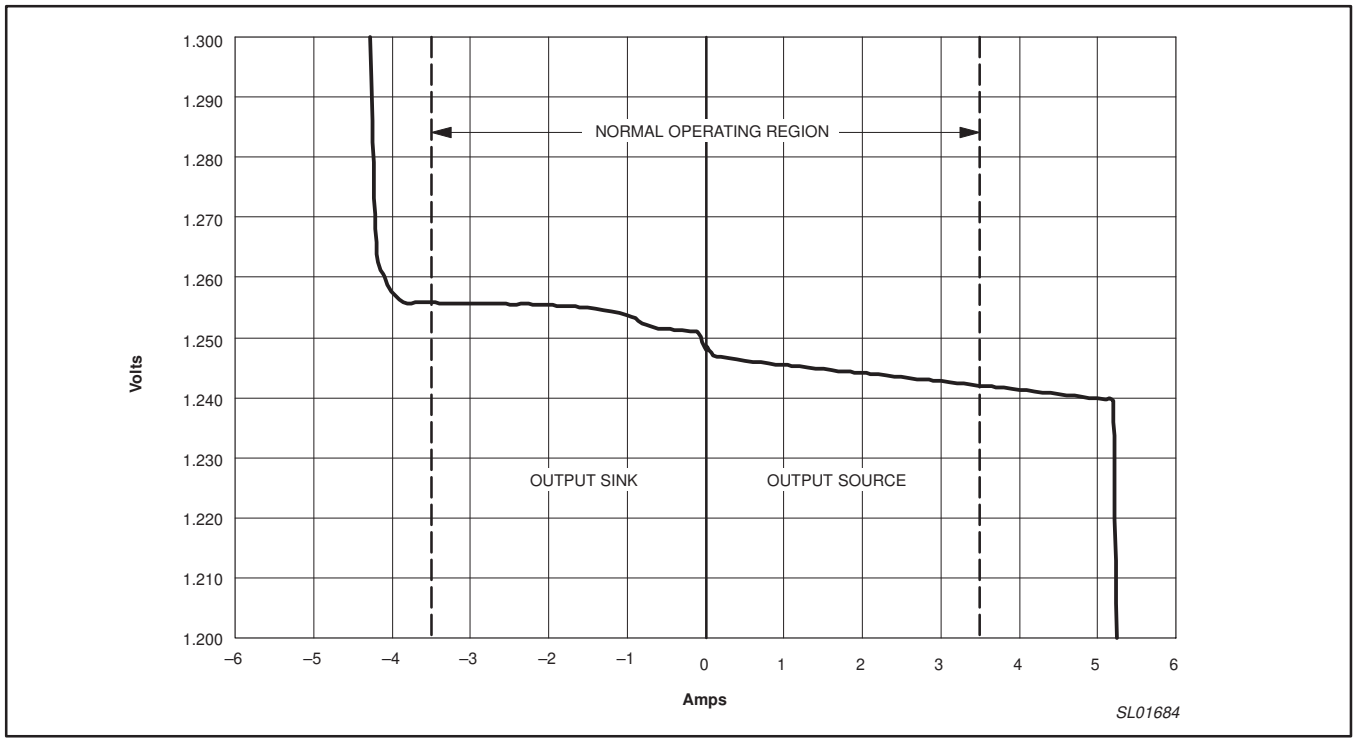


Figure 5. Typical V_{TT} versus output current (V_{DD} = 2.5 V @ 25 °C)

TECHNICAL DISCUSSION

The NE57811 supplies power to the DDR memory bus termination resistors at nominally $^1/_2$ the voltage supplied to the memory ICs or DIMMs. DDR memory output drivers source and sink current into and out of their outputs. A typical DDR memory system is seen in Figure 1 (page 2). Each input/output pin on the bus has a series 20 Ω resistor connected to it. The bus is terminated to the DDR terminator though a 27 to 50 Ω resistance. The memory system will then require current from the V_{TT} terminator bus only when the instantaneous value of the aggregate bus state are not equal amounts of 1s and 0s. When memory bus speeds are in the 200–300 MHz region, the period of any single bus state is extremely small. This permits the DDR bus termination regulator to be a linear 'power Op Amp' that can source and sink current instantly to the DDR bus from the V_{DD} supply voltage.

Figure 6 models the V_{TT} loading condition of each bus line equivalent circuit during operation and with terminating resistors.

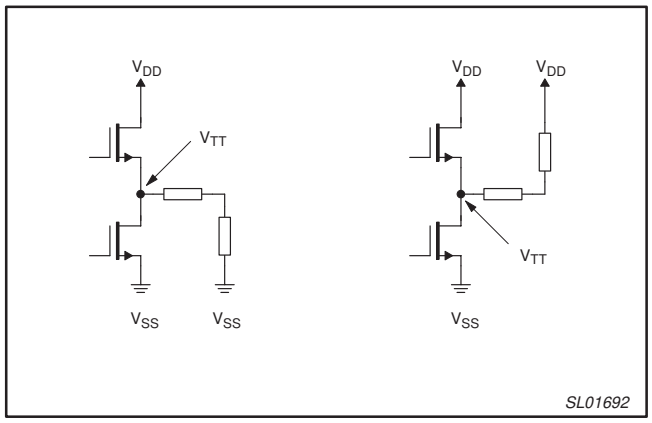


Figure 6. V_{TT} loading conditions.

This yields the worst case current loading equation:

$$I_{O(max)} = \frac{N_{DDR}\ V_{DD}}{2(R_T + R_S)}$$

Where:

N_{DDR} is the total number of terminated control, address and data lines within the DDR memory system. (typically 192)

R_T is the value of the terminating resistors.

R_S is the value of the series resistors from the active output driver.

Hence the worst-case current loading condition, where there are either all 1s or all 0s for an instant, and R_T is 27 Ω and R_S is 20 Ω, produces an instantaneous output current of either + or – 3.5 Amperes.

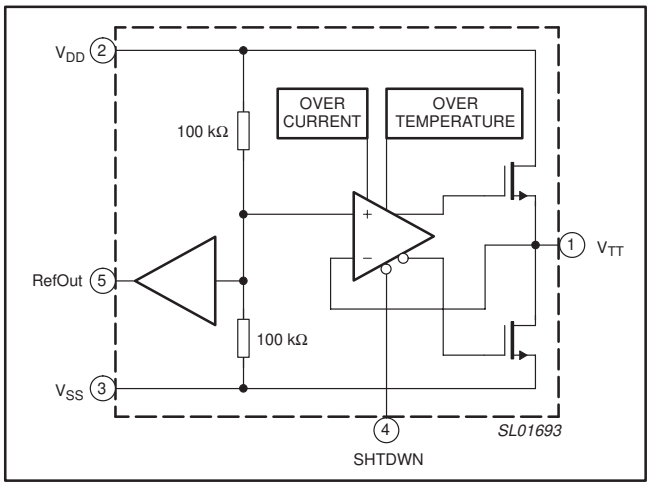


Figure 7. Block diagram.

THERMAL DESIGN

Designing the proper thermal system for the NE57811 is important to its reliable operation. The NE57811 will be operating at an average power level less than the maximum rating of the part. In a typical DDR terminator system the average power dissipation is between 0.8 and 1.5 watts. The termination power will vary as the average number of '1s' and '0s' changes during normal operation of the DDR memory. The load current will assume a new value for each bus cycle at a 266 MHz rate, and will increase and decrease as the statistical average of bus states change.

The terminator heatsink must be designed to accommodate the average power as a steady state condition and be able to withstand momentary periods of increased dissipation, typically 2 – 5 seconds duration. For the typical NE57811 application, the power dissipated by the terminator can be calculated:

$$P_D = I_{DD(VTT)} Watts \quad \textbf{Eqn. (1)}$$

The thermal resistance of a surface mount package is given as $R_{th(j\text{-}a)}$, the thermal resistance from the junction to air. JESD51-7 specifies a 4-layer multiplayer PCB (2oz/1oz/1oz/2oz copper) that is 4 inches on each side. This is probably the best (or lowest) thermal resistance you will see in any application. Most applications cannot afford the PCB area to create this situation, but the thermal performance of a multilayer PCB will still provide a significant heatsinking effect. The actual thermal resistance will be higher than the 16.5 °C/W given for the 4-layer JEDEC PCB.

Figure 8 shows the thermal resistance you can expect for heatsinking PCB areas less than the JEDEC specification. The graph is for a 2 oz. single-sided PCB with a square area of the side dimension as given on the X axis. If you use a double-sided PCB with some plated-through holes to help transfer heat to the bottom side, the thermal resistance only improves by about 3 – 4 °C/W.

After the power is estimated, the minimum PCB area can be determined by calculating the worst case thermal resistance and referring to Figure 8 to determine the PCB area. This is done by:

$$R_{qJA(min)} = \frac{T_j - T_{amb}}{P_D} \quad \textbf{Eqn. (2)}$$

Where:

T_j is the maximum desired junction temperature
T_{amb} is the highest expected local ambient temperature
P_D is the estimated average power

The junction temperature should be kept well away from the over-temperature cutoff threshold temperature (+150 °C) in normal operation.

Using the above power dissipation, the highest ambient temperature and a junction temperature of +125 °C, calculate the maximum thermal resistance (1.5 watts is used only as an example).

$$R_{th(j-a)(min)} = \frac{125\ ^oC - 70\ ^oC}{1.5W} = 36.6\ ^oC/W \quad \textbf{Eqn. (3)}$$

Looking at Figure 8, you see that this power dissipation requires a minimum PCB island area of 225 mm^2 (15 mm on each side). This is the smallest area you could use at this power dissipation. Of course, increasing this area will allow the NE57811 to operate at cooler temperatures, thus enhancing its long-term reliability.

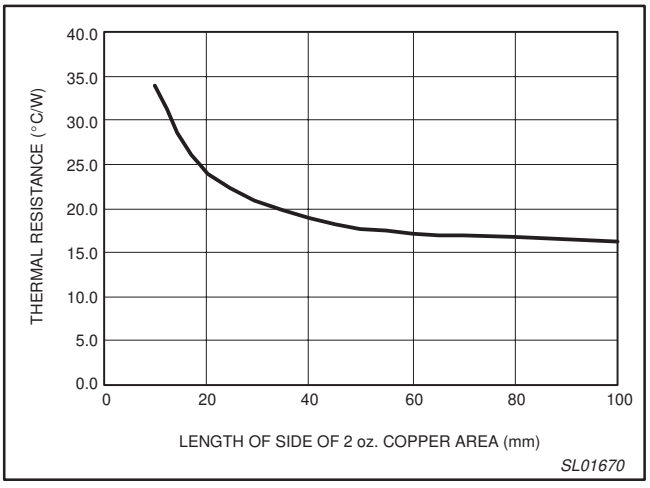


Figure 8. PCB heatsink area versus thermal resistance.

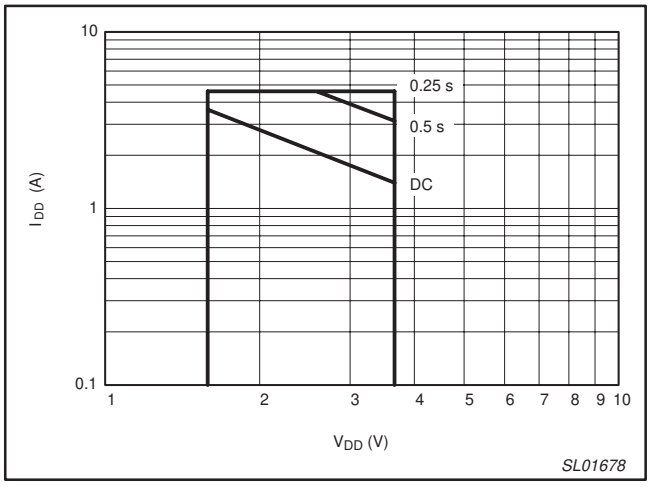


Figure 9. Safe operating area for the NE57811.

APPLICATION INFORMATION

The NE57811 can be used in a variety of DDR memory configurations. Its small footprint, fast transient response and lessened need for large bulk output capacitance, makes it highly adaptable. Some of these methods of use are given below.

Normal operating mode ($V_{TT} = V_{DDR}/2$)

The most common implementation of a DDR terminator regulator using the NE57811 is shown in Figure 10. The NE57811 has an internal resistor divider between the V_{DD} (pin 2) and V_{SS} (pin 3) pins which maintains the output voltage, V_{TT}, at $V_{DD}/2$. Typically, the V_{DD} voltage is the DDR RAM supply voltage, which can range from 1.8 V to 2.5 V. The center node of this resistor divider is the reference for the V_{TT} output voltage and the buffered RefOut signal (pin 5).

There are two components to the memory signal load: a high frequency component caused by the 266 MHz plus speed of the address, data, and control buses, and a low frequency component caused by the time-average skew of all of the bus states away from an equal number of 1s and 0s. Electrolytic and tantalum capacitor appear inductive at the high frequencies. Therefore two types of capacitors are needed for the output filtering.

A very good, low ESR electrolyic capacitor of no less than 470 µF should be placed next to the terminator, which should be placed as close as possible to the memory array. One half of the high frequency filter capacitors should be to V_{DD} and the other half to V_{SS} so that the output will better track any variations in the V_{DD} voltage.

For different memory sizes, the values of the recommended output filter capacitances will change. For a 256 MByte memory space, for example, approximately 100 µF of ceramic surface mount chip capacitors should be evenly distributed across the physical memory layout. Depending upon the PCB noise environment, this could be 10 pieces of 10 µF, 20 pieces of 5 µF, and so on.

It might be possible to reduce the total capacitance, provided the performance remains stable. Examine the behavior of the V_{TT} bus carefully when the system is operating and verify that deviations in the bus voltage do not exceed the DDR specification (±40 mV).

Use of the SHTDWN signal and low power mode

The NE57811 provides an optional SHTDWN pin that may be used to put the device into low power mode. When $\overline{\text{SHUTDOWN}}$ is asserted (LOW), the V_{TT} power amplifier is turned off and the output is 3-Stated. This brings the quiescent current of the entire device to less than 800 µA.

If the pin is not externally connected, and internal 10 kΩ resistor biases the control logic to V_{DD} causing the output sections to be turned on and the NE57811 operates normally.

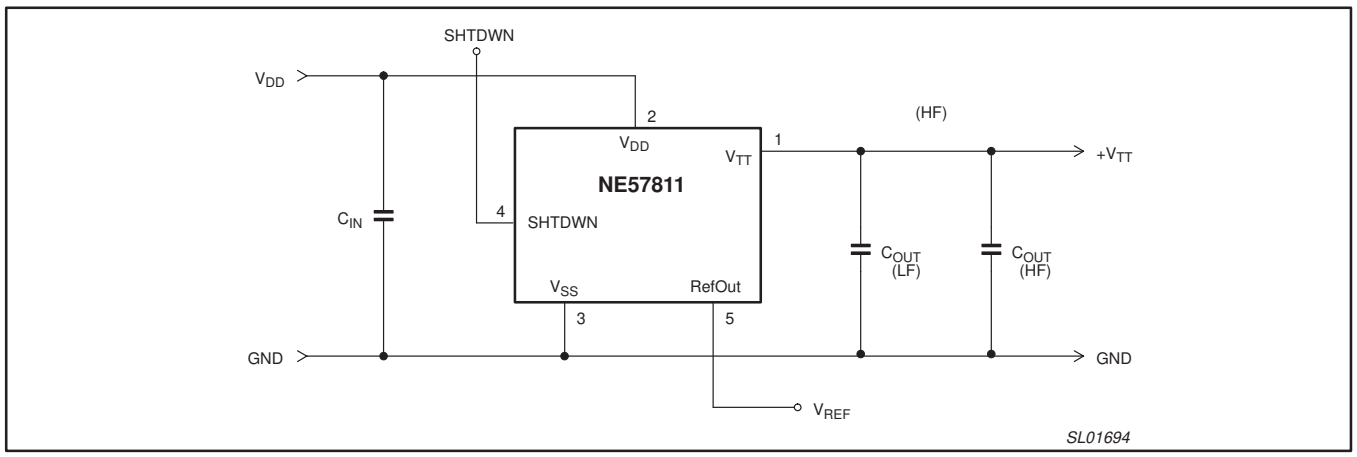


Figure 10. Normal operating method ($V_{TT} = V_{DD}/2$)

TEST CIRCUITS

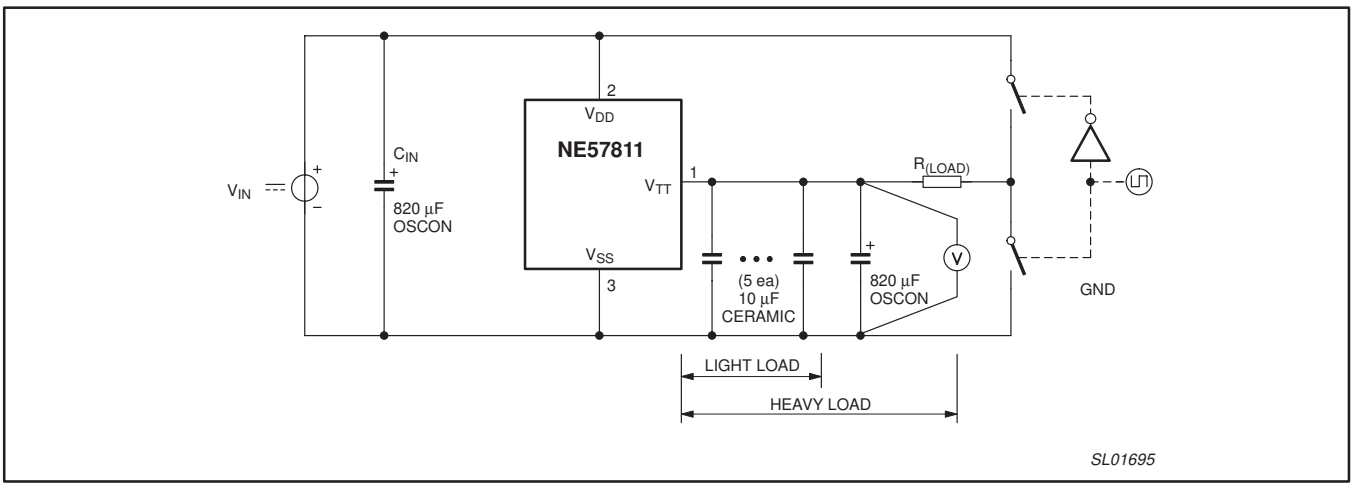


Figure 11. Load transient test (+3 A – –3 A).

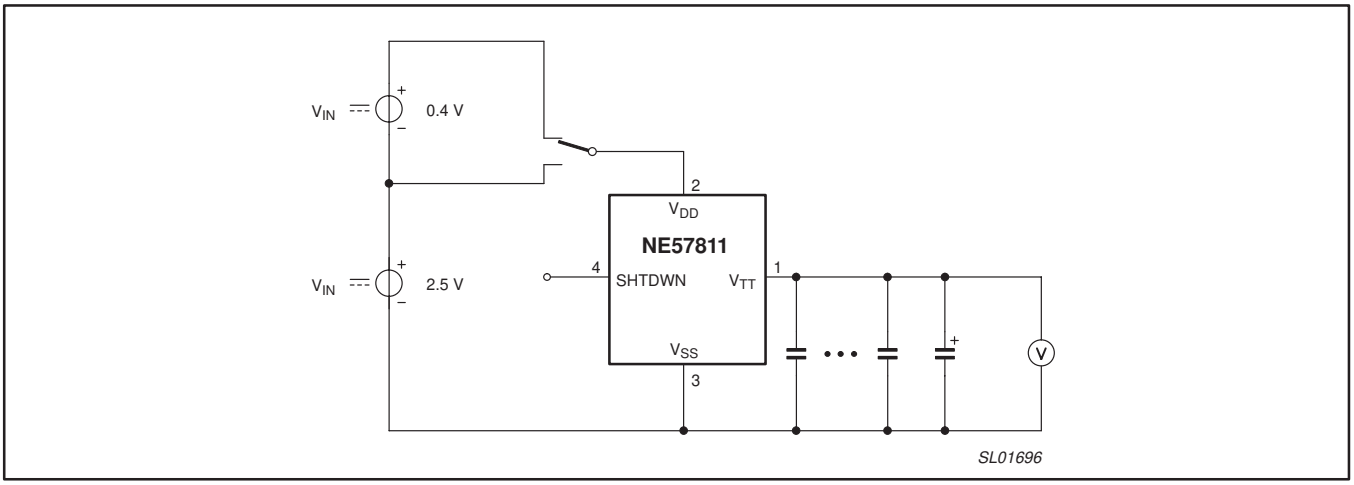


Figure 12. V_{DD} to V_{TT} transient test.

PACKING METHOD

The NE57811 is packed in reels, as shown in Figure 13.

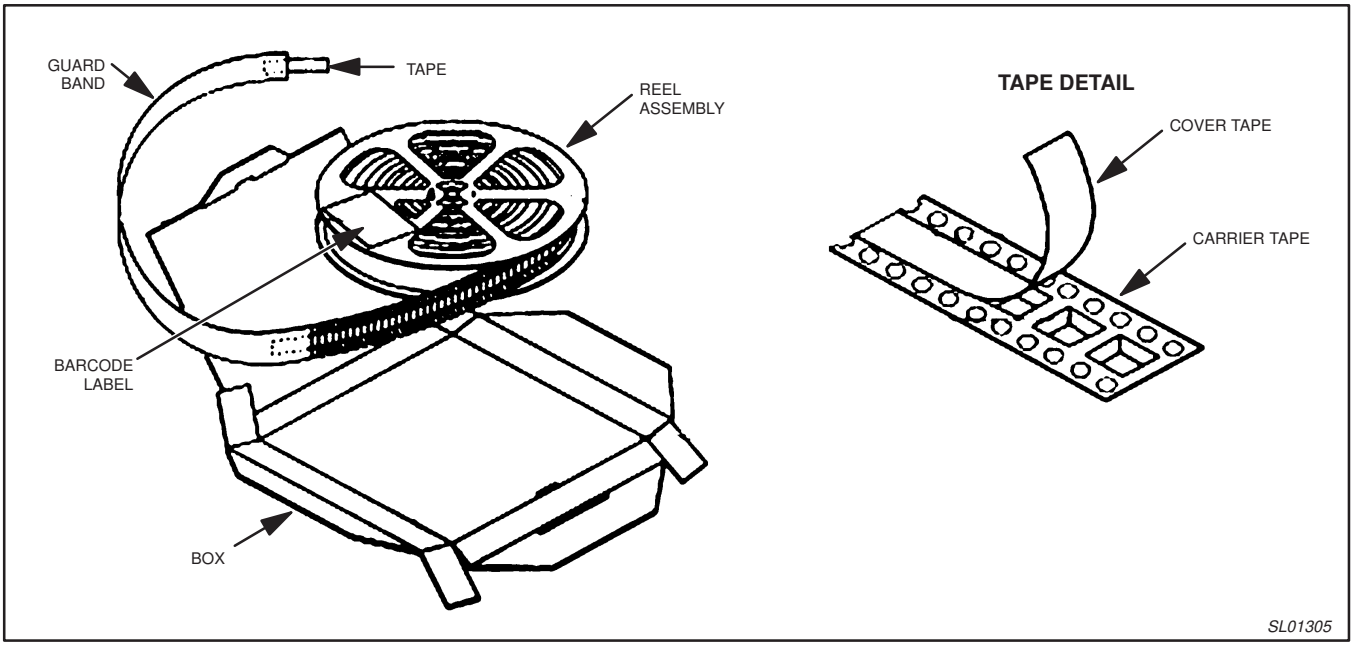
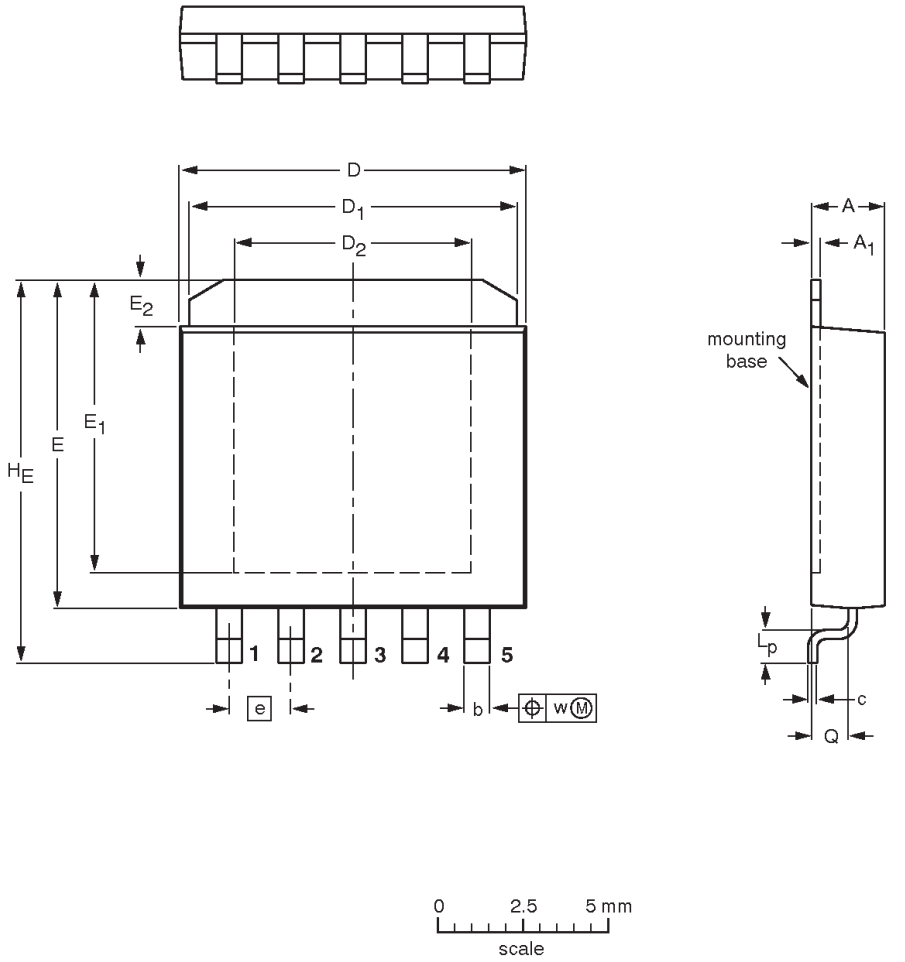


Figure 13. Tape and reel packing method.

Plastic single-ended surface mounted package; 5 leads **SOT756**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b	c max.	D	D_1	D_2 max.	E	E_1 max	E_2	e	H_E	L_p	Q	w
mm	2.03 1.78	0.25	0.79 0.63	0.25	9.52 9.27	9.14 8.89	6.5	9.40 8.63	8.03	1.27 0.76	1.7	10.67 10.41	1.04 0.79	1.14 0.89	0.25

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT756						~~02-03-25~~ 02-03-29

REVISION HISTORY

Rev	Date	Description
_2	20030402	**Product data (9397 750 11216). ECN 853-2360 29724 of 28 March 2003. Supersedes data of 2002 Jul 16.** Modifications: • Page 4, Electrical characteristics table: – (description): from "T_{amb} = 25 °C" to "T_{amb} = 0 °C to +70 °C" – Output voltage accuracy: add symbol "V_{ACC}"; add Note 4; change Min. value from "–10" to "–15"; change Max. value from "+10" to "+15". – Change symbol "I_Q" to "$I_{Q(op)}$"; change Typ. value from "20" to "14" – Add $I_{Q(SD)}$ row to table. – I_{TT}: change Condition from "V_{DD} = 2.25 – 3.6 V" to "2.5 V ≤ V_{DD} ≤ 3.6 V". – ΔV_{TT}, under condition I_{TT} = ±3.5 A: change Min. value from "–20" to "–18"; change Max. value from "+20" to "+18". – RefOut: add condition "IrefOut = 0 A; source or sink"; change Min. value from "–10" to "–15"; change Max. value from "+10" to "+15". – Change subheading row from "Protection" to "Power Stage".
_1	20020716	**Product data (9397 750 10151). ECN 853-2360 28625 of 16 July 2002.**

Advanced DDR memory termination power with shutdown

NE57811

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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