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NET+Works™ for NET+ARM Hardware Reference Guide

This guide provides a description of the NET+ARM 15/40 hardware.

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Conventions

Conventions used in this guide are described as follows.

Convention	Description
Italic type	Used for emphasis and for book and manual titles, and reference documents.
Bold type	Used to indicate specific choices within instructions in procedures. For example, Click on **Software Installation**.
signal, signal*	All signals are active high unless suffixed with an asterisk (*) in which case they are active low.

Note:

- All configuration register settings are reset to their inactive state unless otherwise noted.
- All addresses are defined in hexadecimal unless otherwise noted.

Structure of this Guide

- Chapter 1, *Introduction*, contains information about the NET+ARM chip, its features, the applications in which it can be used, and the pins that support the ENI interface.
- Chapters 2 through 11 contain information on the CPU core and the various modules.
- Chapter 12, *Test Support*, contains information on the various tests that NET+ARM supports, including ATPG, PLL, BIST, ATE, and ARM debugging.
- Chapter 13, *Electrical Specifications*, contains information on DC and AC characteristics, output rise and fall timing, and crystal oscillator specifications.
- Chapter 14, *NET+ARM Package Guide*, contains information on the NET+ARM chip package and dimensions.

Related Documentation

- *NET+Works Getting Started Guide*
- *NET+Works Software Reference Guide* provides a description of the Application Programming Interfaces (APIs) for developing HTML pages.
- *NET+Works User's Guide* explains how to use the NET+Works toolkit to develop programs for your application and hardware.

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Table of Contents

Chapter 1
Introduction

The NETsilicon NET+ARM chip is a single chip 32-bit RISC processor containing an integrated 10/100 Mbit Ethernet MAC and all the peripherals (other than RAM or ROM) required to complete an embedded networking peripheral application.

1.1 NET+ARM Chip Overview

CPU Core

- 32-bit RISC Processor
- 3rd Party Software Support
- 32-bit Internal Bus
- 2 Programmable Timers
- 2 Async Serial Ports
- 4K Cache (NET+40 only)

Bus Interface

- 8-bit, 16-bit, and 32-bit peripherals
- 28-bit External Address Bus
- Multi-master Support
- Normal and Burst Cycles
- 5 Programmable Chip-Selects
- Glueless Interface Flash & DRAM
- Configurable Endian Support

Integrated Ethernet Support

- 10/100 Mbit Media Access Controller MII Interface to External Ethernet PHY
- Bi-directional Capability
- Address Filtering
- Dedicated DMA Support

Integrated ENI Interface

- 4-Port IEEE 1284 Host Interface
- ENI Host Interface
- Register-Mode Interface
- DMA Support

Low Power 3.3V Operation

1.2 NET+ARM Chip Key Features

32-bit ARM7TDMI RISC Processor

- Full 32-bit ARM Mode
- Extremely Cost-efficient 16-bit Thumb Mode
- 15 General Purpose 32-bit Registers
- 32-bit Program Counter and Status Register
- 5 Supervisor Modes, One User Mode
- 15 MIPS Peak Performance - NET+ARM-15 chip and 40 MIPS Peak Performance - NET+ARM-40 chip
- 3rd-Party Software Support

Integrated 10/100 Ethernet MAC

- 10/100 MII-based PHY Interface
- 10Mbit ENDEC Interface
- Supports TP-PMD and Fiber-PMD Devices
- Full Duplex
- Optional 4B/5B Coding
- Full Statistics Gathering (SNMP & RMON)
- Station, Broadcast, Multicast Address Detection & Filtering
- 128 Byte Transmit FIFO
- 2K Receive FIFO
- Intelligent Receive Side Buffer Selection

10 Channel DMA Controller

- 2 Dedicated to Ethernet Transmit and Receive
- 4 Dedicated to Serial Transmit and Receive
- 4 Dedicated to P1284/ENI Interface
- Flexible Buffer Management
- 2 Channels Configurable for External Peripherals

P1284/ENI Interface

- 4 IEEE 1284 Parallel Ports
- 64K Shared RAM ENI Interface (8 or 16 bit)
- Full Duplex FIFO Mode Interface (8 or 16 bit)
- 32 Byte Transmit/Receive FIFO Mode FIFOs

Serial Ports

- 2 Fully Independent Serial Ports (UART, HDLC, SPI)
- 32-Byte Transmit/Receive FIFOs
- Internal Programmable Bit-rate Generators
- Bit Rates from 75 to 518400 in 16X Mode
- Bit Rates from 1200 to 4Mbps in 1X Mode
- Odd, Even, or No Parity
- 5, 6, 7, or 8 Bits
- 1 or 2 Stop Bits
- Both Internal and External Clock Support
- Receive Side Character and Buffer Gap Timers
- 4 Receive Side Data Match Detectors

Bus Interface

- 5 Independent Programmable Chip Selects
- Supports 8-, 16-, and 32-bit Peripherals
- Supports External Address Decoding and Cycle Termination (32-bit peripherals only)
- Supports Dynamic Bus Sizing
- Supports ASYNC and SYNC Peripheral Timing

- All Chip Selects Supports SRAM, FD/EDO DRAM, SDRAM, Flash, EEPROM Without External Glue
- Internal DRAM Address Multiplexing
- Internal Refresh Controller (CAS before RAS)
- 256M Byte Addressing per Chip Select
- Burst-mode Support
- 0-15 Wait States per Chip Select
- Bootstrap Support
- External Bus Master Support
- Supports Internal or External Bus Arbiters

Timers

- Two Independent Programmable Timers (200 us to 500 ms)
- Programmable Watch-Dog Timer (Interrupt or Reset on Expiration)
- Programmable Bus Timer

General Purpose I/O

- 24 Programmable I/O Interface Pins
- 4 Pins with Programmable Interrupt

Clock Generator

- Requires Only a Simple External Crystal
- On-board Programmable Phase Lock Loop
- Supports Direct External Clock Input as well

Package

- 208-pin Plastic Quad Flat Pack (0.020 inch; 0.5 mm pitch)

Power

- 750mW Maximum (outputs switching)

Operating Voltage

- 3.0 - 3.6 Volts

Figure 1-1 provides an overview of the modules that make up the NET+ARM chip.

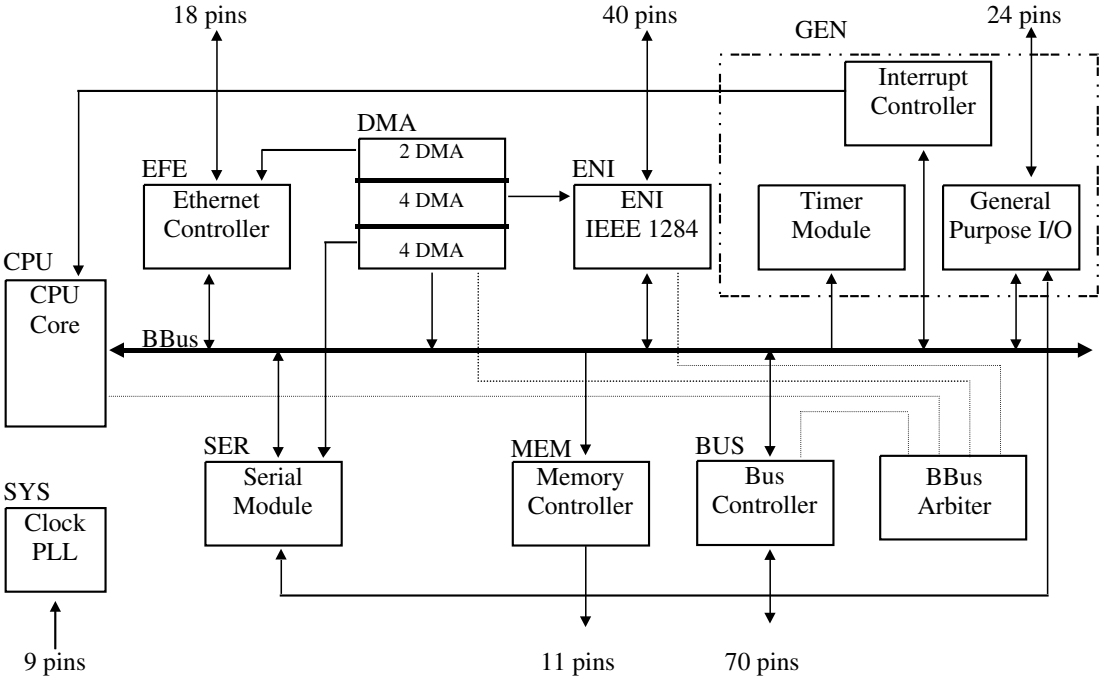

Figure 1-1: NET+ARM Chip Module Block Diagram

1.3 NET+ARM Chip Applications

The NET+ARM chip can be used in any embedded environment requiring networking services in an Ethernet LAN. The NET+ARM chip contains an integrated ARM RISC processor, 10/100 Ethernet MAC, serial ports, IEEE 1284 parallel ports, memory controllers, and parallel I/O. The NET+ARM chip can interface with another processor using a register or shared RAM interface. The NET+ARM chip provides all the tools required for any embedded networking application.

Figure 1-2 shows a typical hardware design used in an embedded networking application. The NET+ARM chip can attach to another processor system using the 1284, ENI shared RAM, or ENI FIFO interfaces. Also, additional application-specific hardware can be attached to the NET+ARM chip system bus for custom applications that make use of the NET+ARM chip internal RISC processor.

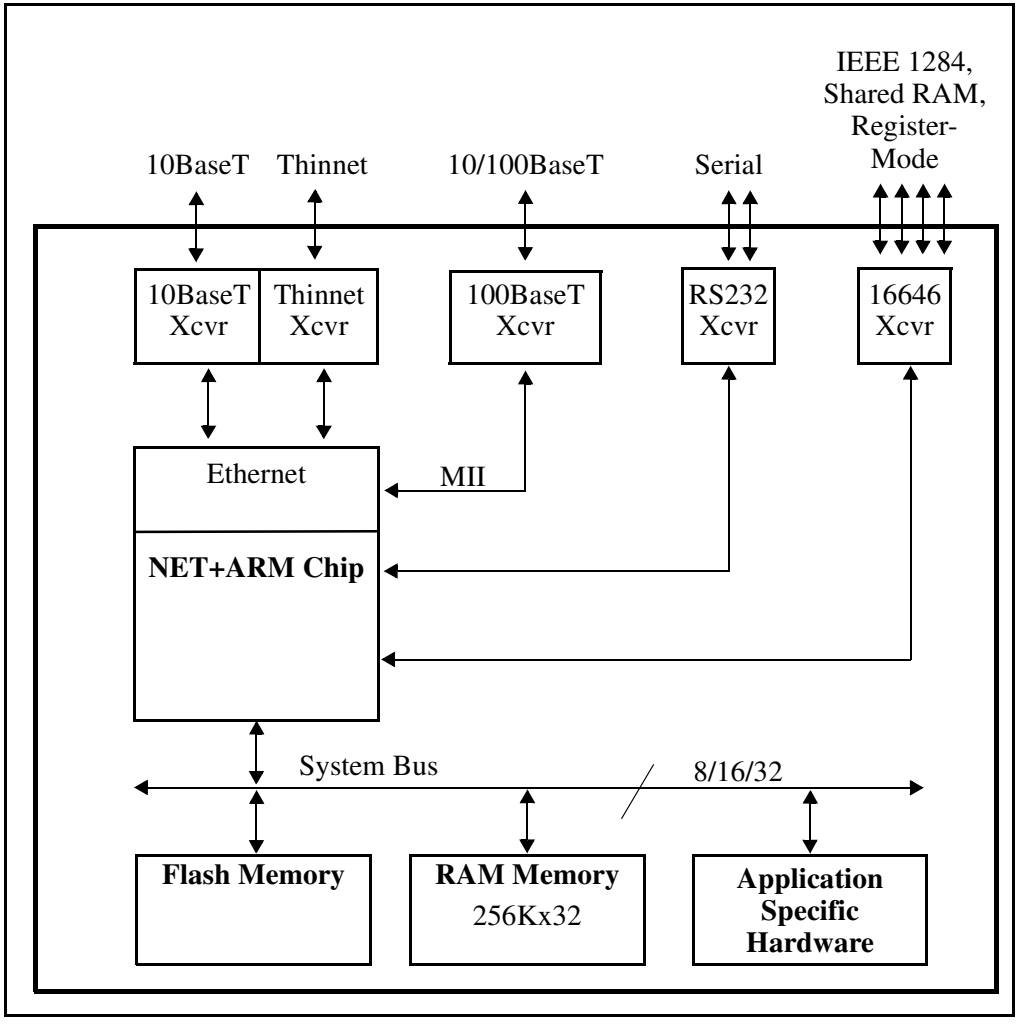

Figure 1-2: NET+ARM Chip Hardware Block Diagram

1.4 NET+ARM Chip Pinout

Refer to Table 1-1 for details concerning the pinout of the NET+ARM chip.

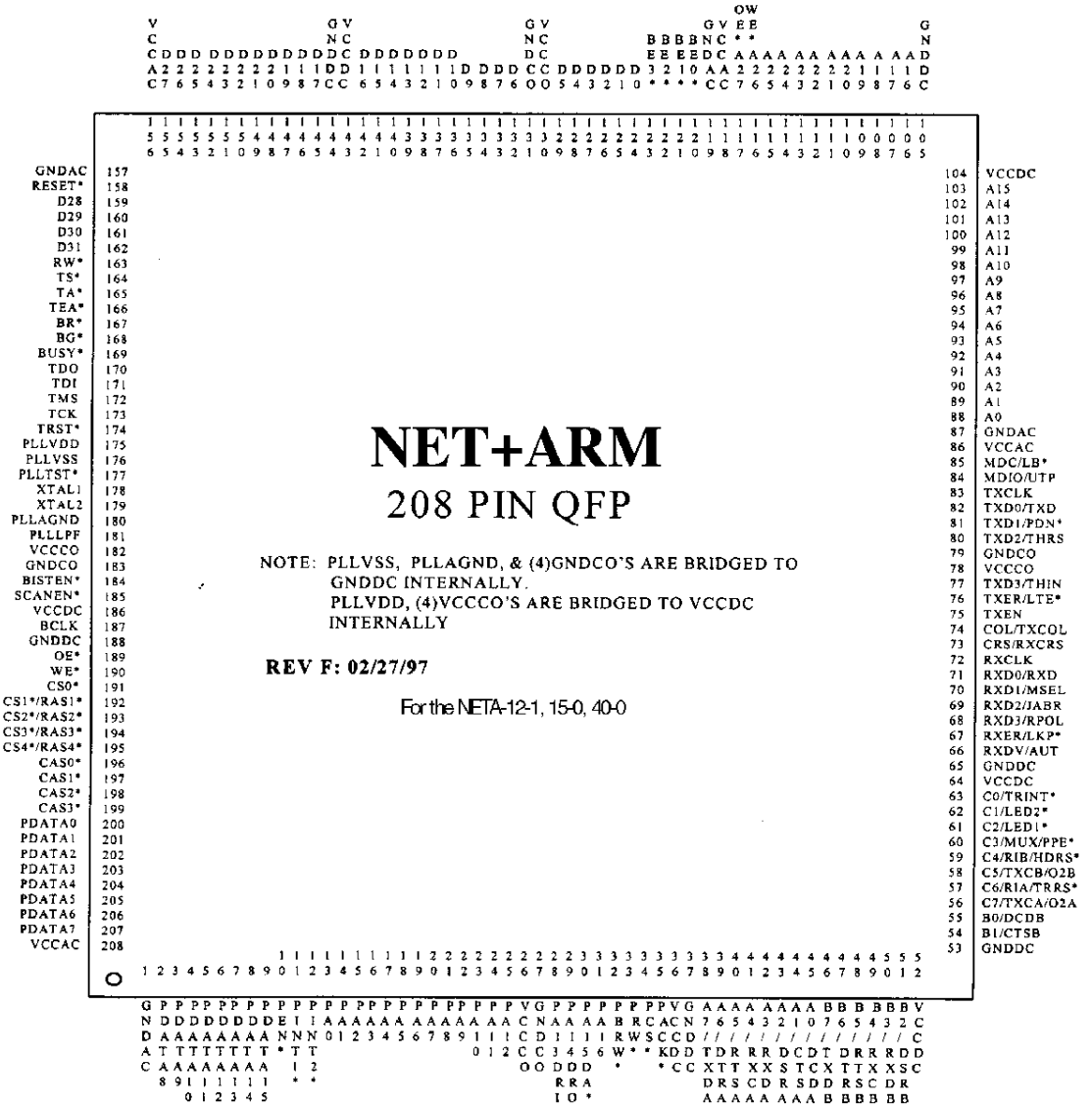

Figure 1-3: NET+ARM Chip Pinout

The *Signal* column identifies the pin name for each I/O signal. Note that some signals have dual modes and are identified accordingly. The mode is configured via firmware using a configuration register (some modes may require hardware configuration during a RESET condition).

The *208QFP* column identifies the pin number assignment for a specific I/O signal.

The *I/O* column identifies whether the signal is input, output, or input/output.

The *Drive* column identifies the drive strength of an output buffer. The NET+ARM chip is being designed using one of three types of drivers; **(2mA), ** (4mA), and **(8mA).

The *Pad Cell* column indicates the type of I/O cell driver selected. All Pad Cells with a suffix of **u** provide an internal pullup resistor. All Pad Cells with a suffix of **d** provide an internal pulldown resistor. The pullup and pulldown resistors can effectively terminate floating inputs, however, these resistors are not strong enough to provide a sharp rising edge for outputs transitioning from Vol to tri-state.

Signal		208 QFP Pin	Pad Cell	I/O	Drive	Description
System Bus Interface						
BCLK		187	pt3t03	O	8	Synchronous Bus Clock
ADDR27	CS0OE*	117	pt3b02u	I/O	4	Address Bus
ADDR26	CS0WE*	116	pt3b02u	I/O	4	
ADDR25		115	pt3b02u	I/O	4	
ADDR24		114	pt3b02u	I/O	4	
ADDR23		113	pt3b02u	I/O	4	
ADDR22		112	pt3b02u	I/O	4	
ADDR21		111	pt3b02u	I/O	4	
ADDR20		110	pt3b02u	I/O	4	
ADDR19		109	pt3b02u	I/O	4	
ADDR18		108	pt3b02u	I/O	4	
ADDR17		107	pt3b02u	I/O	4	
ADDR16		106	pt3b02u	I/O	4	
ADDR15		103	pt3b02u	I/O	4	
ADDR14		102	pt3b02u	I/O	4	
ADDR13		101	pt3b02u	I/O	4	
ADDR12		100	pt3b02u	I/O	4	

Table 1-1: NET+ARM Chip Pinout

Signal	208 QFP Pin	Pad Cell	I/O	Drive	Description
ADDR11	99	pt3b02u	I/O	4	
ADDR10	98	pt3b02u	I/O	4	
ADDR9	97	pt3b02u	I/O	4	
ADDR8	96	pt3b02u	I/O	4	
ADDR7	95	pt3b02u	I/O	4	
ADDR6	94	pt3b02u	I/O	4	
ADDR5	93	pt3b02u	I/O	4	
ADDR4	92	pt3b02u	I/O	4	
ADDR3	91	pt3b02u	I/O	4	
ADDR2	90	pt3b02u	I/O	4	
ADDR1	89	pt3b02u	I/O	4	
ADDR0	88	pt3b02u	I/O	4	
DATA31	162	pt3b02	I/O	4	Data Bus
DATA30	161	pt3b02	I/O	4	
DATA29	160	pt3b02	I/O	4	
DATA28	159	pt3b02	I/O	4	
DATA27	155	pt3b02	I/O	4	
DATA26	154	pt3b02	I/O	4	
DATA25	153	pt3b02	I/O	4	
DATA24	152	pt3b02	I/O	4	
DATA23	151	pt3b02	I/O	4	
DATA22	150	pt3b02	I/O	4	
DATA21	149	pt3b02	I/O	4	
DATA20	148	pt3b02	I/O	4	
DATA19	147	pt3b02	I/O	4	
DATA18	146	pt3b02	I/O	4	
DATA17	145	pt3b02	I/O	4	
DATA16	142	pt3b02	I/O	4	
DATA15	141	pt3b02	I/O	4	
DATA14	140	pt3b02	I/O	4	
DATA13	139	pt3b02	I/O	4	
DATA12	138	pt3b02	I/O	4	

Table 1-1: NET+ARM Chip Pinout (Continued)