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DATA SHEET

Part No.	MN63Y1210A
Package Code No.	SSOP016-P-0225E

About this manual

■ Organization

These specifications provide important information for users of the MN63Y1210A-E1, including an overview and descriptions of functions.

■ Manual Configuration

Each section of this manual consists of a title, main text, and notes. The layout and definition of each section are shown below.

1.1 UART

This section describes the UART specification.

1.1.1 Communication Specifications

Table 1-1 shows the UART specification of this RFID.

Table 1-1 UART Communication Specification

Data transfer method	Asynchronous, half-duplex (Only IRQ notification allows full-duplex)
Data rate	200 bps, 2400 bps, 4800 bps, 9600 bps, 19200 bps, 38400 bps
Character transmission	<ul style="list-style-type: none"> ·LSB-first ·Data (8 bits) ·Start bit (1bit) ·Parity bit (1bit, even) ·Stop bit (1bit) See Note below.
Other	No flow control signal (RTS/CTS)

Note: In order to ensure the timing margin, when sending consecutive data from the host, use a 2-bit stop bit or set the interval between stop bit and next start bit to 1 bit or more.

Middle title

Small title

Text

Note

This is the Note.
Please read.

■ Finding Desired Information

This manual provides two methods for finding desired information quickly and easily.

1. Consult the table of contents at the front of the manual to locate desired titles.
2. Chapter names are located at the top outer corner of each page, and section titles are located at the bottom outer corner of each page.

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1.1 Features

The MN63Y1210A is an LSI for RFID (Radio Frequency Identification), which features the following:

- Built-in 4-Kbit FeRAM non-volatile memory with fast write and low power consumption.
- RF interface compliant with JISX6319-4 (212 kbps / 424 kbps) and ISO/IEC14443 TypeB (106 kbps / 212 kbps) of the 13.56-MHz contactless IC card standards.
- Serial interface compatible with both asynchronous UART (up to 38.4 kbps) and clock synchronous (up to 1 Mbps)
- Batteryless RF communication
- Three communication modes of RF, serial, and tunnel (Tunnel mode allows communications between reader/writer and host CPU via this LSI.)
- Supply voltage range: 1.8 V to 3.6 V or 4.5 V to 5.5 V (when 5V tolerant I/O and clamp function is turned ON)
- 5-V operation (5V tolerant I/O, VDD2 pin clamp circuit built-in)

1.2 Block Diagram

Figure 1-1 shows a block diagram.

This RFID provides RF interface for contactless communication with external reader/writer, serial interface for contact communication with external host, control logic for command processing and various controls, 2-kbit transmit/receive buffer for RF communication, and 4-kbit FeRAM non-volatile memory.

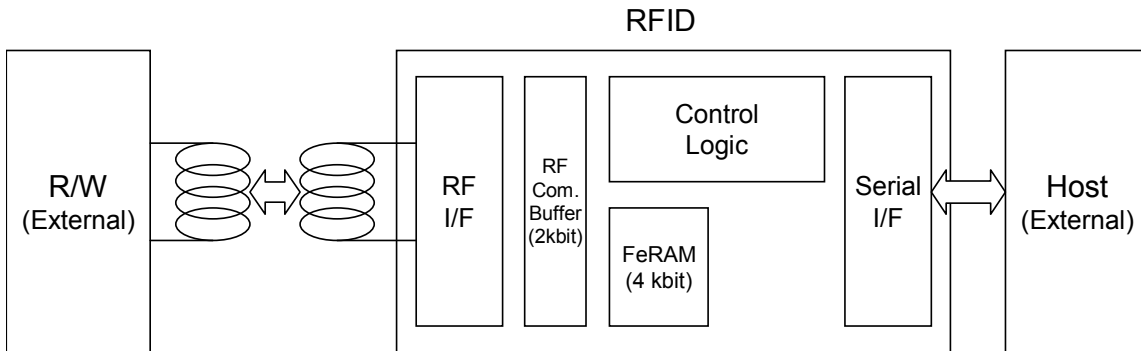


Figure 1-1 Block Diagram

1.3 Operation Mode

This RFID provides three operation modes of RF communication, serial communication, and tunnel. Figure 1-2 gives the overview of each operation mode.

■ RF communication mode

This mode is used for communication between reader/writer and RFID. Reader/writer is the master and RFID is the slave. Key commands are read and write commands to FeRAM of RFID. This mode allows batteryless operations that use only the power supplied from the antenna of reader/writer.

For more information about RF communication mode, see Chapter 4 RF Communication Mode.

■ Serial communication mode

This mode is used for communication between host and RFID. Host is the master and RFID is the slave. Key commands are read and write commands to FeRAM of RFID. This mode requires a power supply to the supply voltage pin (VDD2) of RFID.

For more information about serial communication mode, see Chapter 5 Serial Communication Mode.

■ Tunnel mode

This mode is used for communication between reader/writer and host via RFID. Reader/writer is the master and host is the slave. Key commands are read and write commands to host. This mode requires a power supply to the supply voltage pin (VDD2) of RFID.

For more information about serial communication mode, see Chapter 6 Tunnel Mode.

Additionally, for state transition diagram in each operation mode, see Section 7.2 State Transition Diagram in Operation Mode.

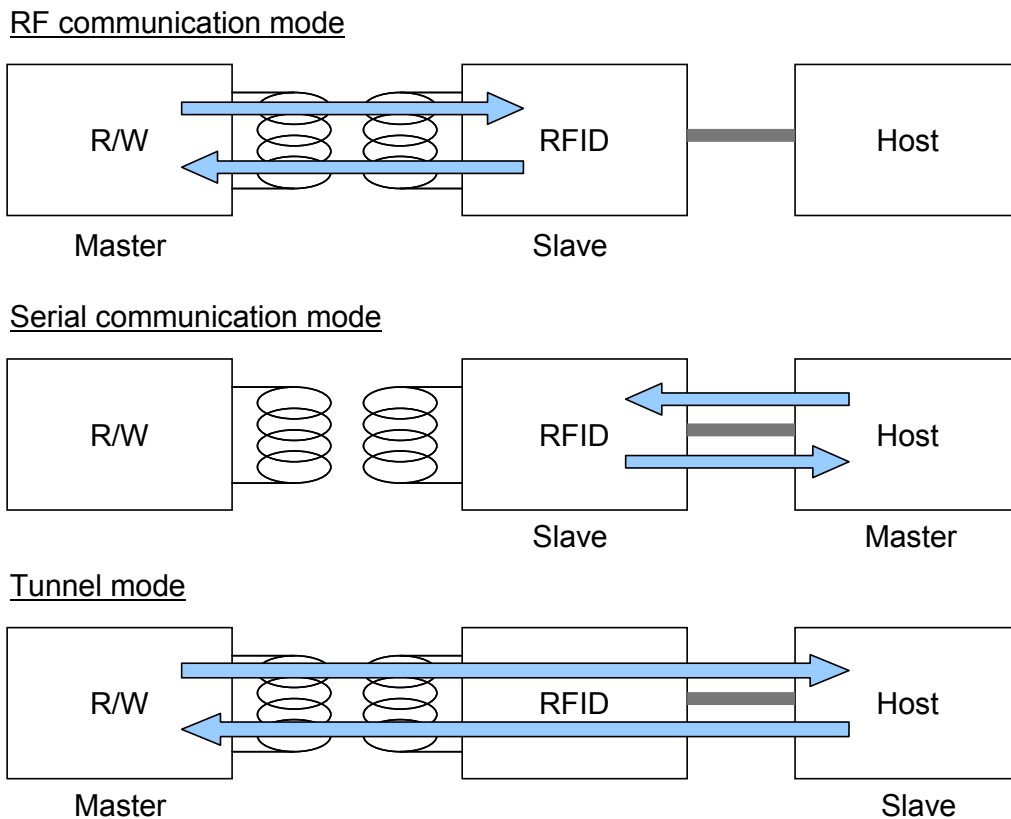


Figure 1-2 Operation Mode

Chapter 2 Pin Descriptions

2.1 List of Pins

Table 2-1 shows a list of pins of this RFID and Figure 2-1 illustrates the pin assignments of this RFID.

Table 2-1 List of Pins

Pin No.	Name	I/O	5V tolerant	Output type	Description
1	NC	-	-	-	Not connected
2	VB	I/O	-	-	Connected to coil
3	VDD2	-	-	-	Serial interface power supply
4	VDD	-	-	-	Internal digital power supply
5	VSS	-	-	-	Ground
6	VDD1	-	-	-	Internal analog power supply
7	VA	I/O	-	-	Connected to coil
8	NC	-	-	-	Not connected
9	TEST	Input	No	-	Test control
10	NCLP	-	No	-	Clamp control
11	RX	Input	Yes	-	Data reception (UART: RX, Clock sync: SCK)
12	TX3V	I/O	No	Open Drain	Data reception for 3 V (UART: TX, Clock sync: I/O)
13	TX5V	I/O	Yes	Open Drain	Data reception for 5 V (UART: TX, Clock sync: I/O)
14	IRQ3V	Output	No	Open Drain	Interrupt request output for 3 V
15	IRQ5V	Output	Yes	Open Drain	Interrupt request output for 5 V
16	SEL	Input	No	-	Serial interface selection

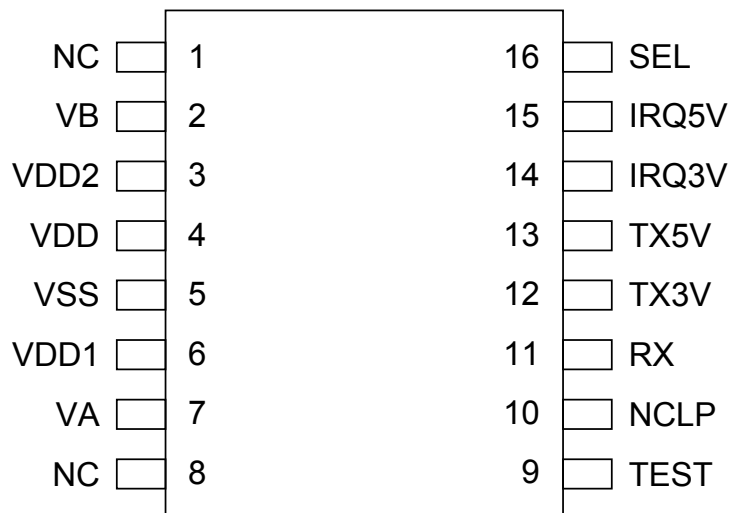


Figure 2-1 Pin Assignments (SSOP16)

2.2 Pin Descriptions

- Coil connection pins (VA, VB)

Used for connecting an antenna coil. Also connect a resonance capacitor for adjusting resonance frequency.

- Ground (VSS)

A reference power supply pin. Connect to the ground of the host CPU.

- Internal analog power supply (VDD1)

An internal analog power supply pin. Connect a capacitor (see the Product Standards for its value) between VDD1 and VSS pins as close as possible to the RFID. It is unnecessary to apply an external power to this pin.

- Internal digital power supply (VDD)

An internal digital power supply pin. Leave this pin open. Connect a capacitor (see the Product Standards for its value) between VDD and VSS pins as close as possible to the RFID. It is unnecessary to apply an external power to this pin.

- Contact power supply VDD2

A contact power supply pin. Apply a high voltage to this pin when communicating data between the host CPU and RFID. Connect a capacitor (see the Product Standards for its value) between VDD2 and VSS pins as close as possible to the RFID.

Additionally, the RFID has a built-in clamp circuit for 5-V operation. When using the circuit, apply a 5-V supply voltage to this pin through a given resistor (see the Product Standards for its value).

- Serial interface select pin (SEL)

Used for selecting serial interfaces. Set the pin to low for UART, and to high for clock synchronous. This pin is 5-V tolerant I/O.

- Data receive pin (RX) [UART: RX; Clock synchronous: SCK]

A data input pin. It is used as RX for UART, and as serial clock input SCK for clock synchronous. This pin is 5-V tolerant I/O.

- Data transmission in 3-V operation (TX3V) [UART: TX; Clock synchronous: I/O]

A data output pin. It is used as TX for UART, and as data I/O for clock synchronous. This pin is open-drain, so should be pulled up. Additionally, this pin is provided for 3-V operation. When not using, leave it open.

- Data transmission in 5-V operation (TX5V) [UART: TX; Clock synchronous: I/O]

A data output pin. It is used as TX for UART, and as data I/O for clock synchronous. This pin is open-drain, so should be pulled up. Additionally, this pin is provided for 5-V operation. When not using, leave it open.

- Interrupt request in 3-V operation (IRQ3V)

An interrupt request output pin. Receiving a command in tunnel mode from external reader/writer generates a low interrupt request signal pulse on this pin. This pin is open-drain, so should be pulled up. Additionally, this pin is provided for 3-V operation. When not using, leave it open.

- Interrupt request in 5-V operation (IRQ5V)

An interrupt request output pin. Receiving a command in tunnel mode from external reader/writer generates a low interrupt request signal pulse on this pin. This pin is open-drain, so should be pulled up. Additionally, this pin is provided for 5-V operation. When not using, leave it open.

- Test control (TEST)

Used in the test mode. Set it to low.

- Clamp control (NCLP)

This pin controls ON/OFF of the clamp circuit connected to the VDD2 pin. Set it to high (OFF) in 3-V

operation. Set it to low (ON) in 5-V operation.

2.3 Connection Example

Several connection examples are shown below.

2.3.1 Using UART and 5 V Power

Figure 2-2 gives an connection example of using UART and 5-V power.

Set SEL to low in UART operation, and set NCLP to low in 5-V operation. With a series resistor connected (see the Product Standards for its value), apply a 5-V supply voltage to VDD2.

This example shows that the host's GPIO controls the RFID's VDD2. In this case, when not using serial communication, turning VDD2 off allows the consumption current of the RFID to be turned off. In addition, it is also possible to supply a voltage to VDD2 directly from the power supply, not from the host's GPIO.

Furthermore, when the host can always receive data from the RFID's TX, an interrupt request (IRQ) is reported from the TX as well, so allowing to omit IRQ connection.

The TX5V and IRQ5V pins are open-drain output. Pull these pins up to the same voltage level as the power supply of the host.

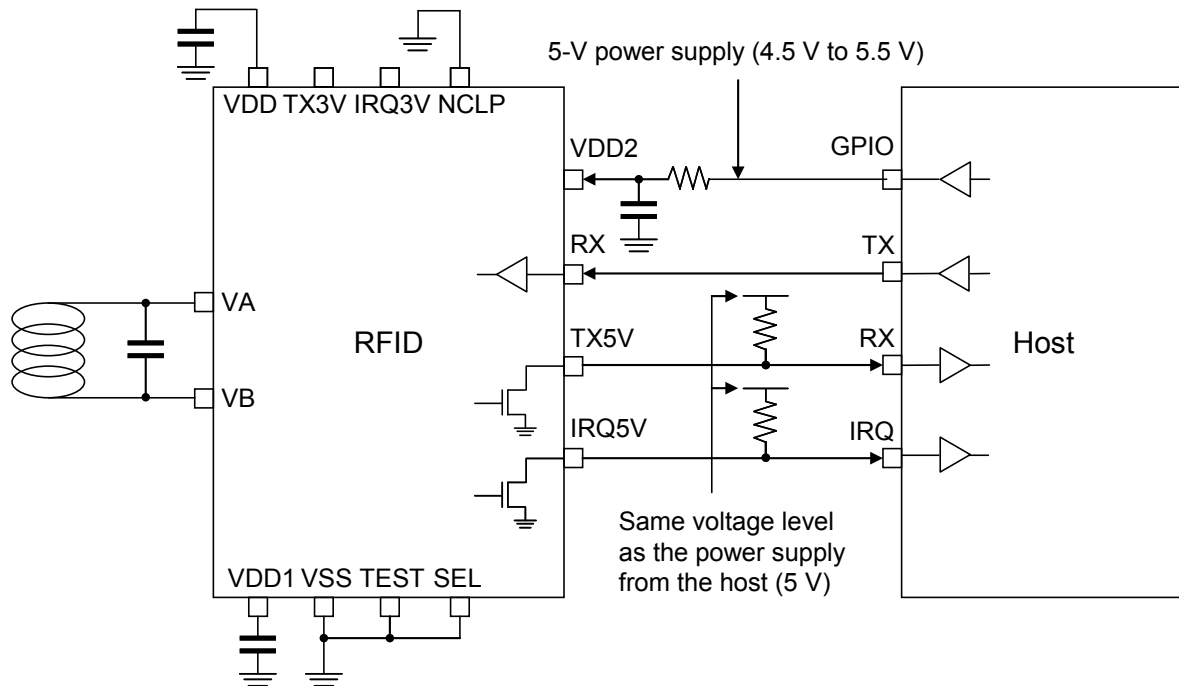


Figure 2-2 Connection Example of UART and 5 V Power Operation

2.3.2 Using UART and 3 V Power

Figure 2-3 gives an connection example of using UART and 3-V power.

Set SEL to low in UART operation, and set NCLP to high in 3-V operation.

This example shows that the host's GPIO controls the RFID's VDD2. In this case, when not using serial communication, turning VDD2 off allows the consumption current of the RFID to be turned off. In addition, it is also possible to supply a voltage to VDD2 directly from the power supply, not from the host's GPIO.

Furthermore, when the host can always receive data from the RFID's TX, an interrupt request (IRQ) is reported from the TX as well, so allowing to omit IRQ signal connection.

The TX3V and IRQ3V pins are open-drain output. Pull these pins up to the same voltage level as VDD2.

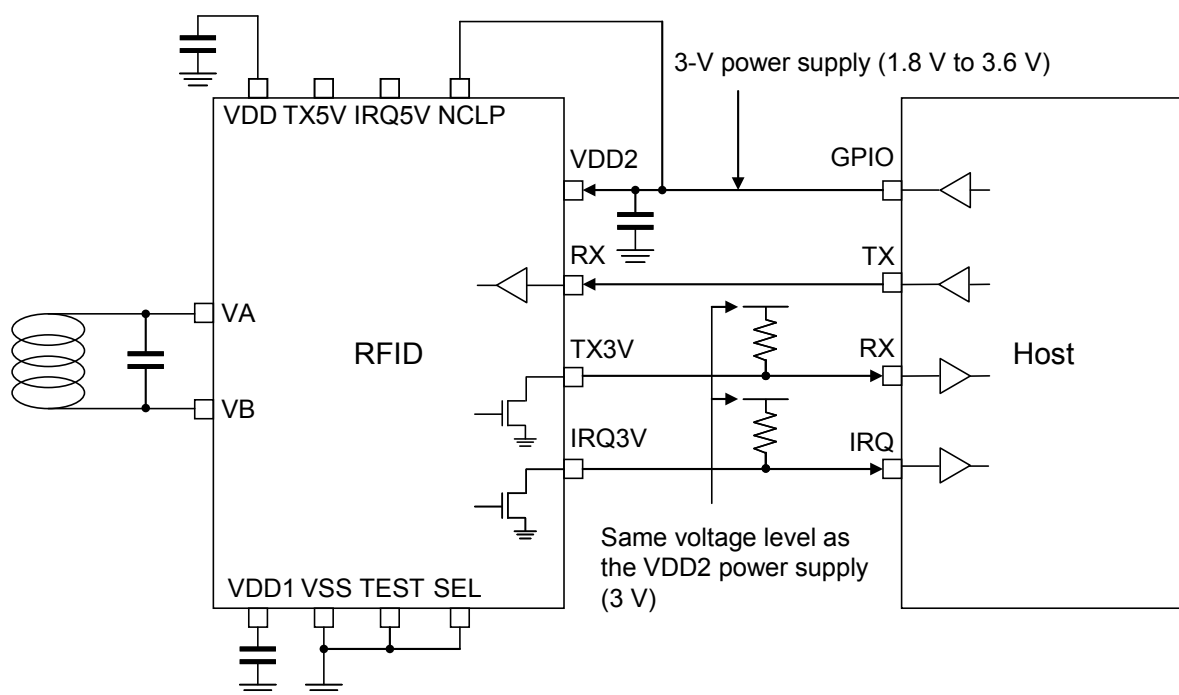


Figure 2-3 Connection Example of UART and 3 V Power Operation

2.3.3 Using Clock Synchronous Mode and 5 V Power

Figure 2-4 gives an connection example of using clock synchronous mode and 5-V power.

Set SEL to high in clock synchronous operation, and set NCLP to low in 5-V operation. With a series resistor connected (see the Product Standards for its value), apply a 5-V supply voltage to VDD2.

This example shows that the host's GPIO controls the RFID's VDD2. In this case, when not using serial communication, turning VDD2 off allows the consumption current of the RFID to be turned off. In addition, it is also possible to supply a voltage to VDD2 directly from the power supply, not from the host's GPIO.

The TX5V (I/O) and IRQ5V pins are open-drain output. Pull these pins up to the same voltage level as the power supply of the host.

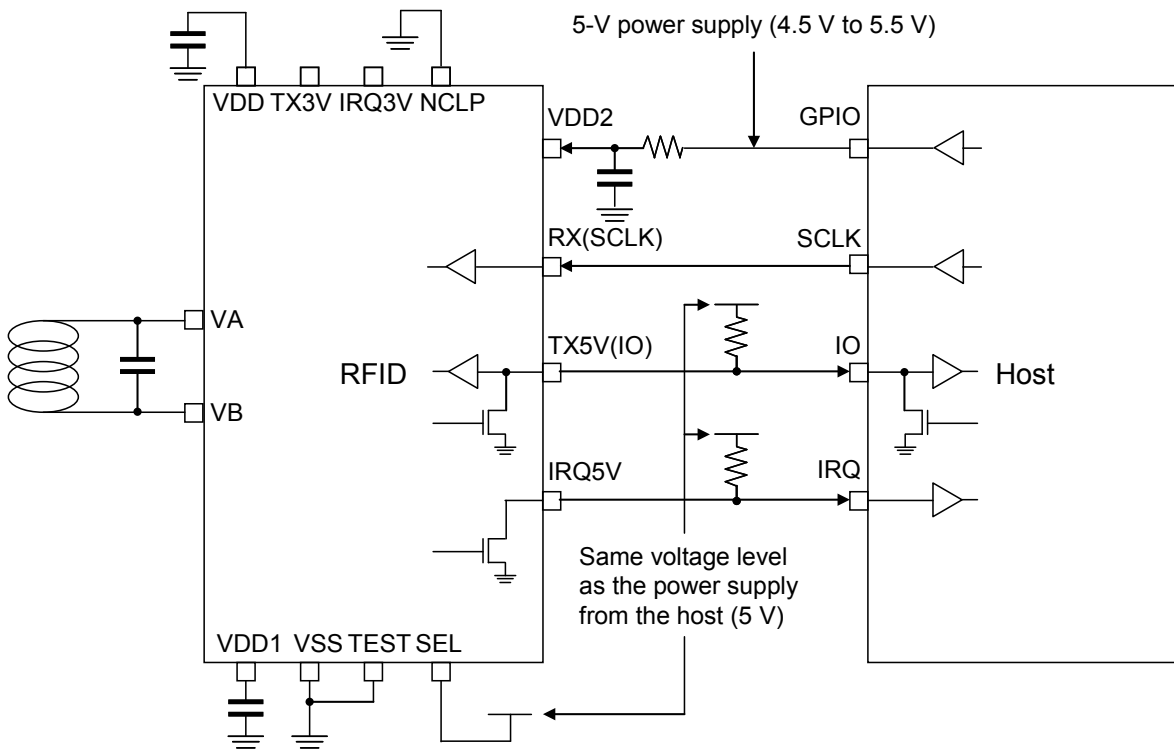


Figure 2-4 Connection Example of Clock Synchronous and 5 V Power Operation

2.3.4 Using Clock Synchronous Mode and 3 V Power

Figure 2-5 gives an connection example of using clock synchronous mode and 3-V power.

Set SEL to high in clock synchronous operation, and set NCLP to low in 3-V operation.

This example shows that the host's GPIO controls the RFID's VDD2. In this case, when not using serial communication, turning VDD2 off allows the consumption current of the RFID to be turned off. In addition, it is also possible to supply a voltage to VDD2 directly from the power supply, not from the host's GPIO.

The TX3V (I/O) and IRQ3V pins are open-drain output. Pull these pins up to the same voltage level as VDD2.

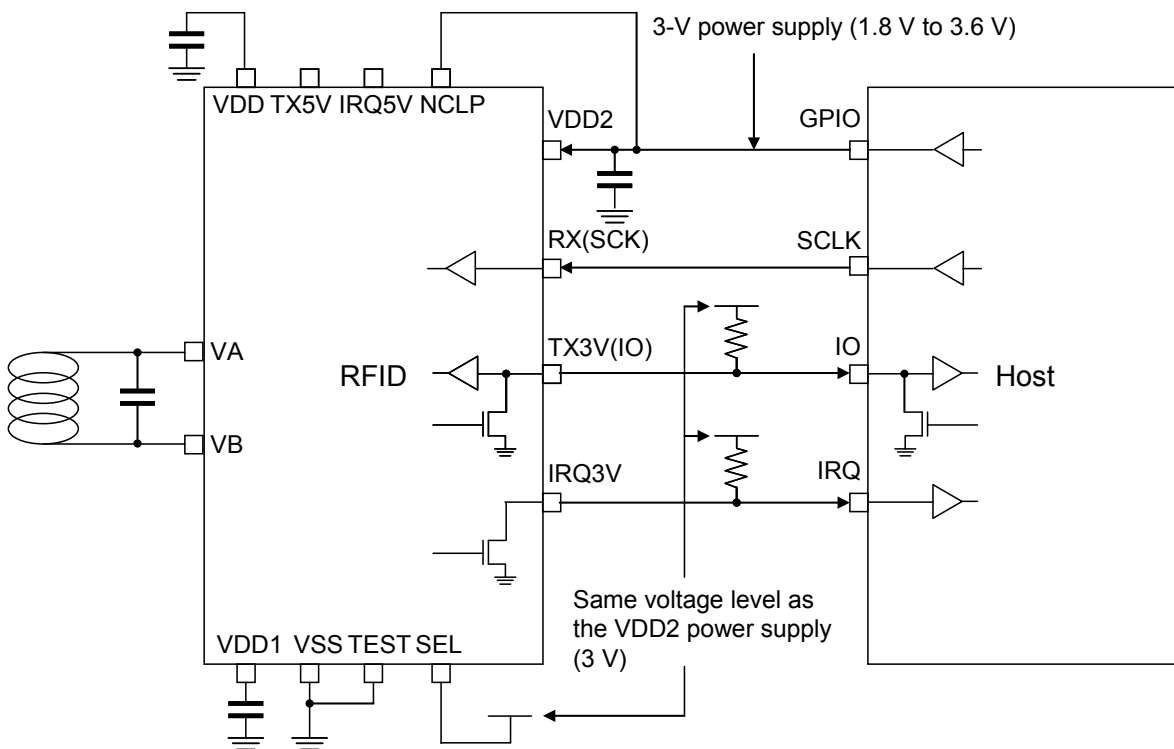


Figure 2-5 Connection Example of Clock Synchronous and 3 V Power Operation

Chapter 3 Memory Map

3.1 Block Configuration

Figure 3-1 illustrates the block configuration of 4-Kbit FeRAM.

This LSI consists of 32 FeRAM blocks. The size of a block is 16 bytes.

The memory consists of two areas: user and system areas.

The system area stores RF-communication-related parameters and memory-access-control-related data, etc.

Block	Area	Type
0	16Bytes FeRAM	User area
1	16Bytes FeRAM	
2	16Bytes FeRAM	
3	16Bytes FeRAM	
...	...	
24	16Bytes FeRAM	
25	16Bytes FeRAM	
26	16Bytes FeRAM	
27	16Bytes FeRAM	System area
28	16Bytes FeRAM	
29	16Bytes FeRAM	
30	16Bytes FeRAM	
31	16Bytes FeRAM	

Figure 3-1 4-Kbit FeRAM Block Configuration

3.2 Physical Memory Map

Figure 3-2 presents the physical memory map.

Block	Address	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF	
0	0x0000	User Area																
1	0x0010	User Area																
2	0x0020	User Area																
3	0x0030	User Area																
4	0x0040	User Area																
5	0x0050	User Area																
6	0x0060	User Area																
7	0x0070	User Area																
8	0x0080	User Area																
9	0x0090	User Area																
10	0x00A0	User Area																
11	0x00B0	User Area																
12	0x00C0	User Area																
13	0x00D0	User Area																
14	0x00E0	User Area																
15	0x00F0	User Area																
16	0x0100	User Area																
17	0x0110	User Area																
18	0x0120	User Area																
19	0x0130	User Area																
20	0x0140	User Area																
21	0x0150	User Area																
22	0x0160	User Area																
23	0x0170	User Area																
24	0x0180	User Area																
25	0x0190	User Area																
26	0x01A0	User Area																
27	0x01B0	CONFIG																
28	0x01C0	CONFIG																
29	0x01D0	CONFIG																
30	0x01E0	SC	IDM						PMM	AFI	FWI	HW						
31	0x01F0	RORF				ROSI				SECURITY				TNPRM	CONFIG			

Figure 3-2 Physical Memory Map