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Ignition IGBT 18 Amps, 400 Volts

N-Channel D²PAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over-Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil-on-Plug Applications
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Integrated Gate–Emitter Resistor (R_{GE})
- Emitter Ballasting for Short-Circuit Capability
- Pb-Free Package is Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CES}	430	V_{DC}
Collector-Gate Voltage	V _{CER}	430	V_{DC}
Gate-Emitter Voltage	V_{GE}	18	V_{DC}
Collector Current–Continuous @ T _C = 25°C – Pulsed	I _C	18 50	A _{DC} A _{AC}
ESD (Human Body Model) R = 1500 Ω , C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω , C = 200 pF	ESD	800	V
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	115 0.77	W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C

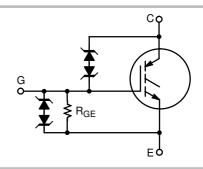
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

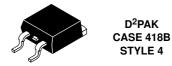


ON Semiconductor®

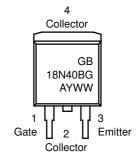
http://onsemi.com

18 AMPS, 400 VOLTS $V_{CE(on)} \le 2.0 \text{ V } @$ $I_C = 10 \text{ A}, V_{GE} \ge 4.5 \text{ V}$





MARKING DIAGRAM



GB18N40B = Device Code

A = Assembly Location

Y = Year WW = Work Week G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping [†]
NGB18N40CLBT4	D ² PAK	800/Tape & Reel
NGB18N40CLBT4G	D ² PAK (Pb–Free)	800/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

UNCLAMPED COLLECTOR-TO-EMITTER AVALANCHE CHARACTERISTICS ($-55^{\circ} \le T_{J} \le 175^{\circ}C$)

Characteristic	Symbol	Value	Unit
Single Pulse Collector–to–Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 21.1 A, L = 1.8 mH, Starting T_J = 25°C V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 18.3 A, L = 1.8 mH, Starting T_J = 125°C	E _{AS}	400 300	mJ
Reverse Avalanche Energy V_{CC} = 100 V, V_{GE} = 20 V, Pk I _L = 25.8 A, L = 6.0 mH, Starting T _J = 25°C	E _{AS(R)}	2000	mJ

MAXIMUM SHORT-CIRCUIT TIMES $(-55^{\circ}C \le T_{J} \le 150^{\circ}C)$

Characteristic	Symbol	Value	Unit
Short Circuit Withstand Time 1 (See Figure 17, 3 Pulses with 10 ms Period)	t _{sc1}	750	μs
Short Circuit Withstand Time 2 (See Figure 18, 3 Pulses with 10 ms Period)	t _{sc2}	5.0	ms

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{ heta JC}$	1.3	°C/W
Thermal Resistance, Junction–to–Ambient D²PAK (Note 1)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Collector-Emitter Clamp Voltage	BV _{CES}	$I_C = 2.0 \text{ mA}$	$T_J = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	380	395	420	V_{DC}
		I _C = 10 mA	$T_J = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	390	405	430	
Zero Gate Voltage Collector Current	I _{CES}		T _J = 25°C	-	2.0	20	μA_{DC}
		$V_{CE} = 350 \text{ V},$ $V_{GE} = 0 \text{ V}$	T _J = 150°C	-	10	40*	
		IGE 01	$T_J = -40^{\circ}C$	-	1.0	10	
Reverse Collector–Emitter Leakage Current	I _{ECS}	V _{CE} = -24 V	T _J = 25°C	-	0.7	2.0	mA
			T _J = 150°C	-	12	25*	
			$T_J = -40^{\circ}C$	-	0.1	1.0	
Reverse Collector-Emitter Clamp Voltage	B _{VCES(R)}		T _J = 25°C	27	33	37	V_{DC}
		$I_C = -75 \text{ mA}$	T _J = 150°C	30	36	40	
			T _J = -40°C	25	32	35	
Gate-Emitter Clamp Voltage	BV _{GES}	$I_G = 5.0 \text{ mA}$	$T_J = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	11	13	15	V_{DC}
Gate-Emitter Leakage Current	I _{GES}	V _{GE} = 10 V	$T_J = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	384	640	100 0	μA _{DC}
Gate Emitter Resistor	R _{GE}	ı	$T_J = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	10	16	26	kΩ

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GE(th)}		T _J = 25°C	1.1	1.4	1.9	V_{DC}
		$I_C = 1.0 \text{ mA},$ $V_{GE} = V_{CE}$	$T_J = 150^{\circ}C$	0.75	1.0	1.4	
		at of	$T_J = -40^{\circ}C$	1.2	1.6	2.1*	
Threshold Temperature Coefficient (Negative)	-	-	-		3.4	_	mV/°C

^{*}Maximum Value of Characteristic across Temperature Range.

^{1.} When surface mounted to an FR4 board using the minimum recommended pad size. 2. Pulse Test: Pulse Width \leq 300 μ S, Duty Cycle \leq 2%.

ELECTRICAL CHARACTERISTICS

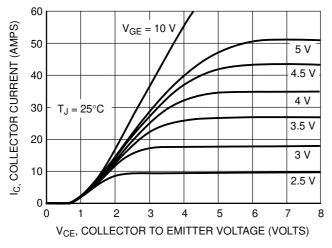
Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
ON CHARACTERISTICS (Note 2)							
Collector-to-Emitter On-Voltage	V _{CE(on)}		T _J = 25°C	1.0	1.4	1.6	V_{DC}
		I _C = 6.0 A, V _{GF} = 4.0 V	T _J = 150°C	0.9	1.3	1.6	
		I GE	T _J = -40°C	1.1	1.45	1.7*	
			T _J = 25°C	1.3	1.6	1.9*	
		$I_{C} = 8.0 \text{ A},$ $V_{GE} = 4.0 \text{ V}$	T _J = 150°C	1.2	1.55	1.8	
		I GE	T _J = -40°C	1.4	1.6	1.9*	
			T _J = 25°C	1.4	1.8	2.05	
		$I_{C} = 10 \text{ A},$ $V_{GE} = 4.0 \text{ V}$	T _J = 150°C	1.5	1.8	2.0	
		I GE	T _J = -40°C	1.4	1.8	2.1*	
			T _J = 25°C	1.8	2.2	2.5	
		I _C = 15 A, V _{GE} = 4.0 V	T _J = 150°C	2.0	2.4	2.6*	
	I GE	T _J = -40°C	1.7	2.1	2.5		
			T _J = 25°C	1.3	1.8	2.0*	1
		I _C = 10 A, V _{GE} = 4.5 V	T _J = 150°C	1.3	1.75	2.0*	
		I GE	T _J = -40°C	1.4	1.8	2.0*	
Forward Transconductance	gfs	$V_{CE} = 5.0 \text{ V}, I_{C} = 6.0 \text{ A}$	$T_J = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	8.0	14	25	Mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance	C _{ISS}	V _{CC} = 25 V, V _{GE} = 0 V	$T_{J} = -40^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	400	800	100 0	pF
Output Capacitance	C _{OSS}	f = 1.0 MHz		50	75	100	
Transfer Capacitance	C _{RSS}			4.0	7.0	10	
SWITCHING CHARACTERISTICS							
Turn-Off Delay Time (Resistive)	t _{d(off)}	$\begin{array}{c} V_{CC} = 300 \text{ V}, \ I_{C} = 6.5 \text{ A} \\ R_{G} = 1.0 \text{ k}\Omega, \ R_{L} = 46 \ \Omega, \end{array}$	T _J = 25°C	_	4.0	10	μSec
Fall Time (Resistive)	t _f	$\begin{aligned} &V_{CC} = 300 \text{ V, } I_{C} = 6.5 \text{ A} \\ &R_{G} = 1.0 \text{ k}\Omega, \ R_{L} = 46 \ \Omega, \end{aligned}$	T _J = 25°C		9.0	15	
Turn-On Delay Time	t _{d(on)}	$V_{CC} = 10 \text{ V}, I_{C} = 6.5 \text{ A}$ $R_{G} = 1.0 \text{ k}\Omega, R_{L} = 1.5 \Omega$	T _J = 25°C	_	0.7	4.0	μSec
Rise Time	t _r	$V_{CC} = 10 \text{ V}, I_{C} = 6.5 \text{ A}$ $R_{G} = 1.0 \text{ k}\Omega, R_{L} = 1.5 \Omega$	T _J = 25°C	-	4.5	7.0	

^{*}Maximum Value of Characteristic across Temperature Range.

1. When surface mounted to an FR4 board using the minimum recommended pad size.

2. Pulse Test: Pulse Width $\leq 300~\mu\text{S}$, Duty Cycle $\leq 2\%$.

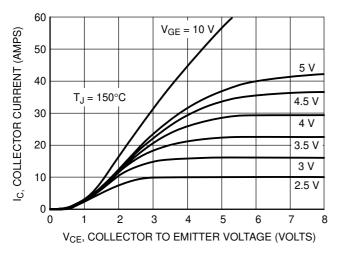
TYPICAL ELECTRICAL CHARACTERISTICS (unless otherwise noted)



60 $V_{GE} = 10 \text{ V}$ IC. COLLECTOR CURRENT (AMPS) 5 V 50 4.5 V 40 $T_J = -40^{\circ}C$ 4 V 30 3.5 V 20 3 V 10 2.5 V 0 V_{CE}, COLLECTOR TO EMITTER VOLTAGE (VOLTS)

Figure 1. Output Characteristics

Figure 2. Output Characteristics



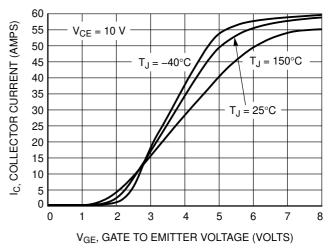
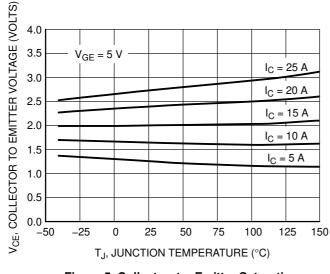


Figure 3. Output Characteristics

Figure 4. Transfer Characteristics



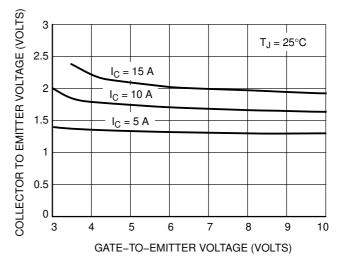
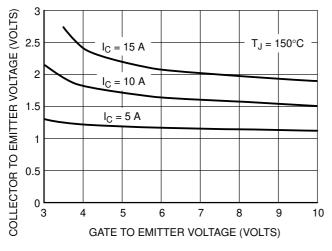


Figure 5. Collector-to-Emitter Saturation Voltage versus Junction Temperature

Figure 6. Collector-to-Emitter Voltage versus Gate-to-Emitter Voltage

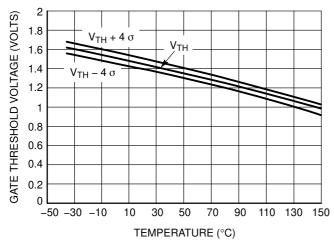
10000



Ciss 1000 C, CAPACITANCE (pF) 100 C_{oss} 10 $\mathsf{C}_{\mathsf{rss}}$ 1 0 0 20 40 60 80 100 120 140 160 180 200 V_{CE}, COLLECTOR TO EMITTER VOLTAGE (VOLTS)

Figure 7. Collector-to-Emitter Voltage versus Gate-to-Emitter Voltage

Figure 8. Capacitance Variation



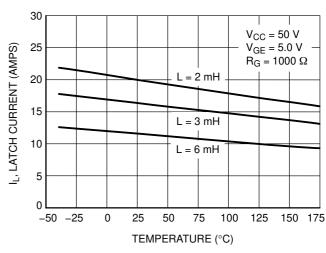
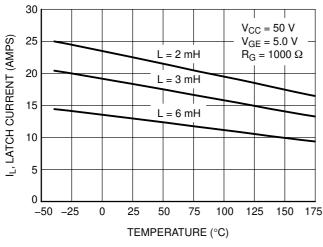


Figure 9. Gate Threshold Voltage versus Temperature

Figure 10. Minimum Open Secondary Latch Current versus Temperature



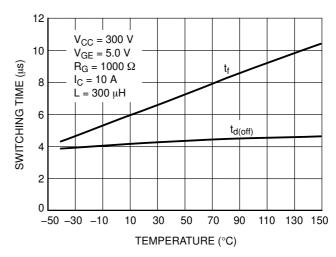


Figure 11. Typical Open Secondary Latch Current versus Temperature

Figure 12. Inductive Switching Fall Time versus Temperature

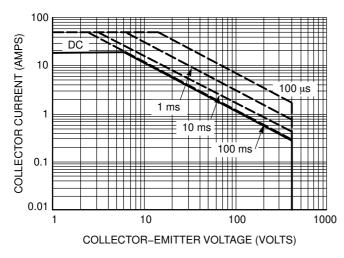


Figure 13. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_A = 25$ °C)

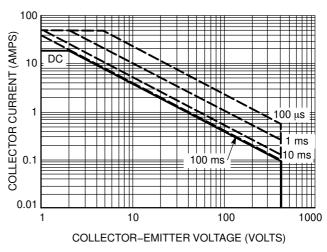


Figure 14. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_A = 125$ °C)

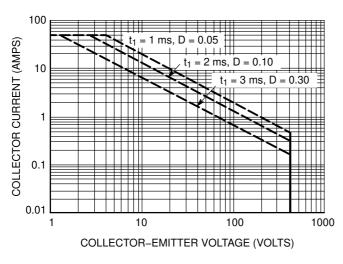


Figure 15. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C = 25^{\circ}C$)

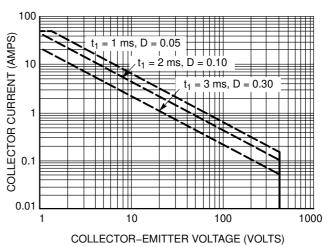


Figure 16. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C = 125^{\circ}C$)

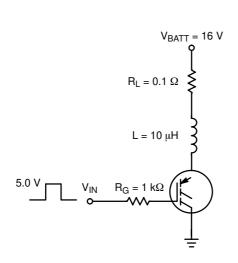


Figure 17. Circuit Configuration for Short Circuit Test #1

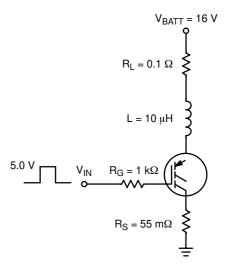


Figure 18. Circuit Configuration for Short Circuit Test #2

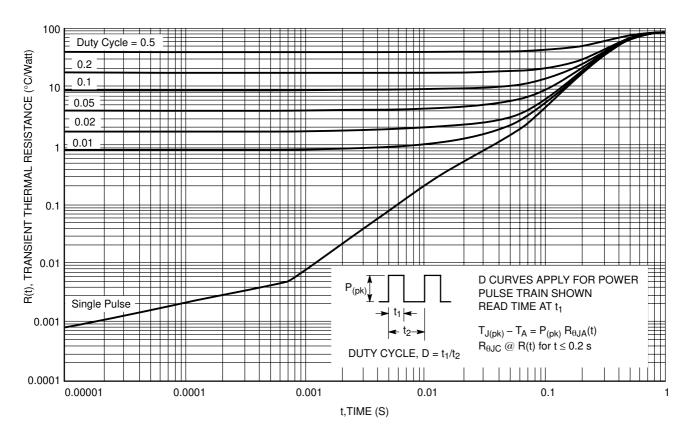
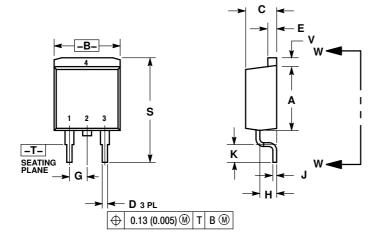


Figure 19. Transient Thermal Resistance (Non-normalized Junction-to-Ambient mounted on minimum pad area)

PACKAGE DIMENSIONS

D²PAK 3 CASE 418B-04 ISSUE J



MILLIMETERS **INCHES** DIM MIN MAX A 0.340 0.380 MIN MAX DIM 8.64 9.65 0.380 0.405 9.65 10.29 C 0.160 0.190 4.06 4.83 D 0.020 0.035 0.51 0.89 0.045 0.055 1.40 1.14 **F** 0.310 0.350 7.87 8.89 G 0.100 BSC 2.54 BSC **H** 0.080 0.110 2.03 2.79 0.018 0.025

 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

NEW STANDARD 418B-04.

CONTROLLING DIMENSION: INCH. 418B-01 THRU 418B-03 OBSOLETE,

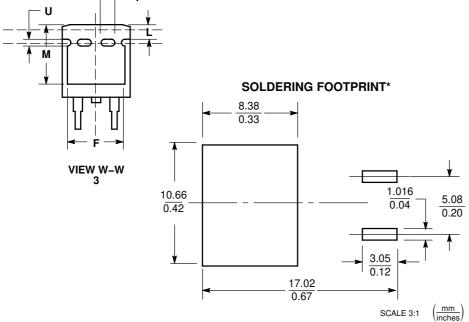
| H | 0.080 | 0.110 | 2.03 | 2.79 | J | 0.018 | 0.025 | 0.46 | 0.64 | K | 0.090 | 0.110 | 2.29 | 2.79 | L | 0.052 | 0.072 | 1.32 | 1.83 | M | 0.280 | 0.320 | 7.11 | 8.13 | M | 0.197 | REF | 5.00 | REF | P | 0.079 | REF | 2.00 | REF | R | 0.039 | REF | 0.99 | REF | S | 0.575 | 0.625 | 14.60 | 15.88 | V | 0.045 | 0.055 | 1.14 | 1.40 |

STYLE 4: PIN 1. GATE

NOTES

3.

COLLECTOR
 EMITTER
 COLLECTOR



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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