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NHD-5.7-320240WFB-ATXI#-1

TFT (Thin-Film-Transistor) Color Liquid Crystal Display Module

| | |
|---------|--------------------------------|
| NHD- | Newhaven Display |
| 5.7- | 5.7" Diagonal |
| 320240- | 320xRGBx240 pixels |
| WFB- | Model |
| A- | Built-in driver, No Controller |
| T- | White LED backlight |
| X- | TFT |
| I- | 6:00 view, Wide Temp |
| #-1 | RoHS Compliant |

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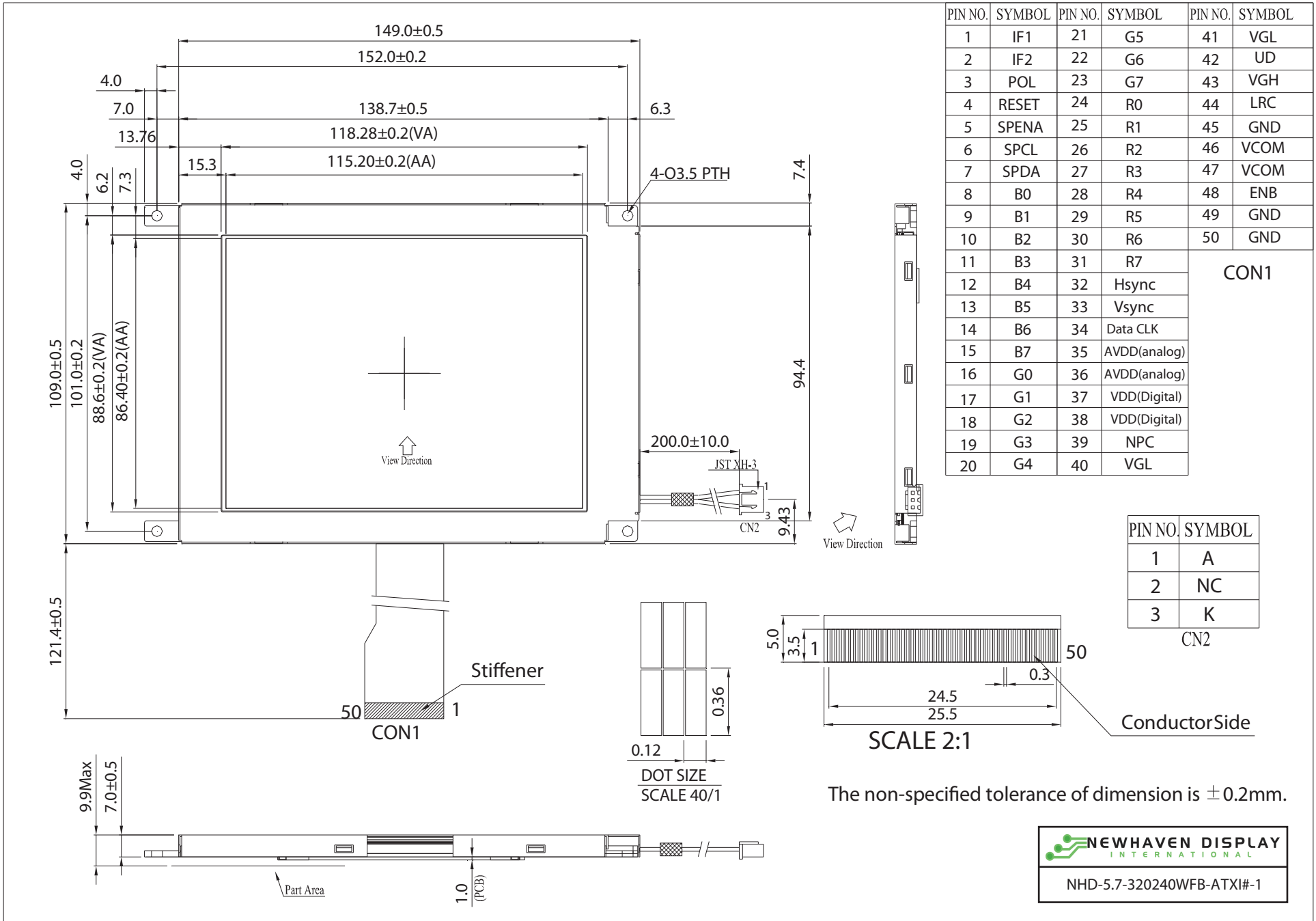
Document Revision History

| Revision | Date | Description | Changed by |
|----------|-----------|---------------------------------|------------|
| 0 | 5/23/2012 | Initial Release | AK |
| 1 | 5/29/2012 | Optical characteristics updated | AK |

Functions and Features

- 320xRGBx240 resolution
- LED backlight
- 24-bit Parallel RGB interface
- Built-in Source Driver: HX8218-A
- Built-in Gate Driver: HX8615

Mechanical Drawing



| PIN NO. | SYMBOL | PIN NO. | SYMBOL | PIN NO. | SYMBOL |
|---------|--------|---------|--------------|---------|--------|
| 1 | IF1 | 21 | G5 | 41 | VGL |
| 2 | IF2 | 22 | G6 | 42 | UD |
| 3 | POL | 23 | G7 | 43 | VGH |
| 4 | RESET | 24 | R0 | 44 | LRC |
| 5 | SPENA | 25 | R1 | 45 | GND |
| 6 | SPCL | 26 | R2 | 46 | VCOM |
| 7 | SPDA | 27 | R3 | 47 | VCOM |
| 8 | B0 | 28 | R4 | 48 | ENB |
| 9 | B1 | 29 | R5 | 49 | GND |
| 10 | B2 | 30 | R6 | 50 | GND |
| 11 | B3 | 31 | R7 | CON1 | |
| 12 | B4 | 32 | Hsync | | |
| 13 | B5 | 33 | Vsync | | |
| 14 | B6 | 34 | Data CLK | | |
| 15 | B7 | 35 | AVDD(analog) | | |
| 16 | G0 | 36 | AVDD(analog) | | |
| 17 | G1 | 37 | VDD(Digital) | | |
| 18 | G2 | 38 | VDD(Digital) | | |
| 19 | G3 | 39 | NPC | | |
| 20 | G4 | 40 | VGL | | |

| PIN NO. | SYMBOL |
|---------|--------|
| 1 | A |
| 2 | NC |
| 3 | K |

CN2

Conductor Side

The non-specified tolerance of dimension is ±0.2mm.



Pin Description

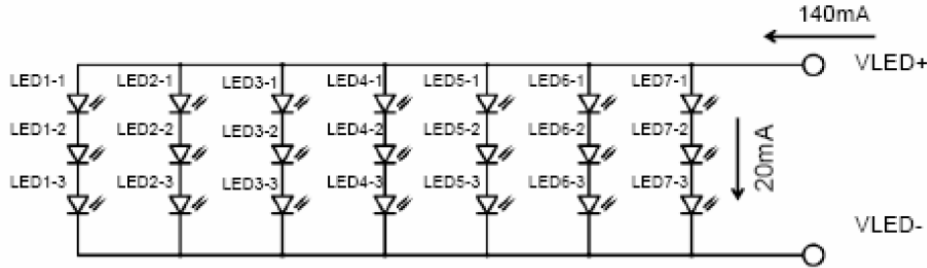
| Pin No. | Symbol | I/O | Description | Remark |
|---------|--------------|-----|--|--------|
| 1 | IF1 | I | Input data format control (Note1) | Note1 |
| 2 | IF2 | I | Input data format control (Note1) | Note1 |
| 3 | POL | O | Polarity Signal connect to VCOM driving circuit. | Note3 |
| 4 | RESET | I | Hardware reset. | |
| 5 | SPENA | I | Chip select | Note2 |
| 6 | SPCL | I | Serial Clock | Note2 |
| 7 | SPDA | I/O | Serial Data | |
| 8 | B0 | I | Blue Data bit (LSB) | |
| 9 | B1 | I | Blue Data bit | |
| 10 | B2 | I | Blue Data bit | |
| 11 | B3 | I | Blue Data bit | |
| 12 | B4 | I | Blue Data bit | |
| 13 | B5 | I | Blue Data bit | |
| 14 | B6 | I | Blue Data bit | |
| 15 | B7 | I | Blue Data bit(MSB) | |
| 16 | G0 | I | Green Data bit(LSB) | |
| 17 | G1 | I | Green Data bit | |
| 18 | G2 | I | Green Data bit | |
| 19 | G3 | I | Green Data bit | |
| 20 | G4 | I | Green Data bit | |
| 21 | G5 | I | Green Data bit | |
| 22 | G6 | I | Green Data bit | |
| 23 | G7 | I | Green Data bit(MSB) | |
| 24 | R0 | I | Red Data bit(LSB) | |
| 25 | R1 | I | Red Data bit | |
| 26 | R2 | I | Red Data bit | |
| 27 | R3 | I | Red Data bit | |
| 28 | R4 | I | Red Data bit | |
| 29 | R5 | I | Red Data bit | |
| 30 | R6 | I | Red Data bit | |
| 31 | R7 | I | Red Data bit(MSB) | |
| 32 | Hsync | I | Horizontal synchronous signal | |
| 33 | Vsync | I | Vertical synchronous signal | |
| 34 | Data CLK | I | Dot data clock | |
| 35 | AVDD(analog) | I | Analog power: 4.5V-5.5V | |
| 36 | AVDD(analog) | I | Analog power: 4.5V-5.5V | |
| 37 | VDD(digital) | I | Digital power: 3V-3.5V | |
| 38 | VDD(digital) | I | Digital power: 3V-3.5V | |
| 39 | NPC | O | NTSC/PAL mode Auto detection result H:NTSC/L:PAL | |
| 40 | VGL | I | Gate off power | |
| 41 | VGL | I | Gate off power | |
| 42 | UD | I | Up/Down scan setting. H: Reverse scan / L: Normal scan | |
| 43 | VGH | I | Gate on power | |
| 44 | LRC | I | Shift direction of device internal shift register control. | |
| 45 | GND | I | GROUND | |
| 46 | VCOM | I | VCOM driving input | Note3 |
| 47 | VCOM | I | VCOM driving input | |
| 48 | ENB | I | Data enable input. Normally pull low. | Note4 |
| 49 | GND | I | GROUND | |
| 50 | GND | I | GROUND | |

Recommended LCD connector: 50-pin, 0.5mm pitch FFC connector. Molex 54132-5097

Backlight:

| Pin No. | Symbol | Connection | Description |
|---------|--------|--------------|-------------------------------|
| 1 | VDD | Power Supply | Red, LED Anode (140mA @ 9.9V) |
| 2 | NC | - | No Connect |
| 3 | VSS | Power Supply | White, LED Cathode |

Backlight connector: JST p/n: XHP-3 **Mates with:** JST p/n: B 3B-XH-A



Note 1: Input data format

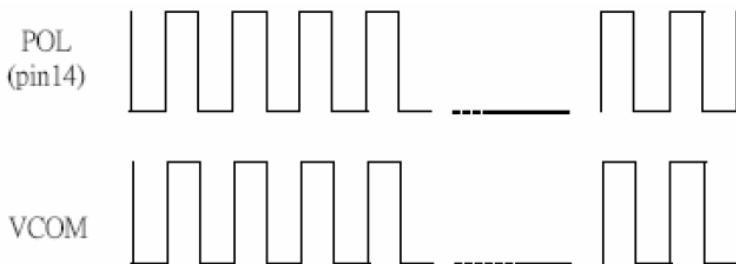
| IF2, IF1 | Input data format |
|---------------|-------------------|
| L,L (default) | Serial RGB |
| L,H | Parallel RGB |
| H,L | CCIR601 |
| H,H | CCIR656 |

Note 2: Pins 5 and 6 typically pulled high

Note 3: Polarity of VCOM (pins 46,47) should be generated from POL (pin 3)

Note 4: For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported. If ENB signal is fixed low, SYNC mode is used. Otherwise, DE+SYNC mode is used.

Note 5: The phase of POL (pin 3):



Driver Information

Built-in Source Driver HX8218-A: http://www.newhavendisplay.com/app_notes/HX8218.pdf

Built-in Gate Driver HX8615: http://www.newhavendisplay.com/app_notes/HX8615.pdf

Electrical Characteristics

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--------------------------------|--------|--------------|---------|------|---------|------|
| Operating Temperature Range | Top | Absolute Max | -20 | - | +70 | °C |
| Storage Temperature Range | Tst | Absolute Max | -30 | - | +80 | °C |
| Supply Voltage for Logic | VDD | | 3.0 | 3.3 | 3.5 | V |
| Supply Voltage for Analog | AVDD | | 4.5 | 5 | 5.5 | V |
| "H" Level input | Vih | | 0.7*VDD | - | VDD | V |
| "L" Level input | Vil | | 0 | - | 0.3*VDD | V |
| TFT Gate ON operating voltage | VGH | Duty=1/240 | - | 15 | - | V |
| TFT Gate OFF operating voltage | VGL | Duty=1/240 | - | -10 | - | V |
| VCOM driving voltage (Note 6) | VCOM | Duty=1/240 | -2.0 | - | 5.5 | V |
| Supply Current for Digital | IDD | VDD=3.3V, | - | 2.2 | 3.5 | mA |
| Supply Current for Analog | IAVDD | AVDD=5V, | - | 4.7 | 7 | mA |
| Supply Current for Gate ON | IGH | VGH=15V, | - | 0.05 | 0.1 | mA |
| Supply Current for Gate OFF | IGL | VGL=-10V | - | 0.05 | 0.1 | mA |
| | | | | | | |
| Backlight Supply Voltage | VLED | | 9.0 | 9.9 | 10.5 | V |
| Backlight Supply Current | ILED | VLED=9.9V | - | 140 | 210 | mA |
| Backlight Lifetime | | | - | 50K | | Hr |

Note 6: VCOM must be adjusted to optimize display quality, contrast ratio, etc.

Optical Characteristics

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------------|--------|-----------|------|------|------|-------------------|
| Viewing Angle – Top (Note 7) | | Cr ≥ 5 | 40 | 60 | | ° |
| Viewing Angle – Bottom (Note 7) | | Cr ≥ 5 | 60 | 70 | | ° |
| Viewing Angle – Left | | Cr ≥ 5 | 60 | 70 | | ° |
| Viewing Angle – Right | | Cr ≥ 5 | 60 | 70 | | ° |
| Contrast Ratio | Cr | | - | 250 | - | |
| Luminance | YL | | 300 | - | - | cd/m ² |
| Response Time (rise) | Tr | - | - | 15 | | ms |
| Response Time (fall) | Tf | - | - | 35 | | ms |

Note 7: Viewing direction – 12:00; Gray Scale inversion direction – 6:00.

Timing Characteristics

CCIR601/656 Interface

Input Signal Characteristics

| PARAMETER | Symbol | Min. | Typ. | Max. | Unit |
|-----------------|-----------|------|------|------|------|
| CLK period | T_{OSC} | - | 37 | - | ns |
| Data setup time | T_{SU} | 12 | - | - | ns |
| Data hold time | T_{HD} | 12 | - | - | ns |

Hardware Reset Timing

| PARAMETER | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------|-----------|------|------|------|---------|
| RESET low pulse width | T_{RSB} | 10 | - | - | μ S |

Output Signal Characteristics

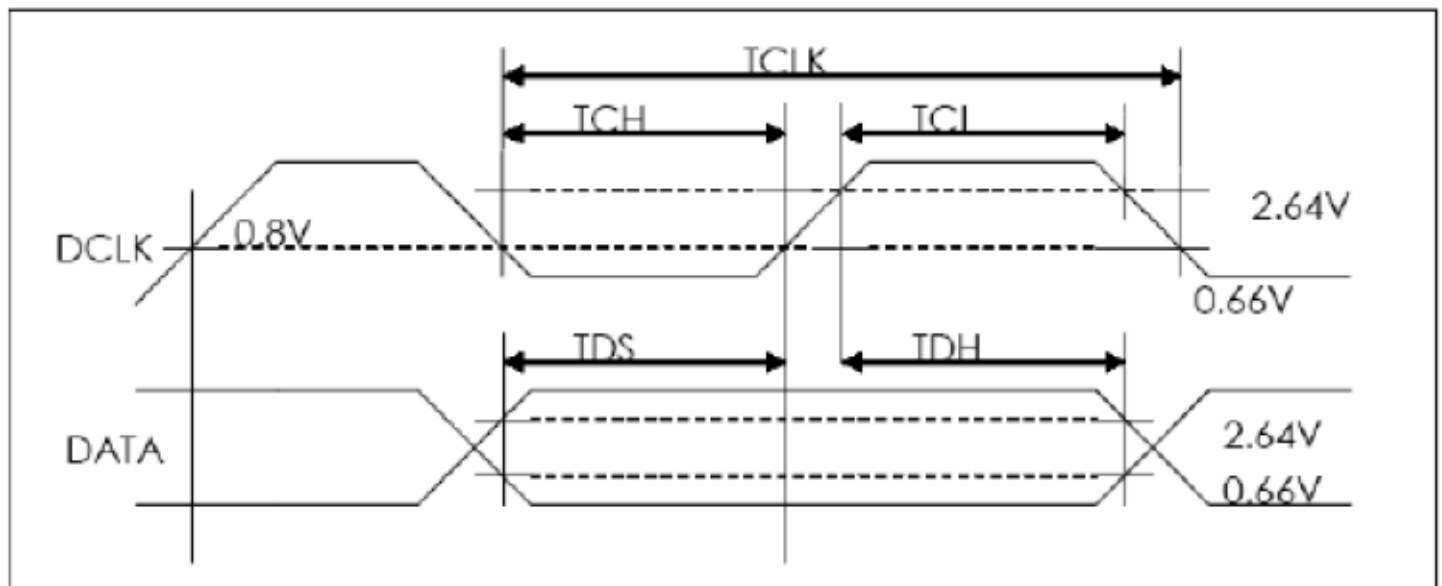
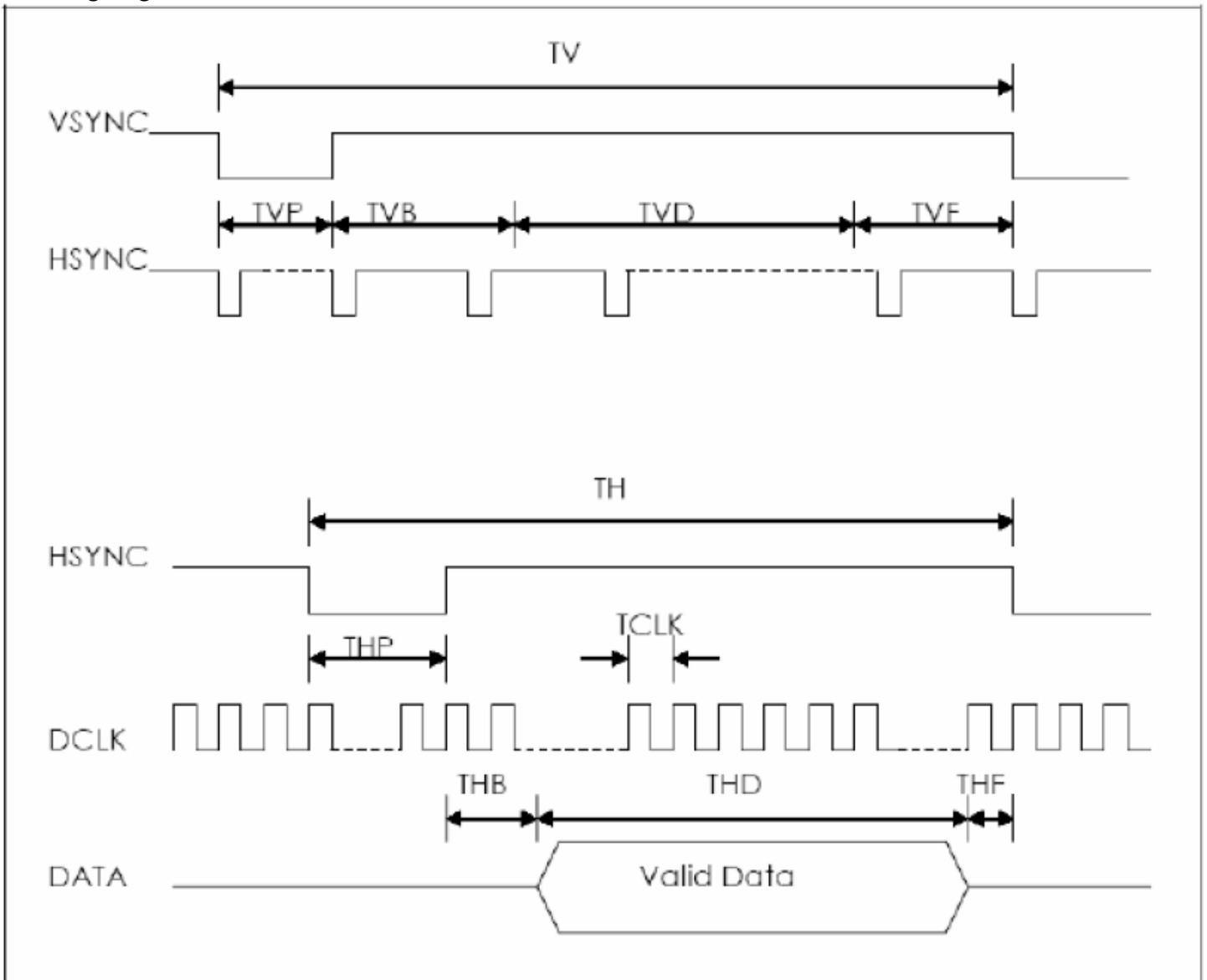
| PARAMETER | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------|-----------|------|------|------|---------|
| Rising time | T_r | - | - | 10 | ns |
| Falling time | T_f | - | - | 10 | ns |
| Internal STH setup time | T_{SUS} | 12 | - | - | ns |
| Internal STH hold time | T_{HDS} | 12 | - | - | ns |
| Internal data setup time | T_{SUD} | 60 | - | - | ns |
| Internal data hold time | T_{HDD} | 40 | - | - | ns |
| OEH pulse width | T_{OEH} | - | 1248 | - | ns |
| OEV pulse width | T_{OEV} | - | 4992 | - | ns |
| CKV pulse width | T_{CKV} | - | 3744 | - | ns |
| Hsync – DEH time | T_1 | - | 4368 | - | ns |
| Hsync – CKV time | T_2 | - | 2496 | - | ns |
| Hsync – OEV time | T_3 | - | 624 | - | ns |
| Vsync – setup time | T_{SUV} | | 1872 | - | ns |
| Vsync – pulse time | T_{STV} | | 1 | - | T_H |
| Vsync – STV time | NTSC | | 19 | - | T_H |
| | PAL | | 27 | - | T_H |
| OEH – STV time | T_{HE} | - | 2 | - | T_H |
| Output settling time | T_{OES} | - | 12 | 20 | μ S |

24-bit Parallel RGB Interface

AC Timing Characteristics

| Signal | Item | | Symbol | Min | Typ | Max | Unit |
|--------|----------------|------|--------|-----|-------|-----|------|
| Dclk | Frequency | | Dclk | - | 6.4 | - | MHZ |
| | High Time | | Tch | - | 78 | - | ns |
| | Low Time | | Tcl | - | 78 | - | ns |
| Data | Setup Time | | Tds | 12 | - | - | ns |
| | Hold Time | | Tdh | 12 | - | - | ns |
| Hsync | Period | | TH | - | 408 | - | DCLK |
| | Pulse Width | | Thp | - | 30 | - | DCLK |
| | Back-Porch | | Thb | - | 38 | - | DCLK |
| | Display Period | | Thd | - | 320 | - | DCLK |
| | Front-Porch | | Thf | - | 20 | - | DCLK |
| Vsync | Period | NTSC | Tv | - | 262.5 | - | TH |
| | | PAL | | | 312.5 | | |
| | Pulse Width | | Tvp | 1 | 3 | 5 | TH |
| | Back-Porch | NTSC | Tvb | - | 15 | - | TH |
| | | PAL | | | 23 | | |
| | Display Period | | Tvd | - | 240 | - | TH |
| | Front-Porch | NTSC | Tvf | - | 4.5 | - | TH |
| | | PAL | | | 46.5 | | |

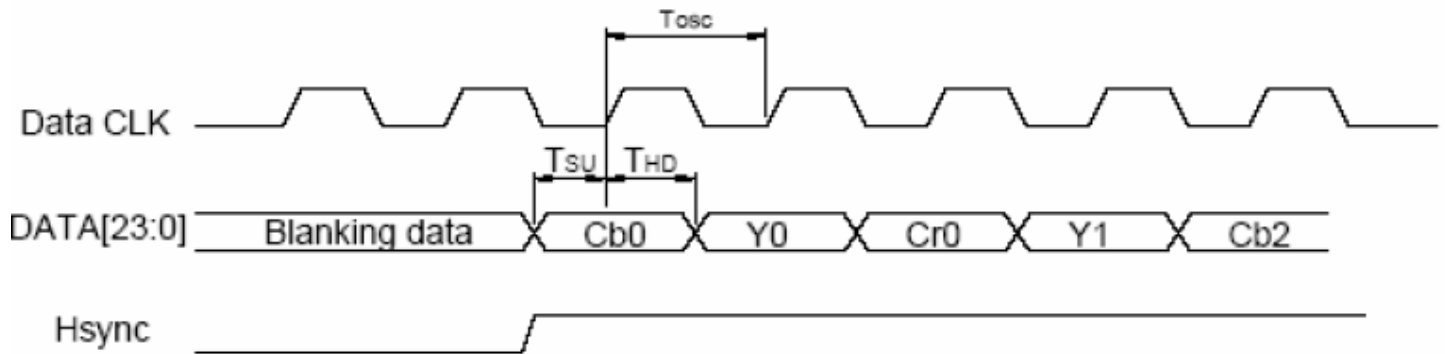
AC Timing Diagrams



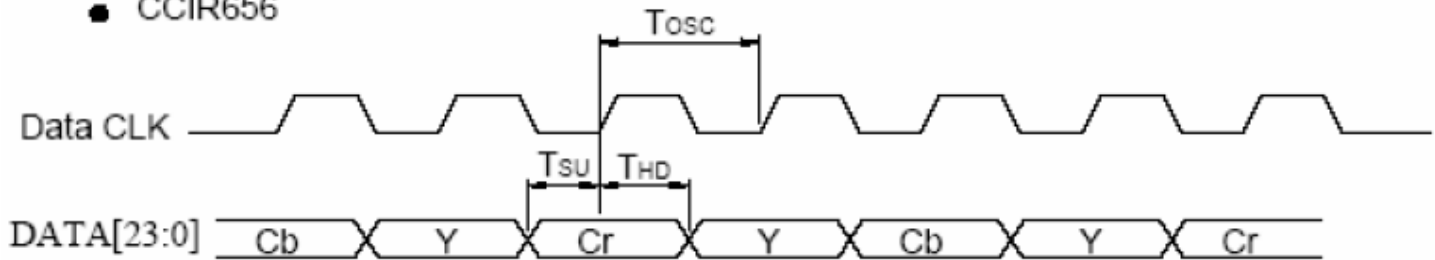
Waveforms

Clock and Data waveform

- CCIR601(HS_POL="L" in Register R2)



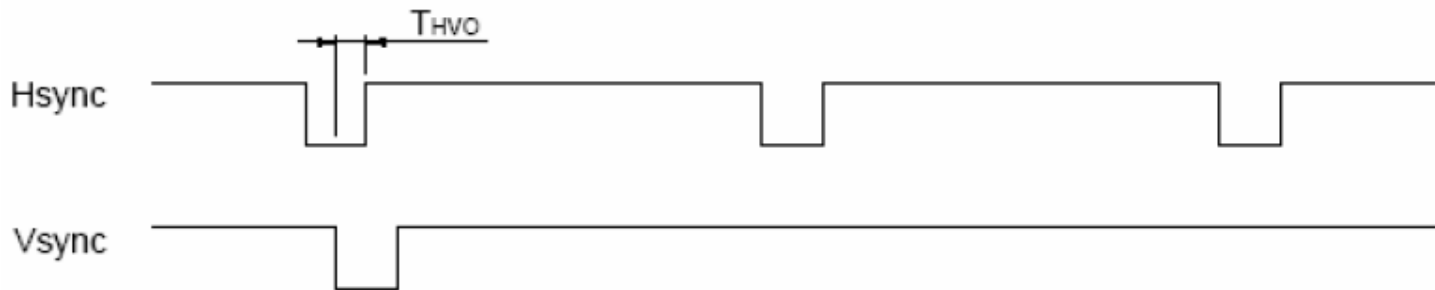
- CCIR656



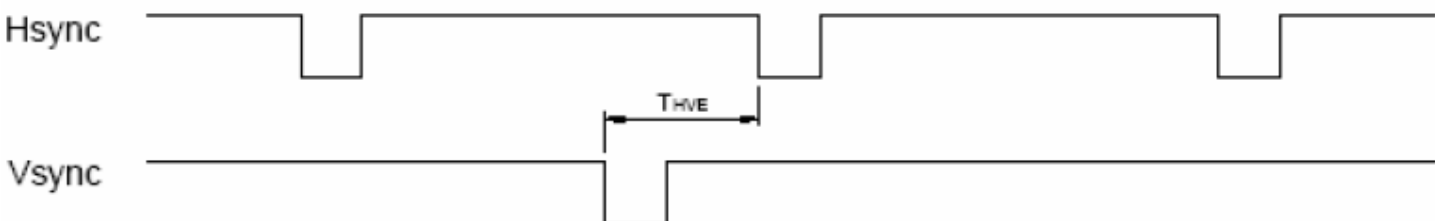
Digital/Analog RGB timing waveform

Hsync and Vsync Timing

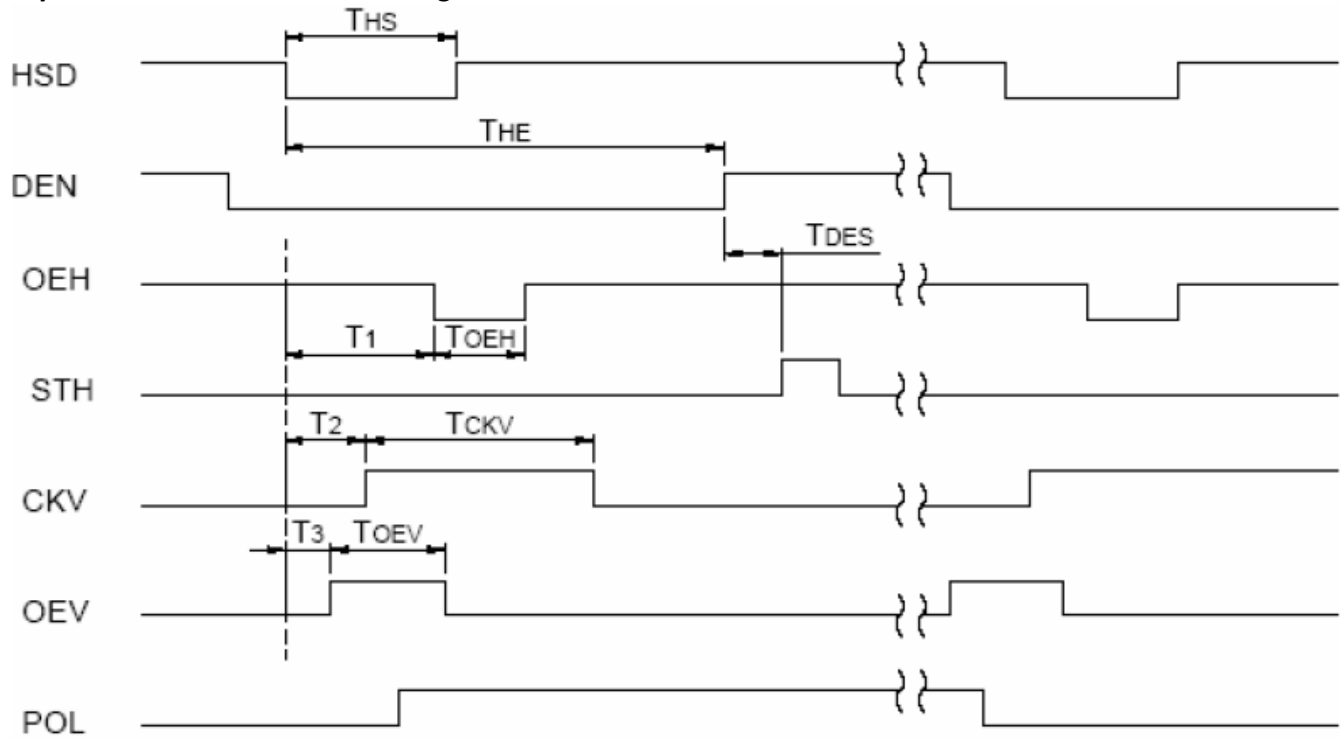
- Odd field



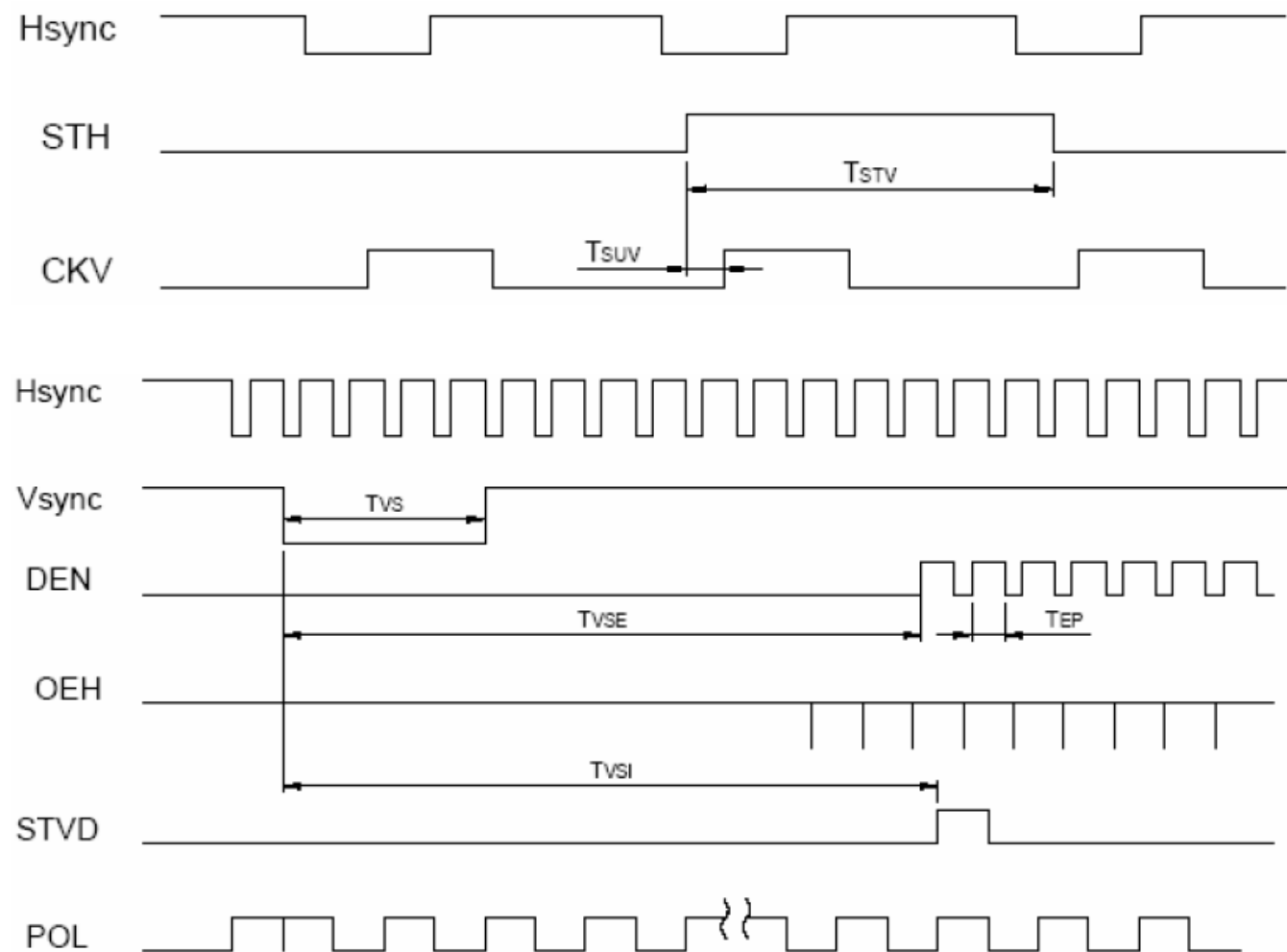
- Even field



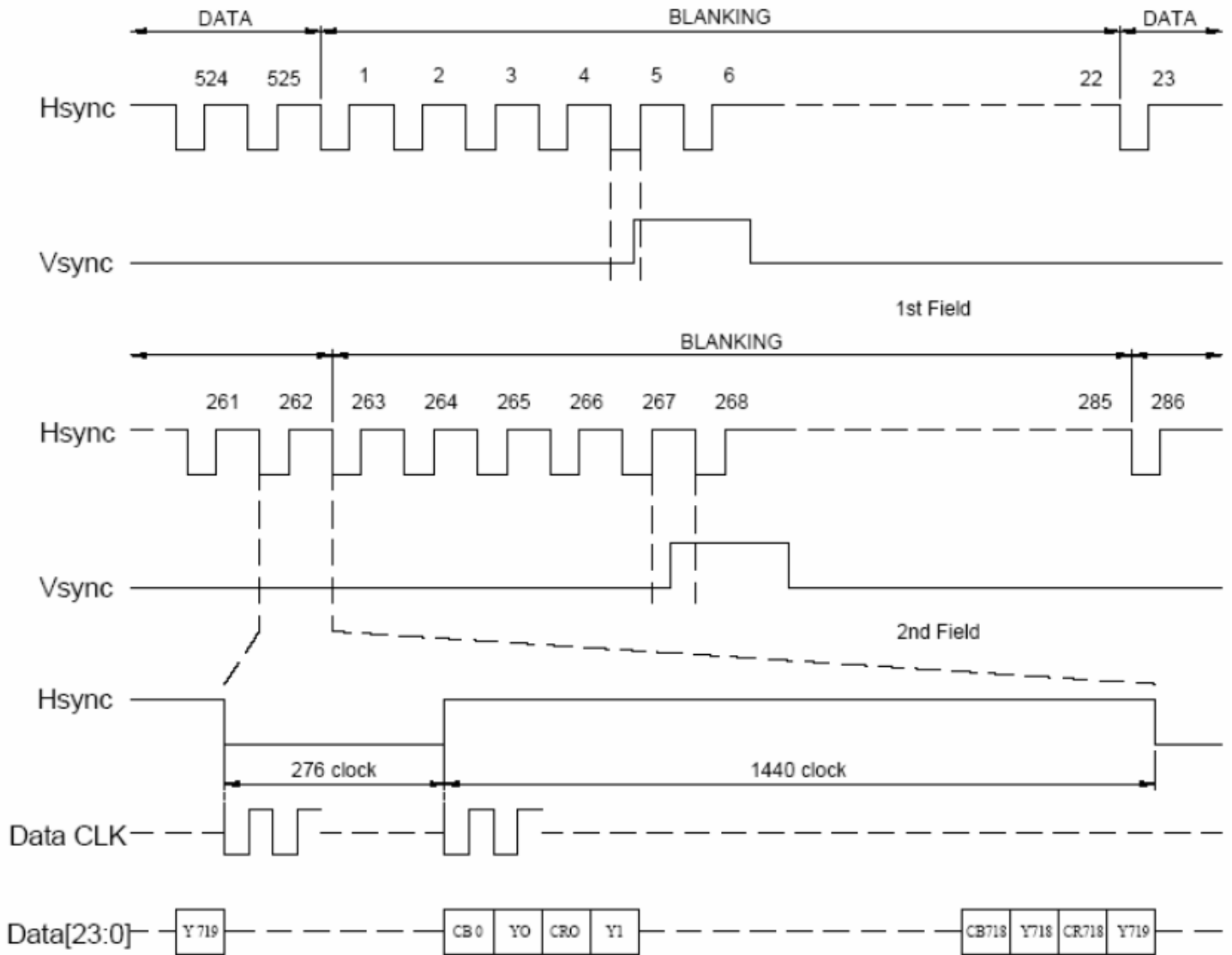
Hsync and Horizontal Control Timing Waveform



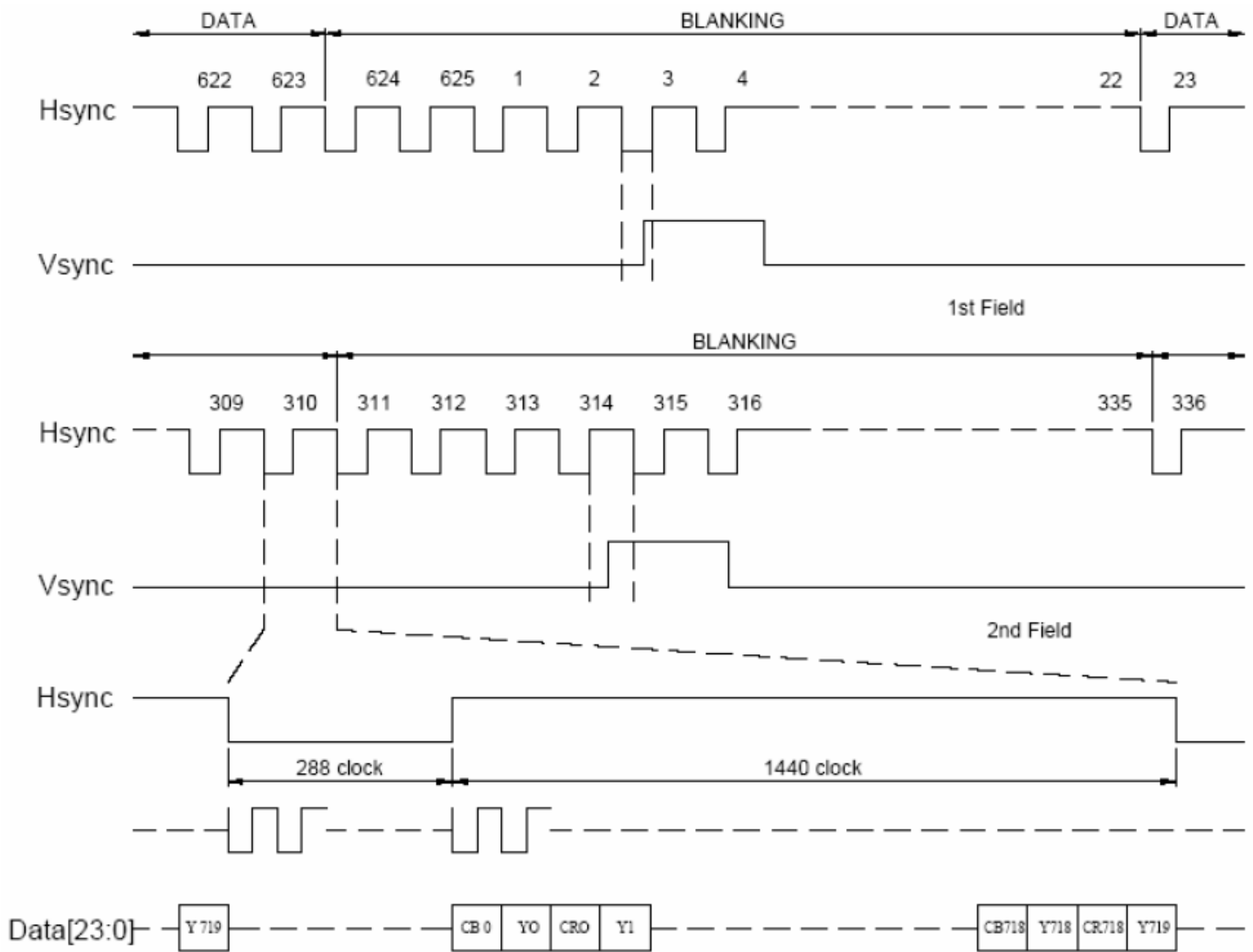
Hsync and Vertical Shift Clock Timing Waveform



CCIR601 Timing Waveform (VS_POL = "H", HS_POL = "L" in register R2)

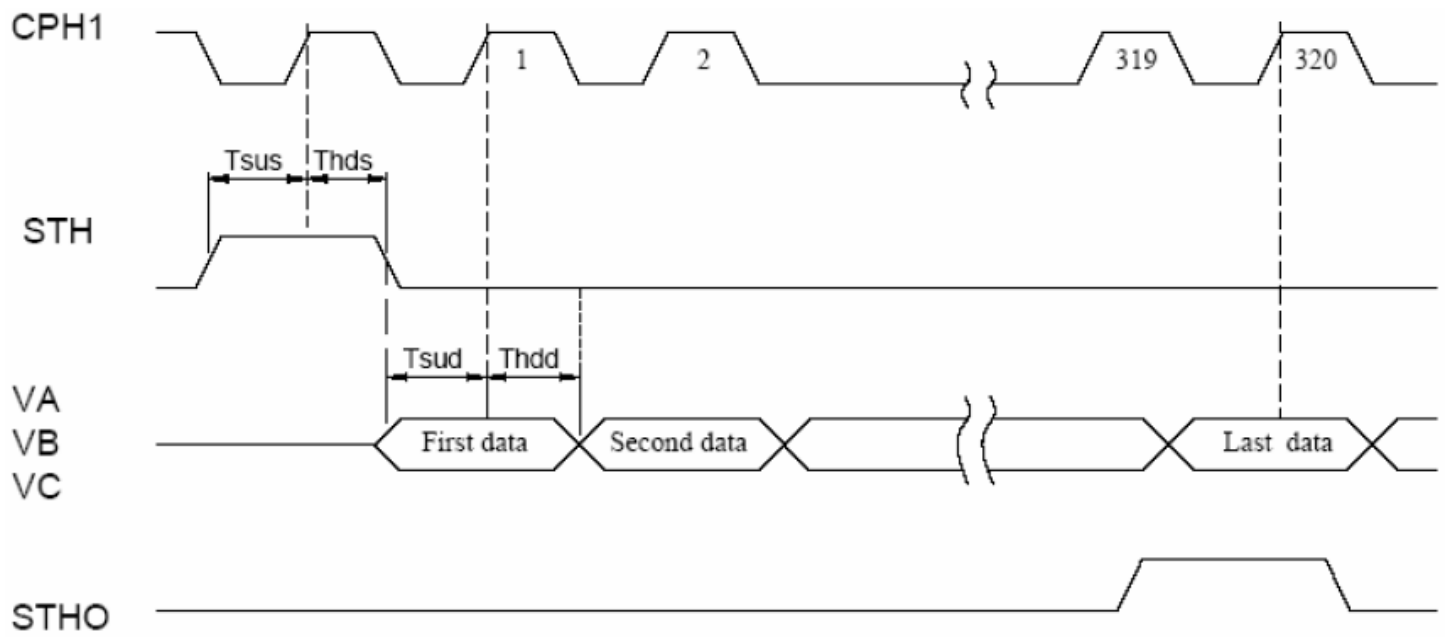


ITU-BT.601 NTSC Input Timing

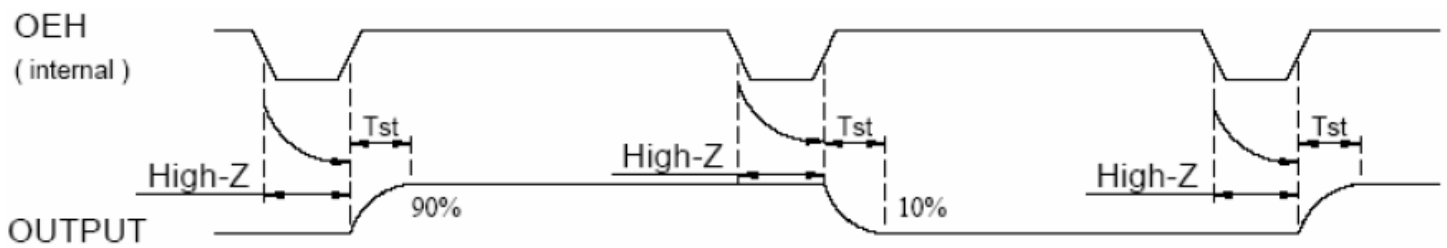


ITU-BT.601 PAL Input Timing

Clock and Start Pulse Timing Waveform

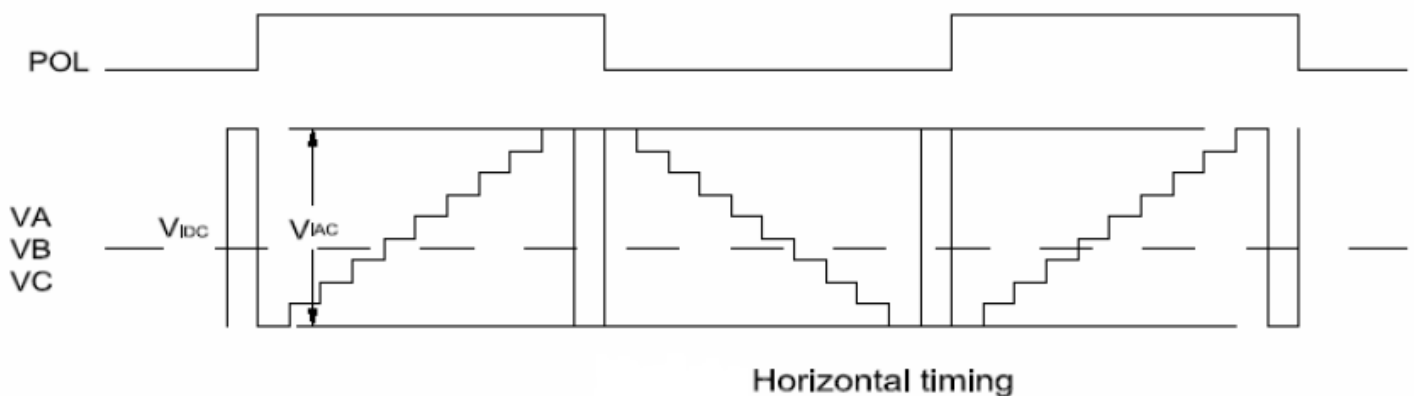


OEH and Data Output timing Waveform



Analog Video Signal Characteristics

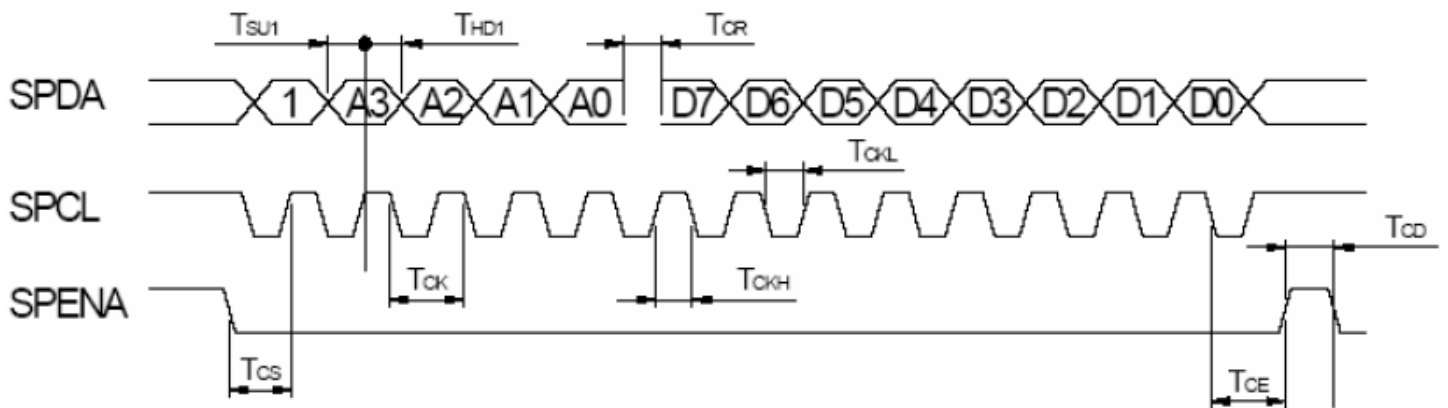
| PARAMETER | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------------|-----------|------|-------|------|------|
| Video signal amplitude (VA, VB, VC) | V_{IAC} | - | 3.81 | - | V |
| | V_{IDC} | - | 2.385 | - | V |



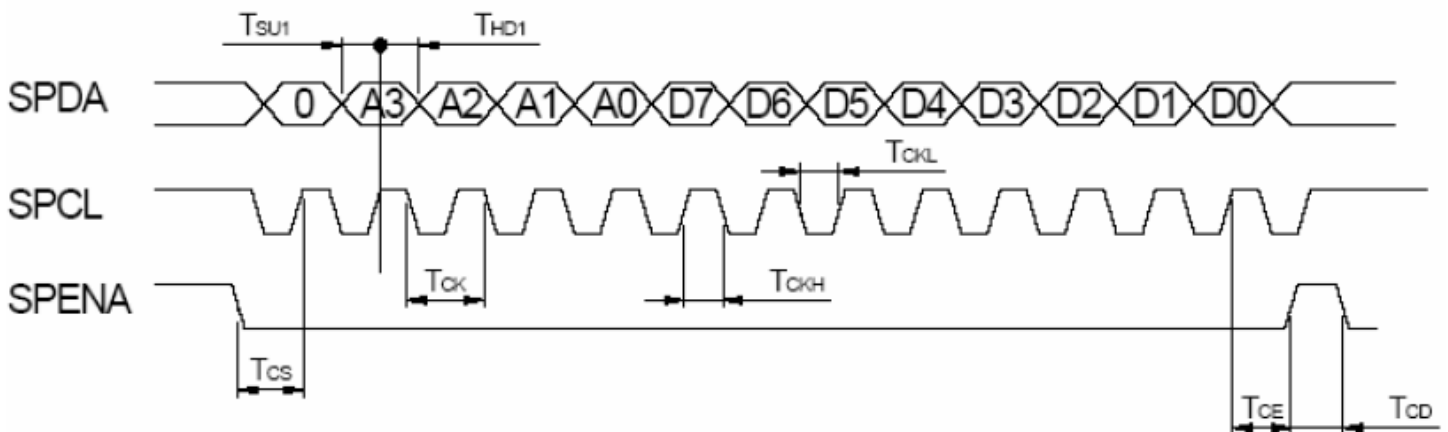
SPI Timing Characteristics

| PARAMETER | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------|-----------|------|------|------|----------|
| SPCL period | T_{CK} | 60 | - | - | ns |
| SPCL high width | T_{CKH} | 30 | - | - | ns |
| SPCL low width | T_{CKL} | 30 | - | - | ns |
| Data setup time | T_{SU1} | 12 | - | - | ns |
| Data hold time | T_{HD1} | 12 | - | - | ns |
| SPENA to SPCK setup time | T_{CS} | 20 | - | - | ns |
| SPENA to SPDA hold time | T_{CE} | 20 | - | - | ns |
| SPENA high pulse width | T_{CD} | 50 | - | - | ns |
| SPDA output latency | T_{CR} | | 1/2 | - | T_{CK} |

● SPI "read" timing

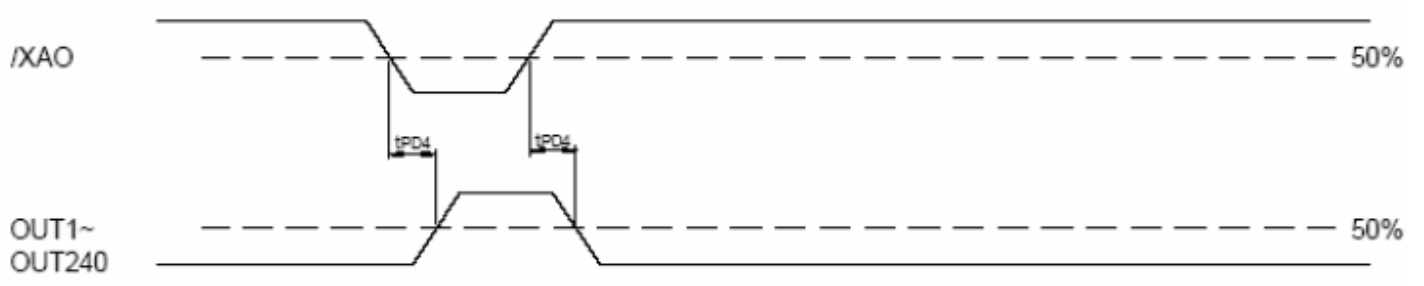
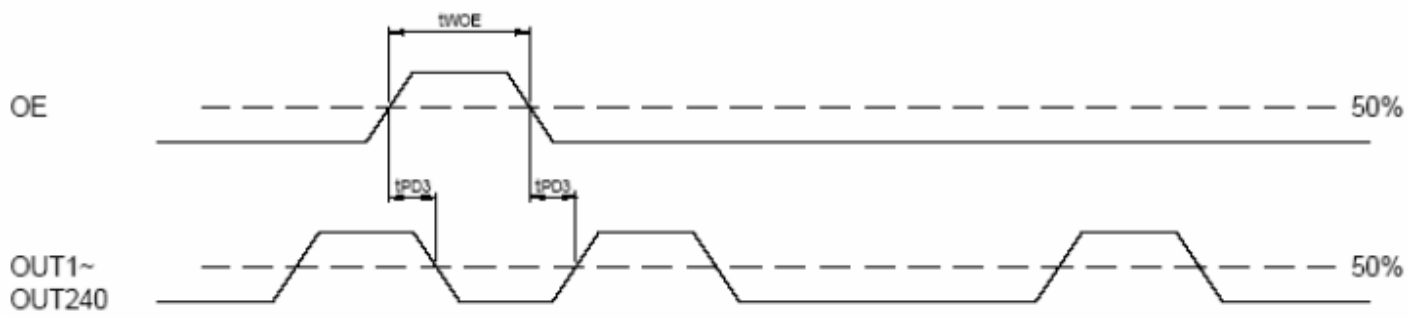
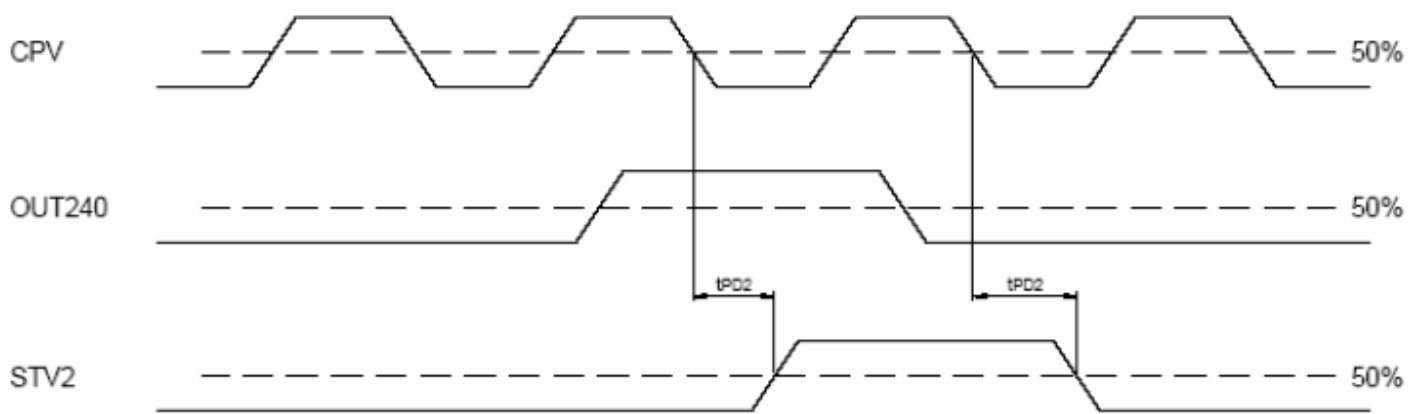
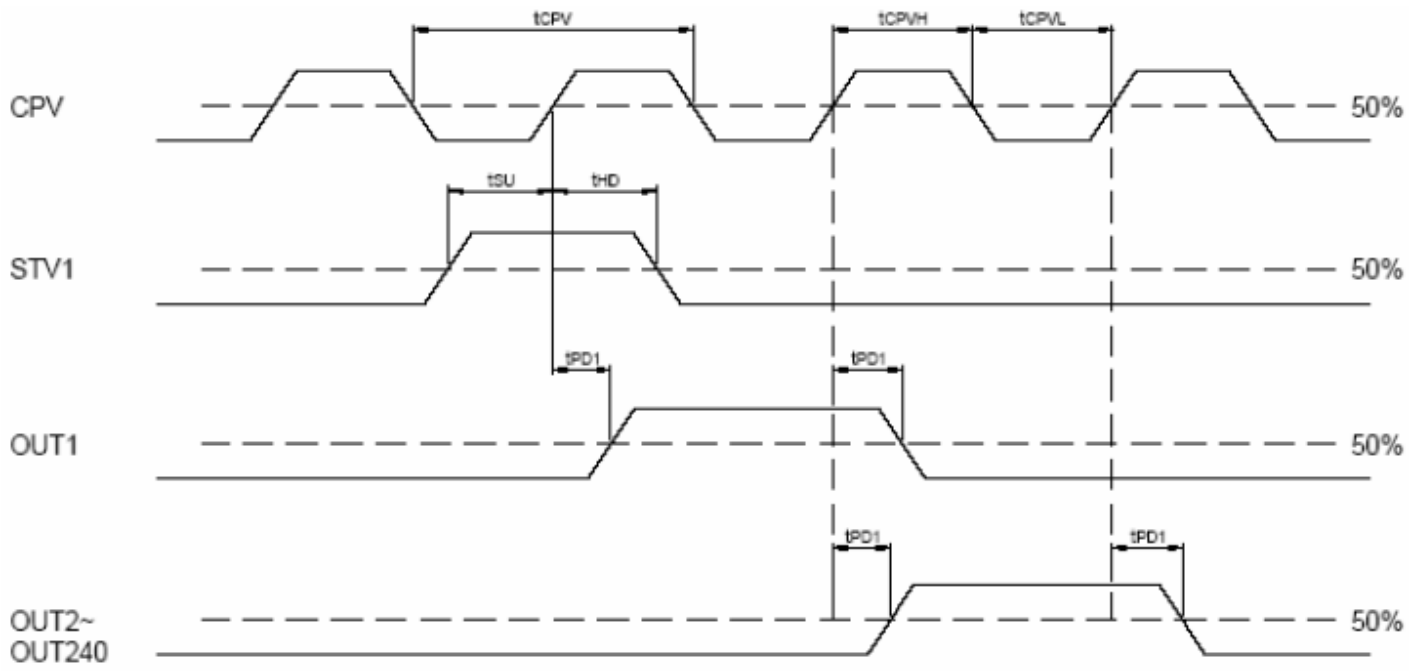


● SPI "write" timing



Gate Driver Timing Chart

| Parameter | Symbol | Condition | Spec | | Unit |
|---------------------|-------------|---------------|------|------|---------|
| | | | Min. | Max. | |
| Operation frequency | tCPV | | 5 | - | μ s |
| CPV pulse width | tCPVH,tCPVL | 50%duty cycle | 2.5 | - | |
| OE pulse width | twOE | | 1 | - | |
| Data setup time | tsu | | 0.4 | - | us |
| Data hold time | thd | | 0.7 | - | |
| Output delay time | tpd1 | CL=300pF | - | 1 | |
| Output delay time | tpd2 | CL=300pF | - | 0.8 | |
| Output delay time | tpd3 | CL=300pF | - | 0.8 | |
| Output delay time | tpd4 | CL=300pF | - | 10 | |



Quality Information

| Test Item | Content of Test | Test Condition | Note |
|---------------------------------------|---|---|------|
| High Temperature storage | Endurance test applying the high storage temperature for a long time. | +80°C , 240hrs | 2 |
| Low Temperature storage | Endurance test applying the low storage temperature for a long time. | -30°C , 240hrs | 1,2 |
| High Temperature Operation | Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time. | +70°C 240hrs | 2 |
| Low Temperature Operation | Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time. | -20°C , 240hrs | 1,2 |
| High Temperature / Humidity Operation | Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time. | +60°C , 90% RH , 240hrs | 1,2 |
| Thermal Shock resistance | Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress. | -20°C,30min -> 25°C,5min -> 70°C,30min = 1 cycle 10 cycles | |
| Vibration test | Endurance test applying vibration to simulate transportation and use. | 10-55Hz , 15mm amplitude. 60 sec in each of 3 directions X,Y,Z For 15 minutes | 3 |
| Static electricity test | Endurance test applying electric static discharge. | VS=800V, RS=1.5kΩ, CS=100pF One time | |

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.

Precautions for using LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information and Terms & Conditions

http://www.newhavendisplay.com/index.php?main_page=terms