Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NHS3100

Temperature logger

Rev. 6.03 — 15 June 2018 Product data sheet

1 General description

The NHS3100 is an IC optimized for temperature monitoring and logging. It has an embedded NFC interface, an internal temperature sensor and a direct battery connection. These features support an effective system solution with a minimal number of external components and a single layer foil implementation for temperature monitoring. The NHS3100 works either battery-powered or NFC-powered.

The embedded ARM Cortex-M0+ offers flexibility to the users of this IC to implement their own dedicated solution. The NHS3100 contains multiple features, including multiple Power-down modes and a selectable CPU frequency of up to 8 MHz, for ultra low power consumption.

Users can program this NHS3100 with the industry-wide standard solutions for ARM Cortex-M0+ processors.

As of September 22, 2017, this device has been certified by the NFC forum (certification ID: 58516).

CAUTION	
	Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

CAUTION	
 msc896	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

2 Features and benefits

2.1 System

- ARM Cortex-M0+ processor running at frequencies of up to 8 MHz
- ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC)
- ARM Serial Wire Debug (SWD)
- System tick timer
- IC reset input

2.2 Memory

- 32 kB on-chip flash programming memory
- 4 kB on-chip EEPROM of which 320 bytes are write-protected
- 8 kB SRAM

2.3 Digital peripherals

- Up to 12 General Purpose Input Output (GPIO) pins with configurable pull-up/pull-down resistors and repeater mode
- GPIO pins which can be used as edge and level sensitive interrupt sources
- High-current drivers (sink only; 20 mA) on four GPIO pins
- High-current drivers (sink only; 20 mA) on two I^2C-bus pins
- Programmable WatchDog Timer (WDT)

2.4 Analog peripherals

- Temperature sensor with ±0.3 °C absolute temperature accuracy between 0 °C and 40 °C and ±0.5 °C in the range −40 °C and +85 °C

2.5 Communication interfaces

- NFC/RFID ISO 14443 type A interface; NFC forum type 2 compatible
- I^2C-bus interface supporting full I^2C-bus specification and Fast-mode with a data rate of 400 kbit/s, with multiple-address recognitions and Monitor mode

2.6 Clock generation

- 8 MHz internal RC oscillator, trimmed to 2 % accuracy, which is used for the system clock
- Timer oscillator operating at 32 kHz linked to the RTC timer unit

2.7 Power control

- Support for 1.72 V to 3.6 V external voltages
- The NHS3100 can also be powered from the NFC field.
- Activation via NFC possible
- Integrated Power Management Unit (PMU) for versatile control of power consumption
- Four reduced power modes for ARM Cortex-M0+: Sleep, Deep-sleep, Deep power-down and Battery-off
- Power gating for each analog peripheral for ultra-low power operation
- < 50 nA IC current consumption in Battery-off mode at 3.0 V
- Power-On Reset (POR)

2.8 General

- Unique device serial number for identification

3 Applications

- Temperature measurement
- Temperature logging
- Cold chain validation

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NHS3100	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3
NHS3100UK	WLCSP25	wafer level chip-scale package; 25 balls; 2.51 × 2.51 × 0.5 mm	SOT1401-1
NHS3100W8	bumped die	bumped die with 8 functional bumps; 2.51 × 2.51 × 0.16 mm	SOT1870-1

5 Marking

Table 2. Marking codes

Type number	Marking code
NHS3100	NHS3100
NHS3100UK	NHS3100
NHS3100W8	no marking code

6 Block diagram

The internal block diagram of the NHS3100 is shown in Figure 1. It consists of a Power Management Unit (PMU), clocks, timers, a digital computation, and a control cluster (ARM Cortex-M0+ and memories) and AHB-APB slave modules.

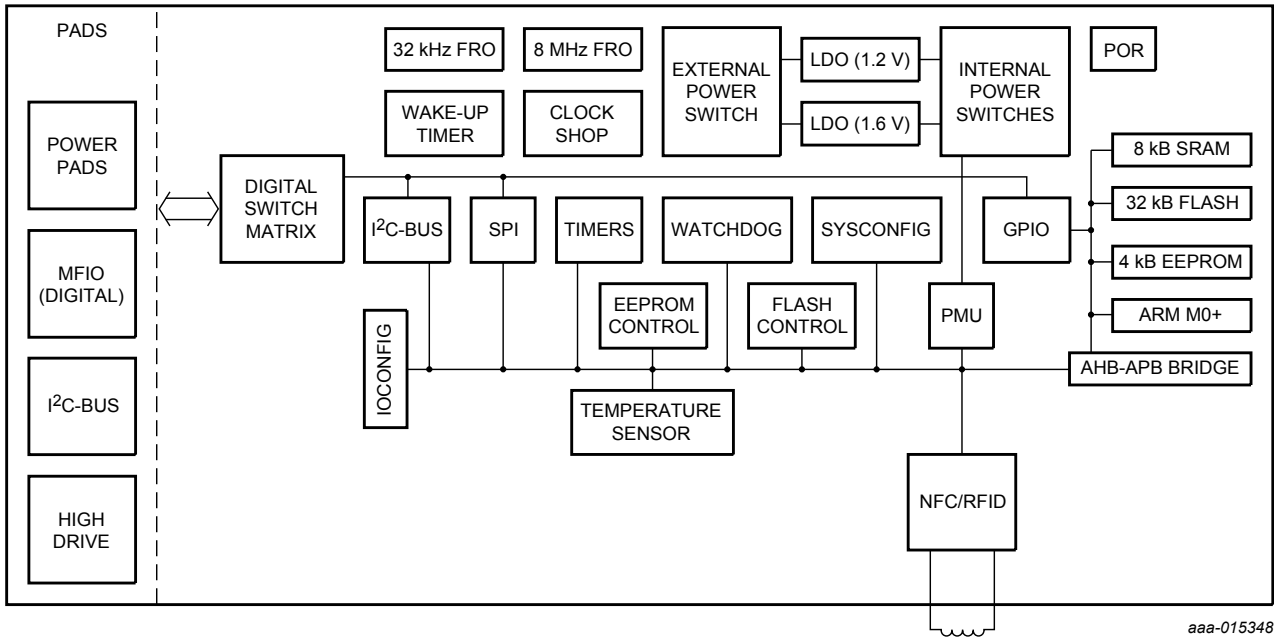

Figure 1. NHS3100 block diagram

7 Pinning information

7.1 Pinning

7.1.1 HVQFN24 package

Figure 2 shows the pad layout of the NHS3100 in the HVQFN24 package.

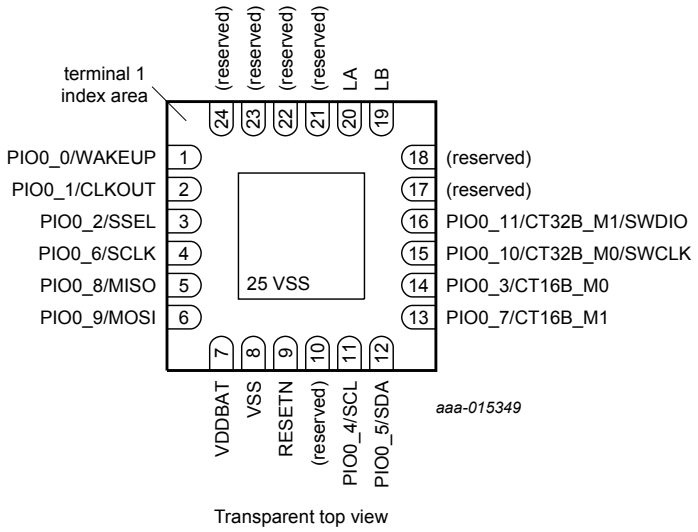

Figure 2. Pad configuration HVQFN24

Table 3. Pad allocation table of the HVQFN24 package

Pad	Symbol	Pad	Symbol
1	PIO0_0/WAKEUP	13[1]	PIO0_7/CT16B_M1
2	PIO0_1/CLKOUT	14[1]	PIO0_3/CT16B_M0
3	PIO0_2/SSEL	15[1]	PIO0_10/CT32B_M0/SWCLK
4	PIO0_6/SCLK	16[1]	PIO0_11/CT32B_M1/SWDIO
5	PIO0_8/MISO	17[2]	(reserved)
6	PIO0_9/MOSI	18[2]	(reserved)
7	VDDBAT	19	LB
8	VSS	20	LA
9	RESETN	21[2]	(reserved)
10	(reserved)	22[2]	(reserved)
11	PIO0_4/SCL	23[2]	(reserved)
12	PIO0_5/SDA	24[2]	(reserved)

[1] High source current pads. See Section 8.6.3.
[2] These pads must be tied to ground.

Table 4. Pad description of the HVQFN24 package

Pad	Symbol	Type	Description
Supply			
7	VDDBAT	supply	positive supply voltage
8	VSS	supply	ground
GPIO[1]			
1	PIO0_0	I/O	GPIO
	WAKEUP	I	Deep power-down mode wake-up pin[2]
2	PIO0_1	I/O	GPIO
	CLKOUT	O	clock output
3	PIO0_2	I/O	GPIO
	SSEL	I	SPI/SSP serial select line
14	PIO0_3	I/O	GPIO
	CT16B_M0	O	16-bit timer match output 0
11	PIO0_4	I/O	GPIO
	SCL	I/O	I^2C-bus SCL clock line
12	PIO0_5	I/O	GPIO
	SDA	I/O	I^2C-bus SDA data line
4	PIO0_6	I/O	GPIO
	SCLK	I/O	SPI/SSP serial clock line
13	PIO0_7	I/O	GPIO
	CT16B_M1	O	16-bit timer match output 1
5	PIO0_8	I/O	GPIO
	MISO	O	SPI/SSP master-in slave-out line
6	PIO0_9	I/O	GPIO
	MOSI	I	SPI/SSP master-out slave-in line
15	PIO0_10	I/O	GPIO
	CT32B_M0	O	32-bit timer match output 0
	SWCLK	I	ARM SWD clock
16	PIO0_11	I/O	GPIO
	CT32B_M1	O	32-bit timer match output 1
	SWDIO	I/O	ARM SWD I/O
Radio			
20	LA	A	NFC antenna/coil terminal A
19	LB	A	NFC antenna/coil terminal B
Reset			
9	RESETN	I	external reset input[3]

[1] The GPIO port is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pads depends on the function selected through the IOCONFIG register block.

[2] If external wake-up is enabled on this pad, it must be pulled HIGH before entering Deep power-down mode and pulled LOW for a minimum of 100 µs to exit Deep power-down mode. It has weak pull-up to VBAT or internal NFC voltage (whichever is highest).

[3] A LOW on this pad resets the device. This reset causes I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. It has weak pull-up to V_{DDBAT}.

7.1.2 WLCSP25 package

Figure 3 shows the ball layout of the NHS3100 in the WLCSP25 package.

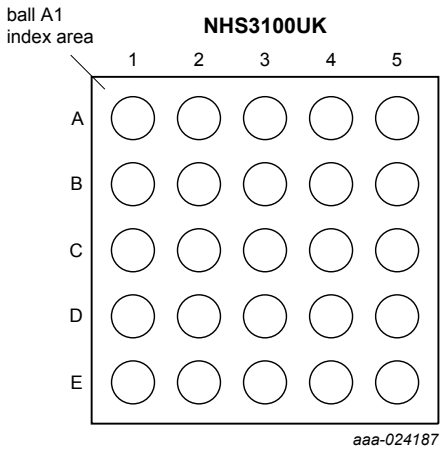

Figure 3. Ball configuration WLCSP25

Table 5. Ball allocation table of the WLCSP25 package

Ball	Symbol	Ball	Symbol
A1	VDDBAT	C4[1]	PIO0_7/CT16B_M1
A2	VSS	C5[1]	PIO0_11/CT32B_M1/SWDIO
A3	RESETN	D1	PIO0_0/WAKEUP
A4	PIO0_4/SCL	D2	PIO0_1/CLKOUT
A5	PIO0_5/SDA	D3[2]	(reserved)
B1	PIO0_8/MISO	D4[2]	(reserved)
B2	PIO0_9/MOSI	D5[2]	(reserved)
B3	(reserved)	E1[2]	(reserved)
B4[1]	PIO0_3/CT16B_M0	E2[2]	(reserved)
B5[1]	PIO0_10/CT32B_M0/SWCLK	E3[2]	(reserved)
C1	PIO0_2/SSEL	E4	LA
C2	PIO0_6/SCLK	E5	LB
C3	VSS	-	-

[1] High source current balls. See Section 8.6.3.

[2] These balls must be tied to ground.

Table 6. Ball description of the WLCSP25 package

Ball	Symbol	Type	Description
Supply			
A1	VDDBAT	supply	positive supply voltage
A2, C3	VSS	supply	ground
GPIO[1]			
D1	PIO0_0	I/O	GPIO
	WAKEUP	I	Deep power-down mode wake-up pin[2]
D2	PIO0_1	I/O	GPIO
	CLKOUT	O	clock output
C1	PIO0_2	I/O	GPIO
	SSEL	I	SPI/SSP serial select line
B4	PIO0_3	I/O	GPIO
	CT16B_M0	O	16-bit timer match output 0
A4	PIO0_4	I/O	GPIO
	SCL	I/O	I^2C-bus SCL clock line
A5	PIO0_5	I/O	GPIO
	SDA	I/O	I^2C-bus SDA data line
C2	PIO0_6	I/O	GPIO
	SCLK	I/O	SPI/SSP serial clock line
C4	PIO0_7	I/O	GPIO
	CT16B_M1	O	16-bit timer match output 1
B1	PIO0_8	I/O	GPIO
	MISO	O	SPI/SSP master-in slave-out line
B2	PIO0_9	I/O	GPIO
	MOSI	I	SPI/SSP master-out slave-in line
B5	PIO0_10	I/O	GPIO
	CT32B_M0	O	32-bit timer match output 0
	SWCLK	I	ARM SWD clock
C5	PIO0_11	I/O	GPIO
	CT32B_M1	O	32-bit timer match output 1
	SWDIO	I/O	ARM SWD I/O
Radio			
E4	LA	A	NFC antenna/coil terminal A
E5	LB	A	NFC antenna/coil terminal B
Reset			
A3	RESETN	I	external reset input[3]

[1] The GPIO port is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depend on the function selected through the IOCONFIG register block.

[2] If external wake-up is enabled on this pin, it must be pulled HIGH before entering Deep power-down mode and pulled LOW for a minimum of 100 µs to exit Deep power-down mode.

[3] A LOW on this pin resets the device. This reset causes I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. It has weak pull-up to V_{DDBAT} or internal NFC voltage (whichever is highest).

7.1.3 NHS3100W8 gold bump version

Figure 4 shows the bump layout of the NHS3100W8.

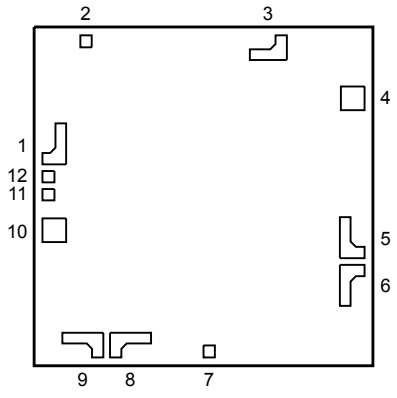

Figure 4. Bump configuration Bump die: Top view, bumps up

Table 7. Bump allocation table of the NHS3100W8 package

Bump	Symbol	Bump	Symbol
1	PIO0_0/WAKEUP	7	TP1
2	TP0	8	VSS
3	LA	9	VDDBAT
4	LB	10	PIO0_6
5	PIO0_11/CT32B_M1/SWDIO	11	TP2
6	PIO0_10/CT32B_M0/SWCLK	12	TP3

Table 8. Bump description of the NHS3100W8 package

Bump	Symbol	Type	Description
Supply			
9	VDDBAT	supply	positive supply voltage
8	VSS	supply	ground
GPIO[1]			
1	PIO0_0	I/O	GPIO
	WAKEUP	I	Deep power-down mode wake-up pin[2]
10	PIO0_6	I/O	GPIO
6	PIO0_10	I/O	GPIO
	CT32B_M0	O	32-bit timer match output 0
	SWCLK	I	ARM SWD clock
5	PIO0_11	I/O	GPIO
	CT32B_M1	O	32-bit timer match output 1
	SWDIO	I/O	ARM SWD I/O
Radio			
3	LA	A	NFC antenna/coil terminal A
4	LB	A	NFC antenna/coil terminal B
Test pins			
2	TP0	-	test pin - do not connect
7	TP1	-	test pin - do not connect, or connect to ground
11	TP2	-	test pin - do not connect
12	TP3	-	test pin - do not connect

[1] The GPIO port is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 balls depends on the function selected through the IOCONFIG register block.

[2] If external wake-up is enabled on this ball, it must be pulled HIGH before entering Deep power-down mode and pulled LOW for a minimum of 100 µs to exit Deep power-down mode.

8 Functional description

8.1 ARM Cortex-M0+ core

Refer to the *Cortex-M0+ Devices Technical Reference Manual* (Ref. 1) for a detailed description of the ARM Cortex-M0+ processor.

The NHS3100 ARM Cortex-M0+ core has the following configuration:

- System options
  - Nested Vectored Interrupt Controller (NVIC)
  - Fast (single-cycle) multiplier
  - System tick timer
  - Support for wake-up interrupt controller
  - Vector table remapping register
  - Reset of all registers
- Debug options
  - Serial Wire Debug (SWD) with two watchpoint comparators and four breakpoint comparators
  - Halting debug is supported

8.2 Memory map

Figure 5 shows the memory and peripheral address space of the NHS3100.

The only AHB peripheral device on the NHS3100 is the GPIO module. The APB peripheral area is 512 kB in size. Each peripheral is allocated 16 kB of space.

All peripheral register addresses are 32-bit word aligned. Byte and halfword addressing is not possible. All reading and writing are done per full word.

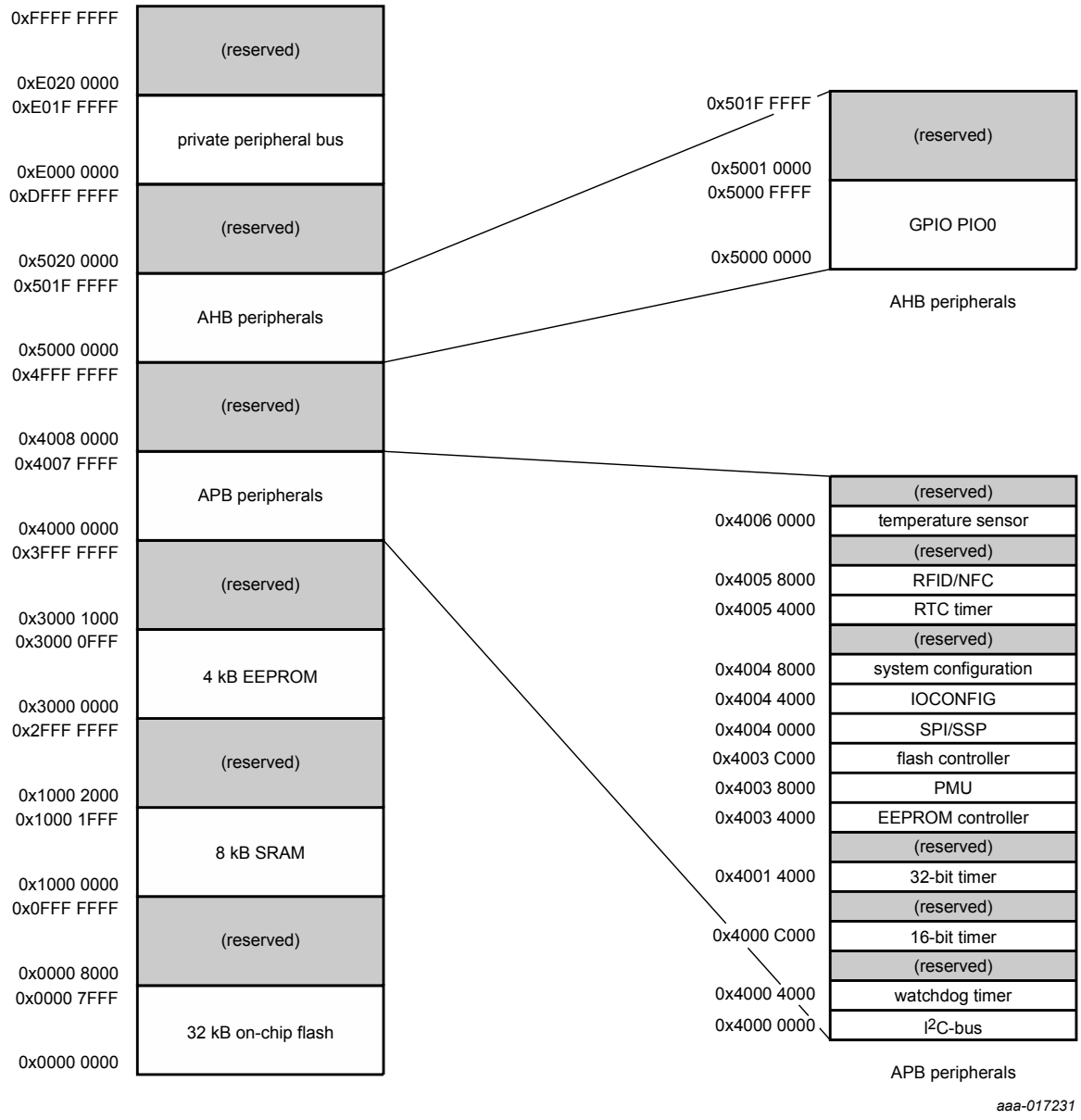

Figure 5. NHS3100 memory map

8.3 System configuration

The system configuration APB block controls oscillators, start logic, and clock generation of the NHS3100. Also included in this block is a register for remapping the interrupt vector table.

8.3.1 Clock generation

The NHS3100 Clock Generator Unit (CGU) includes two independent RC oscillators. These oscillators are the System Free-Running Oscillator (SFRO) and the Timer Free-Running Oscillator (TFRO).

The SFRO runs at 8 MHz. The system clock is derived from it and can be set to 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz, or 62.5 kHz (Note: Some features are not available when using the lower clock speeds). The TFRO runs at 32.768 kHz and is the clock source for the timer unit. The TFRO cannot be disabled.

Following reset, the NHS3100 starts operating at the default 500 kHz system clock frequency to minimize dynamic current consumption during the boot cycle.

The SYSAHBCLKCTRL register gates the system clock to the various peripherals and memories. The temperature sensor receives a fixed clock frequency, irrespective of the system clock divider settings, while the digital part uses the system clock (AHB clock 0).

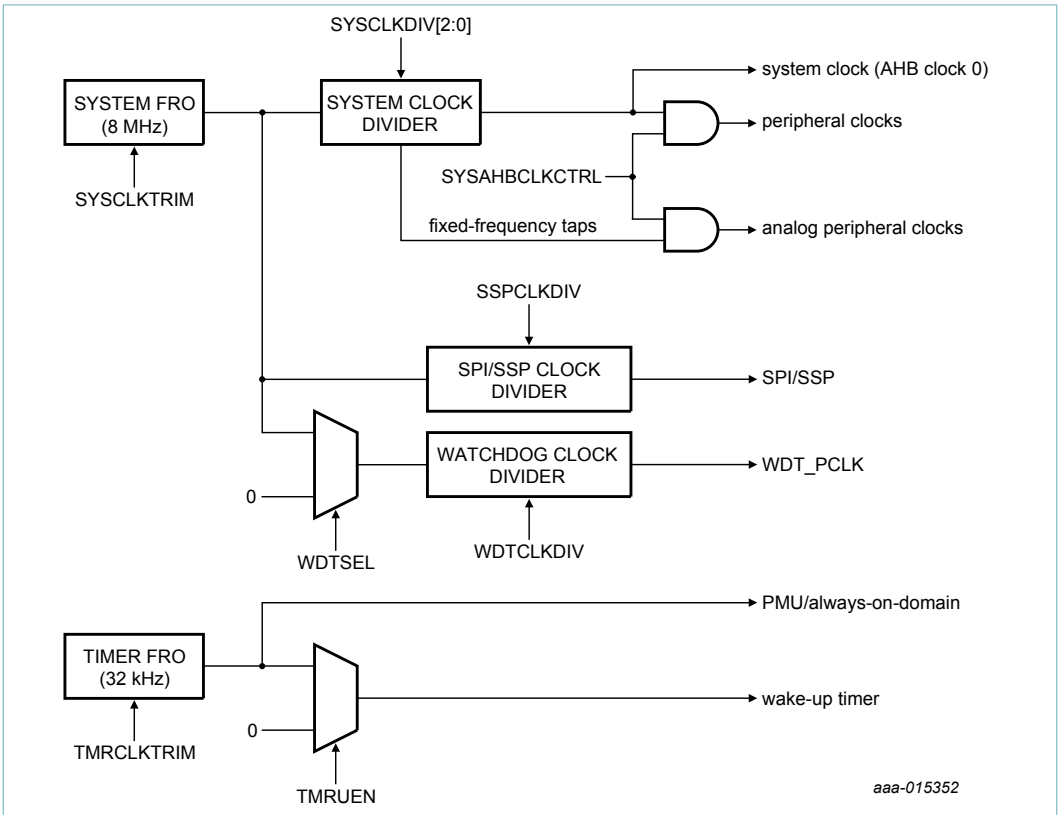

Figure 6. NHS3100 clock generator block diagram

8.3.2 Reset

Reset has three sources on the NHS3100:

- The RESETN pin
- Watchdog reset
- A software reset

8.4 Power management

The Power Management Unit (PMU) controls the switching between available power sources and the powering of the different voltage domains in the IC.

8.4.1 System power architecture

The NHS3100 accepts power from two different sources: from the external power supply pin VDDBAT, or from the built-in NFC/RFID rectifier.

The NHS3100 has a small automatic source selector that monitors the power inputs (VBAT and VNFC, see Figure 7) as well as pin RESETN. The PSWBAT switch is kept open until a trigger is given on pin RESETN or via the NFC field. If the trigger is given, the always-on domain, VDD_ALON, itself is powered via the PSWBAT or the PSWNFC switch: via VBAT, if VBAT > 1.72 V, or VNFC. Priority is given to VBAT when both VBAT and VNFC are present.

The automatic source selector unit in the PMU decides on the powering of the internal domains based on the power source.

- If a voltage > 1.72 V is detected on VBAT and not VNFC, VBAT powers the internal domains after a trigger on pin RESETN or via NFC.
- If a voltage ≤ 1.72 V is detected on VBAT, and a higher voltage is detected on VNFC, the internal domains are powered from VNFC.
- If a voltage > 1.72 V is detected at both VBAT and VNFC, the internal domains are powered from VBAT.
- Switchover between power sources is possible. If initially both VBAT and VNFC are available, the system is powered from VBAT. If VBAT then becomes unavailable (because it is switched off externally, or by a PSWBAT/PSWNFC power switch override), the internal domains are immediately powered from VNFC. Switchover is supported in both directions.
- The user can force the selection of the VBAT input by disabling the automatic power switch, which disables the automatic source selector voltage comparator.

When on NFC power only (passive operation), connecting one or more 100 nF external capacitors in parallel to a GPIO pad, and setting that pad as an output driven to logic 1, is advised. Preferably a high-drive pin should be chosen and several pins can be connected in parallel.

PSWNFC and PSWBAT are the power switches. PSWNFC connects power to the VDD_ALON power net when an RF field is present. PSWBAT connects power from the battery when a positive edge is detected on RESETN. If no RF power is available, the PMU can open this PSWBAT switch, effectively switching off the device. After connecting VDDBAT to a power source, the PSWBAT switch is open until a rising edge is detected on RESETN or RF power is applied.

Each component of the NHS3100 resides in one of several internal power domains, as indicated in Figure 7. The domains are VBAT, VNFC, VDD_ALON, VDD1V2 and VDD1V6. The domains VDD_ALON, VDD1V2 and VDD1V6 are either powered or not powered, depending on the mode of the NHS3100. There are 5 modes:

- Active
- Sleep
- Deep-sleep
- Deep power-down

- Battery-off

The VDD_ALON domain contains BrownOut Detection (BOD). When enabled, it raises a BOD interrupt if the VDD_ALON voltage drops below 1.8 V.

The PMU controls the Active, Sleep, Deep-sleep, and Deep power-down modes. In this way, the power flows to the different internal components.

The PMU has two LDOs powering the internal VDD1V2 and VDD1V6 voltage domains. LDO1V2 converts voltages in the range 1.72 V to 3.6 V to 1.22 V. LDO1V6 converts voltages in the range 1.72 V to 3.6 V to 1.6 V. Each LDO can be enabled separately. When powered via VNFC, a 1.2 nF buffer capacitor is included at the input of the LDOs.

The trigger detector (not shown in Figure 7) and the power gate have a leakage of less than 50 nA, allowing a long shelf life before activation.

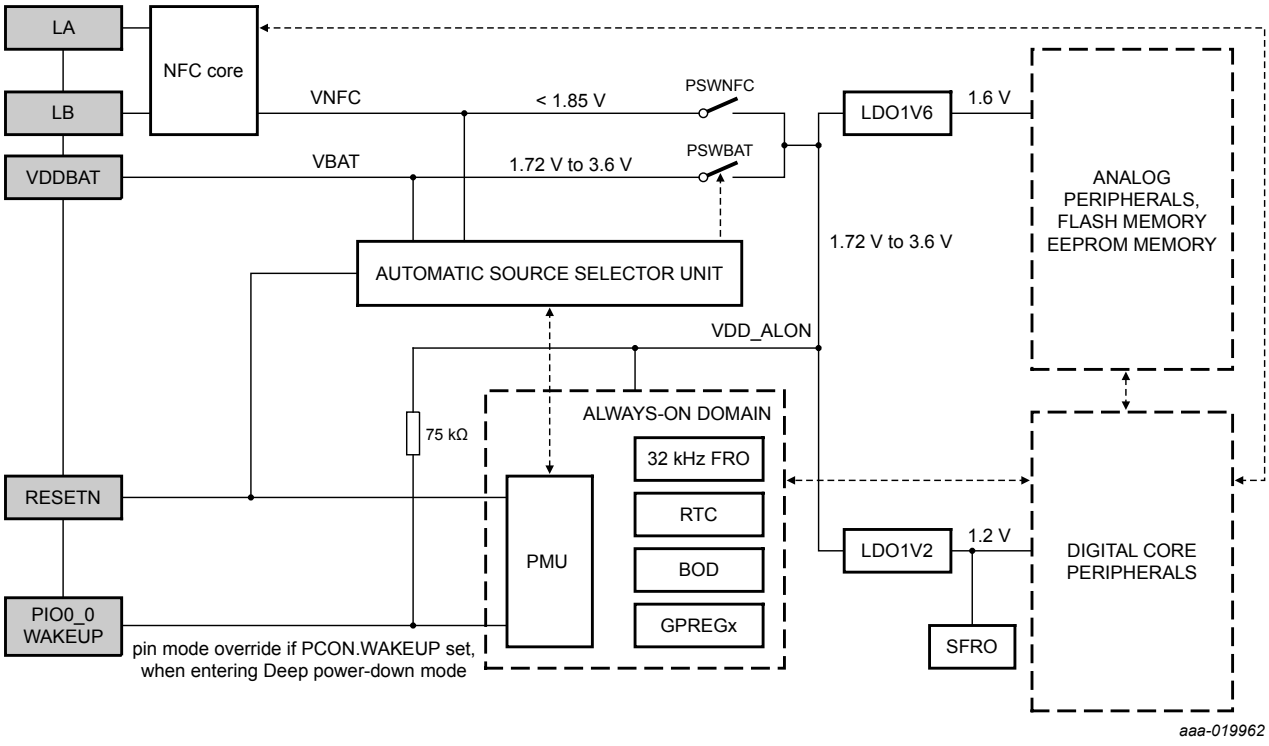

Figure 7. NHS3100 power architecture

Table 9 summarizes the PMU states and settings of the LDOs. Figure 8 shows the state transitions.

Table 10 and Table 11 summarize the events that can influence wake-up from Deep power-down or Deep-sleep modes (DEEPPDN or DEEPSLEEP to ACTIVE state transition).

Table 9. IC power states

State	VDD_ALON	DPDN[1]	Sleep or Deep-sleep	LDO1 (1.2 V)	LDO2 (1.6 V)
BATTERY-OFF (No power)	no	X[2]	X[2]	off	off
ACTIVE	yes	0	0	on	on
DEEPPDN	yes	1	0	off	off

State	VDD_ALON	DPDN[1]	Sleep or Deep-sleep	LDO1 (1.2 V)	LDO2 (1.6 V)
SLEEP/DEEPSLEEP	yes	0	1	on	on

[1] DPDN indicates whether the system is in Deep power-down mode.
[2] X = don't care.

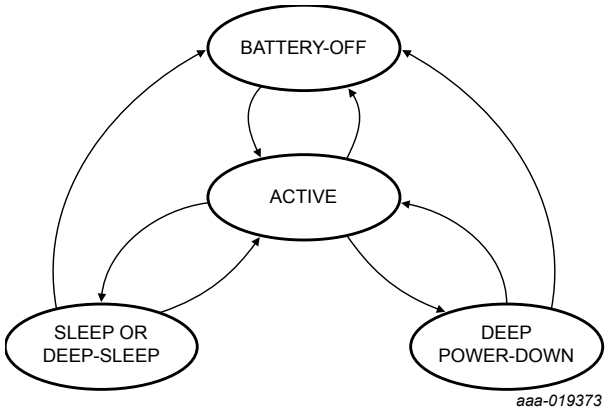

Figure 8. PMU state transition diagram

Figure 9 shows the power-up sequence. Applying battery power when the PSWBAT switch is closed, or NFC power becomes available, provides the always-on part with a Power-On Reset (POR) signal. The TFRO is initiated, which starts a state machine in the PMU. In the first state, the LDO1V2, powering the digital domain, is started. In the second state, the LDO1V6, powering the analog domain, is started which starts the flash memory. Enabling the LDO1V2, and the SFRO stabilizing, triggers the system_por. The system is now considered to be 'on'. The system can boot when the flash memory is fully operational.

The total start-up time from trigger to active mode/boot is about 2.5 ms.

If there is no battery power, but there is RF power, the same procedure is followed except that PSWNFC connects power to the LDOs.

The user cannot disable the TFRO as it is used by the PMU.

Table 10. State transition events for DEEPSLEEP to ACTIVE

Event	Description
RESETN	reset asserted
RTC event	if the timer reaches preset value
Watchdog	watchdog issues interrupt or reset
WAKEUP	signal on WAKEUP pin
RF field	RF field is detected, potential NFC command input (if set in PMU)
Start logic interrupt	one of the enabled start logic interrupts is asserted

Table 11. State transition events for DEEPPDN to ACTIVE

Event	Description
RESETN	reset asserted
RTC event	if the timer reaches preset value
WAKEUP	signal on WAKEUP pin (when enabled)
RF field	RF field is detected, potential NFC command input (if set in PMU)

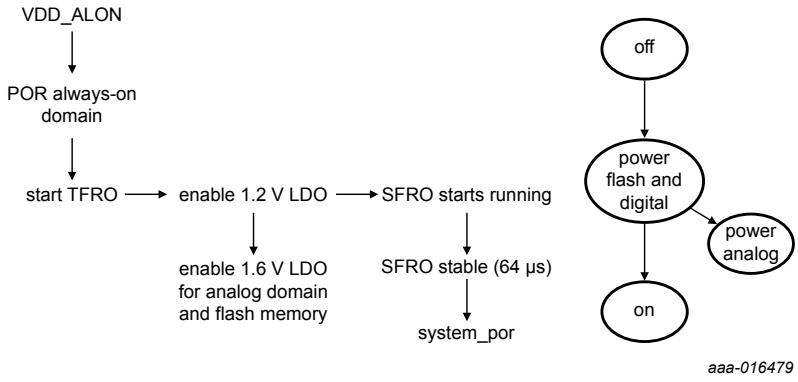

Figure 9. NHS3100 power-up sequence

8.4.2 Power Management Unit (PMU)

The Power Management Unit (PMU) partly resides in the digital power domain and partly in the always-on domain. The PMU controls the Sleep, Deep-sleep, and Deep power-down modes and the power flow to the different internal circuit blocks. Five general-purpose registers in the PMU can be used to retain data during Deep power-down mode. These registers are located in the always-on domain. When configured, the PMU also raises a BOD interrupt if VDD_ALON drops to below 1.8 V.

The power to the different APB analog slaves is controlled through a power-down configuration register.

The power control register selects whether an ARM Cortex-M0+ controlled Power-down mode (Sleep mode or Deep-sleep mode) or the Deep power-down mode is entered. It also provides the flags for Sleep or Deep-sleep modes and Deep power-down mode respectively. In addition, it contains the overrides for the power source selection.

8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is a part of the ARM Cortex-M0+. The tight integration of the processor core and NVIC enables fast processing of interrupts, dramatically reducing the interrupt latency.

8.5.1 Features

- NVIC that is a part of the ARM Cortex-M0+
- Tightly coupled interrupt controller provides low interrupt latency
- Controls system exceptions and peripheral interrupts

- Four programmable interrupt priority levels with hardware priority level masking
- Software interrupt generation

8.5.2 Interrupt sources

Table 12 lists the interrupt sources for each peripheral function. Each peripheral device may have one or more interrupt lines to the Nested Vectored Interrupt Controller. Each line may represent more than one interrupt source. There is no significance or priority about which line is connected where, except for certain standards from ARM.

Table 12. Connection of interrupt source to the Nested Vector Interrupt Controller

Exception number	Vector offset	Function	Flags
0 to 12	-	start logic wake-up interrupts	each interrupt connected to a PIO0 input pin serves as wake-up from Deep-sleep mode[1]
13	-	RFID/NFC	RFID/NFC access detected/command received/read acknowledge
14	-	RTC On/Off timer	RTC on/off timer event interrupt
15	-	I^2C	Slave Input (SI) (state change)
16	-	CT16B	16-bit timer
17	-	PMU	power from NFC field detected
18	-	CT32B	32-bit timer
19	-	BOD	brownout detection (power drop)
20	-	SPI/SSP	TX FIFO half empty/RX FIFO half full/RX time-out/RX overrun
21	-	TSENS	temperature sensor end of conversion/low threshold/ high threshold
22 to 25	-	-	(reserved)
26	-	WDT	watchdog interrupt (WDINT)
27	-	flash	flash memory
28	-	EEPROM	EEPROM memory
29 to 30	-	-	(reserved)
31	-	PIO0	GPIO interrupt status of port 0

[1] Interrupt 0 to 10 correspond to PIO0_0 to PIO0_10; interrupt 11 corresponds to RFID/NFC external access; interrupt 12 corresponds to the RTC On/Off timer.

8.6 I/O configuration

The I/O configuration registers control the electrical characteristics of the pads. The following features are programmable:

- Pin function
- Internal pull-up/pull-down resistor or bus keeper function
- Low-pass filter
- I^2C-bus mode for pads hosting the I^2C-bus function

The IOCON registers control the function (GPIO or peripheral function), the input mode, and the hysteresis of all PIO0_m pins. In addition, the I^2C-bus pins can be configured for different I^2C-bus modes.

The FUNC bits in the IOCON registers can be set to GPIO (FUNC = 000) or to a peripheral function. If the pins are GPIO pins, the GPIO0DIR registers determine whether the pin is configured as an input or output. For any peripheral function, the pin direction is controlled automatically depending on the functionality of the pin. The GPIO0DIR registers have no effect on peripheral functions.

8.6.1 PIO0 pin mode

The MODE bits in the IOCON register allow the selection of on-chip pull-up or pull-down resistors for each pin, or to select the repeater mode. The possible on-chip resistor configurations are pull-up enabled, pull-down enabled, or no pull-up/pull-down. The default value is no pull-up or pull-down enabled. The repeater mode enables the pull-up resistor when the pin is at logic 1, and enables the pull-down resistor when the pin is at logic 0. This mode causes the pin to retain its last known state if it is configured as an input and is not driven externally. The state retention is not applicable to the Deep power-down mode. Repeater mode is typically used to prevent a pin from floating when it is temporarily not driven. Allowing it to float could potentially use significant power.

8.6.2 PIO0 I²C-bus mode

If the FUNC bits of registers PIO0_4 and PIO0_5 select the I²C-bus function, the I²C-bus pins can be configured for different I²C-bus modes:

- Standard-mode/Fast-mode I²C-bus with input glitch filter (including an open-drain output according to the I²C-bus specification)
- Standard open-drain I/O functionality without input filter

8.6.3 PIO0 current source mode

PIO0_3, PIO0_7, PIO0_10 and PIO0_11 are high-source pads that can deliver up to 20 mA to the load. These PIO pins can be set to either digital mode or analog current sink mode. In digital mode, the output voltage of the pad switches between VSS and VDD. In analog current drive mode, the output current sink switches between the values set by the ILO and IHI bits. The maximum pad voltage is limited to 5 V.

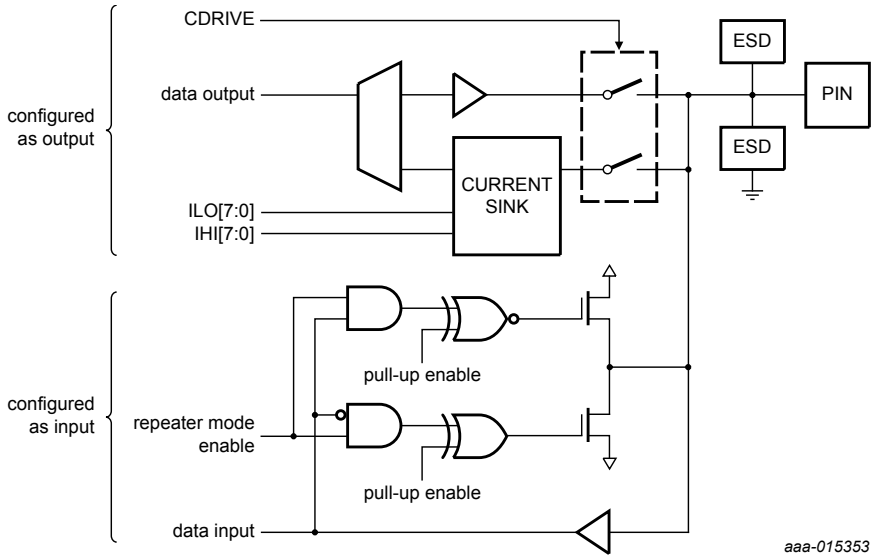

Figure 10. Pin configuration with current source mode

8.7 Fast general-purpose parallel I/O

The GPIO registers control device pins that are not connected to a specific peripheral function. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

The NHS3100 uses accelerated GPIO functions:

- GPIO registers are on the ARM Cortex-M0+ I/O bus for fastest possible single-cycle I/O timing
- An entire port value can be written in one instruction
- Mask, set, and clear operations are supported for the entire port

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin.

8.7.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation
- Direction control of individual bits
- After reset, all I/Os default to GPIO inputs without pull-up or pull-down resistors; The I^2C-bus true open-drain pins PIO0_4 and PIO0_5 and the SWD pins PIO0_10 and PIO0_11 are exceptions
- Pull-up/pull-down Configuration, Repeater, and Open-drain modes can be programmed through the IOCON block for each GPIO pin
- Direction (input/output) can be set and cleared individually per pin
- Pin direction bits can be toggled

8.8 I^2C-bus controller

8.8.1 Features

Standard I^2C-bus compliant interfaces may be configured as master, slave, or master/slave.

- Arbitration is handled between simultaneously transmitting masters without corruption of serial data on the bus
- Programmable clock allows adjustment of I^2C-bus transfer rates
- Data transfer is bidirectional between masters and slaves
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization is used as a handshake mechanism to suspend and resume serial transfer
- Supports Standard-mode (100 kbit/s) and Fast-mode (400 kbit/s)
- Optional recognition of up to four slave addresses
- Monitor mode allows observing all I^2C-bus traffic, regardless of slave address
- The I^2C-bus can be used for test and diagnostic purposes
- The I^2C-bus contains a standard I^2C-bus compliant interface with two pins
- Possibility to wake up NHS3100 on matching I^2C-bus slave address

8.8.2 General description

Two types of data transfers are possible on the I^{2}C-bus, depending on the state of the direction bit (R/W):

- Data transfer from a master transmitter to a slave receiver
  The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
- Data transfer from a slave transmitter to a master receiver
  The master transmits the first byte (the slave address). The slave then returns an acknowledge bit. The slave then transmits the data bytes to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. As a repeated START condition is also the beginning of the next serial transfer, the I^{2}C-bus is not released.

The I^{2}C-bus interface is byte oriented and has four operating modes: Master transmitter mode, Master receiver mode, Slave transmitter mode, and Slave receiver mode.

The I^{2}C-bus interface is completely I^{2}C-bus compliant, supporting the ability to power off the NHS3100 independent of other devices on the same I^{2}C-bus.

The I^{2}C-bus interface requires a minimum 2 MHz system clock to operate in Normal mode, and 8 MHz for Fast-mode.

8.8.3 I^{2}C-bus pin description

Table 13. I^{2}C-bus pin description

Pin	Type	Description
SDA	I/O	I^{2}C-bus serial data
SCL	I/O	I^{2}C-bus serial clock

The I^{2}C-bus pins must be configured through the PIO0_4 and PIO0_5 registers for Standard-mode or Fast-mode. The I^{2}C-bus pins are open-drain outputs and fully compatible with the I^{2}C-bus specification.

8.9 SPI controller

8.9.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments Synchronous Serial Interface (SSI), and National Semiconductor Microwire buses
- Synchronous serial communication
- Supports master or slave operation
- Eight-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

8.9.2 General description

The SPI/SSP is a Synchronous Serial Port (SSP) controller capable of operation on an SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames from 4 bits to 16 bits of bidirectional data flowing between master and slave. In practice, often only one of these two data flows carries meaningful data.

8.9.3 Pin description

Table 14. SPI pin description

Pin name	Type	Interface pin SPI	SSI	Microwire	Description
SCLK	I/O	SCLK	CLK	SK	serial clock
SSEL	I/O	SSEL	FS	CS	frame sync/slave select
MISO	I/O	MISO	DR (M) DX (S)	SI (M) SO (S)	master input slave output
MOSI	I/O	MOSI	DX (M) DR (S)	SO (M) SI (S)	master output slave input

8.9.3.1 Pin detailed description

Serial clock

SCK/CLK/SK is a clock signal used to synchronize the transfer of data. The master drives the clock signal and the slave receives it. When SPI/SSP interface is used, the clock is programmable to be active HIGH or active LOW, otherwise it is always active HIGH. SCK only switches during a data transfer. At any other time, the SPI/SSP interface either stays in its inactive state or is not driven (remains in high-impedance state).

Frame sync/slave select

When the SPI/SSP interface is a bus master, it drives this signal to an active state before the start of serial data. It then releases it to an inactive state after the data has been sent. The active state can be HIGH or LOW depending upon the selected bus and mode. When the SPI/SSP interface is a bus slave, this signal qualifies the presence of data from the master according to the protocol in use.

When there is only one master and slave, the master signals, frame sync, or slave select, can be connected directly to the corresponding slave input. When there are multiple slaves, further qualification of frame sync/slave select inputs is normally necessary to prevent more than one slave from responding to a transfer.

Master Input Slave Output (MISO)

The MISO signal transfers serial data from the slave to the master. When the SPI/SSP is a slave, it outputs serial data on this signal. When the SPI/SSP is a master, it clocks in serial data from this signal. It does not drive this signal and leaves it in a high-impedance state when the SPI/SSP is a slave and not selected by FS/SSEL.

Master Output Slave Input (MOSI)

The MOSI signal transfers serial data from the master to the slave. When the SPI/SSP is a master, it outputs serial data on this signal. When the SPI/SSP is a slave, it clocks in serial data from this signal.

8.10 RFID/NFC communication unit

8.10.1 Features

- ISO/IEC14443A part 1 to part 3 compatible
- MIFARE (Ultralight) EV1 compatible
- NFC Forum Type 2 compatible
- Easy interfacing with standard user memory space READ/WRITE commands
- Passive operation possible

8.10.2 General description

The RFID/NFC interface allows communication using 13.56 MHz proximity signaling.

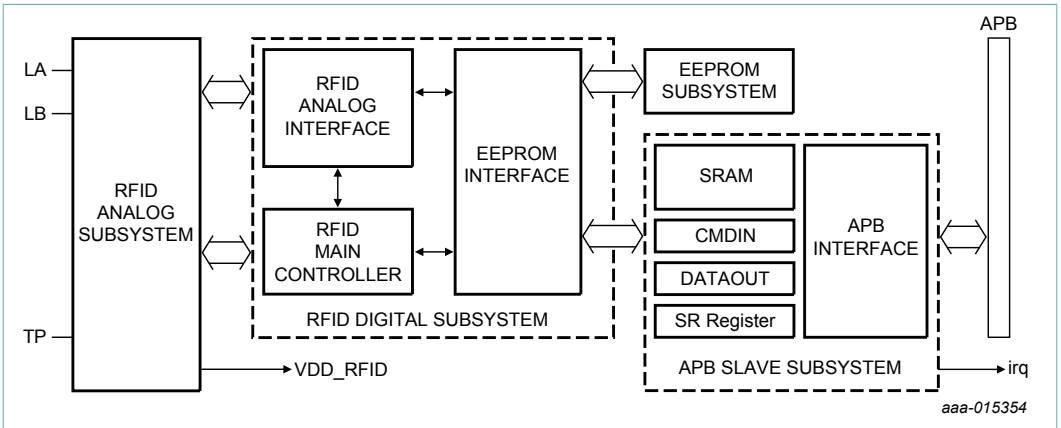

Figure 11. Block diagram of the RFID/NFC interface

The CMDIN, DATAOUT, Status Register (SR), and SRAM are mapped in the user memory space of the RFID core. The RFID READ and WRITE commands allow wireless communication to this shared memory.

Messages can be in Raw mode (user proprietary protocol) or formatted according to NFC Forum Type 2 NDEF messaging and ISO/IEC 11073.

8.11 16-bit timer

8.11.1 Features

One 16-bit timer with a programmable 16-bit prescaler.

- Timer operation
- Four 16-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
- Up to two CT16B external outputs corresponding to the match registers with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match
- Up to two match registers can be configured as Pulse Width Modulation (PWM) allowing the use of up to two match outputs as single edge controlled PWM outputs

8.11.2 General description

The peripheral clock (PCLK), which is derived from the system clock, clocks the timer. The timer can optionally generate interrupts or perform other actions at specified timer values based on four match registers. The peripheral clock is provided by the system clock.

Each timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, four match registers can be used to provide a single-edge controlled PWM output on the match output pins. The use of the match registers that are not pinned out to control the PWM cycle length is recommended.