



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## 16-BIT SERIAL TO PARALLEL CONVERTER

### ■ GENERAL DESCRIPTION

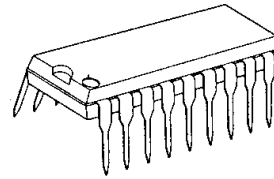
The **NJU3715** is a 16-bit serial to parallel converter especially applying to MPU output expander.

The effective output assignment of MPU is available as the connection between **NJU3715** and MPU using only 4 lines.

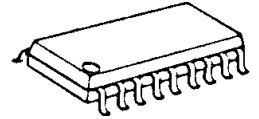
The serial data synchronizing with 5MHz or more clock can be input to the serial data input terminal and the data are output from parallel output buffer through serial in parallel out shift register and parallel data latches.

The hysteresis input circuit realizes wide noise margin and the high drive-ability output buffer (25mA) can drive LED directly.

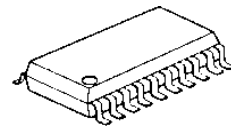
### ■ PACKAGE OUTLINE



**NJU3715L**



**NJU3715G**

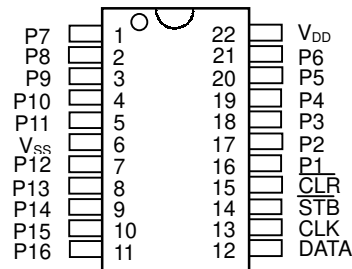


**NJU3715M**

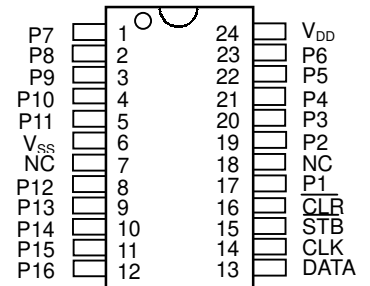
### ■ FEATURES

- 16-Bit Serial In Parallel Out
- Hysteresis Input                    0.5V typ
- Operating Voltage                5V±10%
- Maximum Operating Frequency 5MHz and more
- Output Current                    25mA
- C-MOS Technology
- Package Outline                    SDIP22/SOP22/DMP24

### ■ PIN CONFIGURATION

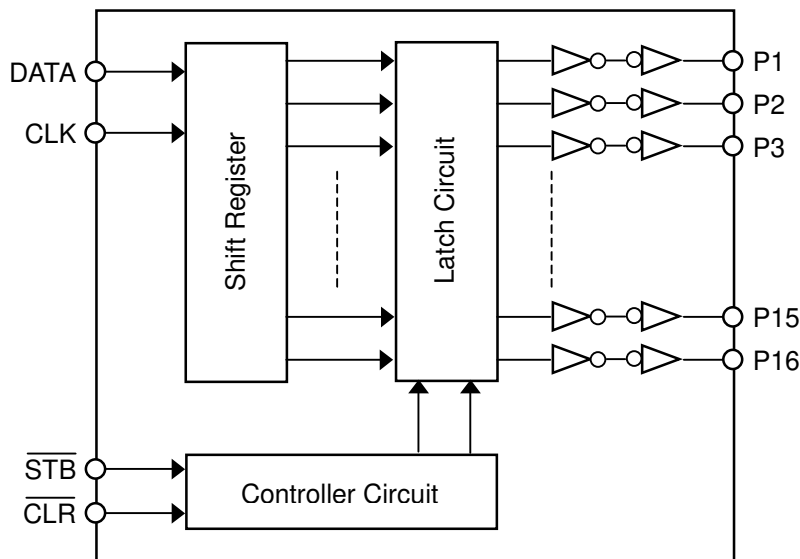


**NJU3715L/G**



**NJU3715M**

### ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION

| No.<br>SDIP22/SOP22 | No.<br>DMP24 | SYMBOL          | I/O | FUNCTION                                  |
|---------------------|--------------|-----------------|-----|---|
| 1                   | 1            | P7              | O   | Parallel Conversion Data Output Terminals |
| 2                   | 2            | P8              | O   |   |
| 3                   | 3            | P9              | O   |   |
| 4                   | 4            | P10             | O   |   |
| 5                   | 5            | P11             | O   |   |
| 6                   | 6            | V <sub>SS</sub> | -   | GND                                       |
| -                   | 7            | NC              | -   | Non Connection                            |
| 7                   | 8            | P12             | O   | Parallel Conversion Data Output Terminals |
| 8                   | 9            | P13             | O   |   |
| 9                   | 10           | P14             | O   |   |
| 10                  | 11           | P15             | O   |   |
| 11                  | 12           | P16             | O   |   |
| 12                  | 13           | DATA            | I   | Serial Data Input Terminal                |
| 13                  | 14           | CLK             | I   | Clock Signal Input Terminal               |
| 14                  | 15           | STB             | I   | Strobe Signal Input Terminal              |
| 15                  | 16           | CLR             | I   | Clear Signal Input Terminal               |
| 16                  | 17           | P1              | O   | Parallel Converts Data Output Terminal    |
| -                   | 18           | NC              | -   | Non Connection                            |
| 17                  | 19           | P2              | O   | Parallel Conversion Data Output Terminals |
| 18                  | 20           | P3              | O   |   |
| 19                  | 21           | P4              | O   |   |
| 20                  | 22           | P5              | O   |   |
| 21                  | 23           | P6              | O   |   |
| 22                  | 24           | V <sub>DD</sub> | -   | Power Supply Terminal (4.5 to 5.5V)       |

## ■ FUNCTIONAL DESCRIPTION

### (1) Reset

When the "L" level is input to the  $\overline{\text{CLR}}$  terminal, all latches are reset and all of parallel conversion output are "L" level.

Normally, the  $\overline{\text{CLR}}$  terminal should be "H" level.



### (2) Data Transmission

In the  $\overline{\text{STB}}$  terminal is "H" level and the clock signals are inputted to the CLK terminal, the serial data into the DATA terminal are shifted in the shift register synchronizing at a rising edge of the clock signal.

When the  $\overline{\text{STB}}$  terminal is changed to "L" level, the data in the shift register are transferred to the latches.

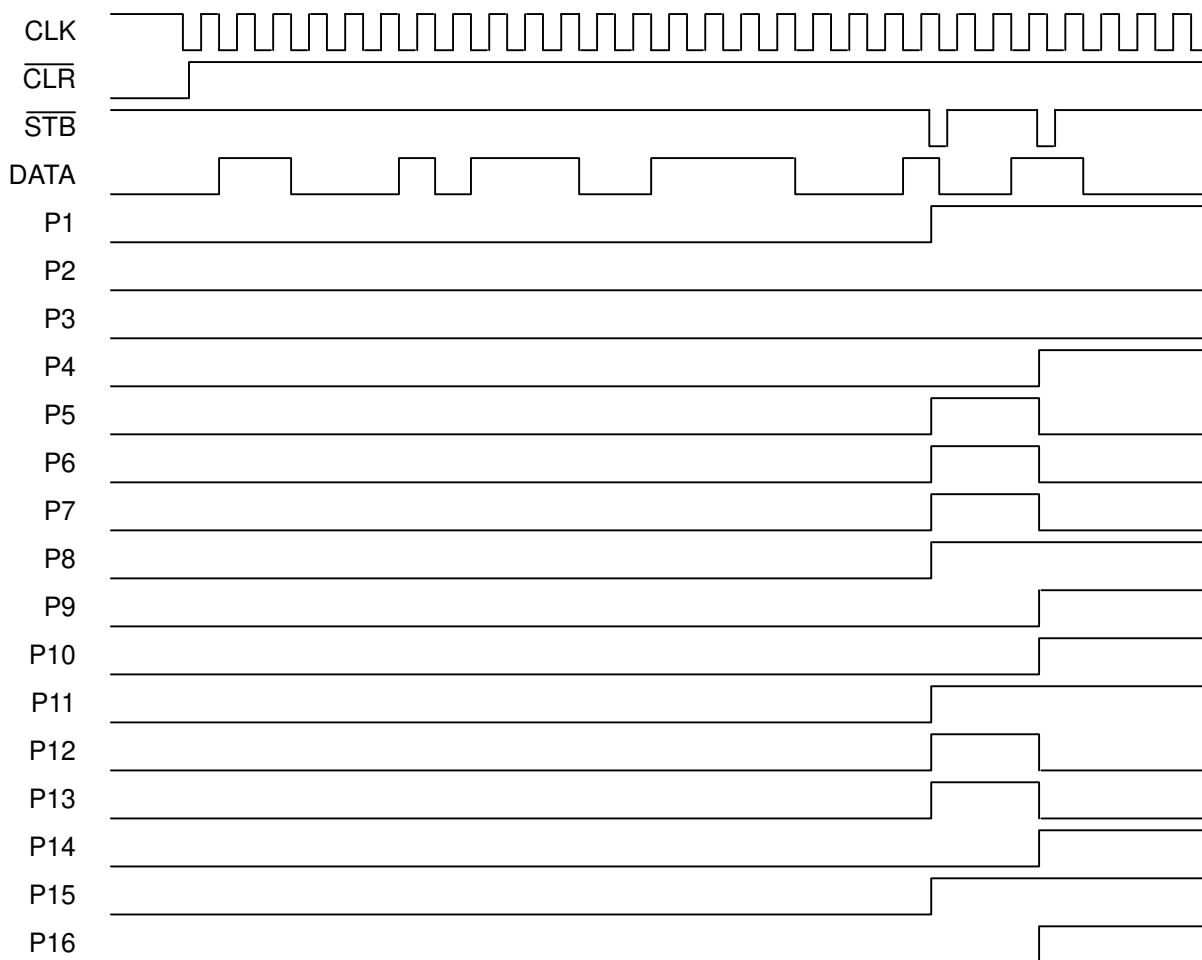
Even if the  $\overline{\text{STB}}$  terminal is "L" level, the input clock signal shifts the data in the shift register, therefore, the clock signal should be controlled for data order.

Furthermore, the 4 input circuits provide a hysteresis characteristics using the schmitt trigger structure to protect the noise.

| CLK   | $\overline{\text{STB}}$ | $\overline{\text{CLR}}$ | OPERATION   |
|---|-------------------------|-------------------------|---|
| X   | X                       | L                       | All of latches are reset (the data in the shift register is no change).<br>All of parallel conversion outputs are "L".  |
|    | H                       | H                       | The serial data into the DATA terminal are inputted to the shift register.<br>In this stage, the data in the latch is not changed.  |
| L   | L                       | H                       | The data in the shift register is transferred to the latch. And the data in the latch is output from the parallel conversion output terminals.  |
| H   |                         |                         |   |
|  |                         |                         |   |
|   |                         |                         | When the clock signal is inputted into the CLK terminal in state of the $\overline{\text{STB}}="L"$ and $\overline{\text{CLR}}="H"$ , the data is shifted in the shift register and latched data is also changed in accordance with the shift register. |

Note 1) X: Don't care

## ■ TIMING CHART



## ■ ABSOLUTE MAXIMUM RATINGS

| (Ta=25°C)  |           |                                      |           |    |
|--|-----------|--------------------------------------|-----------|----|
| PARAMETER  | SYMBOL    | RATINGS                              | UNIT      |    |
| Supply Voltage Range                                   | $V_{DD}$  | -0.5 ~ +7.0                          | V         |    |
| Input Voltage Range                                    | $V_I$     | $V_{SS}-0.5 \sim V_{DD}+0.5$         | V         |    |
| Output Voltage Range                                   | $V_O$     | $V_{SS}-0.5 \sim V_{DD}+0.5$         | V         |    |
| Output Current   | $I_O$     | ±25                                  | mA        |    |
| Output Short Current<br>(P1~P16 Terminals)<br>(Note 5) | $I_{OSD}$ | $V_O=7V, V_I=0V$                     | 20 (max)  | mA |
|  |           | $V_O=0V, V_I=7V$                     | -20 (max) |    |
| Power Dissipation                                      | $P_D$     | 700 (SDIP)<br>400 (SOP)<br>500 (DMP) | mW        |    |
| Operating Temperature Range                            | Topr      | -25 ~ +85                            | °C        |    |
| Storage Temperature Range                              | Tstg      | -65 ~ +150                           | °C        |    |

Note 2) All voltage are relative to  $V_{SS}=0V$  reference.

Note 3) Do not exceed the absolute maximum ratings, otherwise the stress may cause a permanent damage to the IC. It is also recommended that the IC be used in the range specified in the DC electrical characteristics, or the electrical stress may cause malfunctions and impact on the reliability.

Note 4) To stabilize the IC operation, place decoupling capacitor between  $V_{DD}$  and  $V_{SS}$ .

Note 5)  $V_{DD}=7V, V_{SS}=0V$ , less than 1 second per pin.

## ■ DC ELECTRICAL CHARACTERISTICS

( $V_{DD}=4.5\sim 5.5V, V_{SS}=0V, Ta=25^\circ C$ , unless otherwise noted)

| PARAMETER                             | SYMBOL    | CONDITION                      | MIN                 | TYP          | MAX          | UNIT     |   |
|---------------------------------------|-----------|--------------------------------|---------------------|--------------|--------------|----------|---|
| Operating Voltage                     | $V_{DD}$  |                                | 4.5                 | -            | 5.5          | V        |   |
| Operating Current                     | $I_{DDs}$ | $V_{IH}=V_{DD}, V_{IL}=V_{SS}$ | -                   | -            | 0.1          | mA       |   |
| High-level Input Voltage              | $V_{IH}$  |                                | 0.7 $V_{DD}$        | -            | $V_{DD}$     | V        |   |
| Low-level Input Voltage               | $V_{IL}$  |                                | $V_{SS}$            | -            | 0.3 $V_{DD}$ | V        |   |
| Input Leakage Current                 | $I_{LI}$  | $V_I=0\sim V_{DD}$             | -10                 | -            | 10           | μA       |   |
| High-level Output Voltage<br>(Note 6) | $V_{OHD}$ | $I_{OH}=-25mA$                 | P1~P16<br>Terminals | $V_{DD}-1.5$ | -            | $V_{DD}$ | V |
|                                       |           | $I_{OH}=-15mA$                 |                     | $V_{DD}-1.0$ | -            | $V_{DD}$ |   |
|                                       |           | $I_{OH}=-10mA$                 |                     | $V_{DD}-0.5$ | -            | $V_{DD}$ |   |
| Low-level Output Voltage<br>(Note 6)  | $V_{OLD}$ | $I_{OL}=+25mA$                 | P1~P16<br>Terminals | $V_{SS}$     | -            | 1.5      | V |
|                                       |           | $I_{OL}=+15mA$                 |                     | $V_{SS}$     | -            | 0.8      |   |
|                                       |           | $I_{OL}=+10mA$                 |                     | $V_{SS}$     | -            | 0.4      |   |

Note 6) Specified value represent output current per pin. When use, total current consideration and less than power dissipation in rating operation should be required.

# NJU3715

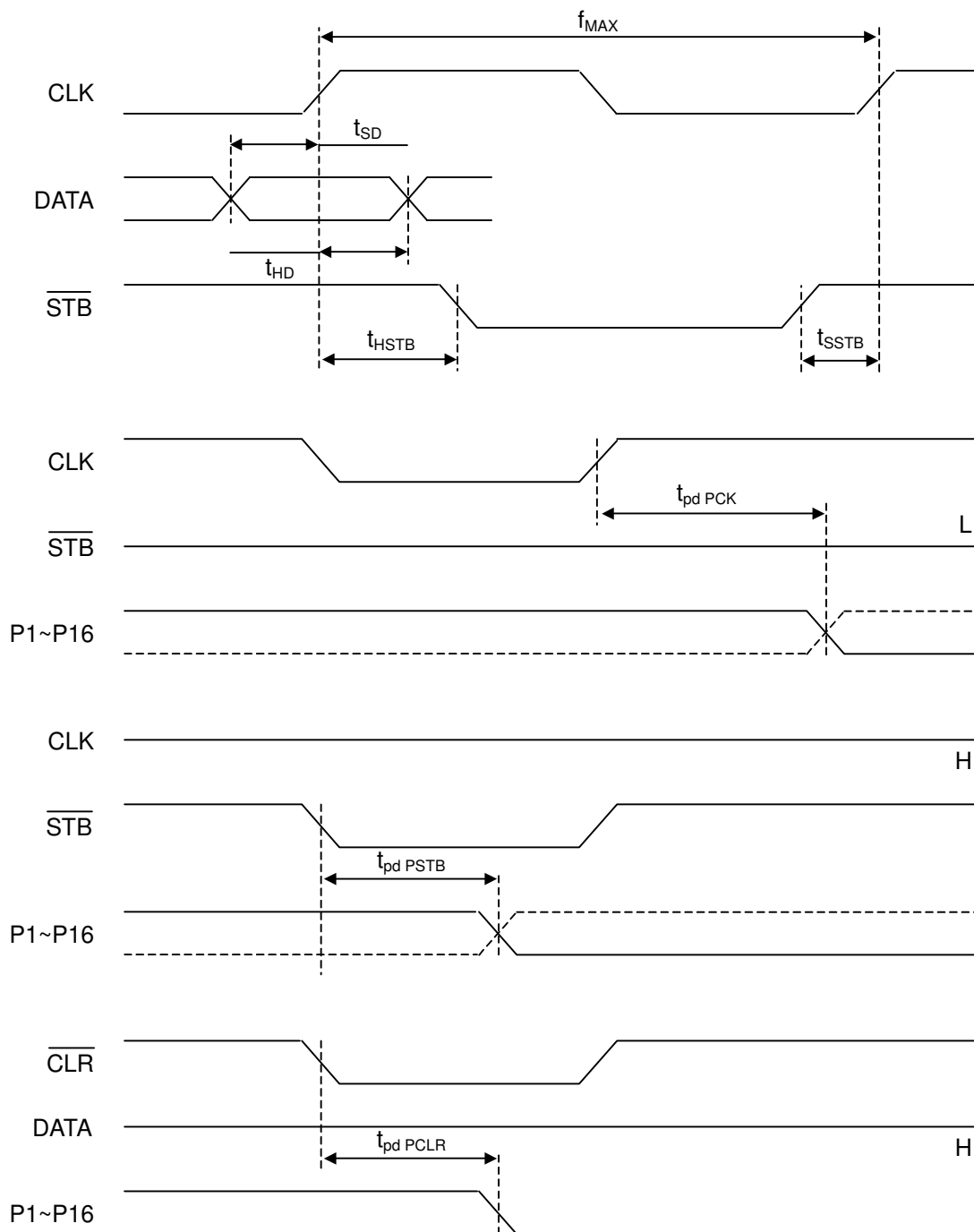
## ■ SWITCHING CHARACTERISTICS

( $V_{DD}=4.5\sim 5.5V$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ , unless otherwise noted)

| PARAMETER                   | SYMBOL         | CONDITION                | MIN | TYP | MAX | UNIT |
|-----------------------------|----------------|--------------------------|-----|-----|-----|------|
| Set-Up Time                 | $t_{SD}$       | DATA-CLK                 | 20  | -   | -   | ns   |
| Hold Time                   | $t_{HD}$       | CLK-DATA                 | 20  | -   | -   | ns   |
| Set-Up Time                 | $t_{SSTB}$     | $\overline{STB}$ -CLK    | 30  | -   | -   | ns   |
| Hold Time                   | $t_{HSTB}$     | CLK- $\overline{STB}$    | 30  | -   | -   | ns   |
| Output Delay Time           | $t_{pd\ PCK}$  | CLK-P1~P16               | -   | -   | 100 | ns   |
|                             | $t_{pd\ PSTB}$ | $\overline{STB}$ -P1~P16 | -   | -   | 80  | ns   |
|                             | $t_{pd\ PCLR}$ | $\overline{CLR}$ -P1~P16 | -   | -   | 80  | ns   |
| Maximum Operating Frequency | $f_{MAX}$      |                          | 5   | -   | -   | MHz  |

Note 7)  $C_{OUT}=50pF$

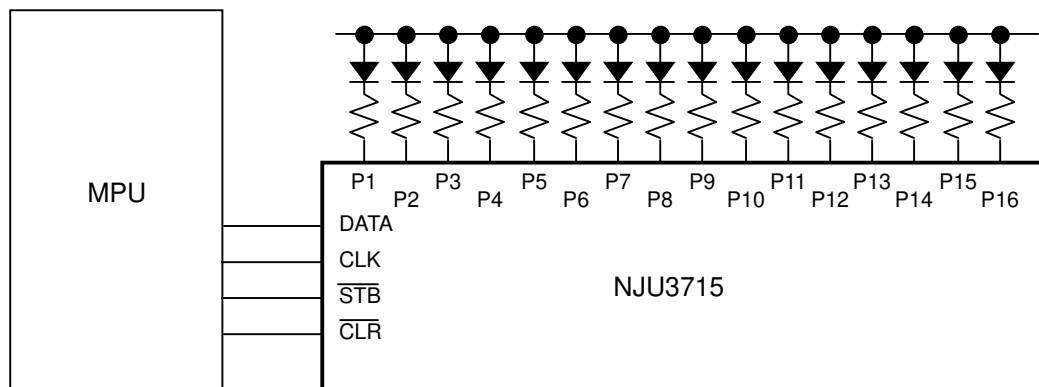
## SWITCHING CHARACTERISTICS TEST WAVEFORM





# NJU3715

## ■ APPLICATION CIRCUIT



**[CAUTION]**

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.