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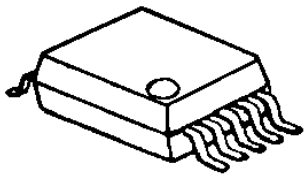
3V Operation Switching Driver for Class D Amplifier

■ GENERAL DESCRIPTION

The **NJU8711** is a Switching Driver for class D Amplifier including BEEP and BPZ (Bipolar Zero) output circuits. It converts 1bit digital signal input, such as PWM or PDM signal, to analog signal output with simple external LC low-pass filter.

The **NJU8711** realizes very high power-efficiency by class D operation. Therefore, It is suitable for portable audio set and others.

■ PACKAGE OUTLINE

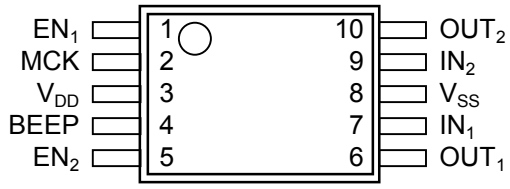


NJU8711V

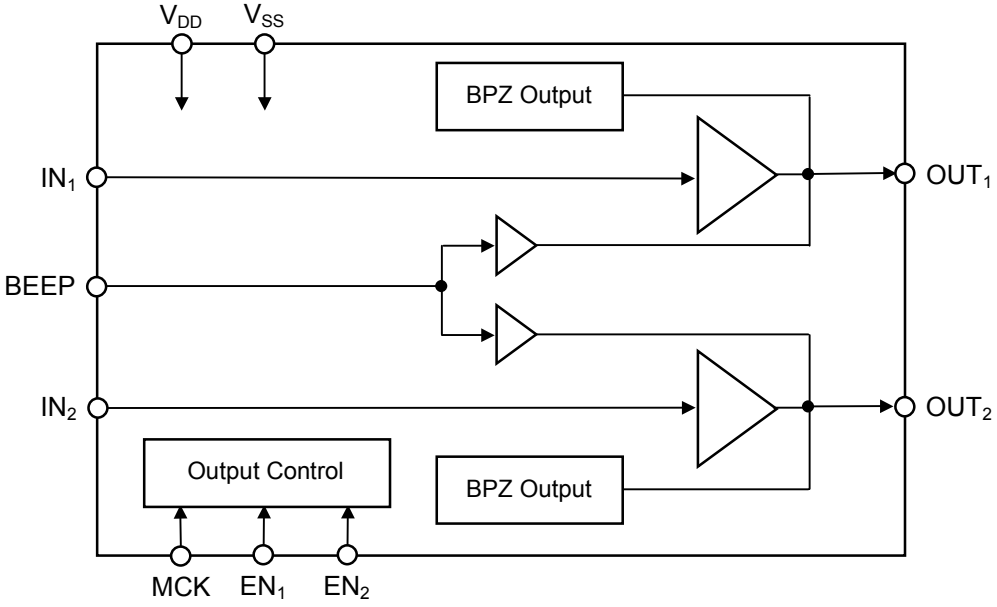
■ FEATURES

- 2-channel 1bit Audio Signal Input
- Standby(Hi-Z), BPZ Control
- Internal BPZ Charger
- Beep Function
- Operating Voltage : 2.0V to 3.6V
- CMOS Technology
- Package Outline : SSOP10

■ PIN CONFIGURATION



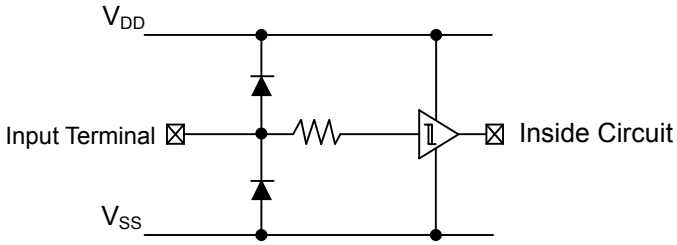
■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	Function
3	V_{DD}	-	Power Supply, V_{DD}=3V
8	V_{SS}	-	Power GND, V_{SS}=0V
2	MCK	I	Master Clock Input Terminal The condition of the data input terminal is fetched with the rising edge of this signal.
1 5	EN_1 EN_2	I	Output Control Terminal Output circuit is selected by the condition of this terminal.
7 9	IN_1 IN_2	I	Audio Signal Input Terminal 1-bit Audio Signal inputs into this terminal.
4	BEEP	I	Beep Signal Input Terminal Beep signal inputs into this terminal.
6 10	OUT_1 OUT_2	O	Output Terminal • When Output Terminal selects Audio Signal, IN_1 terminal input data outputs from OUT_1 terminal and IN_2 terminal input data outputs from OUT_2 terminal. • When Output Terminal selects Beep Signal, BEEP terminal input data outputs from OUT_1 and OUT_2 terminals.

■ INPUT TERMINAL STRUCTURE



■ FUNCTIONAL DESCRIPTION

(1) Signal Output

PWM signals of L channel and R output from OUT_1 and OUT_2 terminals respectively. These signals are converted to analog signal by external 2nd-order or over LC filter. The output driver power supplied from V_{DD} and V_{SS} are required high response power supply against voltage fluctuation like as switching regulator because Output T.H.D is effected by power supply stability.

(2) Master Clock

Master clock (MCK) synchronizes the Audio signal inputs (IN_1 and IN_2). The setup time and the hold time should be kept in the AC characteristics because IN_1 and IN_2 are fetched with the rising edge of MCK. MCK requires jitter-free or jitter as small as possible because the jitter downs S/N ratio.

OUT_1 and OUT_2 occur the pop noise when MCK is stopped in operation without standby mode. Therefore, the standby mode should be set before MCK stop.

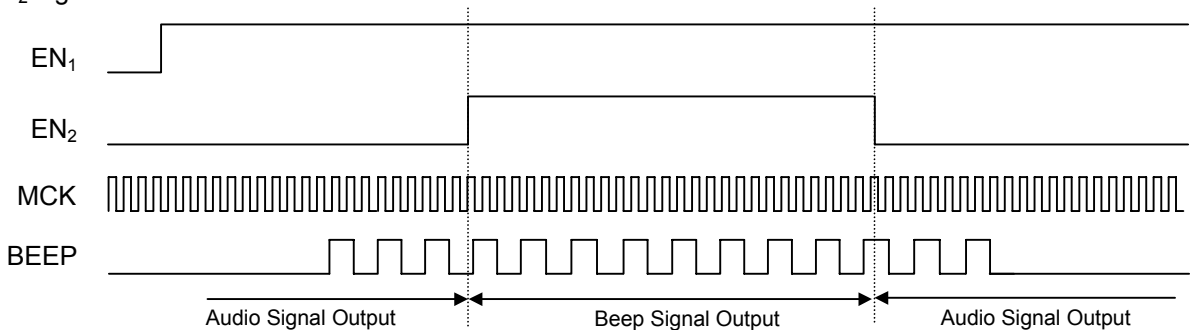
(3) Output Control

Output circuit is selected by the conditions of EN_1 and EN_2 terminals.

EN_2	EN_1	Output State of OUT_1 & OUT_2
0	0	Standby(High impedance)
0	1	Audio Signal Output
1	0	BPZ Output
1	1	Beep Signal Output

(4) Beep Function

The beep signal must be input before the rising edge of EN_2 signal and must be stopped after the falling edge of EN_2 signal.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	-0.3 to +4.0	V
Input Voltage		Vin	-0.3 to V_{DD}+0.3	V
Operating Temperature		Topr	-40 to +85	°C
Storage Temperature		Tstg	-40 to +125	°C
Power Dissipation	SSOP10	P_D	280	mW

Note 1) All voltage values are specified as V_{SS}=0V.
Note 2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.
Note 3) Decoupling capacitors should be connected between V_{DD}-V_{SS} due to the stabilized operation.

■ ELECTRICAL CHARACTERISTICS

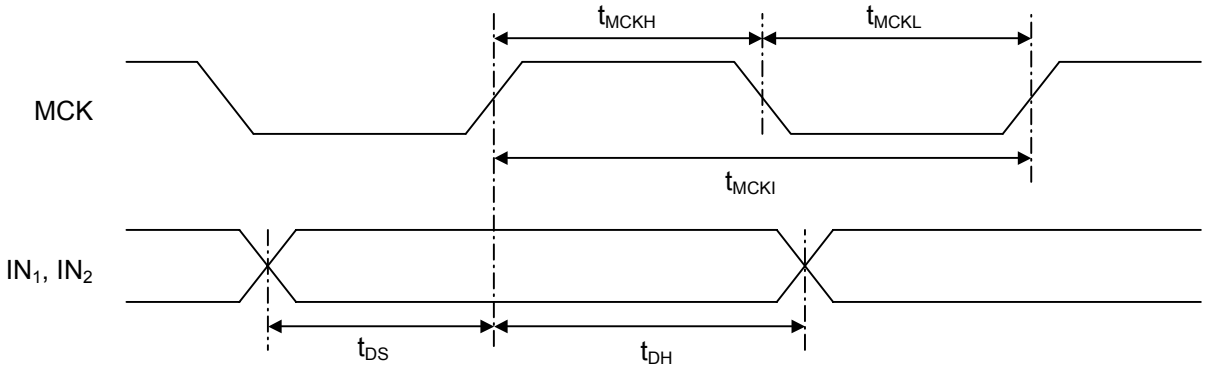
(Ta=25°C, V_{DD}=3.0V, V_{SS}=0.0V, Load Impedance=16Ω, f_S=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} Supply Voltage	V_{DD}		2.0	3.0	3.6	V
BPZ Driving Voltage	V_{BPZ}		V_{DD} /2-0.2	V_{DD} /2	V_{DD} /2+0.2	V
Output Driver High side Resistance	R_H	V_{OUT}=V_{DD}-0.1V	-	1.5	2	Ω
Output Driver Low side Resistance	R_L	V_{OUT}=0.1V	-	1.5	2	Ω
Beep High side Current	I_{BH}	V_{OUT}=V_{DD}-1V	100	250	600	uA
Beep Low side Current	I_{BL}	V_{OUT}=1V	100	250	600	uA
Operating Current At Standby	I_{ST}	Stopping MCK, IN_1, IN_2, BEEP	-	-	1	uA
Operating Current At no input signal	I_{DD}	No-load operating IN_1, IN_2=32f_S MCK=256f_S	-	1	2	mA
Input Voltage	V_{IH}		0.7V_{DD}	-	V_{DD}	V
	V_{IL}		0	-	0.3V_{DD}	V
Input Leakage Current	I_{LK}		-	-	±1	uA

Note 4) When V_{DD} Supply Voltage is lower than typical voltage, a pop noise may occur in output change between BPZ and Audio Signal. Therefore, please consider and check the circuit carefully against pop noise.

■ TIMING CHARACTERISTICS

- Audio Signal Input



(Ta=25°C, V_{DD}=3.0V, V_{SS}=0.0V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MCK Frequency	f_{MCKI}		8	-	25	MHz
MCK Pulse Width (H)	t_{MCKH}		12	-	-	ns
MCK Pulse Width (L)	t_{MCKL}		12	-	-	ns
IN_1,IN_2 Setup Time	t_{DS}		20	-	-	ns
IN_1,IN_2 Hold Time	t_{DH}		20	-	-	ns

Note 5) t_{MCKI} shows the cycle of the MCK signal.

- Output Control Signal Input

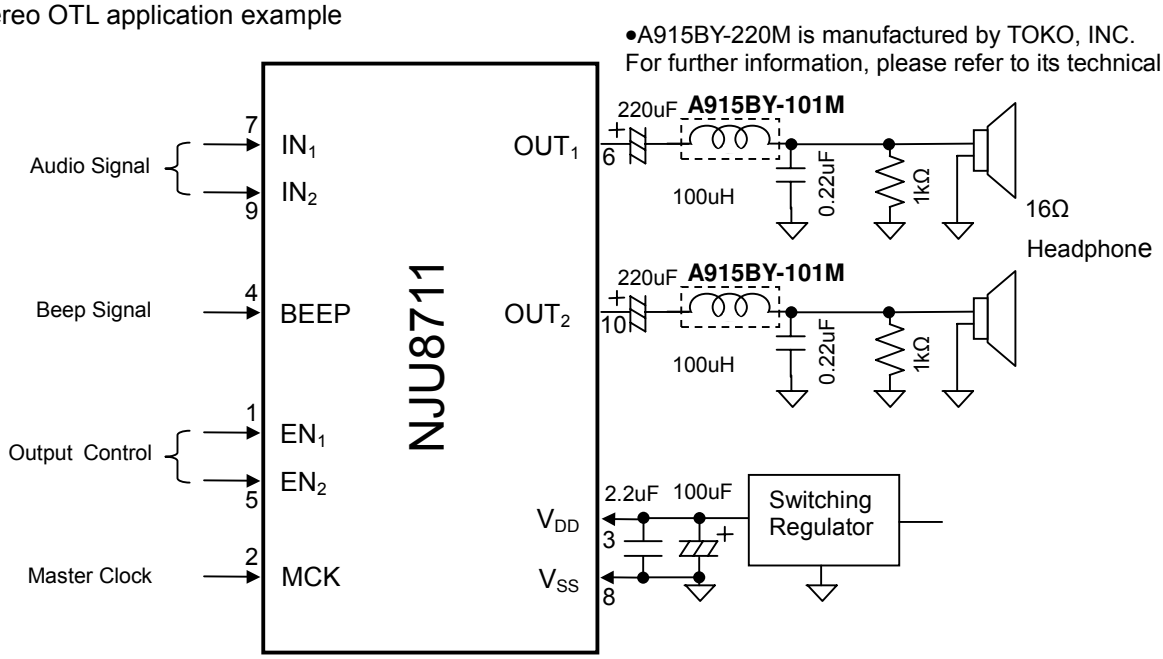
(Ta=25°C, V_{DD}=3.0V, V_{SS}=0.0V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise Time	t_{UP}		-	-	100	ns
Fall Time	t_{DN}		-	-	100	ns

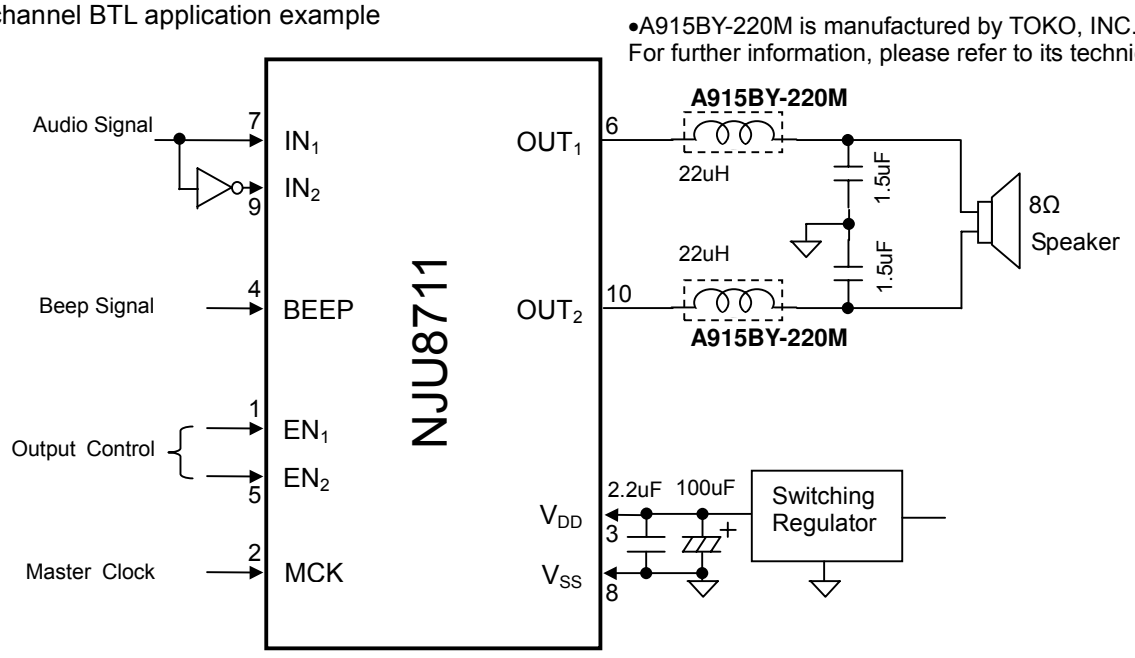
Note 6) All timings are based on 30% and 70% voltage level of V_{DD}.

■ APPLICATION CIRCUIT

- Stereo OTL application example



- 1 channel BTL application example



Note 7) De-coupling capacitors must be connected between each power supply pin and GND pin.
Note 8) The power supply for V_{DD} requires fast driving response performance such as a switching regulator for THD.
Note 9) The bigger capacitor value of external AC-coupling capacitors realize better low frequency response characteristics. In addition, ESR(Equivalent Series Resistance) should be low.
Note 10) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please consider and check the circuit carefully to fit your application.

[CAUTION]
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