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Low Power Analog Front End

■FEATURES

- ●Supply Voltage +2.4 to +3.6V
- ●Low Current Consumption 4µA (OPA,OPB), 150µA (ADC)
- ●Low Noise Amplifier 1.3µVpp typ. (0.1 to 10Hz)
- ●Low Offset Voltage Amplifier 300µV max.
- ●RF immunity Amplifier
- ●Programmable Cell Bias Voltage
  - OPA: 0.3V to 1.7V (7 steps)
  - OPB: 0.25V to 1.75V (50mV step)
- ●Programmable Gain Pre-Amplifier 1V/V to 8V/V
- ●High resolution Programmable Gain ADC
  - 1V/V to 8V/V, 16-Bit (NFB), 32sps to 2k sps
- ●System Calibration for offset & gain drift
- ●Control external EEPROM as a Master device
- ●Ambient Operating Temperature -40°C to +85°C
- ●Interface I^2C (3-Bit selectable slave address)
- ●Package EQFN-24-LE (4mm x 4mm)

■GENERAL DESCRIPTION

NJU9101 is a Low Power Analog Front End IC for use in micro-power sensing applications, especially electrochemical sensors. It provides a complete signal processing solution between sensor and micro-processor as smart-sensor module.

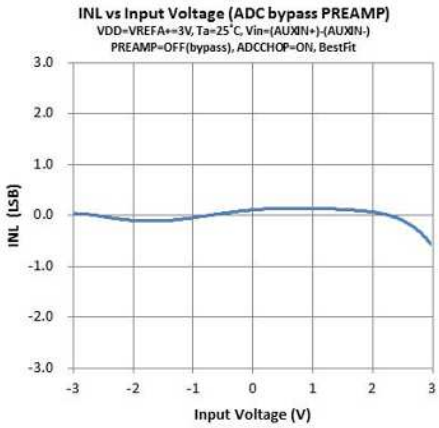
NJU9101 has 2 channel low power operational amplifiers. These amplifiers provide potentiostat and trans-impedance-amplifiers to constitute gas sensor systems. The NJU9101 has calibration circuit by using output data of built-in high precision ADC. It is suitable for temperature variation of sensor.

NJU9101 operates over voltage range of 2.4V to 3.6V. Total average current consumption can be less than 5µA.

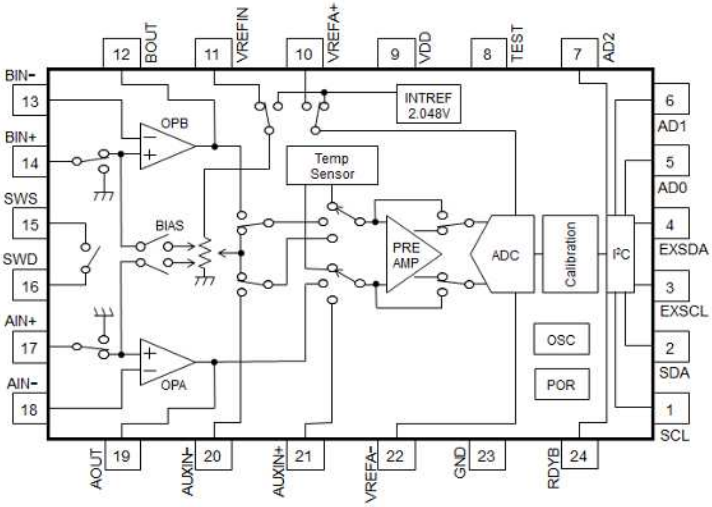
■APPLICATION

- ●Gas Monitor
- ●Blood Glucose Meter
- ●Current Sensing Systems
- ●Low Power Systems
- ●Photodiode Sensing Systems
- ●Portable equipment

■INL vs Input Voltage (ADC)

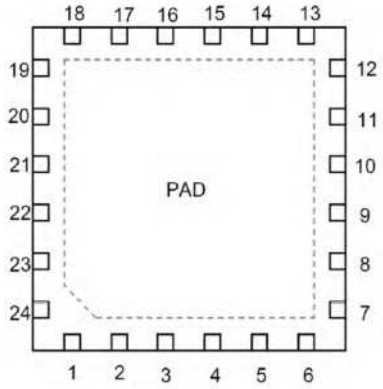


■EQUIVALENT CIRCUIT ・BLOCK DIAGRAM



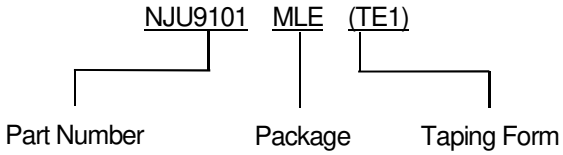
■PIN CONFIGURATION

EQFN-24-LE



PIN NO.	SYMBOL	DESCRIPTION		Pin Type
1	SCL	I^2C serial clock input		Digital Input
2	SDA	I^2C serial data input / output (which requires an pull-up resistor)		Digital Input / Output
3	EXSCL	I^2C serial clock output for external EEPROM (which requires an pull-up register)		Digital Output
4	EXSDA	I^2C serial data input / output for external EEPROM (which requires an pull-up resister)		Digital Input / Output
5	AD0	Chip address selection input 0	Select 7 chip address from “000” to “110”. Do not select address “111”, which address is for production test purpose	Digital Input
6	AD1	Chip address selection input 1		Digital Input
7	AD2	Chip address selection input 2		Digital Input
8	TEST	TEST terminal (This terminal is used for production test. Connect to VDD)		Analog Input
9	VDD	Voltage Supply		Power Supply
10	VREFA+	Positive voltage reference input for ADC		Analog Input
11	VREFIN	Voltage reference input for Bias Registor		Analog Input
12	BOUT	Voltage output for Bch. OpAmp		Analog Output
13	BIN-	Negative voltage input for Bch. OpAmp		Analog Input
14	BIN+	Positive voltage input for Bch. OpAmp		Analog Input
15	SWS	Switch Source Input 1		Swtich
16	SWD	Switch Drain Input 2		Swtich
17	AIN+	Positive voltage input for Ach. OpAmp		Analog Input
18	AIN-	Negative voltage input for Ach. OpAmp		Analog Input
19	AOUT	Voltage output for Ach. OpAmp		Analog Output
20	AUXIN-	Auxiliary positive input		Analog Input
21	AUXIN+	Auxiliary negative input		Analog Input
22	VREFA-	Negative voltage reference input for ADC (connect to GND, is recommended)		Analog Input
23	GND	GND		GND
24	RDYB	RDYB output / GPIO		Digital Input / Output
PAD	EXPPAD	Exposed PAD on backside (connect to GND)		GND

■MARK INFORMATION



■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJU9101MLE	EQFN-24-LE	O	O	Sn-2Bi	9101	31	1,000

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{DD}	5	V
Analog Input Voltage(1)	V_{IA}	-0.3 to V_{DD}+0.3 not exceeding 5	V
Digital Input Voltage	V_{ID}	-0.3 to 6	V
Switch Input Voltage(1)	V_{IS}	-0.3 to V_{DD}+0.3 not exceeding 5	V
On State Switch Current	I_{SO}	-40 to +40(3)	mA
Power Dissipation(T_a=25°C)(2)	P_D	830(4) / 2100(5) (2-layer / 4-layer)	mW
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(1): The input pins have clamp diodes to the power supply pins. Limit the input current to 10mA or less whenever input signals exceed the power supply rail by 0.3V.

(2): Power dissipation is the power that can be consumed by the IC at T_a=25°C, and is the typical measured value based on JEDEC condition. When using the IC over T_a=25°C subtract the value [mW/°C] = P_D / T_{st} max.- 25) per temperature.

(3): Mounted on glass epoxy board.
(101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(4): Mounted on glass epoxy board.
(101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{DD}	+2.4 to +3.6	V
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

■ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits ensured for T_a = 25°C, V_{DD} = V_{REFIN} = V_{REFA+} = 3V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
OPA, OPB						
Input Offset Voltage	V_{IO}	V_{ICM} = V_{DD}/2, R_s = 50Ω	-	-	±300	μV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$		-	±1	-	μV/°C
Input Bias Current	I_B		-	10	-	pA
Open Loop Gain	A_V		-	100	-	dB
Common Mode Rejection Ratio	CMR	V_{ICM} = GND to 2V	65	80	-	dB
Common Mode Input Voltage Range	V_{ICM}	CMR ≥ 65dB	GND	-	2	V
Maximum Output Voltage	V_{OH}	I_{SOUECE} = 1mA	2.8	2.85	-	V
	V_{OL}	I_{SINK} = 1mA	-	0.15	0.2	V
Gain Band Width	GBW		-	30	-	kHz
Slew Rate	SR		-	0.01	-	V/μs
Equivalent Input Noise Voltage	e_n	f = 100Hz, R_S = 50Ω	-	50	-	nV/√Hz
		f = 0.1Hz to 10Hz	-	1.3	-	μV_{pp}

Unless otherwise specified, all limits ensured for T_a = 25°C, V_{DD} = V_{REFIN} = V_{REFA+} = 3V, ADC reference Voltage = External

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
OPA, OPB with BIASRES (Potentiostat)						
OPA referred to OPB Input Offset Voltage 1	V_{IO1A-B}	OPA BIAS = 1V OPB BIAS = 1V	-	-	±0.6	mV
OPA referred to OPB Input Offset Drift 1	ΔV_{IO1A-B} / ΔT	OPA BIAS = 1V OPB BIAS = 1V	-	±2	-	μV/°C
OPA referred to OPB Input Offset Voltage 2	V_{IO2A-B}	OPA BIAS = 1V OPB BIAS = 0.7V	295	300	305	mV
OPA referred to OPB Input Offset Drift 2	ΔV_{IO2A-B} / ΔT	OPA BIAS = 1V OPB BIAS = 0.7V	-	±5	-	μV/°C
OPA referred to OPB Input Offset Voltage 3	V_{IO3A-B}	OPA BIAS = 1V OPB BIAS = 1.6V	-605	-600	-595	mV
OPA referred to OPB Input Offset Drift 3	ΔV_{IO3A-B} / ΔT	OPA BIAS = 1V OPB BIAS = 1.6V	-	±8	-	μV/°C

Unless otherwise specified, all limits ensured for T_a = 25°C, V_{DD} = V_{REFIN} = V_{REFA+} = 3V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Analog Switch (ANASW)						
On State Resistance	R_{ON}	Analog Switch = ON I_{DS} = -10mA		10	30	Ω
Off Leakage Current	I_{LOFFD}	Analog Switch = OFF V_{SWS}=2V/1V, V_{SWD}=1V/2V	-	±1	-	nA

Unless otherwise specified, all limits ensured for T_a = 25°C, V_{DD} = V_{REFIN} = V_{REFA+} = 3V, Temperature Input Mode

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature Sensor						
Temperature Accuracy (Error) 1	T_{ACC1}	T_a = 25°C	-	±1	±5	°C
Temperature Accuracy (Error) 2	T_{ACC2}	T_a = -40°C to +85°C	-	±3	-	°C
Temperature Resolution	T_{RES}		-	0.25	-	°C

Unless otherwise specified, all limits ensured for T_a = 25°C, V_{DD} = 3V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Internal Reference						
Internal Reference Voltage	V_{IREF}	±1%	2.028	2.048	2.068	V
Internal Reference Drift	ΔV_{IREF} / ΔT	T_a = -40°C to +85°C	-	30	-	ppm/°C

Unless otherwise specified, all limits ensured for T_a = 25°C, V_{DD} = V_{REFIN} = V_{REFA+} = 3V, Auxiliary Differential Input Mode

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PREAMP						
PREAMP Gain Error	G_{ACCP}	PREAMP Gain = 1V/1V to 8V/V	-	±0.1	-	%
PREAMP Common Mode Rejection	CMR_{PRE}	PREAMP Gain = 1V/V AUXIN+ = AUXIN- = GND+0.05 to V_{DD}-1	70	90	-	dB
PREAMP Common Mode Input Voltage	V_{ICMP}	PREAMP Gain = 1V/V CMR_{PRE} ≥ 70dB	GND +0.05	-	V_{CC}-1	V

Unless otherwise specified, all limits ensured for T_a = 25°C, V_{DD} = V_{REFIN} = V_{REFA+} = 3V, Auxiliary Input Mode
ADC Chopping = ON, ADC Reference Voltage = External, ADC Gain = 1V/V, ADC Decimation Ratio = "320"

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ADC						
Resolution	N	No missing code(6)	16	-	-	Bit
Noise Free Bit	NFB		-	16	-	Bit
Conversion Time	DR	See p.22 "ADC Conversion Time"	-	-	-	SPS
Output Noise	V_{nADC}	VREFA+ = 3V	-	13.9	-	µVrms
Integral Non Linearity	INL		-	±1	-	LSB
Gain Error		ADC Gain = 1V/1V to 8V/1V	-	±0.1	-	%
Offset Error		AUXIN+ = AUXIN- = V_{DD}/2	-	±1	-	LSB
Differential Input Voltage Range	V_{IDADC}	V_{REF} = |(VREFA+)-(VREFA-)|	-	±V_{REF}	-	V
ADC Common Mode Rejection	CMR_{ADC}	AUXIN+ = AUXIN- = GND to V_{DD}	80	90	-	dB
ADC Common Mode Input Voltage Range	V_{ICADC}	CMR_{ADC} ≥ 80dB	GND	-	V_{DD}	V

(6) This Parameter is not production tested, please refer Typical Characteristics.

Unless otherwise specified, all limits ensured for T_a = 25°C, V_{DD} = V_{REFIN} = V_{REFA+} = 3V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply / OSC						
Voltage Range	V_{DD}		2.4	-	3.6	V
Bias Resistance	R_{BIAS}		-	1.5	-	MΩ
Supply Current 1	I_{DD1}	All Circuit Block Off	-	0.5	1	μA
Supply Current 2	I_{DD2}	OPA、OPB	-	4	5.5	μA
Supply Current 3	I_{DD3}	Internal Reference Voltage (2.048V)	-	31	40	μA
Supply Current 4	I_{DD4}	PREAMP	-	55	75	μA
Supply Current 5	I_{DD5}	ADC	-	150	200	μA
OSC Frequency	f_{OSC}	±10%	276	307	338	kHz

■CHARACTERISTICS OF I/O STAGES FOR I²C-BUS Compatible (SDA, SCL)

I²C BUS Load Conditions

STANDARD MODE: Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 200pF (Connected to GND)

FASE MODE: Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard Mode			Fast Mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V_{IL}	0.0	-	$0.3V_{DD}$	0.0	-	1.5	V
High Level Input Voltage	V_{IH}	$0.7V_{DD}$	-	5.5	2.7	-	5.5	V
Low Level Output Voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	0	-	0.4	V
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DD}$ max.	I_i	-10	-	10	-10	-	10	µA

■CHARACTERISTICS OF BUS LINES (SDA, SCL) FOR I²C-BUS Compatible Devices

I²C BUS Load Conditions

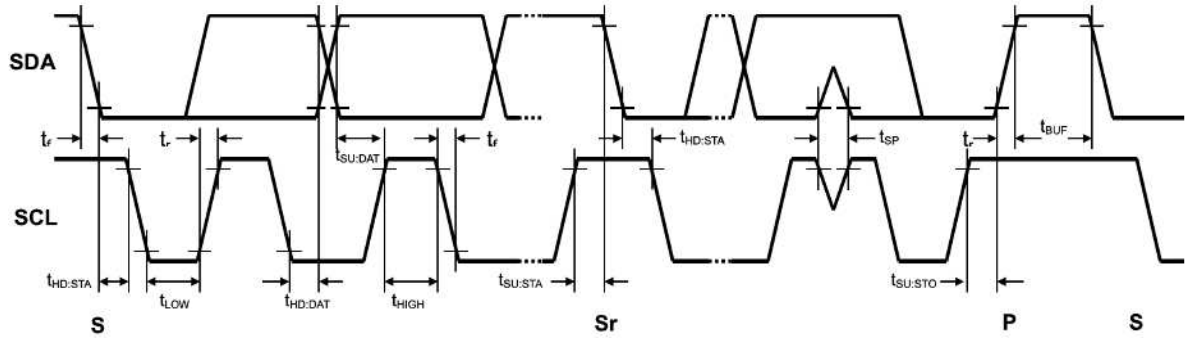
STANDARD MODE: Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 200pF (Connected to GND)

FASE MODE: Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard Mode			Fast Mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL clock frequency	f_{SCL}	10	-	100	10	-	400	kHz
Hold time (repeated) START condition	$t_{HD:STA}$	4.0	-	-	0.6	-	-	µs
Low period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	µs
High period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	µs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	-	0.6	-	-	µs
Data hold time	$t_{HD:DAT}$	0	-	-	0	-	-	µs
Data set-up time	$t_{SU:DAT}$	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	t_r	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	t_f	-	-	300	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	-	0.6	-	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	µs
Capacitive load for each bus line	C_b	-	-	400	-	-	400	pF
Noise margin at the Low Level	V_{nL}	0.5	-	-	0.5	-	-	V
Noise margin at the High Level	V_{nH}	1	-	-	1	-	-	V

C_b: Total capacitance of one bus line in pF.

■TIMING ON THE I²C BUS (SDA, SCL)



■CHARACTERISTICS OF I/O STAGES FOR EEPROM I²C-BUS (EXSDA, EXSCL)

I²C BUS Load Conditions

Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Low Level Input Voltage	V_{IL}	0.0	-	$0.3V_{DD}$	V
High Level Input Voltage	V_{IH}	$0.7V_{DD}$	-	-	V
Low Level Output Voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	V
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DD}$ max.	I_i	-10	-	10	μA

■CHARACTERISTICS OF BUS LINES (EXSDA, EXSCL)

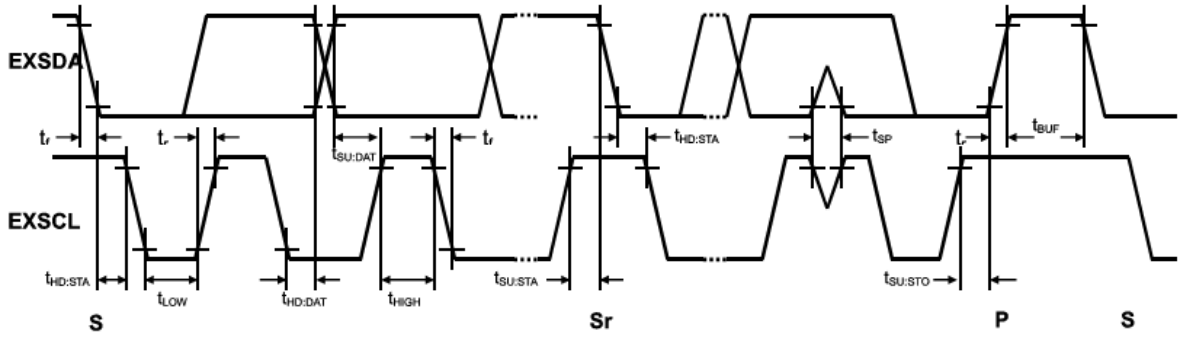
I²C BUS Load Conditions

Pull up resistance 4kΩ (Connected to V_{DD}), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
EXSCL clock frequency	f_{SCL}	92	102.3	112.7	kHz
Hold time (repeat) START condition	$t_{HD:STA}$	7.2	6.5	5.9	μs
Low period of the EXSCL clock	t_{LOW}	7.2	6.5	5.9	μs
High period of the EXSCL clock	t_{HIGH}	3.6	3.3	3.0	μs
Set-up time for a repeated START condition	$t_{SU:STA}$	7.2	6.5	5.9	μs
Data hold time (EXSDA input)	$t_{HD:DAT}$	0	-	-	μs
Data hold time (EXSDA output)	$t_{HD:DAT}$	7.2	6.5	5.9	μs
Data Set-up time (EXSDA input)	$t_{SU:DAT}$	0	-	-	μs
Data Set-up time (EXSDA output)	$t_{SU:DAT}$	7.2	6.5	5.9	μs
Rise time of both SDA and SCL signals	t_r	-	-	300	ns
Fall time of SDA and SCL signals	t_f	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	7.2	6.5	5.9	μs
Bus free time between a STOP and START condition	t_{BUF}	7.2	6.5	5.9	μs
Capacitive load for each bus line	C_b	-	-	400	pF
Noise margin at the Low level	V_{nL}	0.5	-	-	V
Noise margin at the High level	V_{nH}	1	-	-	V

C_b: total capacitance of one bus line in pF.

■TIMING ON THE EEPROM I2C BUS (EXSDA, EXSCL)



■REGISTER DESCRIPTION

NJU9101 has register (list shown below) which can access it through I^2C bus.

It can control the external EEPROM address corresponding to each register address from NJU9101.

REGISTER ADDRESS	EEPROM ADDRESS	REGISTER NAME	BIT							
			D7	D6	D5	D4	D3	D2	D1	D0
0x00	-	CTRL	-	RST	SENSCK [1:0]		MEAS	MEAS_SEL [1:0]		MEAS_SC
0x01	-	STATUS	-	-	BOOT	CLKRUN	RDYB	OV	CERR	OFOV
0x02	-	AMPDATA0	AMPDATA [15:8]							
0x03	-	AMPDATA1	AMPDATA [7:0]							
0x04	-	AUXDATA0	AUXDATA [15:8]							
0x05	-	AUXDATA1	AUXDATA [7:0]							
0x06	-	TMPDATA0	TMPDATA [9:2]							
0x07	-	TMPDATA1	TMPDATA [1:0]		-	-	-	-	-	-
0x08	-	ID	ID [7:0]							
0x09	-	ROMADR0	-	-	-	-	-	ROMADR [10:8]		
0x0A	-	ROMADR1	ROMADR [7:0]							
0x0B	-	ROMDATA	ROMDATA [7:0]							
0x0C	-	ROMCTRL	-	-	ROMERR	ROMBUSY	ROMSTOP	ROMACT	ROMMODE [1:0]	
0x0D	-	TEST	TEST [7:0]							
0x0E	0x000	ANAGAIN	-	-	-	-	PRE_GAIN [1:0]		ADC_GAIN [1:0]	
0x0F	0x001	BLKCONN0	-	-	BIASSWA	BIASSWB	PRE_BIAS [3:0]			
0x10	0x002	BLKCONN1	OPA_BIAS [2:0]			OPB_BIAS [4:0]				
0x11	0x003	BLKCONN2	PREMODE	INPSWA	INPSWB	ANASW	BIASSWN	PAMPSEL	BIASSEL	VREFSEL
0x12	0x004	BLKCTRL	BLKCTRL [7:0]							
0x13	0x005	ADCCONV	-	ADCCHOP	CLKDIV [1:0]		REJ [1:0]		OSR [1:0]	
0x14	0x006	SYSPRESET	RDYBOE	RDYBDAT	RDYBMODE [1:0]		-	-	-	AMPAUX
0x15	0x007	SCAL1A0	-	-	-	-	-	-	-	SCAL1A [8]
0x16	0x008	SCAL1A1	SCAL1A [7:0]							
0x17	0x009	SCAL2A0	-	-	-	-	-	-	-	SCAL2A [8]
0x18	0x00A	SCAL2A1	SCAL2A [7:0]							
0x19	0x00B	SCAL3A0	-	-	-	-	-	-	-	SCAL3A [8]
0x1A	0x00C	SCAL3A1	SCAL3A [7:0]							
0x1B	0x00D	SCAL4A0	-	-	-	-	-	-	-	SCAL4A [8]
0x1C	0x00E	SCAL4A1	SCAL4A [7:0]							
0x1D	0x00F	SCAL1B0	SCAL1B [15:8]							
0x1E	0x010	SCAL1B1	SCAL1B [7:0]							
0x1F	0x011	SCAL2B0	SCAL2B [15:8]							
0x20	0x012	SCAL2B1	SCAL2B [7:0]							
0x21	0x013	SCAL3B0	SCAL3B [15:8]							
0x22	0x014	SCAL3B1	SCAL3B [7:0]							
0x23	0x015	SCAL4B0	SCAL4B [15:8]							
0x24	0x016	SCAL4B1	SCAL4B [7:0]							
0x25	0x017	OCAL1A0	-	-	-	-	-	-	OCAL1A [9:8]	
0x26	0x018	OCAL1A1	OCAL1A [7:0]							

0x27	0x019	OCAL2A0	-	-	-	-	-	-	OCAL2A [9:8]
0x28	0x01A	OCAL2A1	OCAL2A [7:0]						
0x29	0x01B	OCAL3A0	-	-	-	-	-	-	OCAL3A [9:8]
0x2A	0x01C	OCAL3A1	OCAL3A [7:0]						
0x2B	0x01D	OCAL4A0	-	-	-	-	-	-	OCAL4A [9:8]
0x2C	0x01E	OCAL4A1	OCAL4A [7:0]						
0x2D	0x01F	OCAL1B0	-	OCAL1B [14:8]					
0x2E	0x020	OCAL1B1	OCAL1B [7:0]						
0x2F	0x021	OCAL2B0	-	OCAL2B [14:8]					
0x30	0x022	OCAL2B1	OCAL2B [7:0]						
0x31	0x023	OCAL3B0	-	OCAL3B [14:8]					
0x32	0x024	OCAL3B1	OCAL3B [7:0]						
0x33	0x025	OCAL4B0	-	OCAL4B [14:8]					
0x34	0x026	OCAL4B1	OCAL4B [7:0]						
0x35	0x027	SCAL1	SCAL1 [7:0]						
0x36	0x028	SCAL2	SCAL2 [7:0]						
0x37	0x029	SCAL3	SCAL3 [7:0]						
0x38	0x02A	OCAL1	OCAL1 [7:0]						
0x39	0x02B	OCAL2	OCAL2 [7:0]						
0x3A	0x02C	OCAL3	OCAL3 [7:0]						
0x3B	0x02D	AUXSCAL0	AUX_SCAL [15:8]						
0x3C	0x02E	AUXSCAL1	AUX_SCAL [7:0]						
0x3D	0x02F	AUXOCAL0	AUX_OCAL [15:8]						
0x3E	0x030	AUXOCAL1	AUX_OCAL [7:0]						
0x3F	-	CHKSUM	CHKSUM [7:0]						

■EVERY REGISTER DESCRIPTION

CTRL Register Register Address: 0x00, EEPROM Address: -

CTRL								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	RST	SENSCK [1:0]		MEAS	MEAS_SEL [1:0]		MEAS_SC
R / W	-	WS	RW		RW	RW		RW
RESET	-	-	0x0		0	0x0		0

BIT	BIT NAME	FUNCTION
[6]	RST	Write Software Reset. When read this bit, always return “0”. 0: No effect 1: Reset
[5:4]	SENSCK	Change offset voltage of OPB to check sensor diagnostic. 00: OFF (No change) 01: Plus Offset (Change Offset Voltage ≈ +5.0mV) 10: Minus Offset (Change Offset Voltage ≈ -5.0mV) 11: Reserve
[3]	MEAS	Measurement Switch When write “1”, ADC conversion starts. When read this bit, returns “1” in case of under conversion, “0” in case of idle condition. When select “Single Conversion” mode, this bit is set to “0” automatically after conversion completion. When select “Continuous Conversion” mode and write “0”, ADC conversion stop and return to an idol state. 0: Measurement OFF (Operating condition of this chip follows “BLKCTRL” condition) 1: Measurement ON
[2:1]	MEAS_SEL	Measurement Mode Selection. 00: Temperature sensor input mode 01: Amplifier input mode 10: Auxiliary input mode 11: Reserve
[0]	MEAS_SC	Measurement Mode for ADC 0: Single Conversion 1: Continuous Conversion

STATUS Register Register Address: 0x01, EEPROM Address: -

STATUS								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	BOOT	CLKRUN	RDYB	OV	CERR	OFOV
R / W	-	-	R	R	R	R	R	R
RESET	-	-	1	-	1	0	0	0

BIT	BIT NAME	FUNCTION
[5]	BOOT	Booting flag for IC. NJU9101 reads initial register value from external EEPROM as booting. This bit returns "1" until the reading of the initial register value is completed from start. 0: Completion of booting 1: Under booting
[4]	CLKRUN	System Clock Condition. 0: System Clock is sleeping 1: System Clock is operating
[3]	RDYB	Data Ready Flag. When conversion data is updated, this bit is cleared to "0". When either "AMPDATA0", "AUXDATA0", or "TMPDATA" is read, this bit is set to "1". 0: New ADC data is ready 1: New ADC data is not ready
[2]	OV	Overflow flag in sensitivity calibration of ADC output data. When over flow is occurred in sensitivity calibration of ADC conversion data, this bit is set to "1". When this bit is "1", ADC output data ("AMPDATA" or "AUXDATA") is set to 0x7FFF (positive over flow) or 0x8000 (negative over flow). When either "AMPDATA0", "AUXDATA0", or "TMPDATA" is read, this bit is cleared to "0". 0: ADC conversion data is valid 1: ADC conversion data is over flow (set 0x7FFF or 0x8000)
[1]	CERR	Overflow flag in calibration coefficient data. When over flow is occurred in setting of calibration coefficient data, this bit is set to "1". In case of "1", ADC output data is invalid value. When either "AMPDATA0", "AUXDATA0" or "TMPDATA" is read, this bit is cleared to "0". 0: No overflow in calibration coefficient calculation 1: Overflow in calibration coefficient calculation (Output data is invalid)
[0]	OFOV	Overflow flag in offset calibration of ADC output data. When over flow is occurred in offset calibration of ADC conversion data, this bit is set to "1". In case of "1", ADC output data is invalid value. When either "AMPDATA0", "AUXDATA0" or "TMPDATA" is read, this bit is cleared to "0". 0: No overflow in offset calibration data 1: Overflow in offset calibration data (Output data is invalid)

AMPDATA0 / AMPDATA1 Register Register Address: 0x02 / 0x03, EEPROM Address: -

	AMPDATA0								AMPDATA1							
	Register Address: 0x02								Register Address: 0x03							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	AMPDATA [15:0]															
R / W	R															
RESET	-															

BIT	BIT NAME	FUNCTION
AMPDATA0 [7:0] + AMPDATA1 [7:0]	AMPDATA[15:0]	ADC output data register for amplifier input mode. Singed 16-Bit data.

AUXDATA0 / AUXDATA1 Register Register Address: 0x04 / 0x05, EEPROM Address: -

	AUXDATA0								AUXDATA1							
	Register Address: 0x04								Register Address: 0x05							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	AUXDATA [15:0]															
R / W	R															
RESET	-															

BIT	BIT NAME	FUNCTION
AUXDATA0 [7:0] + AUXDATA1 [7:0]	AUXDATA[15:0]	ADC output data register for Auxiliary input mode. Signed 16-Bit data.

TMPDATA0 / TMPDATA1 Register Register Address: 0x06 / 0x07, EEPROM Address: -

	TMPDATA0								TMPDATA1							
	Register Address: 0x06								Register Address: 0x07							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	TMPDATA [9:0]										-	-	-	-	-	-
R / W	R/W										-	-	-	-	-	-
RESET	-										-	-	-	-	-	-

ビット	ビット名	機能
TMPDATA0 [7:0] + TMPDATA1 [7:6]	TMPDATA[9:0]	ADC output data register for Temperature sensor input mode. Signed 8.2 fixed point format. (-45°C to +127.75°C) Temperature calibration calculation is executed by value of TEMPDATA. When calibration is executed by using external temperature sensor, write data which getting from external temperature sensor to this register.

ID Register Register Address: 0x08, EEPROM Address: -

ID								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	ID [7:0]							
R / W	R							
RESET	0x55							

BIT	BIT NAME	FUNCTION
[7:0]	ID	Fixed value “0x55” is stored as a chip identification code in this register.

ROMADR0 / ROMADR1 Register Register Address: 0x09 / 0x0A, EEPROM Address: -

	ROMADR0								ROMADR1							
	Register Address: 0x09								Register Address: 0x0A							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	-	-	ROMADR [10:0]										
R / W	-	-	-	-	-	RW										
RESET	-	-	-	-	-	0x0										

ビット	ビット名	機能
ROMADR0 [2:0] + ROMADR1 [7:0]	ROMADR[10:0]	This is EEPROM address selection register that read/write from/to EEPROM.

*Be sure to set ROMADR0[4:3] = “00” to control EEPROM.

ROMDATA Register Register Address: 0x0B, EEPROM Address: -

ROMDATA								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	ROMDATA [7:0]							
R / W	RW							
RESET	0x00							

BIT	BIT NAME	FUNCTION
[7:0]	ROMDATA	In read mode, return a reading data from EEPROM. In write mode, set a writing data to EEPROM.

*Be sure to set ROMADR0[4:3] = “00” to control EEPROM.

ROMCCTL Register Register Address: 0x0C, EEPROM Address: -

ROMCCTL								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	ROMERR	ROMBUSY	ROMSTOP	ROMACT	ROMMODE [1:0]	
R / W	-	-	RC	R	WS	WS	W	
RESET	-	-	-	-	0x0	0x0	0x0	

BIT	BIT NAME	FUNCTION
[5]	ROMERR	When I^2C bus communication error occurs during accessing to external EEPROM, this bit is set to "1". It is communication error in the following cases, 1) When NJU9101 outputs address, data, acknowledge data, it receives the EXSDA data different from the EXSDA data which outputs. 2) NJU9101 receives NACK response in the timing which it is expected to receive ACK response. And, It is cleared to "0" when this bit is written in "1". 0: I2C communication is not error 1: I2C communication is error
[4]	ROMBUSY	This bit shows accessing status to external EEOPROM. 0: Completion of the access 1: Under accsessing
[3]	ROMSTOP	When write "1" to "ROMSTOP" bit, stop accessing to external EEPROM. "ROMBUSY" bit is cleared to "0" immediately. When it stops accessing during writing to external EEPROM, ROM data is not guaranteed. In the read mode, this bit always returns "0". 1: stop accessing to external EEPROM
[2]	ROMACT	When write "1" to ROMACT bit, start accessing to external EEPROM with following "ROMMODE[1:0]" data. In write "0" case, it is not started accessing. And, to start accessing to external EEPROM, it is necessary that it is not accessing timing to external EEPROM ("ROMBUSY" bit = "0"), and system clock is during operation ("CLKRUN" bit = "1"). In the read mode, this bit always returns "0". 1: start accessing to external EEPROM
[1:0]	ROMMODE	Write operation for external EEPROM. In the read mode, this bit returns "0". 00: Read one byte data from external EEPROM (address ROMADR[10:0]), and, store this one byte data to ROMDATA[7:0] bit register in NJU9101. 01: Write ROMDATA[7:0] bit data to register in external EEPROM which is assigned by ROMADR[10:0] address. 10: Load external EEPROM data to Host-register (ex. MPU) 11: Store Host-register setting (ex. MPU) into external EEPROM data.

*Be sure to set ROMADR0[4:3] = "00" to control EEPROM.

TEST Register Register Address: 0x0D, EEPROM Address: –

TEST								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	TEST [7:0]							
R / W	RW							
RESET	0x00							

*This register if for production test purpose. Do not write data to this register.

ANAGAIN Register Register Address: 0x0E, EEPROM Address: 0x000

ANAGAIN								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	-	PRE_GAIN [1:0]		ADC_GAIN [1:0]	
R / W	-	-	-	-	RW		RW	
RESET	-	-	-	-	0x0		0x0	

BIT	BIT NAME	FUNCTION
[3:2]	PRE_GAIN	Pre-amplifier gain selection 00: 1 V/V 01: 2 V/V 10: 4 V/V 11: 8 V/V
[1:0]	ADC_GAIN	Programmable-gain-amplifier in ADC selection 00: 1 V/V 01: 2 V/V 10: 4 V/V 11: 8 V/V

BLKCONN0 Register Register Address: 0x0F, EEPROM Address: 0x001

BLKCONN0								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	BIASSWA	BIASSWB	PRE_BIAS [3:0]			
R / W	-	-	RW	RW	RW			
RESET	-	-	0x0	0x0	0x0			

BIT	BIT NAME	FUNCTION
[5]	BIASSWA	This is Switch for connecting “BIASRES” and “OPA positive input” 00: Open “BIASRES” and “OPA positive input” 01: Connect “BIASRES” and “OPA positive input”
[4]	BIASSWB	This is Switch for connecting “BIASRES” and “OPB positive input” 00: Open “BIASRES” and “OPB positive input” 01: Connect “BIASRES” and “OPB positive input”
[3:0]	PRE_BIAS	Negative input bias level for PREAMP (From 0.3V to 1.7V are 100mV steps) This bias level is set by “BIASRES” Circuit Block. V_{REFIN} = 3V or at INTVREF(2.048V) as follows 0000: GND 0001: 0.3V 0010: 0.4V 0011: 0.5V : : 1101: 1.5V 1110: 1.6V 1111: 1.7V

BLKCONN1 Register Register Address: 0x10, EEPROM Address: 0x002

BLKCONN1								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	OPA_BIAS [2:0]			OPB_BIAS [4:0]				
R / W	RW			RW				
RESET	0x0			0x0				

BIT	BIT NAME	FUNCTION
[7:5]	OPA_BIAS	Bias Level for OPA, This bias level is set by "BIASRES" Block. V_{REFIN} = 3V or at INTVREF(2.048V) as follows 000: GND 001: 0.3V 010: 0.5V 011: 0.7V 100: 1.0V 101: 1.3V 110: 1.5V 111: 1.7V
[4:0]	OPB_BIAS	Bias Level for OPB (From 0.25V to 1.75V are 50mV steps). V_{REFIN} = 3V or at INTVREF(2.048V) as follows 00000: GND 00001: 0.25V 00010: 0.3V 00011: 0.35V : 11101: 1.65V 11110: 1.7V 11111: 1.75V

BLKCONN2 Register Register Address: 0x11, EEPROM Address: 0x003

BLKCONN2								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	PREMODE	INPSWA	INPSWB	ANASW	BIASSWN	PAMPSEL	BIASSEL	VREFSEL
R / W	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

BIT	BIT NAME	FUNCTION
[7]	PREMODE	Select PREAMP mode 0: Non-Inverted Amplifier mode 1: Instrumentation Amplifier mode
[6]	INPSWA	OPA positive input connection 0: GND Positive input is connected to GND. 1: AINP Positive input is connected to AINP Pin.
[5]	INPSWB	OPB positive input connection 0: GND Positive input is connected to GND. 1: BINP Positive input is connected to BINP Pin.
[4]	ANASW	Build in Analog Switch Status 0: Switch OFF 1: Switch ON On Resistance is 10Ω typ. Absolute Maximum Input Current is ±50mA.
[3]	BIASSWN	Select switch for PREAMP / ADC Negative Input at AMP / AUX input mode. 0: OPB Output / AUXIN- 1: BIASRES This is selectable bias level set by “PRE-BIAS”.
[2]	PAMPSEL	Enable / Disable PREAMP for signal path. 0: Disable (Bypass PREAMP) 1: Enable
[1]	BIASSEL	Reference Voltage selection for Bias Register 0: Internal Reference (2.048V) 1: External Reference
[0]	VREFSEL	Reference Voltage selection for ADC 0: Internal Reference (2.048V) 1: External Reference

BLKCTRL Register Register Address: 0x12, EEPROM Address: 0x004

BLKCNT								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	BLKCTRL [7:0]							
R / W	RW							
RESET	0x00							

BIT	BIT NAME	FUNCTION
[7:0]	BLKCTRL	Circuit Block Powered down selection. When ADC is in the idle state, circuit block which this bit is set to “0” is automatically powered down. The circuit block which this bit is set to “1” is kept powered on state even in case of ADC idle state. When all bits are “0”, NJU9101 goes “power down mode” except for Digital block. [7] : BIASRES block [6] : OPB block [5] : OPA block [4] : OSC block [3] : PREAMP block [2] : INTVREF(2.048V) block [1] : ADC block [0] : Temperature Sensor block

ADCCONV Register Register Address: 0x13, EEPROM Address: 0x005

ADCCONV								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	ADCCHOP	CLKDIV [1:0]		REJ [1:0]		OSR [1:0]	
R / W	-	RW	RW		RW		RW	
RESET	-	0x0	0x0		0x0		0x0	

BIT	BIT NAME	FUNCTION
[6]	ADCCHOP	ADC CHOP Switch. It's effective in reducing offset Voltage of PREAMP and ADC. Reduce offset voltage by chopping input signal. When this bit is "1", conversion time becomes long. (ex. 16.2ms(ADCCHOP="0") -> 31.1ms(ADCCHOP="1")) 0: CHOP OFF 1: CHOP ON
[5:4]	CLKDIV	Select operation clock frequency for sigma-delta modulator. f_{OSC}=307.2kHz typ. 00: $f_{mod}=(1/2) \times f_{OSC}$ 01: $f_{mod}=(1/4) \times f_{OSC}$ 10: $f_{mod}=(1/8) \times f_{OSC}$ 11: $f_{mod}=(1/16) \times f_{OSC}$
[3:2]	REJ	Select rejection mode for Sinc3 filter 00: 50/60Hz Rejection 01: 50Hz Rejection 10: 60Hz Rejection 11: Reserved
[1:0]	OSR	Select Decimation ratio for Sinc3 filter. Total Decimation Ratio is decided by REJ / OSC bits combination.

ADC Decimation Ratio

OSR [1:0]	REJ [1:0]			
	00	01	10	11
00	768	768	640	-
01	384	384	320	-
10	192	192	160	-
11	96	96	80	-

ADC Conversion Time [ms]

OSR [1:0]	REJ [1:0]															
	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
00	16.2	16.2	13.7	-	31.3	31.3	26.3	-	5	5	4.2	-	15.3	15.3	12.8	-
01	8.7	8.7	7.5	-	16.3	16.3	13.8	-	2.5	2.5	2.1	-	7.8	7.8	6.5	-
10	5.0	5.0	4.3	-	8.8	8.8	7.6	-	1.3	1.3	1.0	-	4.0	4.0	3.4	-
11	3.1	3.1	2.8	-	5.1	5.1	4.5	-	0.6	0.6	0.5	-	2.1	2.1	1.8	-
State	Single Conversion								Continuous Conversion							
	CHOP: OFF				CHOP: ON				CHOP: OFF				CHOP: ON			

Conversion Time vs Resolution (ADC)

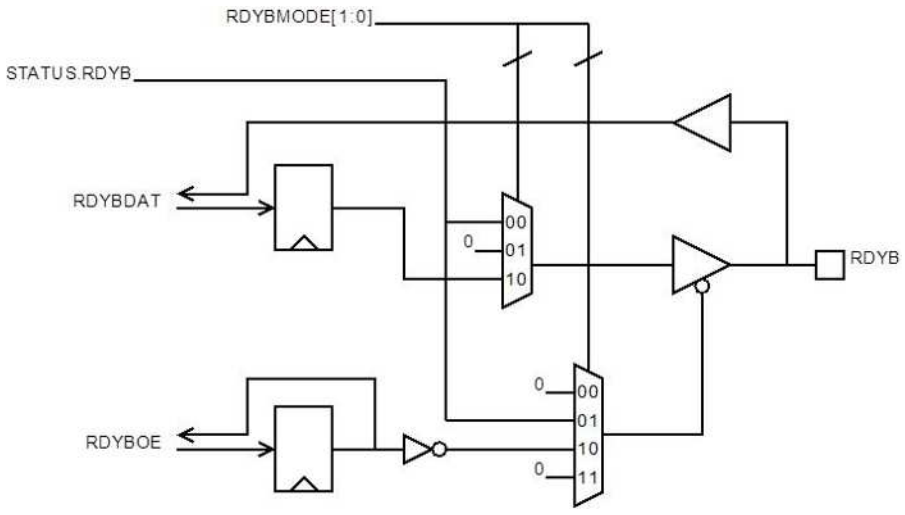
ADC Conversion Time	CHOP: ON				CHOP: OFF			
	ADC Gain				ADC Gain			
	1V/V	2V/V	4 V/V	8 V/V	1 V/V	2 V/V	4 V/V	8 V/V
26.3ms	16 / (16)	16 / (16)	16 / (16)	16 / (16)	16 / (16)	16 / (16)	15.6 / (16)	15.3 / (16)
13.8ms	16 / (16)	16 / (16)	15.2 / (16)	16 / (16)	16 / (16)	16 / (16)	15 / (16)	14.8 / (16)
7.6ms	15 / (16)	14.7 / (16)	14.5 / (16)	14 / (16)	15 / (16)	14.7 / (16)	14.1 / (16)	13.5 / (16)
4.5ms	14 / (16)	14 / (16)	13.5 / (16)	12 / (14.7)	14 / (16)	14 / (16)	13.6 / (16)	12 / (14.7)

Noise Free Bit / (Effective Number of Bits), Unit: bit

SYSPRESET Register Register Address: 0x14, EEPROM Address: 0x006

SYSPRESET								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	RDYBOE	RDYBDAT	RDYBMODE [1:0]		-	-	-	AMPAUX
R / W	RW	RW	RW		-	-	-	RW
RESET	0x0	-	0x1		-	-	-	0x0

BIT	BIT NAME	FUNCTION
[7]	RDYBOE	RDYB terminal direction of GPIO mode 0: RDYB terminal is input mode 1: RDYB terminal is Output mode
[6]	RDYBDAT	Return RDYB terminal level in input mode. Store RDYB terminal level in Output mode.
[5:4]	RDYBMODE	Select function of RDYB terminal 00: RDYB terminal outputs “RDYB” bit in STATUS register. 01: RDYB terminal outputs “RDYB” bit in STATUS register. with open-drain circuit style. 10: RDYB terminal is used as GPIO. Output condition is set by “RDYBDAT” and “RDYBOE”. 11: Reserved
[0]	AMPAUX	Select Calibration channel coefficient assignment. 0: AMPDATA uses SCAL/OCAL calibration coefficient. AUXDATA uses AUX_SCAL / AUX_OCAL calibration coefficient. 1: AMPDATA uses AUX_SCAL / AUX_OCAL calibration coefficient. AUXDATA uses SCAL/OCAL calibration coefficient.



SCALxA0 / SCALxA1 Register Register Address: 0x15 to 0x1C, EEPROM Address: 0x007 to 0x00E

	SCALxA0 (x=1 to 4)								SCALxA1 (x=1 to 4)							
	Register Address: 0x15, 0x17, 0x19, 0x1B EEPROM Address: 0x007, 0x009, 0x00B, 0x00D								Register Address: 0x16, 0x18, 0x1A, 0x1C EEPROM Address: 0x008, 0x00A, 0x00C, 0x00E							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	-	-	-	-	SCALxA [8:0]								
R / W	-	-	-	-	-	-	-	RW								
RESET	-	-	-	-	-	-	-	-								

BIT	BIT NAME	FUNCTION
SCALxA0 [0] + SCALxA1 [7:0]	SCALxA [8:0] (x=1 to 4)	1ST order Gain Calibration parameter for AMPDATA. This parameter is signal 9-Bit data.

SCALxB0 / SCALxB1 Register Register Address: 0x1D to 0x24, EEPROM Address: 0x00F to 0x016

	SCALxB0 (x=1 to 4)								SCALxB1 (x=1 to 4)							
	Register Address: 0x1D, 0x1F, 0x21, 0x23 EEPROM Address: 0x00F, 0x011, 0x013, 0x15								Register Address: 0x1E, 0x20, 0x22, 0x24 EEPROM Address: 0x010, 0x012, 0x014, 0x016							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	SCALxB [15:0]															
R / W	RW															
RESET	-															

BIT	BIT NAME	FUNCTION
SCALxB0 [7:0] + SCALxB1 [7:0]	SCALxB [15:0] (x=1 to 4)	Zero-order Gain Calibration parameter for AMPDATA. This parameter is unsigned 16-Bit data.

OCALxA0 / OCALxA1 Register Register Address: 0x25 to 0x2C, EEPROM Address: 0x017 to 0x01E

	OCALxA0 (x=1 to 4)								OCALxA1 (x=1 to 4)							
	Register Address: 0x25 to 0x28 EEPROM Address: 0x017 to 0x01A								Register Address: 0x29 to 0x2C EEPROM Address: 0x01B to 0x01E							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	-	-	-	OCALxA [9:0]									
R / W	-	-	-	-	-	-	RW									
RESET	-	-	-	-	-	-	-									

BIT	BIT NAME	FUNCTION
OCALxA0 [1:0] + OCALxA1 [7:0]	OCALxA [9:0] (x=1 to 4)	1ST order Offset Calibration parameter for AMPDATA. This parameter is signed 10-Bit data.

OCALxB0 / OCALxB1 Register Register Address: 0x2D to 0x34, EEPROM Address: 0x01F to 0x026

	OCALxB0 (x=1 to 4)								OCALxB1 (x=1 to 4)							
	Register Address: 0x2D, 0x2F, 0x31, 0x33 EEPROM Address: 0x01F, 0x021, 0x023, 0x025								Register Address: 0x2E, 0x30, 0x32, 0x34 EEPROM Address: 0x020, 0x022, 0x024, 0x026							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	OCALxB [14:0]														
R / W	-	RW														
RESET	-	-														

BIT	BIT NAME	FUNCTION
OCALxB0 [6:0] + OCALxB1 [7:0]	OCALxB [14:0] (x=1 to 4)	Zero-order Offset Calibration parameter for AMPDATA. This parameter is signed 15-Bit data.

SCALx Register Register Address: 0x35 to 0x37, EEPROM Address: 0x027 to 0x029

	SCALx (x=1 to 3)							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	SCALx [7:0]							
R / W	RW							
RESET	-							

BIT	BIT NAME	FUNCTION
[7:0]	SCALx (x=1 to 3)	Threshold Temperature for AMPDATA Sensitivity Calibration. Signed 8.0 fixed point format. (-45°C to +127°C) -45°C ≤ SCAL1 < SCAL2 < SCAL3 ≤ +127°C