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Analog Front End with High Gain PGA

■ FEATURES

- ●Supply Voltage +2.7V to +3.6V
- ●Ambient Operating Temperature -40°C to +125°C
- ●ADC Resolution 16-Bit (No missing codes)
- ●Data Rate 0.814k to 6.51ksps(1)
- ●Input mode Differential
  Single-ended(2)
  Pseudo-differential(3)
- ●PGA 1V/V to 512V/V
- ●System Calibration for offset & gain drift
- ●Conversion mode Single / Continuous
- ●Interface SPI
- ●Package DFN8 (ESON8-V1) / 2.3mm x 2.3mm
  SSOP8 / 3.5mm x 6.4mm

(1) Case of single conversion.
(Continuous conversion is three times the data rate.)

(2) PGA2 can be used only. (PGA1 cannot be used.)
Two channels of VINP & VINN can be used.

(3) Bias voltage of VINP & VINN is common to VDD / 2.
Input Signal can be used VINP only.

■ GENERAL DESCRIPTION

NJU9103 is a small size AFE with up to 512 times internal PGA (Programmable Gain Amplifier).

Internal 16-bit ΔΣ type A / D converter can perform conversion rates from 0.814ksps to 6.51ksps.

The customer can choose internal A/D converter's input, among single-ended input, differential input and pseudo-differential input.

NJU9103 can set the optimum gain to the pressure sensor, flow sensor by a wide range of gain setting.

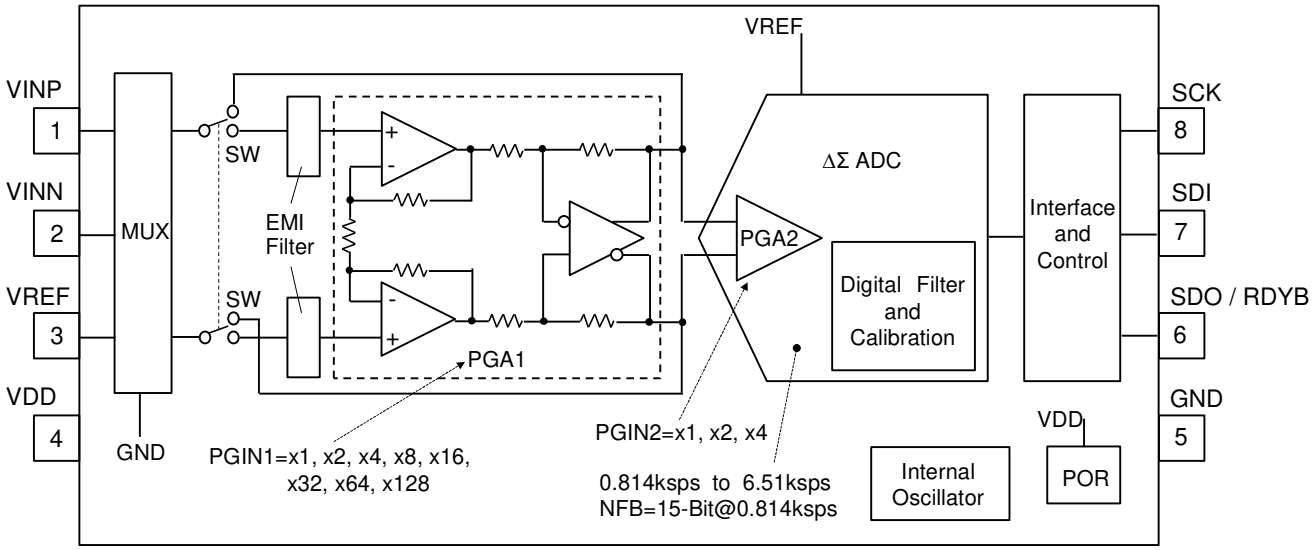
Sensor of the offset is corrected by internal D / A converter. Various parameters (such as gain, conversion rate, correction) settings can be easily set in the SPI communication from an external MCU.

NJU9103 will contribute to the customer's development time reduction and the series product release. NJU9103 is also can be mounted in a narrow application footprint by a small 8-pin package. Package is preparing the DFN and SSOP

■ APPLICATION

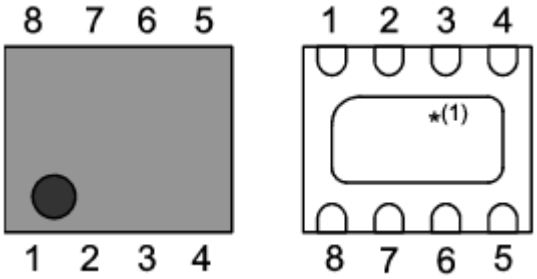
- ●Pressure sensors
- ●Flowmeters
- ●Thermostat
- ●PLC
- ●Digital Panel Meters

■ EQUIVALENT CIRCUIT BLOCK DAIGRAM

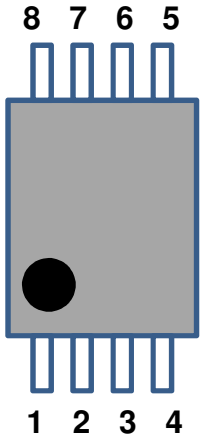


■ PIN CONFIGURATION

DFN8 (ESON8-V1)



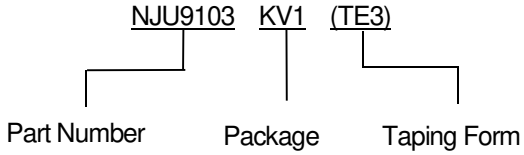
SSOP8



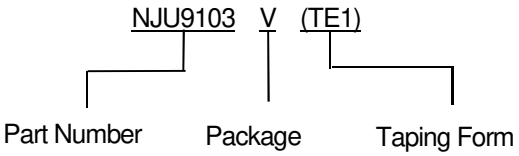
PIN NO.	SYMBOL	PIN TYPE
1	VINP	+INPUT for differential mode / INPUT1 for Single-ended mode
2	VINN	-INPUT for differential mode / INPUT2 for single-ended mode
3	VREF	Reference Voltage Input
4	VDD	Supply Voltage
5	GND	GND
6	SDO / RDYB	SPI serial data output / RDYB output
7	SDI	SPI serial data input
8	SCK	SPI serial clock input
*(1)	Exposed PAD DFN8(ESON8-V1) only	Exposed PAD on backside connects to GND.

■ MARK INFORMATION

DFN8 (ESON8-V1)



SSOP8



■ ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	Halogen-Free	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJU9103KV1	DFN8 (ESON8-V1)	○	○	Sn-2Bi	9103	7.2	3,000
NJU9103V	SSOP8	○	○	Sn-2Bi	9103	42	2,000

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	VDD	5 (4)	V
Power Dissipation (T_a=25°C)	P_D	DFN8 (ESON8-V1) : 580 (5) / 1785 (6) SSOP8 : 460 (5) / 595 (6)	mW
Analog Input Voltage	V_{IN}	-0.3 to (VDD+0.3) (7)	V
Operating Temperature Range	T_{opr}	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(4) The difference between the absolute maximum power supply voltage and the operating power supply voltage is small. Please be careful so that the operating power supply voltage does not exceed the absolute maximum supply voltage by spike voltage.

(5) Mounted on glass epoxy board.
(114.3 x 76.2 x 1.57mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(6) Mounted on glass epoxy board
(114.3 x 76.2 x 1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)

(7) Input pin is connected to the clamp diode to the power supply pin. When the input signal exceeds the supply rails 0.3V or more (below the GND rail 0.3V or more), the input current must be limited to less than 10mA.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	VDD	+2.7 to +3.6	V
Operating Temperature Range	T_{opr}	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

■ ELECTRICAL CHARACTERISTICS (Analog Input)

Unless otherwise specified, all limits ensured for T_a=+25°C, VDD=3.3V, GND=0V, VREF=0.5 x VDD, PGAIN1=PGAIN2=1, VCIN2=0.5 x VDD, DR=0.814ksps or 1.63ksps

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Analog Input 1 (PGA1=unused, PGA2=used, PGAIN2=1 or 2 or 4)						
Differential Input Voltage Range 1	VDIN1		-	±VREF / (PGAIN2)	-	V
Common Mode Input Voltage Range 1	VCIN1		GND	-	VDD	V
Input Impedance 1	ZIN1	FMOD = 1.25MHz PGAIN2 = 1	-	400	-	kΩ
		FMOD = 1.25MHz PGAIN2 = 2 or 4	-	200	-	kΩ
Common Mode Rejection Ratio 1	CMRR1	PGAIN2 = 1	70	90	-	dB
Analog Input 2 (PGA1, 2=used, PGAIN1=1 or 2 or 4 or 8 or 16 or 32 or 64 or 128, PGAIN2=1 or 2 or 4)						
Differential Input Voltage Range2	VDIN2	PGAIN1 ≥ 2	-	(±VREF) / (PGAIN1 x PGAIN2)	-	V
Common Mode Input Voltage Range 2	VCIN2		0.1	-	VDD -1.2	V
Input Impedance 2	ZIN2		-	100	-	MΩ
Common Mode Rejection Ratio 2	CMRR2	PGAIN1 = 2 PGAIN2 = 1	40	60	-	dB
		PGAIN1 = 2 PGAIN2 = 1 CHOP= ON DR = 0.407ksps	70	90	-	dB

■ ELECTRICAL CHARACTERISTICS (Reference Voltage Input)

Unless otherwise specified, all limits ensured for T_a=+25°C, VDD=3.3V, GND=0V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Reference Voltage	VREF		0.5 x VDD	-	VDD	V
Input Impedance 3	ZIN3	FMOD = 1.25MHz PGAIN2 = 1 or 2	-	180	-	kΩ
		FMOD = 1.25MHz PGAIN2 = 4	-	300	-	kΩ

■ ELECTRICAL CHARACTERISTICS (Internal Oscillator)

Unless otherwise specified, all limits ensured for T_a=+25°C, VDD=3.3V, GND=0V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
OSC Frequency	FOSC		1.75	2.5	3.25	MHz

■ ELECTRICAL CHARACTERISTICS (Programmable Gain Amplifier)

Unless otherwise specified, all limits ensured for T_a=+25°C, VDD=3.3V, GND=0V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PGA1 Gain	PGAIN1		-	1, 2, 4, 8, 16, 32, 64, 128,	-	V/V
PGA2 Gain	PGAIN2		-	1, 2, 4	-	V/V

■ ELECTRICAL CHARACTERISTICS (Analog to Digital Convertor)

Unless otherwise specified, all limits ensured for T_a=+25°C, VDD=3.3V, GND=0V, VREF=0.5 x VDD, PGAIN1=PGAIN2=1, VCIN2=0.5 x VDD

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution	N	No missing codes(8)	16			Bit
Data Rate	DR	Single Conversion(9)	0.814k, 1.63k, 3.26k, 6.51k			sps
Clock Frequency	FMOD (MDCK)	FMOD = FOSC/2	0.875	1.25	1.625	MHz
Integral Non Linearity	INL	best-fit-line method(10) VREF = VDD PGAIN1 = 2	-	±30	±60	ppm
Offset Error	OE	PGAIN1 = 128 Input-Referred Offset	-	200	-	µV
		PGAIN1 = 128 Input-Referred Offset CHOP=ON	-	±2	±10	µV
Gain Error	GE	PGAIN1 = 128 DR = 3.26ksps	1.0	2.5	4.0	%
Noise Free Bit(11)	NFB	VDIN2 = 0V VREF = 3.3V DR = 0.814ksps(8)	14	15	-	Bit
		VDIN2 = 0V VREF = 3.3V DR = 1.63ksps(8)	13	14	-	Bit

(8) This parameter is not production tested, please refer Typical Characteristics.

(9) There is no latency by one settling behavior.

(10) Guaranteed by design evaluation and several points test

(11) NFB represents the ADC output code variations 6.6σ with the differential input shorted.

■ ELECTRICAL CHARACTERISTICS (Power Supply / Supply Current)

Unless otherwise specified, all limits ensured for T_a=+25°C, VDD=3.3V, GND=0V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	VDD		2.7	3.3	3.6	V
Supply Current 1	IDD	PGA OFF	1.65	2.3	3.0	mA
		PGA ON	3.0	4.0	5.0	mA
Supply Current 2	IDD_{pd}	Power Down Mode	12.75	17.00	21.25	µA

■ ELECTRICAL CHARACTERISTICS (Digital I/Os)

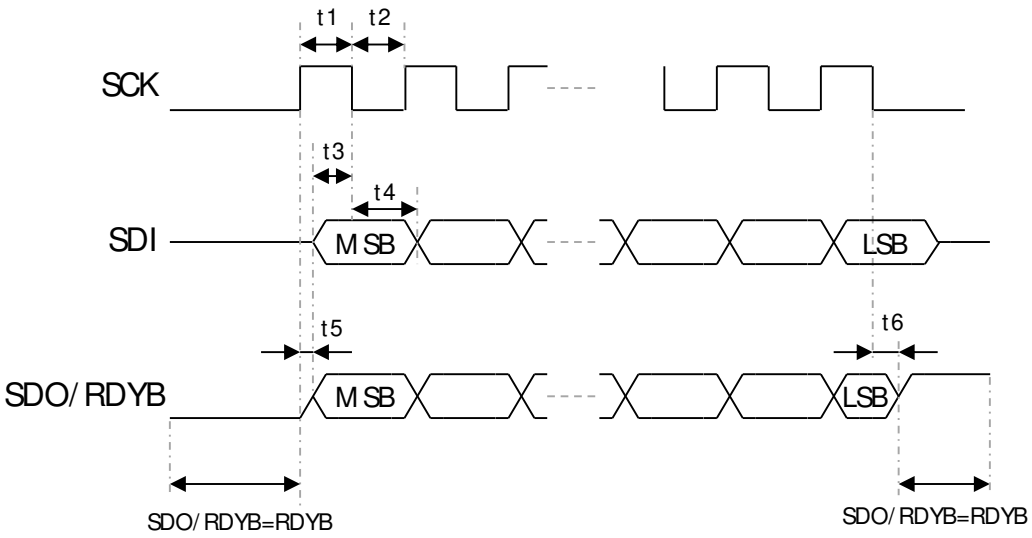
Unless otherwise specified, all limits ensured for T_a=+25°C, VDD=3.3V, GND=0V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Positive-going input threshold voltage	$V_{th}+$		-	1.6	-	V
Negative-going input threshold voltage	$V_{th}-$		-	1.2	-	V
Input voltage hysteresis	V_{hyst}	VDD = 3.0V	-	280	-	mV
High-level input voltage	V_{ih}		0.7 x VDD	-	-	V
Low-level input voltage	V_{il}		-	-	0.3 x VDD	V
High-level output voltage	V_{oh}	I_{oh} max.= 6mA	0.8 x VDD	-	-	V
Low-level output voltage	V_{ol}	I_{ol} max.= 6mA	-	-	0.4	V

■ ELECTRICAL CHARACTERISTICS (Serial Peripheral Interface)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
SPI clock frequency	F_{sck}	-	-	10	MHz
High period of the SCK clock	t1	45	-	-	ns
Low period of the SCK clock	t2	45	-	-	ns
SDI input data setup time	t3	5	-	-	ns
SDI input data hold time	t4	5	-	-	ns
SDO / RDYB output data setup time	t5	0	-	40	ns
SDO / RDYB output data hold time	t6	10	-	50	ns
Reset time	t_{rstw}	-	-	400	ns

- The SPI of AC timing is shown in the figure below. At the maximum, it is the communication of 10Mbps.
- Load of SDO / RDB terminal is assumed to 40pF
- CSB terminal (chip select terminal) is fixed at a low level inside the chip.
- In order to connect a plurality of NJU9103, it requires SPI bus that is equally the number of NJU9103.



■ REGISTER DESCRIPTION

NJU9103 has register (list shown below) which can access it through SPI bus.

REGISTER ADDRESS	REGISTER NAME	BIT [7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0	CTRL	RDYB	OV / CHSEL [2]	CHSEL [1:0]		MODE [3:0]			
0x1	ADCDATA0	ADCDATA [15:8]							
0x2	ADCDATA1	ADCDATA [7:0]							
0x3	PGACONF	-	-	PGA2GAIN [1:0]		PGA1EN	PGA1GAIN [2:0]		
0x4	CLKCONF	-	-	CLKDIV [1:0]		-	OSR [2:0]		
0x5	DACCONF	-	-	CALDACEN	CALDAC [4:0]				
0x6	OPTION0	CHIPID [6:0]							AUTOSLP
0x7	Not used	-							
0x8	GAIN0	GAIN [23:16]							
0x9	GAIN1	GAIN [15:8]							
0xA	GAIN2	GAIN [7:0]							
0xB	OFFSET0	OFFSET [23:16]							
0xC	OFFSET1	OFFSET [15:8]							
0xD	OFFSET2	OFFSET [7:0]							
0xE	Not used	-							
0xF	Not used	-							

< View of the register table>

REGISTER NAME								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME								
R / W								
RESET								

R / W: Bit of attribute (Write or Read)

- R (Read Only) : Read only
- W (Write Only) : Write only (At the time of read, return "0".)
- RW (Read Write) : Read & Write

Reset: Reset value in register

Set to the reset value by SPI reset command and power-on.

■ EVERY REGISTER DESCRIPTION

CTRL Register Register Address: 0x0

CTRL								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	RDYB	OV	-		MODE [3:0]			
		CHSEL [2:0]						
R / W	R	R / W	RW		RW			
RESET	1	0	0x0		0x0			

BIT	BIT NAME	FUNCTION
[7]	RDYB	Data Ready Flag. When conversion data is updated, this bit is set to “0”. When “ADCDATA0” is read, this bit is set to “1”. 0: Ready 1: Not ready
[6]	OV	Overflow flag. When conversion data is overflow, this bit is set to “1”. When “ADCDATA0” is read, this bit is set to “1”. 0: Valid 1: Overflow (Data is invalid)
[5:4]	CHSEL [2:0]	Analog input channel setting. Please refer to Table 1 for details.
[3:0]	MODE	Operation mode setting. When this bit is read, returns the current configuration state. Please refer to Table 2 for details.

Table 1 CHSEL [2:0]

CHSEL [2:0]	Positive	Negative
0x0	VINP	VINN
0x1	Not used(12)	
0x2	VINP	GND
0x3	VINN	GND
0x4	VREF	GND
0x5	GND	GND
0x6	VINN	VINN
0x7	Not used(12)	

(12) Please do not absolutely use the “Not used” code. It will be the cause of failure.

Table 2 MODE [3:0]

MODE [3:0]	Operation	Processing
0x0	idle	Conversion operation waiting state
0x1	Not used(13)	-
0x2	Single conversion	Convert once the input channel that is selected in the CHSEL [2:0]. After the conversion, the operation is “idle (0x0)” state. Using the value of the “OFFSET0, 1, 2” register.
0x3	Continuous conversion	Convert continuous the input channel that is selected in the CHSEL[2:0]. Until the operation is set to "idle (0x0)", conversion will continue. Using the value of the “OFFSET0, 1, 2” register.
0x4	Single conversion + CHOP	This is the same as “Single conversion (0x2)”, but the data rate is 1/2. Not using the value of the “OFFSET0, 1, 2” register.
0x5	Continuous conversion + CHOP	This is the same as “Continuous conversion (0x3)”, but the data rate is 1/3. Not using the value of the “OFFSET0, 1, 2” register.
0x6	Not used(13)	-
0x7	Not used(13)	-
0x8	Calibration ADC offset	When you run this command, the following will be processed automatically. - PGA1 turn off, PGA2 gain is set to “x1”. - Input is fixed to GND/GND internally, ADC offset will be calibrated. - Coefficient is stored in the offset register. In this case, the CHSEL [2:0] setting is invalid.
0x9	Calibration ADC gain	When you run this command, the following will be processed automatically. - PGA1 turn off, PGA2 gain is set to “x1”. - Input is fixed to VREF/GND internally, ADC gain will be calibrated. - Coefficient is stored in the gain register. In this case, the CHSEL [2:0] setting is invalid.
0xA	Calibration PGA offset(14)	When you run this command, the following will be processed automatically. However, before the execution of this command to set the PGA1 / PGA2 gain. - Input is fixed to VNN/VNN internally, PGA offset will be calibrated. - Coefficient is stored in the offset register. In this case, the CHSEL [2:0] setting is invalid.
0xB	Not used(13)	-
0xC	Calibration system offset	This command is calibrated in a state in which to connect the sensor. When you run this command, the following will be processed automatically. However, before the execution of this command to set the input channel. - Input is selected by CHSEL [2:0], system offset will be calibrated. - Coefficient is stored in the offset register.
0xD	Calibration system gain	This command is calibrated in a state in which to connect the sensor. When you run this command, the following will be processed automatically. However, before the execution of this command to set the input channel. - Input is selected by CHSEL [2:0], system gain will be calibrated. - Coefficient is stored in the gain register.
0xE	Not used(13)	-
0xF	Boot	Read-only. It shows the state from the reset to change to idle (0x0). After the initial setting, automatically shifts to the "idle (0x0)".

(13) Please do not absolutely use the “Not used” code. It will be the cause of failure.

(14) Before the commands are executed, please set PGA1/ 2 of the gain to PGACONF register.

ADCDATA0 / ADCDATA1 Register Register Address: 0x1 / 0x2

	ADCDATA0								ADCDATA1							
	Register Address: 0x1								Register Address: 0x2							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	ADCDATA [15:0]															
R / W	R															
RESET	-															

BIT	BIT NAME	FUNCTION
ADCDATA0 [7:0] + ADCDATA1 [7:0]	ADCDATA [15:0]	Store the converted data of the ADC.(15) Conversion data is expressed as a signed 16-bit. - Negative full-scale voltage is 0x8000 - When the input voltage is zero 0x0000 - Positive full-scale voltage will be 0x7FFF. (in decimal -32768 to +32767) Please be sure to perform a read in order of ADCDATA0, ADCDATA1.

(15) Relationship of conversion data ADCDATA and the analog input voltage Vin is as the following equation.
(It assumed that the offset error and gain error are zero.)

$$ADCDATA = \frac{V_{in}}{2 \times VREF} \times PGAIN1 \times PGAIN2 \times 2^{16} = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 2^{15}$$

PGACONF Register Register Address: 0x3

PGACONF								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	PGA2GAIN		PGA1EN	PGA1GAIN		
R / W	-	-	RW		RW	RW		
RESET	-	-	0x0		0	0x0		

BIT	BIT NAME	FUNCTION
[5:4]	PGA2GAIN	Gain setting of PGA2. 0x0: x1 0x1: x2 0x2: x4 0x3: Not used(16)
[3]	PGA1EN	Setting ON / OFF of PGA1. 0: OFF 1: ON
[2:0]	PGA1GAIN	Gain setting of PGA1. 0x0: x1 0x1: x2 0x2: x4 0x3: x8 0x4: x16 0x5: x32 0x6: x64 0x7: x128

(16) Please do not absolutely use the “Not used” code. It will be the cause of failure.

CLKCONF Register Register Address: 0x4

CLKCONF								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	CLKDIV		-	OSR		
R / W	-	-	RW		-	RW		
RESET	-	-	0x0		-	0x3		

BIT	BIT NAME	FUNCTION
[5:4]	CLKDIV(17)	Setting of the ADC operating clock frequency (FMOD). FOSC is the operating clock of the internal OSC. 0x0: FOSC / 2 0x1: FOSC / 4 0x2: FOSC / 8 0x3: FOSC/ 16
[2:0]	OSR	Setting of the oversampling ratio of the digital filter 0x0: 64 0x1: 128 0x2: 256 0x3: 512 0x4 to 0x7 : Not used(18)

(17) Data rate is derived by the following equation. It will be the data rate of a single conversion.

$$DR = F_{OSC} \times \frac{1}{OSR} \times \frac{1}{2^{(CLKDIV+1)}} \times \frac{1}{3}$$

If FOSC is 2.5MHz of (TYP.), Conversion data rate will be set in the table below.

OSR	Date Rate [sps]			
	CLKDIV=0 (Recommendation)	CLKDIV=1(*)	CLKDIV=2(*)	CLKDIV=3(*)
512	0.814k	0.407k	0.204k	0.102k
256	1.63k	0.814k	0.407k	0.204k
128	3.26k	1.63k	0.814k	0.407k
64	6.51k	3.26k	1.63k	0.814k

(*) Design guarantee.

(18) Please do not absolutely use the “Not used” code. It will be the cause of failure.

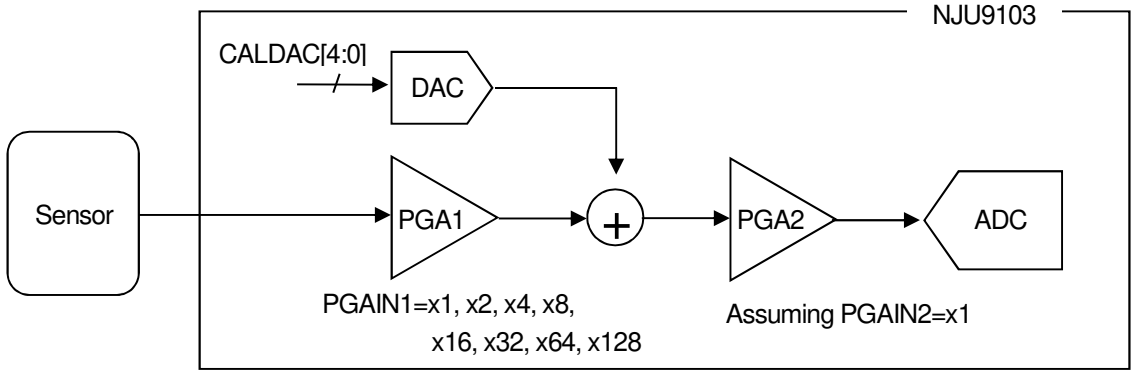
DACCONF Register Register Address: 0x5

DACCONF								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	CALDACEN	CALDAC [4:0]				
R / W	-	-	RW	RW				
RESET	-	-	0	0x00				

BIT	BIT NAME	FUNCTION
[5]	CALDACEN	Setting ON/OFF of DAC 0: OFF (Power down) 1: ON
[4:0]	CALDAC(19)	The sensor offset is corrected to add or subtract the DAC voltage from the output PGA1. CALDAC is a signed 5-bit code, MSB is the sign bit.

(19) NJU9103 contains internal calibration DAC.
When the gain of NJU9103 is large and the offset of sensor is 10mV, the data conversion does not work correctly by the constraints of the D-range of the analog circuit. To correct this, DAC will generate a voltage opposite to offset voltage of the sensor.

A simplified block diagram of the input section of the NJU9103 is shown below.

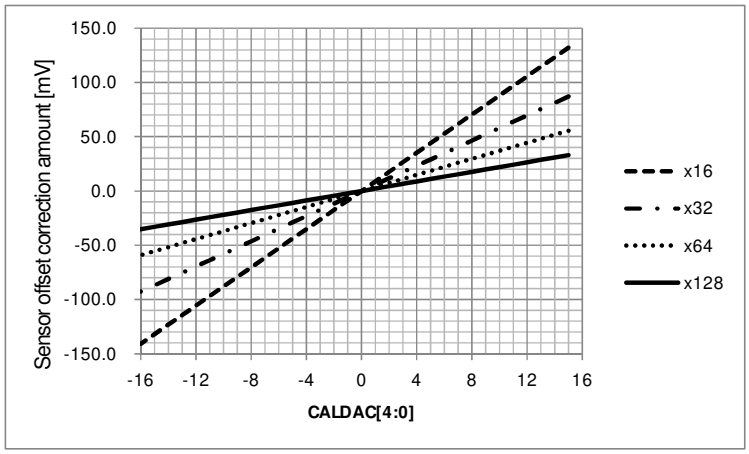


The correction range and resolution (voltage step) of sensor are changed by PGA1 gain.
It can be derived by the following equation.

"Sensor offset correction value" = "Resolution" x CALDAC[4:0]

(Note) Design assurance at VDD = 3.3V.
The variation of the resolution (error) is about ± 15%.

PGAIN1	Resolution[mV]
x16	8.8
x32	5.8
x64	3.7
x128	2.2



OPTION0 Register Register Address: 0x6

OPTION0								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	CHIPID [6:0]							AUTOSLP
R / W	R							RW
RESET	0x00							0

BIT	BIT NAME	FUNCTION
[7:1]	CHIPID	Used to identify the chip.
[0]	AUTOSLP	Wen MODE[3:0] is idle (0x0), set to ON / OFF of analog block 0: ON (Wait) 1 : OFF (Power down) When the customer change AUTOSLP from 1to 0, conversion start is necessary to start-up time of the analog block.

GAIN0 / GAIN1 / GAIN2 Register Register Address: 0x8, 0x9, 0xA

	GAIN0								GAIN1								GAIN2							
	Register Address: 0x8								Register Address: 0x9								Register Address: 0xA							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
BIT NAME	GAIN [23:0]																							
R / W	RW																							
RESET	0x01								0x00								0x00							

BIT	BIT NAME	FUNCTION
GAIN0 [7:0] + GAIN1 [7:0] + GAIN2 [7:0]	GAIN [23:0]	Gain coefficient derived in gain calibration or the external writing gain coefficient. 18-bit unsigned coefficient, GAIN [23:18] is always "0". The customer can do the external writing gain coefficient, when internal clock is active only. Please set to "0" AUTOSLP bit of OPTION0 register.

OFFSET0 / OFFSET1 / OFFSET2 Register Register Address: 0xB, 0xC, 0xD

	OFFSET0								OFFSET1								OFFSET2							
	Register Address: 0xB								Register Address: 0xC								Register Address: 0xD							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
BIT NAME	OFFSET [23:0]																							
R / W	RW																							
RESET	0x00								0x00								0x00							

BIT	BIT NAME	FUNSTION
OFFSET0 [7:0] + OFFSET1 [7:0] + OFFSET2 [7:0]	OFFSET [23:0]	Offset coefficient derived in offset calibration or the external writing offset coefficient. 20-bit signed coefficient, OFFSET [23:20] is sign-extended value. (20) The customer can do the external writing offset coefficient, when internal clock is active only. Please set to "0" AUTOSLP bit of OPTION0 register.

(20) Sign-extended: If the sign is (-) fill the 1 in the free space. If the sign is (+) fill the "0" in the free space

- In the case of -4 in decimal 8- bit is “11111100”.
  16-bit sign extension is “11111111 11111100”.
- In the case of +4 in decimel 8-bit is “00000100”
  16-bit sign extension is “00000000 00000100”

■ APPLICATION NOTE / GLOSSARY

■ Power up sequence

When the power supply is started, the reset cancellation is valid.
After a reset cancellation, the circuit will start operating.

The time from the reset cancellation to the operation start state is required waiting time of about 30μs.
(The rise time of power signal is not included.)

■ Effective resolution, Noise Free Bit (NFB)

Data Rate (DR) is speed at the time of single conversion (1 settling).
Output code variation σ is the effective resolution in the VINP and VINN connected to VDD/2, 6.6σ is the NFB.

< Condition >

- FMOD=1.25MHz
- VDD=3.3V, GND=0V
- VREF=3.3V
- Differential input
- T_a=+25°C

DR vs. Effective resolution (Unit: bit)

DR [sps]	PGA OFF	PGA ON									
		x1	x2	x4	x8	X16	x32	x64	x128	x256	x512
0.814k	16	16	16	16	16	16	16	16	15.5	15	14
1.63k	16	16	16	16	16	16	16	16	15	14	13
3.26k	15.5	15.5	15.5	15.5	15.5	15.5	15.5	15.5	14.5	13.5	12.5
6.51k	14	14	14	14	14	14	14	14	13.5	13	11.5

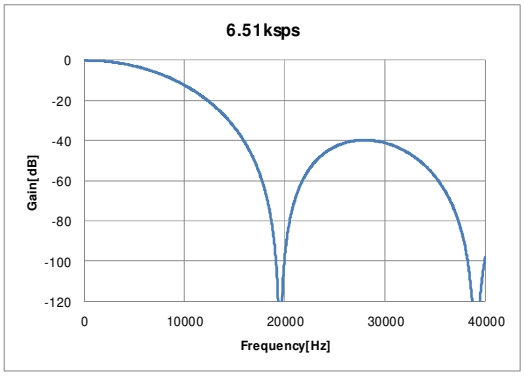
DR vs. NFB (Unit: bit)

DR [sps]	PGA OFF	PGA ON									
		x1	x2	x4	x8	x16	x32	x64	x128	x256	x512
0.814k	15	15	15	15	14.5	14.5	14.5	13.5	13	12	11
1.63k	14	14	14	14	14	14	14	13.5	12.5	11.5	10.5
3.26k	13	13	13	13	13	13	13	12.5	12	11	10
6.51k	11	11	11	11	11	11	11	11	11	10	9

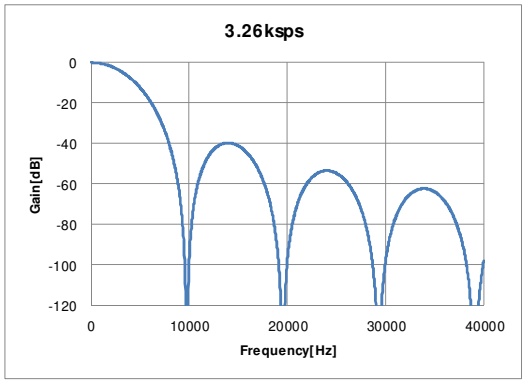
■ Digital filter frequency characteristic

The output of the ΔΣ modulator is converted to a digital value of high resolution by a digital filter (third-order Sinc filter). Frequency characteristics will change depending on the data rate.

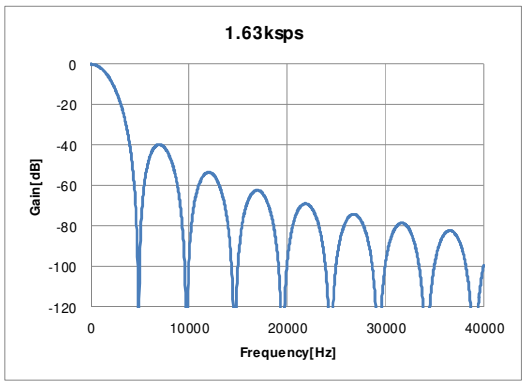
When the conversion data rate (DR) is 6.51ksps, 3.26ksps, 1.63ksps, 0.814ksps, frequency characteristics of the digital filter is shown below. Characteristic is the case of FMOD=1.25MHz.



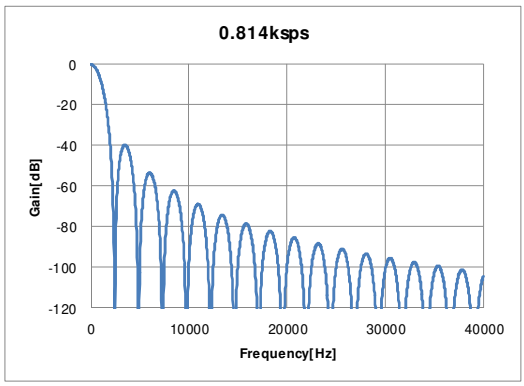
DR=6.51ksps



DR=3.26ksps



DR=1.63ksps



DR=0.814ksps

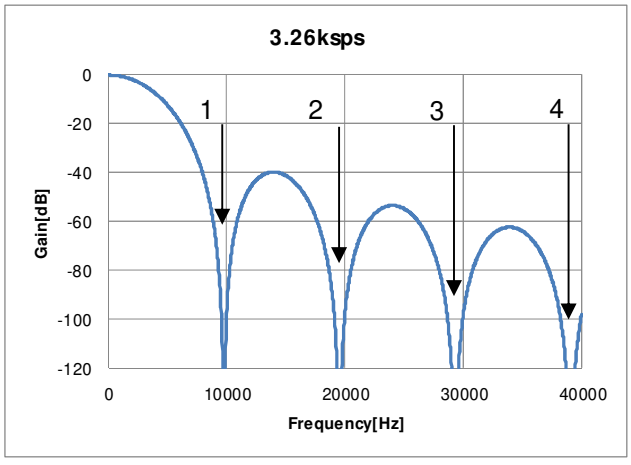
It has a first notch in the frequency of the data rate x 3.
Or later, it has a notch to the integer multiple of the position.(21)

(e.x.) In the case 3.26ksps (Figure of right)
Position of the notch

1. 9.8kHz (3.26kHz x 3 x 1)
2. 19.6kHz (3.26kHz x 3 x 2)
3. 29.3kHz (3.26kHz x 3 x 3)
4. 39.1kHz (3.26kHz x 3 x 4)

.
.

(N) 3.26kHz x 3 x N (N is an integer)

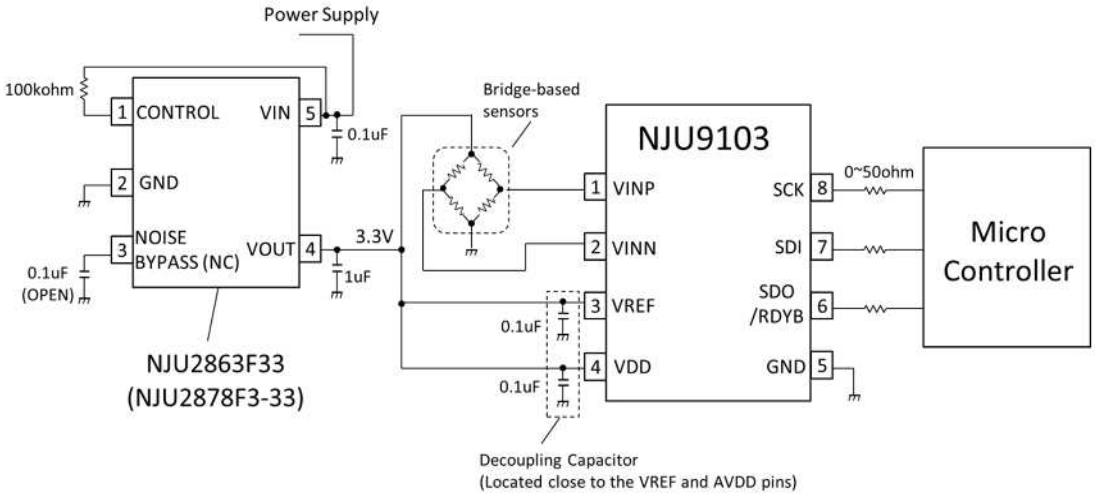


DR=3.26ksps

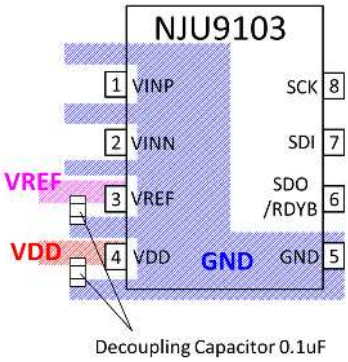
(21) Position of the notch varies in proportion to the frequency of the FMOD
FMOD is ±25% variation. Position of the notch is likely to vary ±25% from the above figure.

■ System Example

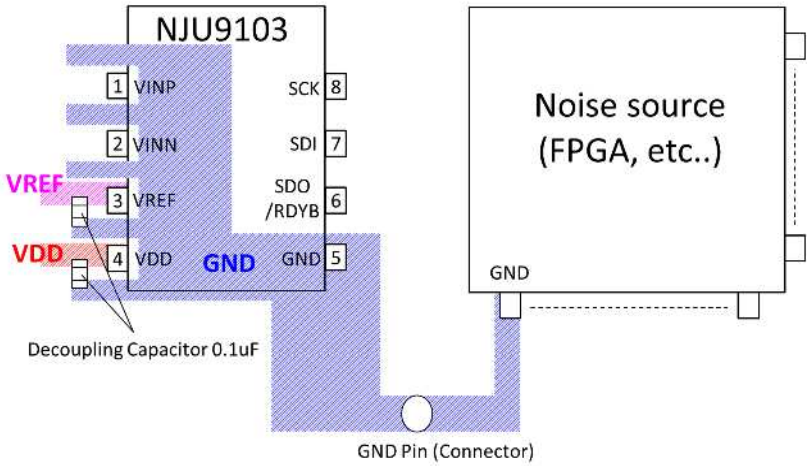
An example of an application that uses the bridge sensor is shown below.
In order to draw the best performance of Analog-to-Digital Converter (ADC), the customer is careful about the printed circuit board (PCB) layout pattern and a bypass capacitor placement.



The PCB layout pattern example of NJU9103 is shown below.
GND of decoupling capacitor and GND of NJU9103 make to equipotential as much as possible.



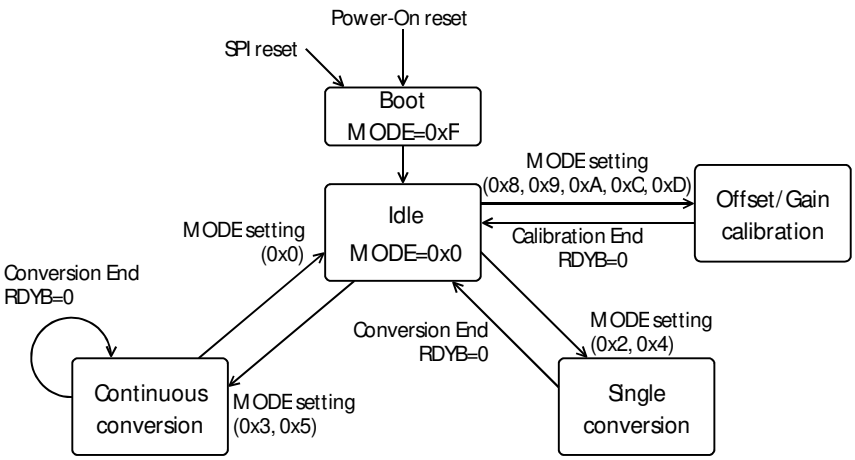
If the noise source and the NJU9103 is mounted on the same PCB, GND of the noise source and GND of NJU9103 separate until just before the GND Pin (connector).



■ Conversion Control

Set the conversion operation by MODE [3: 0] bit of CTRL register.

MODE[3:0]	OPERATION
0x0	Idle
0x1	Not used
0x2	Single conversion
0x3	Continuous conversion
0x4	Single conversion + CHOP
0x5	Continuous conversion + CHOP
0x6, 0x7	Not used
0x8	Calibration ADC offset
0x9	Calibration ADC gain
0xA	Calibration PGA offset
0xB	Not used
0xC	Calibration system offset
0xD	Calibration system gain
0xE	Not used
0xF	Boot



< Definition of time >

(1) ADC conversion time of basic : T_{adc}

$$T_{adc} = OSR / FMOD$$

OSR : Over Sampling Rate
FMOD : Clock Frequency of ADC

(2) Calculation time for data correction (after ADC conversion) : T_{cal}

$$T_{cal} = 40 / FOSC$$

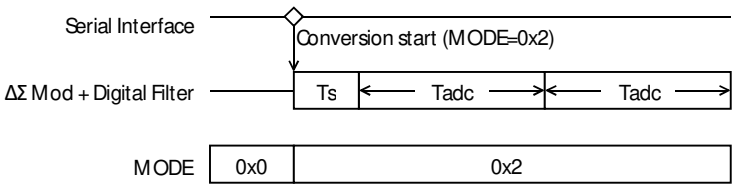
FOSC : Clock Frequency of Internal Oscillator

(3) Calculation time for gain coefficient (after gain calibration) : T_{div}

$$T_{div} = 70 / FOSC$$

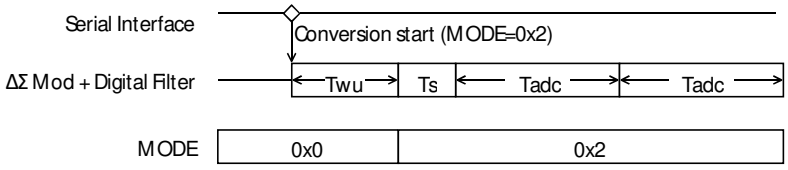
(4) Setup time : T_s

When the analog block is ON (AUTOSLP bit of OPTION 0 register = "0"), setting the MODE [3: 0] bit in CTRL register to operation mode starts operation after Ts (about 10µs). The case where the MODE [3: 0] bit is switched from "sleep (0x0)" to "single conversion (0x2)" is shown below.



(5) Startup wait time : T_{wu}

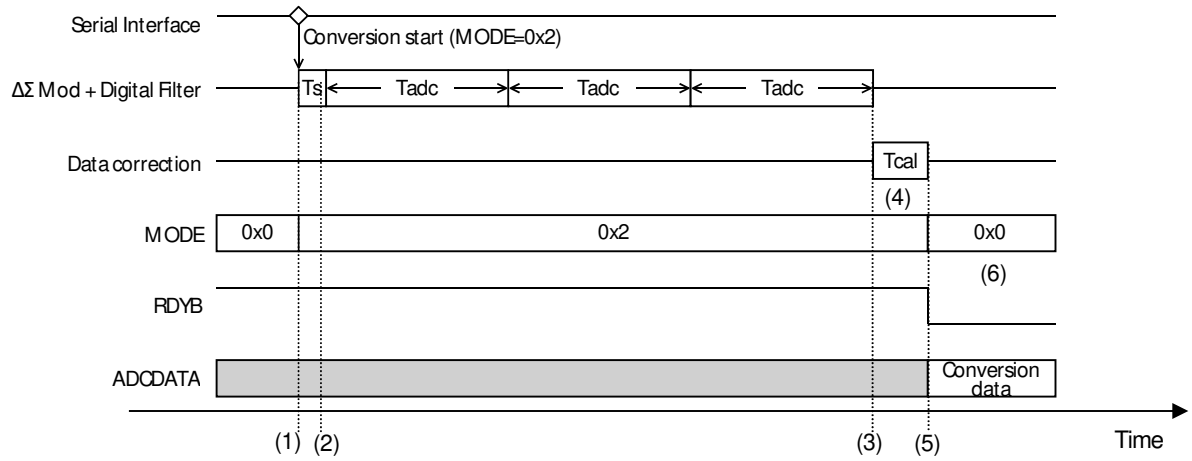
Waiting time of Twu (about 70µs) is required when changing the analog block from OFF to ON (AUTOSLP bit from "1" to "0"). The figure below shows the case where the MODE [3: 0] bit is switched from "sleep (0x0)" to "single conversion (0x2)".



1. Single Conversion operation (MODE[3:0] = 0x2)

It is the basic conversion of NJU9103.
Even if the input signal is switched by the multiplexer (external), waiting time for converted data is unnecessary.
(1 settling, zero latency)

When the conversion cycle is long, the recommended usage is that converting once and power-down the remaining period. So, the consumption current of NJU9103 can be reduced. It is the optimum conversion method for "switching input signals with multiplexer" and "low power consumption".



STEP	DETAILS
(1)	Set to single conversion. (MODE [3: 0] bit in CTRL register = "0x2")
(2)	After the set-up time (Ts), start the conversion.
(3)	Conversion completed with conversion time (3 x Tadc). The conversion data is the result of the convolution integration of 3 x Tadc. (ΔΣ Mod + Digital Filter)
(4)	Data is corrected with calculation time (Tcal).
(5)	Conversion data stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	Shift to Idle state. (MODE[3:0] bit= "0x0")

In NJU9103, the data rate is specified by the following formula. (Single conversion)

$$DR = F_{OSC} \times \frac{1}{OSR} \times \frac{1}{2^{(CLKDIV+1)}} \times \frac{1}{3}$$

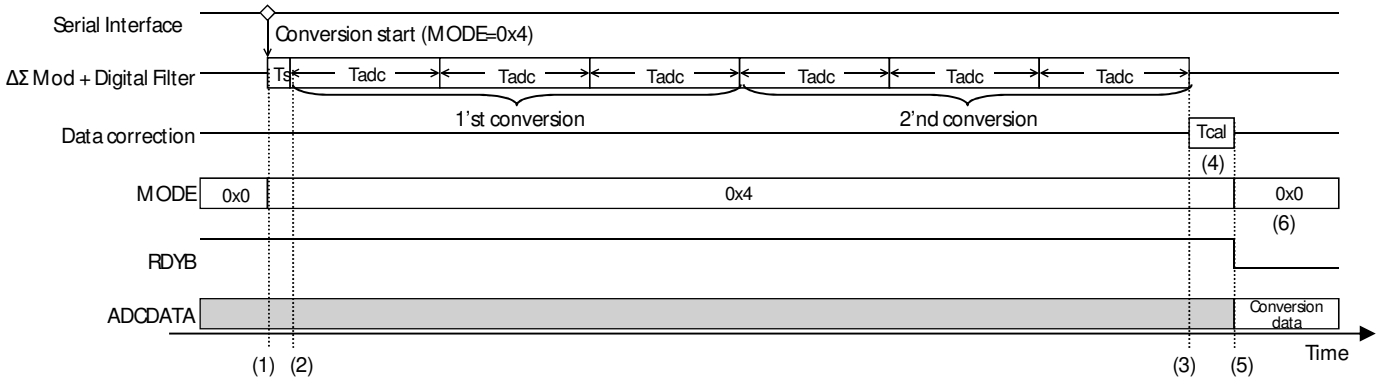
The conversion data rate (DR) is DR_all when Ts and Tcal are considered. (In the table below, CLKDIV=0)

OSR	DR [sps]	3xTadc(=1/DR) [s]	3xTadc+Ts+Tcal [s]	DR_all (=1/(3xTadc+Ts+Tcal)) [sps]
512	0.814k	1.23m	1.26m	0.794k
256	1.63k	0.614m	0.640m	1.56k
128	3.26k	0.307m	0.333m	3.00k
64	6.51k	0.154m	0.180m	5.56k

2. "Single conversion + CHOP" operation (MODE[3:0] = 0x4)

Single conversion performs single conversion twice. By change VINP and VINN at the second conversion, the NJU9103 offset can be removed in real time. The change of VINP and NINN is done automatically by the internal switch.

With single conversion, it is the optimum conversion method for "when you want to calibrate the offset in real time". Though, the data rate is half of single conversion.

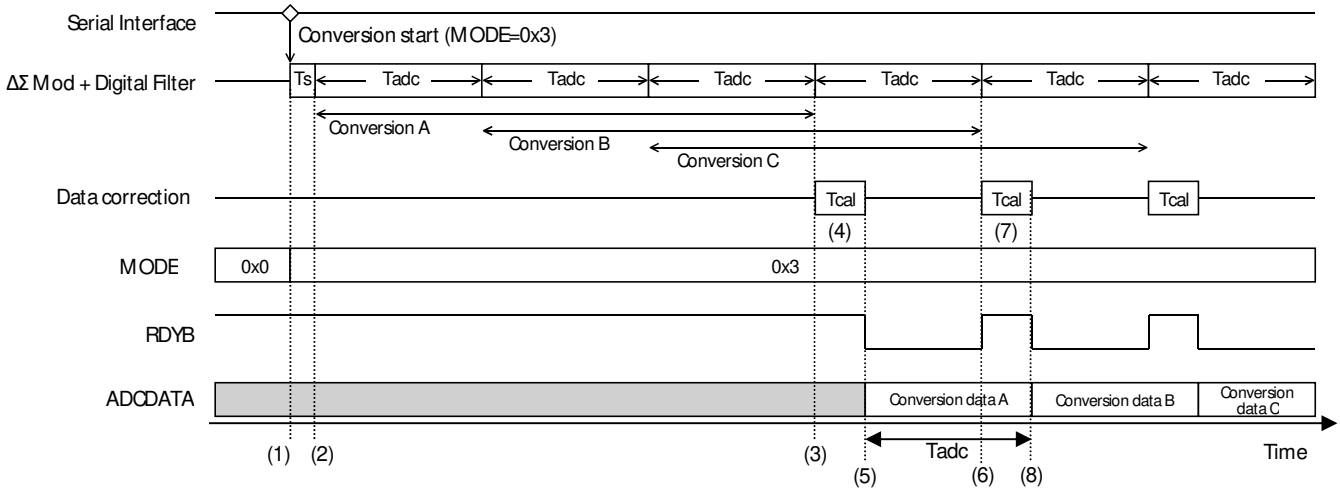


STEP	DETAILS
(1)	Set to single conversion + CHOP. (MODE [3: 0] bit in CTRL register = "0x4")
(2)	After the set-up time (Ts), start the conversion.
(3)	Conversion completed in conversion time (6 x Tadc). The conversion data is the result of the convolution integration of 6 x Tadc. (1'st & 2'nd conversion of "ΔΣ Mod + Digital Filter".)
(4)	Data is corrected in calculation time (Tcal).
(5)	Conversion data stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	Shift to Idle state. (MODE[3:0] bit= "0x0")

3. Continuous conversion operation (MODE[3:0] = 0x3)

When input signals are switched by the multiplexer, the same waiting time as the first conversion (conversion A) is required. When input signal is not switched by multiplexer, wait time after the second conversion (conversion B) is unnecessary.

It is the optimum conversion method for "when input is not switched by multiplexer" and "when you want to maximize data rate". The data rate is three times that of single conversion.



STEP	DETAILS
(1)	Set to continuous conversion. (MODE [3: 0] bit in CTRL register = "0x3")
(2)	After the set-up time (Ts), start the conversion.
(3)	Conversion A (1'st) completed in conversion time (3 x Tadc). The conversion data A is the result of the convolution integration of conversion A ("3 x Tadc" of ΔΣ Mod + Digital Filter")
(4)	Data is corrected in calculation time (Tcal)
(5)	Conversion data A (1'st) stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	After completion of conversion B (2'nd), RDYB bit changes from "0" to "1". The conversion data B is the result of the convolution integration of conversion B ("3 x Tadc" of ΔΣ Mod + Digital Filter)
(7)	Data is corrected in calculation time (Tcal).
(8)	Conversion data B (2'nd) stored (overwrite) in ADCDATA register. At that time, RDYB bit changes from "1" to "0".

Repeat steps (5) to (8) until the operation mode is set to idle (MODE [3: 0] bit is set to "0x0").

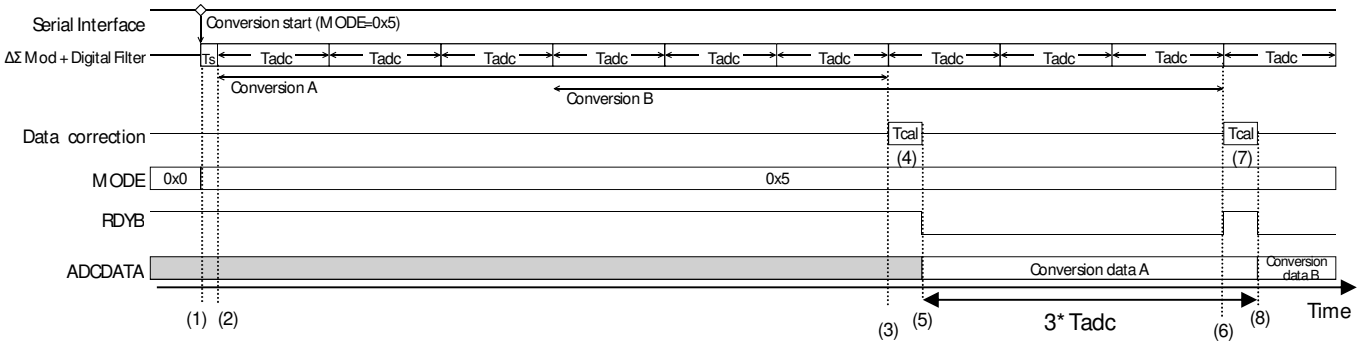
4. "Continuous conversion + CHOP" operation (MODE[3:0] = 0x5)

By changing VINP and VINN every "3 x Tadc", the NJU9103 offset can be removed in real time. The change of VINP and VINN is done automatically by the internal switch.

When input signals are switched by the multiplexer, the same waiting time as the first conversion (conversion A) is required. When input signal is not switched by multiplexer, wait time after the second conversion (conversion B) is unnecessary.

As with "single conversion + CHOP" operation, offset of whole chip can be calibrated in real time.

It is the optimal conversion method for "when you want to calibrate offsets in real time" with continuous conversion. Though, the data rate is 1/3 of continuous conversion. (Same data rate as single conversion)



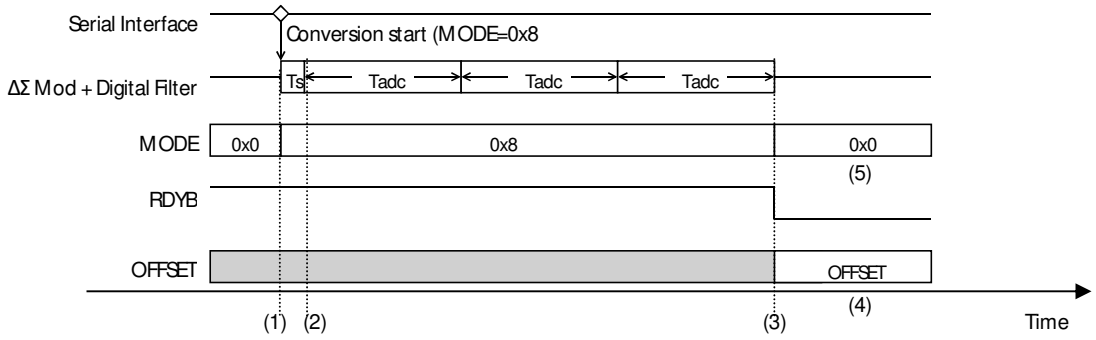
STEP	DETAILS
(1)	Set to continuous conversion + CHOP. (MODE [3: 0] bit in CTRL register = "0x5")
(2)	After the set-up time (Ts), start the conversion.
(3)	Conversion A (1'st) completed in conversion time (6 x Tadc). The conversion data A is the result of the convolution integration of conversion A ("6 x Tadc" of ΔΣ Mod + Digital Filter")
(4)	Data is corrected in calculation time (Tcal).
(5)	Conversion data A (1'st) stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	After completion of conversion B (2'nd), RDYB bit changes from "0" to "1". The conversion data B is the result of the convolution integration of conversion B ("6 x Tadc" of ΔΣ Mod + Digital Filter)
(7)	Data is corrected in calculation time (Tcal).
(8)	Conversion data B (2'nd) stored (overwrite) in ADCDATA register. At that time, RDYB bit changes from "1" to "0".

Repeat steps (5) to (8) until the operation mode is set to idle (MODE [3: 0] bit is set to "0x0").

5. Offset calibration operation (MODE[3:0] = 0x8, 0xA, 0xC)

Timing is almost the same as single conversion operation.

Calculate the offset amount and save it in the OFFSET register (OFFSET0, OFFSET1, and OFFSET2).



STEP	DETAILS
(1)	Set to offset calibration. (MODE [3: 0] bit in CTRL register = 0x8 or 0xA or 0xC)
(2)	After the set-up time (Ts), start the conversion.
(3)	Conversion is complete in conversion time (3 xTadc).
(4)	Conversion data stored in OFFSET register (OFFSET0, OFFSET1, OFFSET2). At that time, RDYB bit changes from "1" to "0".
(5)	Shift to Idle state. (MODE[3:0] bit= ”0x0”)

The NJU 9103 supports the following three types of offset calibration operation.

A. Internal offset calibration (MODE[3:0] = 0x8)

When the internal offset calibration command is executed, the following processing is automatically performed.

- Set PGA1 to OFF and set the PGA2 gain to “x1”.
- Applying GND internally to IN^+ and IN^- of the ADC to calculate the offset.
- Store calculated offset in OFFSET registers.

B. PGA1 offset calibration (MODE[3:0] = 0xA)

Set the gain of PGA1 and PGA2 before executing the PGA1 offset calibration command.

When the PGA1 offset calibration command is executed, the following processing is automatically performed.

- Connect VINN to the plus and minus inputs of PGA 1 and calculate the offset.
- Store calculated offset in OFFSET registers.

C. System offset calibration (MODE[3:0] = 0xC)

CHSEL [2: 0] bit selects the input channel.

When the system offset calibration command is executed, the following processing is automatically performed.

- Calculate the offset using the input channel selected with the CHSEL [2: 0] bits.
- Store calculated offset in OFFSET registers.