Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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NLAS5223B, NLAS5223BL

Ultra-Low 0.35 Ω Dual SPDT Analog Switch

The NLAS5223B is an advanced CMOS analog switch fabricated in Sub−micron silicon gate CMOS technology. The device is a dual Independent Single Pole Double Throw (SPDT) switch featuring Ultra−Low R_{ON} of 0.35 Ω, at V_{CC} = 4.3 V.

The part also features guaranteed Break Before Make (BBM) switching, assuring the switches never short the driver.

Features

- Ultra−Low R_{ON}, 0.35 Ω (typ) at V_{CC} = 4.3 V
- NLAS5223B Interfaces with 2.8 V Chipset
- NLAS5223BL Interfaces with 1.8 V Chipset
- Single Supply Operation from 1.65−4.5 V
- Full 0−V_{CC} Signal Handling Capability
- High Off−Channel Isolation
- Low Standby Current, < 50 nA
- Low Distortion
- R_{ON} Flatness of 0.15 Ω
- High Continuous Current Capability
  - ±320 mA Through Each Switch
- Large Current Clamping Diodes at Analog Inputs
  - ±100 mA Continuous Current Capability
- Package:
  - 1.4 x 1.8 x 0.75 mm WQFN10 Pb−Free
  - 1.4 x 1.8 x 0.55 mm UQFN10 Pb−Free
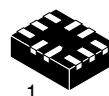- These are Pb−Free Devices

Applications

- Cell Phone Audio Block
- Speaker and Earphone Switching
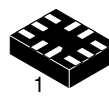- Ring−Tone Chip/Amplifier Switching
- Modems

MARKING DIAGRAM

WQFN10 CASE 488AQ

UQFN10 CASE 488AT
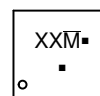
XX	= Specific Device Code
	AD = NLAS5223BMNR2G
	AE = NLAS5223BLMNR2G
	AP = NLAS5223BMUR2G
$\overline{M}$	= Date Code/Assembly Location
▪	= Pb−Free Device

(Note: Microdot may be in either location)
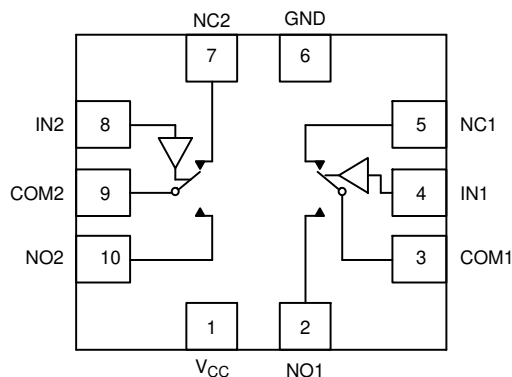
FUNCTION TABLE

IN 1, 2	NO 1, 2	NC 1, 2
0	OFF	ON
1	ON	OFF

ORDERING INFORMATION

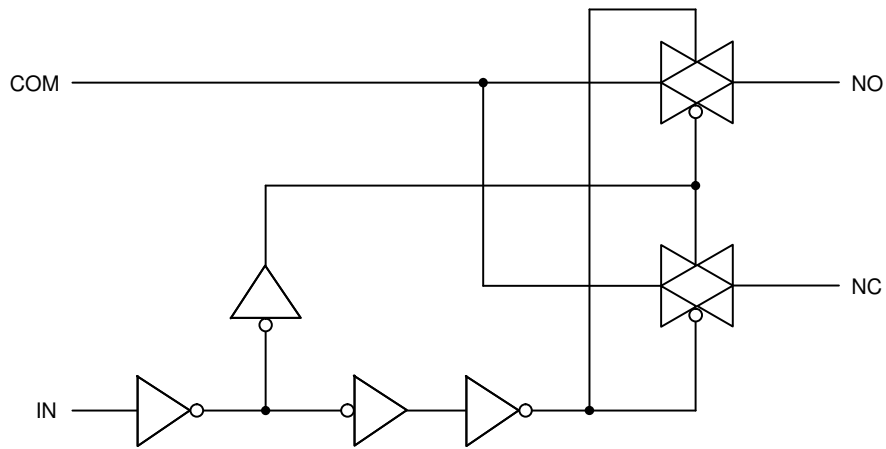See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

Figure 1. Logic Equivalent Circuit

PIN DESCRIPTION

QFN PIN #	Symbol	Name and Function
2, 5, 7, 10	NC1 to NC2, NO1 to NO2	Independent Channels
4, 8	IN1 and IN2	Controls
3, 9	COM1 and COM2	Common Channels
6	GND	Ground (V)
1	V_{CC}	Positive Supply Voltage

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage	−0.5 to +5.5	V
V_{IS}	Analog Input Voltage (V_{NO}, V_{NC}, or V_{COM})	$-0.5 \leq V_{IS} \leq V_{CC} + 0.5$	V
V_{IN}	Digital Select Input Voltage	$-0.5 \leq V_{IN} \leq +5.5$	V
I_{anl1}	Continuous DC Current from COM to NC/NO	±320	mA
$I_{anl-pk1}$	Peak Current from COM to NC/NO, 10% Duty Cycle, 100 ms = t_{ON} (Note 1)	±600	mA
$I_{anl-pk2}$	Instantaneous Peak Current from COM to NC/NO, 10% Duty Cycle, $t_{ON} < 1 \mu s$	±850	mA
I_{clmp}	Continuous DC Current into COM/NO/NC with Respect to V_{CC} or GND	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Defined as 10% ON, 90% OFF Duty Cycle.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	1.65	4.5	V
V_{IN}	Digital Select Input Voltage (OVT) Overvoltage Tolerance	GND	4.5	V
V_{IS}	Analog Input Voltage (NC, NO, COM)	GND	V_{CC}	V
T_A	Operating Temperature Range	−40	+85	°C
t_r, t_f	Input Rise or Fall Time, SELECT V_{CC} = 1.6 V – 2.7 V V_{CC} = 3.0 V – 4.5 V		20 10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NLAS5223B DC CHARACTERISTICS − DIGITAL SECTION (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit 25°C	Guaranteed Limit −40°C to +85°C	Unit
V_{IH}	Minimum High−Level Input Voltage, Select Inputs		3.0 4.3	1.4 2.0	1.4 2.0	V
V_{IL}	Maximum Low−Level Input Voltage, Select Inputs		3.0 4.3	0.7 0.8	0.7 0.8	V
I_{IN}	Maximum Input Leakage Current, Select Inputs	$V_{IN} = V_{CC}$ or GND	4.3	±0.1	±1.0	µA
I_{OFF}	Power Off Leakage Current	$V_{IN} = V_{CC}$ or GND	0	±0.5	±2.0	µA
I_{CC}	Maximum Quiescent Supply Current (Note 2)	Select and $V_{IS} = V_{CC}$ or GND	1.65 to 4.5	±1.0	±2.0	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

NLAS5223B DC ELECTRICAL CHARACTERISTICS − ANALOG SECTION

Symbol	Parameter	Condition	V_{CC}	25°C Min	25°C Max	−40°C to +85°C Min	−40°C to +85°C Max	Unit
R_{ON}	NC/NO On−Resistance (Note 3)	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$ $V_{IS} = $ GND to V_{CC} $I_{COM} = 100$ mA	3.0 4.3		0.4 0.35		0.5 0.4	Ω
R_{FLAT}	NC/NO On−Resistance Flatness (Notes 3 and 4)	$I_{COM} = 100$ mA $V_{IS} = 0$ to V_{CC}	3.0 4.3		0.16 0.11		0.20 0.14	Ω
ΔR_{ON}	On−Resistance Match Between Channels (Notes 3 and 5)	$V_{IS} = 1.5$ V; $I_{COM} = 100$ mA $V_{IS} = 2.2$ V; $I_{COM} = 100$ mA	3.0 4.3		0.05 0.05		0.05 0.05	Ω
$I_{NC(OFF)}$ $I_{NO(OFF)}$	NC or NO Off Leakage Current (Note 3)	$V_{IN} = V_{IL}$ or V_{IH} V_{NO} or $V_{NC} = 0.3$ V $V_{COM} = 4.0$ V	4.3	−5.0	5.0	−50	50	nA
$I_{COM(ON)}$	COM ON Leakage Current (Note 3)	$V_{IN} = V_{IL}$ or V_{IH} V_{NO} 0.3 V or 4.0 V with V_{NC} floating or V_{NC} 0.3 V or 4.0 V with V_{NO} floating $V_{COM} = 0.3$ V or 4.0 V	4.3	−10	10	−100	100	nA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.
4. Flatness is defined as the difference between the maximum and minimum value of On−resistance as measured over the specified analog signal ranges.
5. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$ between NC1 and NC2 or between NO1 and NO2.

NLAS5223BL DC CHARACTERISTICS – DIGITAL SECTION (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit		Unit
				25°C	–40°C to +85°C	
V_{IH}	Minimum High–Level Input Voltage, Select Inputs		3.0 4.3	1.3 1.6	1.3 1.6	V
V_{IL}	Maximum Low–Level Input Voltage, Select Inputs		3.0 4.3	0.5 0.6	0.5 0.6	V
I_{IN}	Maximum Input Leakage Current, Select Inputs	V_{IN} = 4.5 V or GND	4.3	±0.1	±1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 4.5 V or GND	0	±0.5	±2.0	μA
I_{CC}	Maximum Quiescent Supply Current (Note 6)	Select and V_{IS} = V_{CC} or GND	1.65 to 4.5	±1.0	±2.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

NLAS5223BL DC ELECTRICAL CHARACTERISTICS – ANALOG SECTION

Symbol	Parameter	Condition	V_{CC}	Guaranteed Maximum Limit				Unit
				25°C		–40°C to +85°C		
				Min	Max	Min	Max	
R_{ON}	NC/NO On–Resistance (Note 7)	V_{IN} = V_{IL} or V_{IN} = V_{IH} V_{IS} = GND to V_{CC} I_{COM} = 100 mA	3.0 4.3		0.4 0.35		0.5 0.4	Ω
R_{FLAT}	NC/NO On–Resistance Flatness (Notes 7 and 8)	I_{COM} = 100 mA V_{IS} = 0 to V_{CC}	3.0 4.3		0.16 0.11		0.20 0.14	Ω
ΔR_{ON}	On–Resistance Match Between Channels (Notes 7 and 9)	V_{IS} = 1.5 V; I_{COM} = 100 mA V_{IS} = 2.2 V; I_{COM} = 100 mA	3.0 4.3		0.05 0.05		0.05 0.05	Ω
$I_{NC(OFF)}$ $I_{NO(OFF)}$	NC or NO Off Leakage Current (Note 7)	V_{IN} = V_{IL} or V_{IH} V_{NO} or V_{NC} = 0.3 V V_{COM} = 4.0 V	4.3	–10	10	–100	100	nA
$I_{COM(ON)}$	COM ON Leakage Current (Note 7)	V_{IN} = V_{IL} or V_{IH} V_{NO} 0.3 V or 4.0 V with V_{NC} floating or V_{NC} 0.3 V or 4.0 V with V_{NO} floating V_{COM} = 0.3 V or 4.0 V	4.3	–10	10	–100	100	nA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
7. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.
8. Flatness is defined as the difference between the maximum and minimum value of On–resistance as measured over the specified analog signal ranges.
9. ΔR_{ON} = $R_{ON(MAX)}$ – $R_{ON(MIN)}$ between NC1 and NC2 or between NO1 and NO2.

NLAS5223B, NLAS5223BL

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	V_{IS} (V)	25°C			−40°C to +85°C		Unit
					Min	Typ*	Max	Min	Max	
t_{ON}	Turn−On Time	$R_L = 50\ \Omega$, $C_L = 35$ pF (Figures 3 and 4)	2.3 – 4.5	1.5			50		60	ns
t_{OFF}	Turn−Off Time	$R_L = 50\ \Omega$, $C_L = 35$ pF (Figures 3 and 4)	2.3 – 4.5	1.5			30		40	ns
t_{BBM}	Minimum Break−Before−Make Time	$V_{IS} = 3.0$ $R_L = 50\ \Omega$, $C_L = 35$ pF (Figure 2)	3.0	1.5	2	15				ns

		Typical @ 25, V_{CC} = 3.6 V	
C_{IN}	Control Pin Input Capacitance	3.5	pF
$C_{NO/NC}$	NO, NC Port Capacitance	60	pF
C_{COM}	COM Port Capacitance When Switch is Enabled	200	pF

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V_{CC} (V)	25°C Typical	Unit
BW	Maximum On−Channel −3 dB Bandwidth or Minimum Frequency Response	V_{IN} centered between V_{CC} and GND (Figure 5)	1.65 – 4.5	19	MHz
V_{ONL}	Maximum Feed−through On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 5)	1.65 – 4.5	−0.06	dB
V_{ISO}	Off−Channel Isolation	f = 100 kHz; $V_{IS} = 1$ V RMS; $C_L = 5.0$ pF V_{IN} centered between V_{CC} and GND (Figure 5)	1.65 – 4.5	−68	dB
Q	Charge Injection Select Input to Common I/O	$V_{IN} = V_{CC}$ to GND, $R_{IS} = 0\ \Omega$, $C_L = 1.0$ nF $Q = C_L \times DV_{OUT}$ (Figure 6)	1.65 – 4.5	38	pC
THD	Total Harmonic Distortion THD + Noise	$F_{IS} = 20$ Hz to 20 kHz, $R_L = R_{gen} = 600\ \Omega$, $C_L = 50$ pF $V_{IS} = 2.0$ V RMS	3.0	0.08	%
VCT	Channel−to−Channel Crosstalk	f = 100 kHz; $V_{IS} = 1.0$ V RMS, $C_L = 5.0$ pF, $R_L = 50\ \Omega$ V_{IN} centered between V_{CC} and GND (Figure 5)	1.65 – 4.5	−70	dB

10. Off−Channel Isolation = 20log10 (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to off switch.
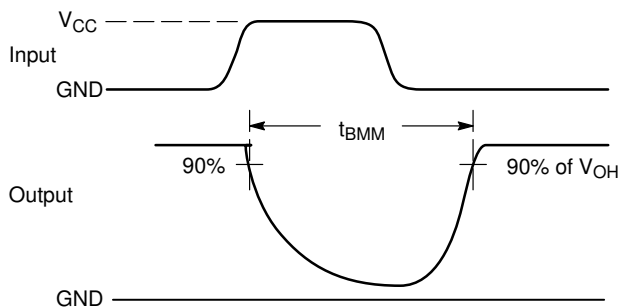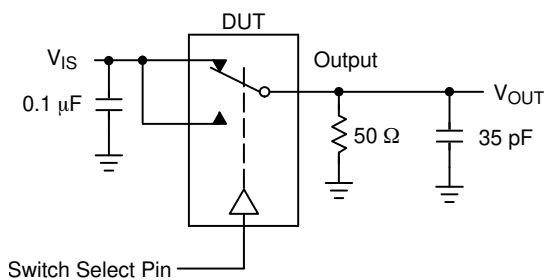
Figure 2. t$_{BBM}$ (Time Break−Before−Make)
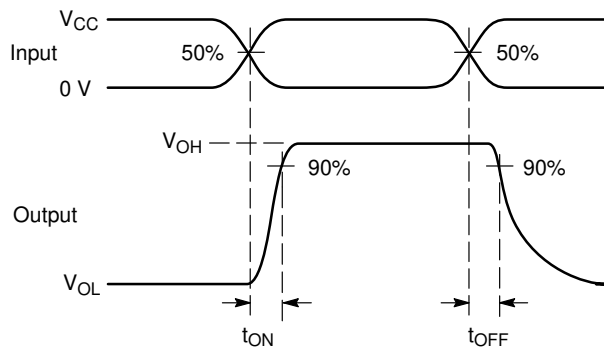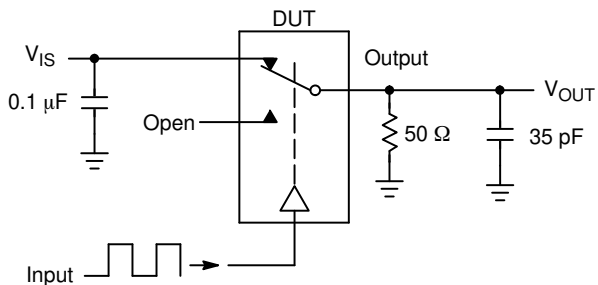
Figure 3. t$_{ON}$/t$_{OFF}$
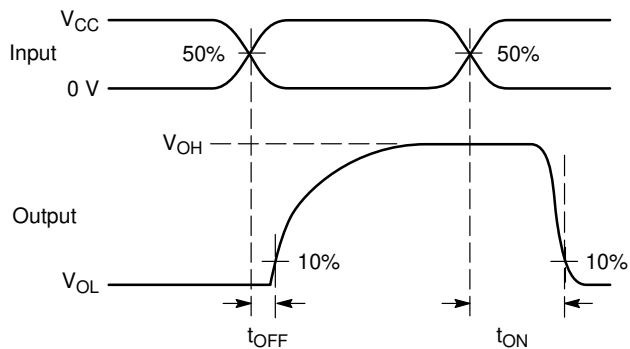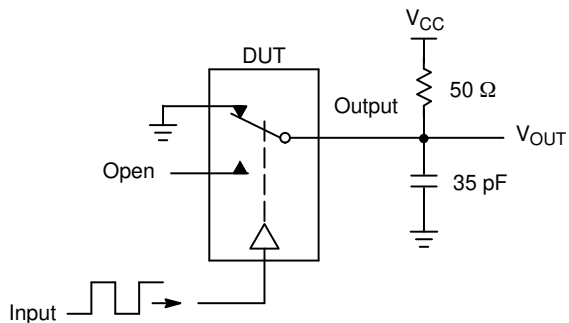
Figure 4. t$_{ON}$/t$_{OFF}$

NLAS5223B, NLAS5223BL
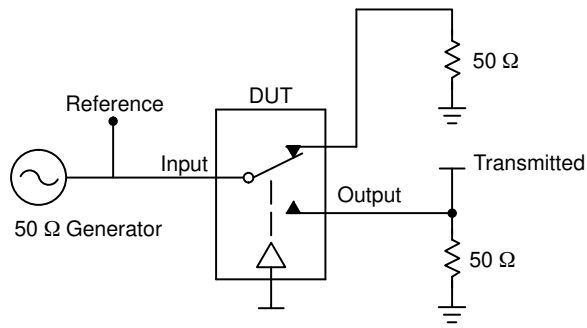
Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.
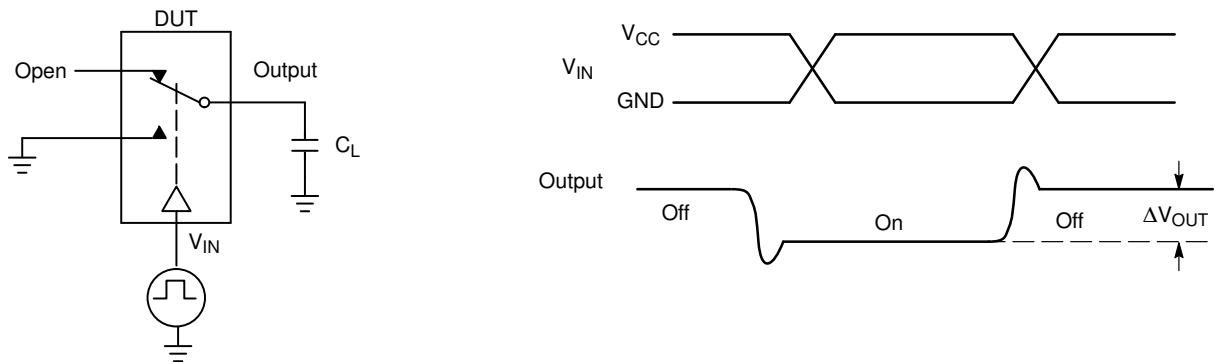
V_{ISO} = Off Channel Isolation = $20 \log\left(\dfrac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = $20 \log\left(\dfrac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

Figure 6. Charge Injection: (Q)
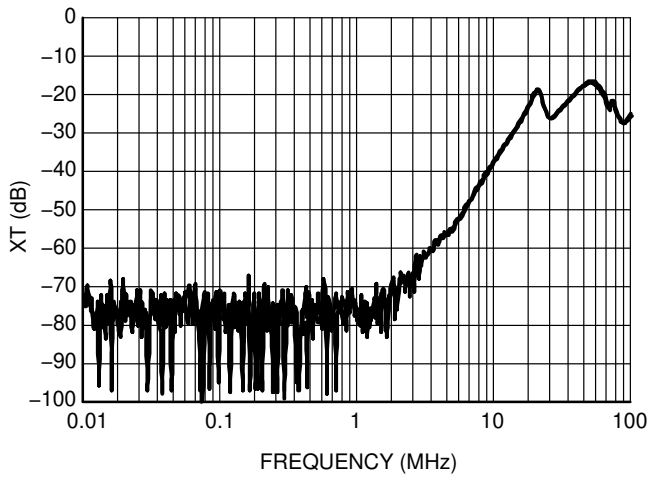
Figure 7. Cross Talk vs. Frequency
@ V_CC = 4.3 V
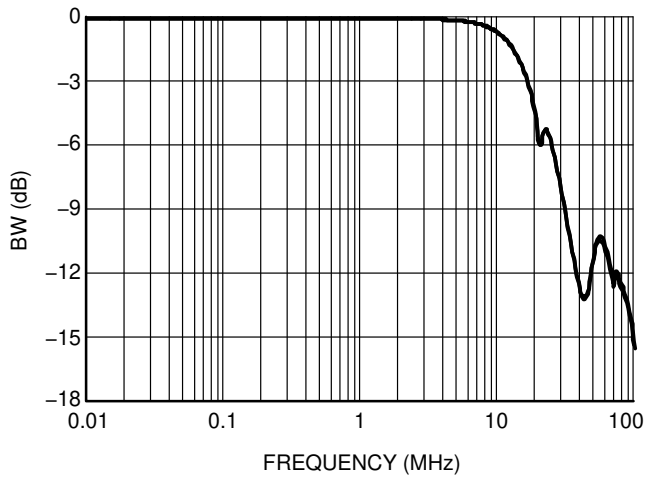
Figure 8. Bandwidth vs. Frequency
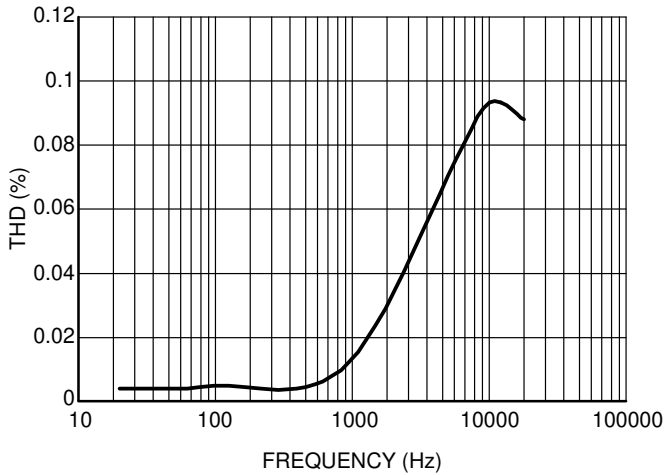
Figure 9. Total Harmonic Distortion
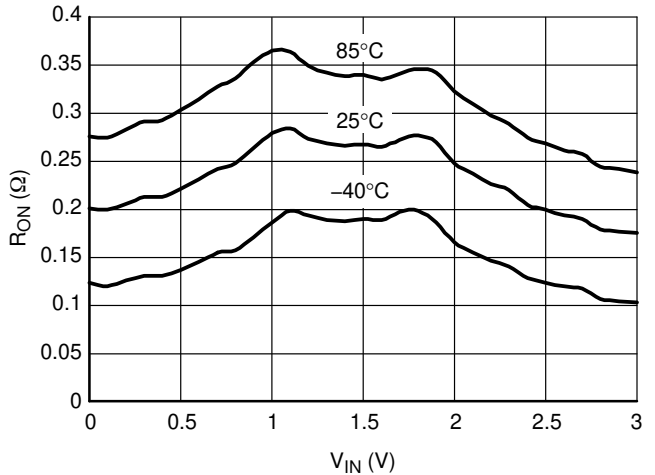
Figure 10. On−Resistance vs. Input Voltage
@ V_CC = 3.0 V
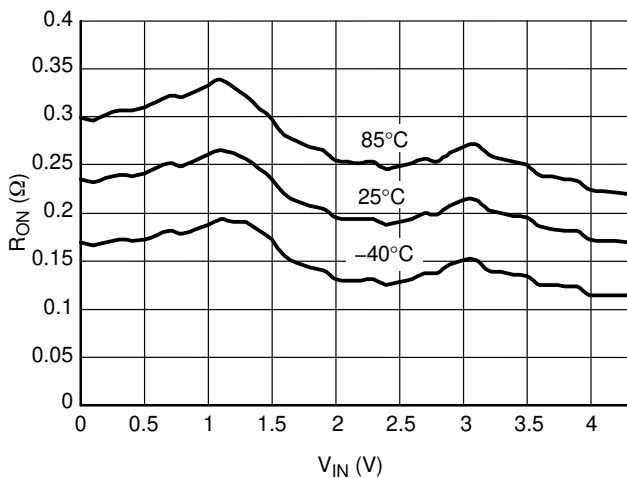
Figure 11. On−Resistance vs. Input Voltage
@ V_CC = 4.3 V
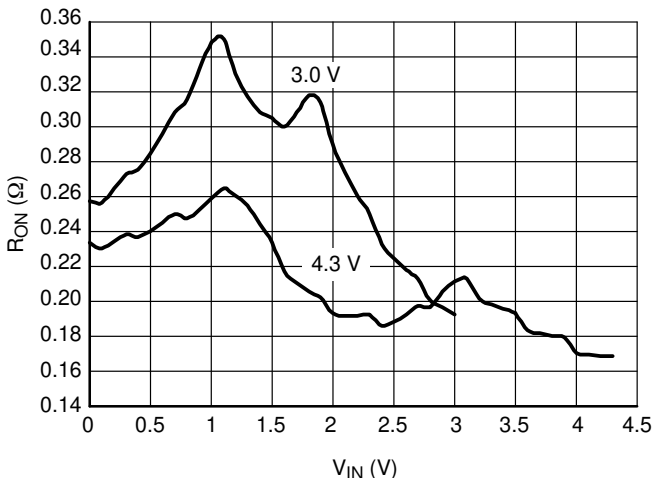
Figure 12. On−Resistance vs. Input Voltage

ORDERING INFORMATION

Device	Package	Shipping†
NLAS5223BMNR2G	WQFN10 (Pb−Free)	3000 / Tape & Reel
NLAS5223BLMNR2G	WQFN10 (Pb−Free)	3000 / Tape & Reel
NLAS5223BMUR2G	UQFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

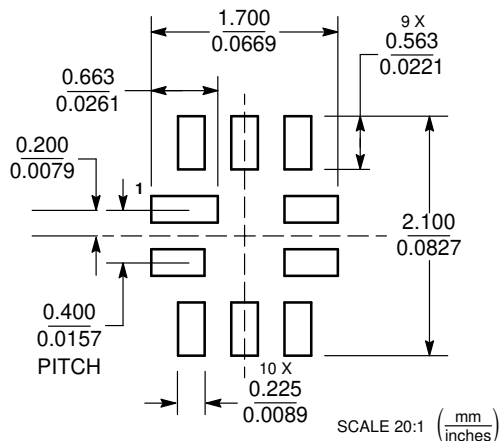## PACKAGE DIMENSIONS

WQFN10, 1.4x1.8, 0.4P
CASE 488AQ
ISSUE C
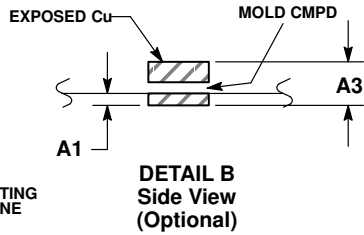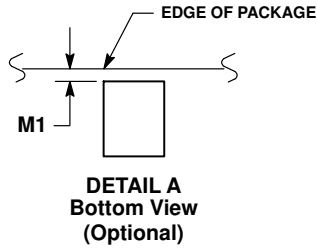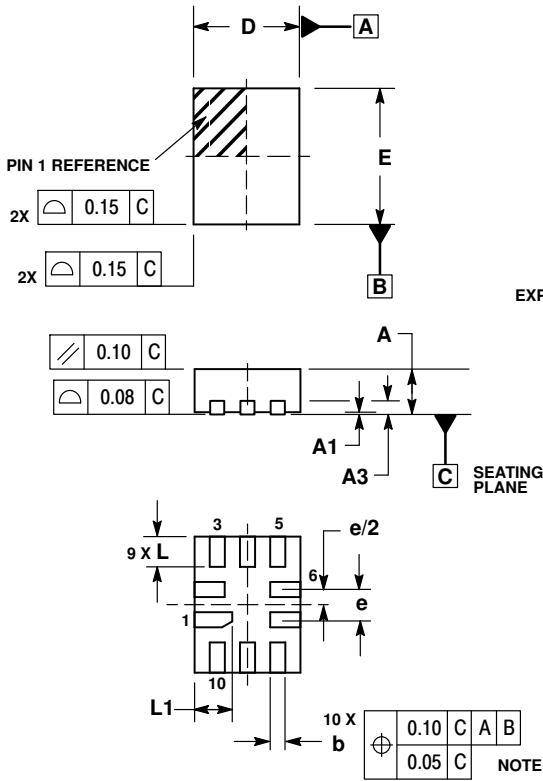
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.40	0.60
M1	0.00	0.05

DETAIL A
Bottom View
(Optional)

DETAIL B
Side View
(Optional)

EDGE OF PACKAGE

EXPOSED Cu   MOLD CMPD

PIN 1 REFERENCE

2X [⌒ | 0.15 | C]

2X [⌒ | 0.15 | C]

[⫽ | 0.10 | C]

[⌒ | 0.08 | C]

SEATING PLANE

9 X L

e/2

e

L1

10 X [⊕ | 0.10 | C | A | B]
[| 0.05 | C] NOTE 3

b

MOUNTING FOOTPRINT

1.700
0.0669

9 X
0.563
0.0221

0.663
0.0261

0.200
0.0079

2.100
0.0827

0.400
0.0157
PITCH

10 X
0.225
0.0089

SCALE 20:1 $\left(\dfrac{mm}{inches}\right)$
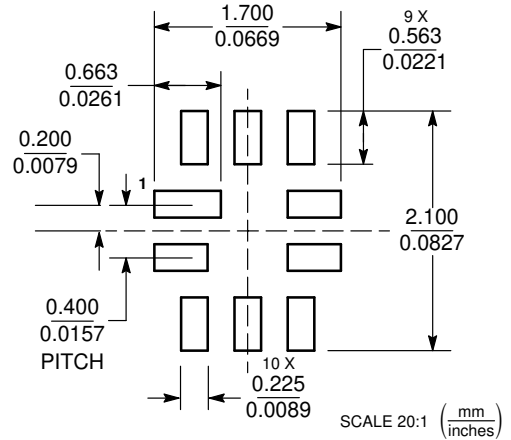
PACKAGE DIMENSIONS

UQFN10, 1.4x1.8, 0.4P
CASE 488AT
ISSUE A
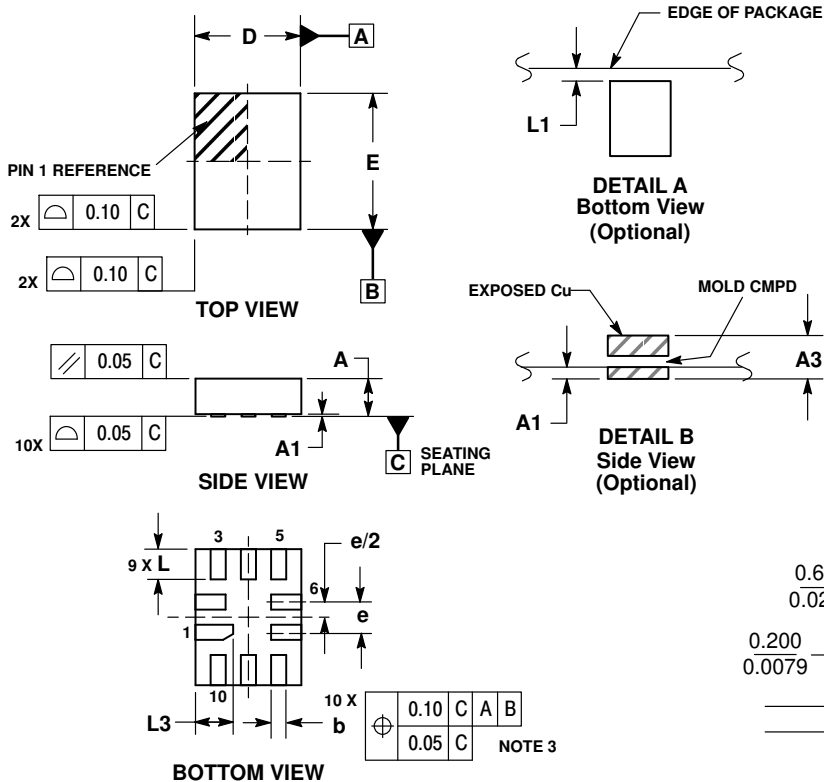
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

TOP VIEW

2X ⌒ 0.10 C
2X ⌒ 0.10 C

PIN 1 REFERENCE

DETAIL A
Bottom View
(Optional)

EDGE OF PACKAGE
L1

SIDE VIEW

⫽ 0.05 C
10X ⌒ 0.05 C

SEATING PLANE

DETAIL B
Side View
(Optional)

EXPOSED Cu
MOLD CMPD
A3
A1

BOTTOM VIEW

9 X L
e/2
e
L3
b

10 X | ⌖ | 0.10 | C | A | B |
| | 0.05 | C | |
NOTE 3

MOUNTING FOOTPRINT

1.700 / 0.0669
0.663 / 0.0261
0.200 / 0.0079
0.400 / 0.0157 PITCH
9 X 0.563 / 0.0221
2.100 / 0.0827
10 X 0.225 / 0.0089

SCALE 20:1 (mm / inches)

NLAS5223B/D