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Panasonic

NN31000A

http://www.semicon.panasonic.co.jp/en/

10 A Synchronous DC-DC Step down Regulator, Power Supply in Package (V_{IN} = 4.5 V to 28 V, V_{OUT} = 0.6 V to 5.5 V)

FEATURES

- High-Speed Response DC-DC Step Down Regulator Circuit that employs Hysteretic Control System
- Built-in inductor and capacitors
- Skip (discontinuous) Mode for high efficiency at light load
  Maximum Output Current : 10 A
- Input Voltage Range : PVIN=AVIN = 4.5 V to 28 V,
  Output Voltage Range : 0.6 V to 5.5 V
  Selectable Switching Frequency 400 kHz / 600 kHz / 800 kHz
- Built-in Feed Back Resistors for 1.0 V / 3.3 V default settings
  Configurable output voltage settings using external Resistors
- Adjustable Soft Start
- Low Operating and Standby Quiescent Current
- Open Drain Power Good Indication for Output Over / Under Voltage
- Selectable Auto recovery / latch off protection system
- Adjustable current limit threshold
- Built-in Under Voltage Lockout (UVLO),
  Thermal Shut Down (TSD), Under Voltage Detection (UVD),
  Over Voltage Detection (OVD), Short Circuit Protection (SCP)
  Over Current Protection (OCP)
- Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type, Size : 8.5 mm × 7.5 mm, 0.5 mm pitch)

DESCRIPTION

NN31000A is a synchronous DC-DC step down regulator (1-ch), Power Supply in Package (PSiP), which integrates a Controller IC that employs a hysteretic control system, two Power MOSFETs, an Inductor and Capacitors into a single 8.5 x 7.5 x 4.7mm QFN package.

The easiness of mounting PSiP onto a Printed Circuit Board (PCB), a very small footprint and a highly reduced number of external components, offers very compact and simplified solutions for applications requiring point-of-load design.

The number of external components have been reduced to only input/output capacitor, slow start capacitor and feedback resistors.

Furthermore, for applications requiring an output voltage of 1.0 V / 3.3 V, the external feedback resistors can be eliminated, resulting into even a smaller footprint.

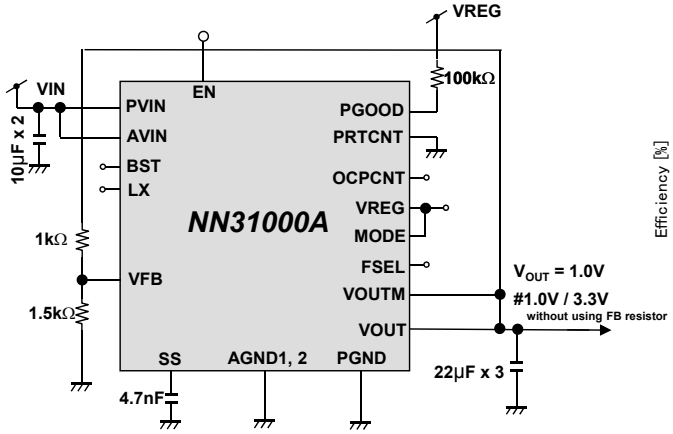
The PSiP achieves efficiencies of greater than 95 % with very good power dissipation capabilities.

APPLICATIONS

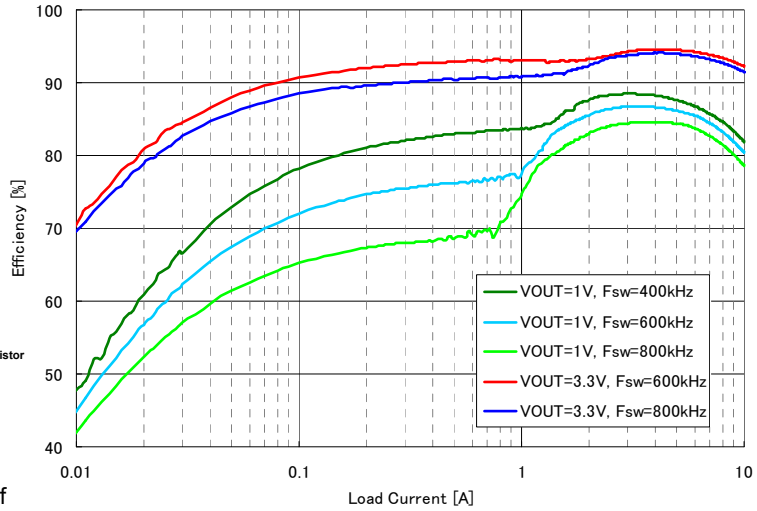
High Current Distributed Power Systems such as

- DSP and FPGA Point-of-Load Applications
- Routers
- Industrial Equipment
- Space constrained Applications etc.

SIMPLIFIED APPLICATION



Note : The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.



Condition :
Vin = 12 V, V_{OUT} Setting = 1.0 V / 3.3 V
Switching Frequency = 400 / 600 / 800 kHz, Skip mode
Co = 66 µF (22 µF x 3)

Established : 2014-07-03
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ORDERING INFORMATION

Order Number	Feature	Package	Output Supply
NN31000A-BB	Maximum Output Current : 10 A	57 pin HQFN	Emboss Taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{IN}	30	V	*1
Operating free-air temperature	T_{opr}	– 40 to + 85	°C	*2
Operating junction temperature	T_j	– 40 to + 150	°C	*2
Storage temperature	T_{stg}	– 55 to + 150	°C	*2
Input Voltage Range	V_{MODE},V_{FSEL},V_{OUTM},V_{PRTCNT} V_{OCPCNT},V_{FB}	– 0.3 to (V_{REG} + 0.3)	V	*1 *3
	V_{EN}	– 0.3 to 6.0	V	*1
Output Voltage Range	V_{PGOOD}	– 0.3 to (V_{REG} + 0.3)	V	*1 *3
	V_{LX}	– 0.3 to (V_{IN} + 0.3)	V	*1 *4
ESD	HBM	2	kV	—

Notes : This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range.

When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

V_{IN} is voltage for AVIN, PVIN. V_{IN} = AV_{IN} = PV_{IN}.

Do not apply external currents and voltages to any pin not specifically mentioned.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25 °C.

*3 :(V_{REG} + 0.3) V must not exceed 6 V.

*4 : (V_{IN} + 0.3) V must not exceed 30 V.

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POWER DISSIPATION RATING

Package	$\theta_{j\text{-}C}$	PD (Ta = 25 °C)	PD (Ta = 85 °C)	Notes
Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)	6.7 °C / W	3.49 W	1.82 W	*1
	5.7 °C / W	5.56 W	2.89 W	*2

Notes : For the actual usage, please follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1:Glass Epoxy Substrate (4 Layers) [50 × 50 × 0.8 t (mm)]

*2:Glass Epoxy Substrate (4 Layers) [50 × 50 × 1.57 t (mm)]

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage range	AV_{IN}	4.5	12	28	V	—
	PV_{IN}	4.5	12	28	V	—
Input Voltage Range	V_{MODE}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{FSEL}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{PRTCNT}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{EN}	– 0.3	—	5.0	V	—
Output Voltage Range	V_{PGOOD}	– 0.3	—	V_{REG} + 0.3	V	*1
	V_{LX}	– 0.3	—	V_{IN} + 0.3	V	*2

Notes : Voltage values, unless otherwise specified, are with respect to GND.

GND is voltage for AGND, PGND. AGND = PGND

V_{IN} is voltage for AVIN, PVIN. $V_{IN} = AV_{IN} = PV_{IN}$.

Do not apply external currents or voltages to any pin not specifically mentioned.

*1 : (V_{REG} + 0.3) V must not exceed 6 V.

*2 : (V_{IN} + 0.3) V must not exceed 30 V.

ELECTRICAL CHARACTERISTICS

C_O = 22 µF × 3, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V, Switching Frequency = 600 kHz
V_{MODE} = V_{REG} (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
Current Consumption at active1 (Skip mode)	$I_{VDDACTN1}$	I_{OUT} = 0 A, V_{FB} = 0.620 V R_{FB1} = 1.0 kΩ R_{FB2} = 1.5 kΩ V_{MODE} = 0 V, V_{EN} = 5 V	—	700	1200	µA	—
Current Consumption at active2 (FCCM)	$I_{VDDACTN2}$	V_{EN} = 5 V , I_{OUT} = 0 A R_{FB1} = 1.0 kΩ R_{FB2} = 1.5 kΩ V_{MODE} = V_{REG} V_{FSEL} = OPEN	—	15	23	mA	—
AVIN/PVIN Current Consumption at standby	I_{VINSTB}	AV_{IN} = PV_{IN} = 12 V V_{EN} = 0 V	—	2	5	µA	—
Logic Pin Characteristics							
EN pin Low-level input voltage	V_{ENL}	—	—	—	0.3	V	—
EN pin High-level input voltage	V_{ENH}	—	1.5	—	5.0	V	—
EN pin leakage current	I_{LEAKEN}	V_{EN} = 5 V	—	5	10	µA	—
MODE pin Low-level input voltage	V_{MODEL}	—	—	—	V_{REG} × 0.3	V	—
MODE pin High-level input voltage	V_{MODEH}	—	V_{REG} × 0.7	—	V_{REG}	V	—
MODE pin leakage current	I_{LEAKMD}	V_{MODE} = 5 V	—	12.5	25	µA	—
PRTCNT pin Low-level input voltage	V_{PRTL}	—	—	—	0.3	V	—
PRTCNT pin High-level input voltage	V_{PRTH}	—	V_{REG} – 0.3	—	—	V	—
PRTCNT pin leakage current	$I_{LEAKPRT}$	V_{EN} = 5 V, V_{PRTCNT} = 5 V	—	0	2	µA	—
FSEL pin Low-level input voltage	V_{FSELL}	—	—	—	0.3	V	—
FSEL pin High-level input voltage	V_{FSELH}	—	V_{REG} – 0.3	—	—	V	—
FSEL pin High leakage current	$I_{LEAKFSH}$	V_{FSEL} = 5 V	—	6.25	12.5	µA	—
FSEL pin Low leakage current	$I_{LEAKFSL}$	V_{FSEL} = 0 V	—	6.25	12.5	µA	—

Established : 2014-07-03
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ELECTRICAL CHARACTERISTICS (Continued)

C_O = 22 µF × 3, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V, Switching Frequency = 600 kHz
V_{MODE} = V_{REG} (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VREG Characteristics							
Output voltage	V_{REGO}	I_{VREG} = 5mA	5.3	5.6	5.9	V	—
Input voltage variation	V_{REGLIN}	V_{REGLIN} = V_{REG} (V_{IN} =12 V) -V_{REG} (V_{IN} =6 V) I_{VREG} = 5mA	—	—	150	mV	—
Drop out voltage	V_{REGDO}	V_{IN} = 4.5 V, I_{VREG} = 5mA	4.1	—	—	V	—
VFB Characteristics							
VFB comparator threshold	V_{FBTH}	—	0.594	0.600	0.606	V	—
VFB pin leakage current 1	$I_{LEAKFB1}$	V_{FB} = 0 V	– 1	—	1	µA	—
VFB pin leakage current 2	$I_{LEAKFB2}$	V_{FB} = 6 V	– 1	—	1	µA	—
Under Voltage Lock Out							
UVLO shutdown voltage	V_{UVLODE}	V_{IN} = 5 V to 0 V	3.97	4.10	4.23	V	—
UVLO wakeup voltage	V_{UVLORE}	V_{IN} = 0 V to 5 V	4.17	4.30	4.43	V	—
UVLO hysteresis	ΔV_{UVLO}	—	150	200	250	mV	—
PGOOD							
PGOOD Threshold 1 (VFB ratio for UVD detect)	V_{PGUV}	PGOOD : High to Low	77	85	93	%	—
PGOOD Hysteresis 1 (VFB ratio for UVD release)	ΔV_{PGUV}	PGOOD : Low to High	3.5	5.0	6.5	%	—
PGOOD Threshold 2 (VFB ratio for OVD detect)	V_{PGOV}	PGOOD : High to Low	107	115	123	%	—
PGOOD Hysteresis 2 (VFB ratio for OVD release)	ΔV_{PGOV}	PGOOD : Low to High	3.5	5.0	6.5	%	—
PGOOD start up delay time (After reached V_{FB} = 0.6 V)	T_{PGD}	—	0.4	1.0	1.6	ms	—
PGOOD ON resistance	R_{PG}	—	—	10	15	Ω	—

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ELECTRICAL CHARACTERISTICS (Continued)

C_O = 22 µF × 3, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V, Switching Frequency = 600 kHz
V_{MODE} = V_{REG} (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC Characteristics							
Output voltage 1	V_{o1}	R_{FB1} = 1.0 kΩ R_{FB2} = 1.5 kΩ V_{MODE} = V_{REG} I_{OUT} = 5 A	0.985	1.000	1.015	V	—
Output voltage 2	V_{o2}	R_{FB1} = 4.5 kΩ R_{FB2} = 1 kΩ V_{MODE} = V_{REG} I_{OUT} = 5 A	3.250	3.300	3.350	V	—
Output voltage 3	V_{o3}	V_{FB} = OPEN before V_{EN} = 0 V to 1.5 V V_{MODE} = V_{REG} I_{OUT} = 5 A	0.985	1.000	1.015	V	—
Output voltage 4	V_{o4}	V_{FB} = V_{REG} before V_{EN} = 0 V to 1.5 V V_{MODE} = V_{REG} I_{OUT} = 5 A	3.250	3.300	3.350	V	—
Efficiency 1	V_{EFF1}	PV_{IN} = 12 V V_{OUT} = 5 V, I_{OUT} = 4 A V_{FSEL} = V_{REG} (800kHz)	—	95	—	%	*1
Efficiency 2	V_{EFF2}	PV_{IN} = 12 V V_{OUT} = 3.3 V, I_{OUT} = 4 A V_{FSEL} = OPEN (600kHz)	—	95	—	%	*1
Efficiency 3	V_{EFF3}	PV_{IN} = 12 V V_{OUT} = 3.3 V, I_{OUT} = 4 A V_{FSEL} = V_{REG} (800kHz)	—	94	—	%	*1
Efficiency 4	V_{EFF4}	PV_{IN} = 12 V V_{OUT} = 1.0 V, I_{OUT} = 4 A V_{FSEL} = 0 V (400kHz)	—	88	—	%	*1
Efficiency 5	V_{EFF5}	PV_{IN} = 12 V V_{OUT} = 1.0 V, I_{OUT} = 4 A V_{FSEL} = OPEN (600kHz)	—	87	—	%	*1
Efficiency 6	V_{EFF6}	PV_{IN} = 12 V V_{OUT} = 1.0 V, I_{OUT} = 4 A V_{FSEL} = V_{REG} (800kHz)	—	85	—	%	*1

Note : *1 : Typical design value

ELECTRICAL CHARACTERISTICS (Continued)

C_O = 22 µF × 3, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V, Switching Frequency = 600 kHz
V_{MODE} = V_{REG} (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC Characteristics							
Load regulation1	V_{LOA1}	I_{OUT} = 10 mA to 10 A V_{MODE} = 0 V	—	2.0	—	%	*1
Load regulation2	V_{LOA2}	I_{OUT} = 10 mA to 10 A V_{MODE} = V_{REG}	—	1.0	—	%	*1
Line regulation	V_{LIN}	PV_{IN} = 6 V to 28 V V_{MODE} = V_{REG} I_{OUT} = 2.0 A	—	0.1	0.3	%/V	—
Output ripple voltage 1	V_{RL1}	I_{OUT} = 10 mA V_{MODE} = 0 V	—	30	—	mV [p-p]	*1
Output ripple voltage 2	V_{RL2}	I_{OUT} = 10 mA V_{MODE} = V_{REG}	—	15	—	mV [p-p]	*1
Output ripple voltage 3	V_{RL3}	I_{OUT} = 5 A V_{MODE} = V_{REG}	—	10	—	mV [p-p]	*1
Load transient response 1	ΔV_{TR1}	I_{OUT} = 100 mA to 5 A Δt = 0.5 A / µs V_{MODE} = 0 V or V_{REG}	—	15	—	mV	*1
Load transient response 2	ΔV_{TR2}	I_{OUT} = 5 A to 100 mA Δt = 0.5 A / µs V_{MODE} = 0 V or V_{REG}	—	20	—	mV	*1
Minimum Input and output voltage difference	V_{DIFF}	V_{DIFF} = V_{IN} – V_{OUT}	—	2.5	—	V	*1

Note : *1 : Typical design value

ELECTRICAL CHARACTERISTICS (Continued)

C_O = 22 µF × 3, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 12 V, Switching Frequency = 600 kHz
V_{MODE} = V_{REG} (FCCM), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Protection							
DC-DC Over Current Protection Limit 1	I_{LMT1}	OCPCNT=OPEN	—	13	—	A	*1
DC-DC Over Current Protection Limit 2	I_{LMT2}	OCPCNT=220 kΩ	—	11.5	—	A	*1
DC-DC Over Current Protection Limit 3	I_{LMT3}	OCPCNT=100 kΩ	—	10	—	A	*1
Thermal Shut Down (TSD) Threshold	T_{TSDTH}	—	—	130	—	°C	*1
Thermal Shut Down (TSD) Hysteresis	T_{TSDHYS}	—	—	30	—	°C	*1
Soft-Start Timing							
SS Charge Current	I_{SSCHG}	V_{SS} = 0.3 V	1	2	4	µA	—
SS Discharge Resistance (Shut-down)	R_{SSDIS}	V_{EN} = 0 V	—	5	10	kΩ	—
Switching Frequency Adjustment							
DC-DC Switching Frequency 1	F_{SW1}	I_{OUT} = 4 A, V_{FSEL} = 0 V	—	400	—	kHz	*1
DC-DC Switching Frequency 2	F_{SW2}	I_{OUT} = 4 A, V_{FSEL} = OPEN	—	600	—	kHz	*1
DC-DC Switching Frequency 3	F_{SW3}	I_{OUT} = 4 A, V_{FSEL} = V_{REG}	—	800	—	kHz	*1

Note : *1 : Typical design value

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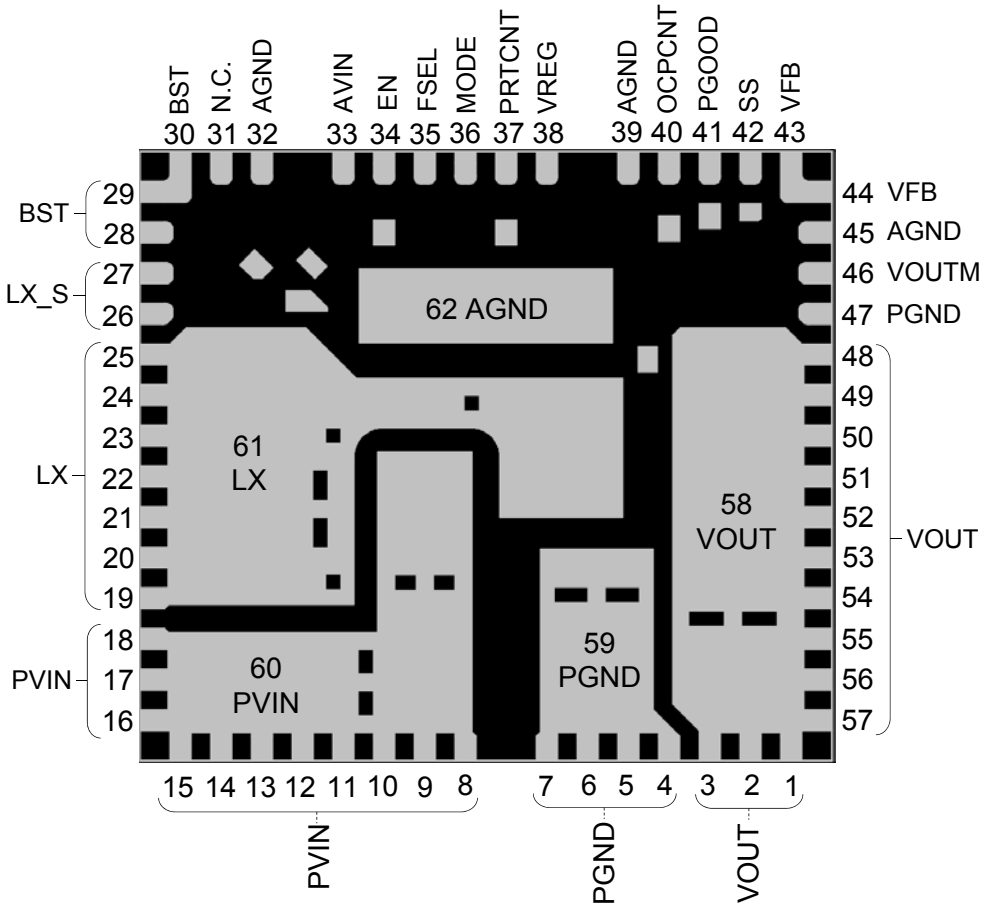
PIN CONFIGURATION

Bottom View



PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	VOUT	Output	Output voltage pin
2			
3			
48			
49			
50			
51			
52			
53			
54			
55			
56			
57			

Note : Detailed pin descriptions are provided in the OPERATION and APPLICATION INFORMATION section.

Established : 2014-07-03
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PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
4	PGND	Ground	Ground pin for Power MOSFET * Pin No. 47 : recommended settings – no connection
5			
6			
7			
47			
8	PVIN	Power supply	Power supply pin for Power MOSFET Recommended rise time (time to reach 90 % of set value) setting is greater than or equal to 10 µs and less than or equal to 1 s.
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19	LX	Output	Power MOSFET output pin An inductor is connected and switching operation is carried out between V_{IN} and GND. * Pin No. 19 to 25 : recommended settings – no connection
20			
21			
22			
23			
24			
25			
26	LX_S	Output	Power MOSFET output sense pin * Pin No. 26 to 27 : recommended settings – no connection
27			
28	BST	Output	High side Power MOSFET gate driver pin Bootstrap operation is carried out in order to drive the gate voltage of High side Power MOSFET. * Pin No. 28 to 30 : recommended settings – no connection
29			
30			
31	NC	-	Non Connection pin
32	AGND	Ground	Ground pin
39			
45			
33	AVIN	Power supply	Power supply pin Recommended rise time (time to reach 90 % of set value) setting is greater than or equal to 10 µs and less than or equal to 1 s.
34	EN	Input	ON / OFF control pin DC-DC is stopped at Low level input, and it is started at High level input.

Note : Detailed pin descriptions are provided in the OPERATION and APPLICATION INFORMATION section.

Established : 2014-07-03
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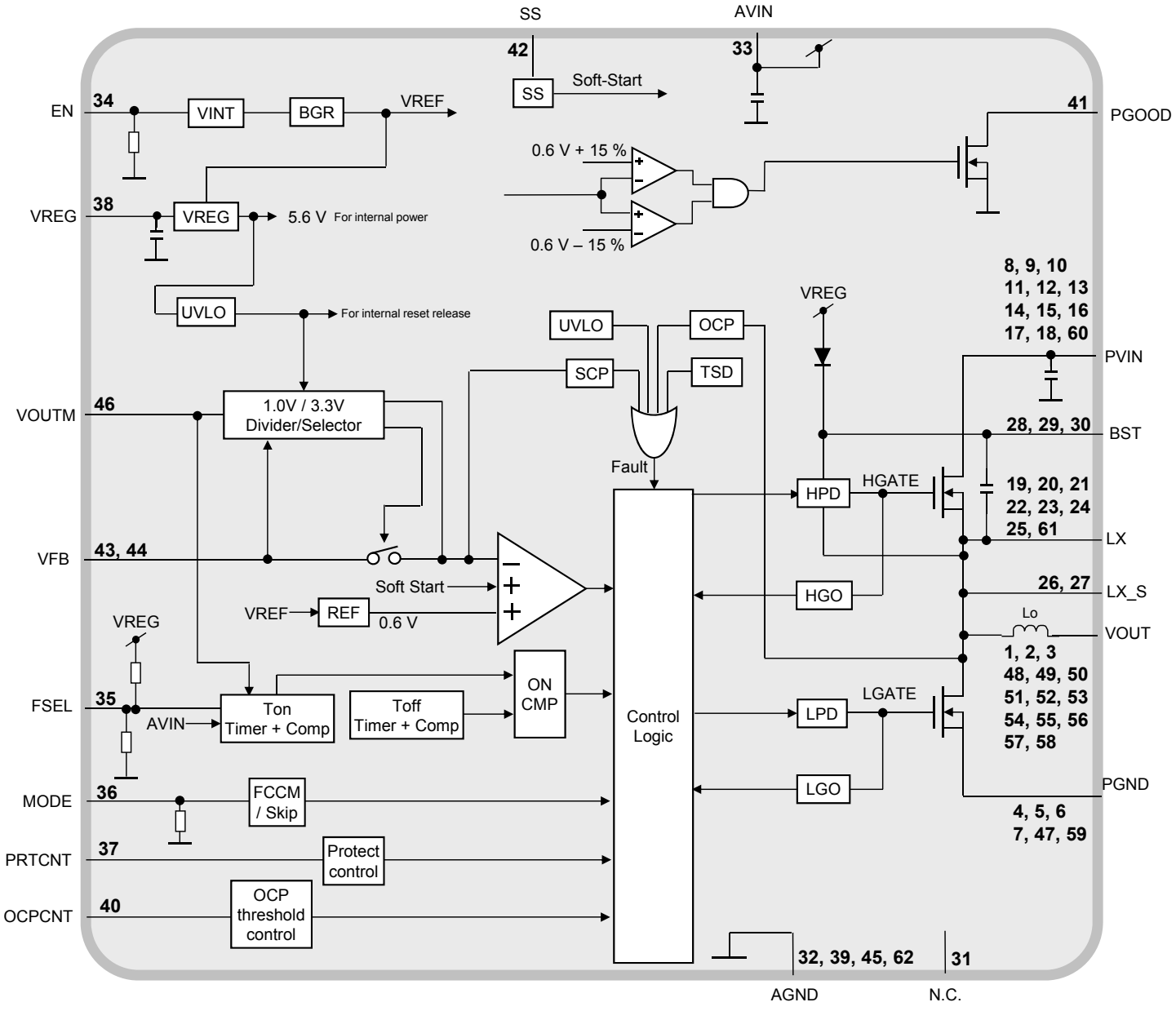
PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
35	FSEL	Input	Frequency select pin This is set to 400 kHz at Low level input, 800 kHz at High level input, and 600 kHz at open.
36	MODE	Input	Skip (discontinuous) mode / FCCM (Forced Continuous Conduction Mode) select pin Skip mode is set at Low level input, FCCM is set at High level input.
37	PRTCNT	Input	Protection Control Set pin for Latch mode / Auto recovery mode during OVD / SCP operations
38	VREG	Output	LDO output pin This is Output pin of Power supply (LDO) for internal control circuit.
40	OCPCNT	Input	Programmable over-current protection. Connected resistor on this pin will adjust the over-current protection threshold.
41	PGOOD	Output	Power good open drain pin A pull up resistor between PGOOD and V_{REG} terminal is necessary. Output is low during Over or Under Voltage Detection conditions.
42	SS	Output	Soft start capacitor connect pin The output voltage at a start up is smoothly controlled by adjusting Soft Start time. Please connect capacitor between SS and GND.
43 44	VFB	Input	Comparator negative input pin / 1.0 V, 3.3 V output voltage select pin VFB terminal voltage is regulated to REF output (internal reference voltage). Since VFB is a high impedance terminal, it should not be routed near other noisy path (LX, BST, etc.) Routing path should be kept as short as possible.
46	VOUTM	Input	Output voltage sense pin Switching frequency is controlled by monitoring output voltage. This pin is also used as Feedback pin during internal feedback function.
58	VOUT	Output	Voltage output pin for heat radiation
59	PGND	Ground	Ground pin of Power MOSFET for heat radiation
60	PVIN	Power supply	Power supply pin for heat radiation
61	LX	Output	Power MOSFET output pin for heat radiation
62	AGND	Ground	Ground pin for heat radiation

Note : Detailed pin descriptions are provided in the OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Note : This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

1. Protection

(1) Output Over-Current Protection (OCP) function And Short-Circuit Protection (SCP) function

1) The Over Current Protection is activated at about 13 A (Typ.) when OCPCNT pin is set to open. This device uses pulse – by – pulse valley current protection method. When the low side MOSFET is turned on, the voltage across the drain and source is monitored which is proportional to the inductor current. The high side MOSFET is only allowed to turn on when the current flowing in the low side MOSFET falls below the OCP level. Hence, during the OCP, the output voltage continues to drop at the specified current.

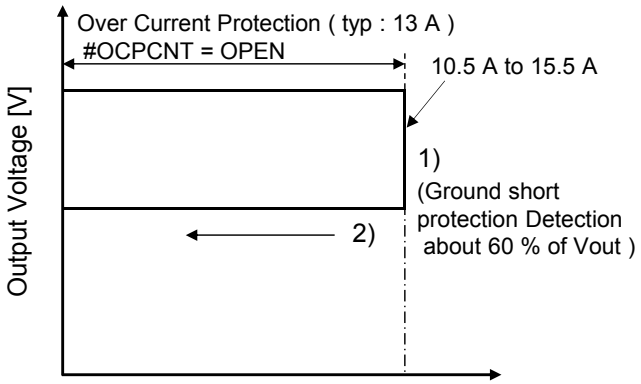

Figure : OCP and SCP Operation

Note: PRTCNT = V_{REG} (SCP latch off mode)

2) The Over Current Protection threshold level can be programmed by connecting a pull down resistor at OCPCNT pin. The value of the resistor connected between OCPCNT pin and ground will determine the OCP threshold level.

Note: The OCP level is fixed to around 0.7 A when OCPCNT pin is connected to Ground.

OCP level (typ)	OCPCNT resistor
13 A	OPEN (more than 1MΩ)
11.5 A	220 kΩ
10 A	100 kΩ

Table : OCP threshold level

The accuracy of OCP level is around ± 20 % of the typical value in the above table.
OCP level with resistor at OCPCNT pin (R_{OCP}) can be calculated by the following approximate equation.

$$OCP\ level[\mathrm{A}] = 13 - \frac{315}{R_{OCP}[k\Omega]}$$

Note: R_{OCP} is recommended to be more than 100 kΩ.

3) The Short-Circuit Protection function is implemented when the output voltage decreases and the VFB pin reaches to about 60 % of the set voltage of 0.6 V. If the VFB voltage stays below 70 % of 0.6 V for more than 250 µs after SCP triggers, both high side and low side MOSFET will be turned off and the output will be discharged by internal MOS transistor.
(The above operation after SCP triggered is at latch off mode. The details are described in the next page)

(2) Output Over Voltage Detection

If the VFB pin voltage exceeds 115 % of a predetermined value (0.6 V) and lasts more than 10ns, overvoltage detection will be triggered and PGOOD pin will be pulled down. Furthermore, in an overvoltage condition, high side and low side MOSFETs are turned off to stop PWM operation. If the VFB pin voltage drops below 110 % of the predetermined value (0.6 V) within 2 ms after overvoltage detection triggers, PGOOD pin will be pulled up again and PWM operation will resume. Otherwise, IC is transferred to latch off state and the output will be discharged by internal MOS transistor.
(The above operation after OVD triggered is at latch off mode. The details are described in the next page)

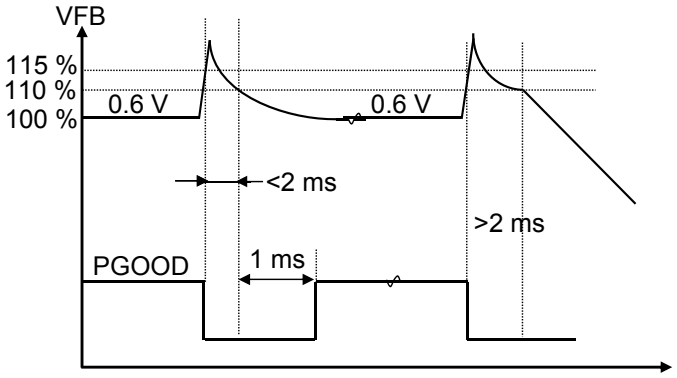

Figure : OVD Operation

Note: PRTCNT = V_{REG} (OVD latch off mode)

(3) Output discharging function

When EN is low, the output is discharged by an internal MOSFET transistor.

When EN is high, if the controller is turned off either by Under Voltage Lock Out (UVLO), Over Voltage Detection (OVD) or Short Circuit Protection (SCP), the output is discharged by an internal MOSFET transistor. The ON-resistance of the internal MOSFET transistor is about 35 Ω.

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OPERATION (Continued)

1. Protection (Continued)

(4) Protection control (PRTCNT) function

The IC turn-off operation after Over Voltage Detection and Short Circuit Protection can be programmed by PRTCNT pin voltage. Changing the input level of PRTCNT will select Latch off and Auto recovery mode for OVD and SCP operations. The following table and figures represents detailed explanation of this function.

After latch off detection, power reset or EN pin reset is necessary to activate the device again.

PRTCNT	OVD operation	SCP operation
L	Auto recovery	
OPEN	Latch off	Auto recovery
V_{REG}	Latch off	

Table : PRTCNT pin threshold level and protection mode

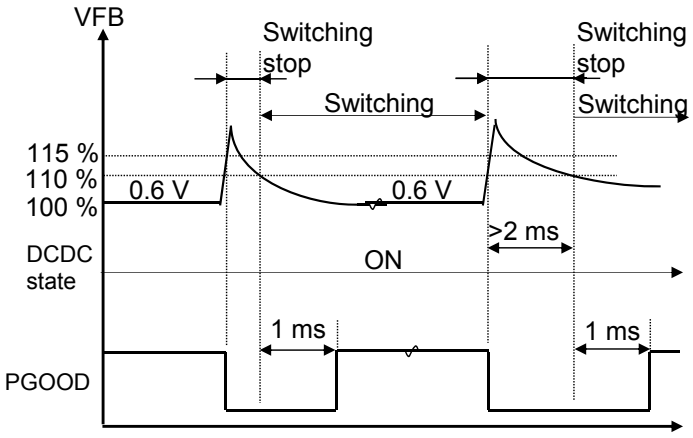


Figure : OVD Operation1
PRTCNT = L : Auto recovery case

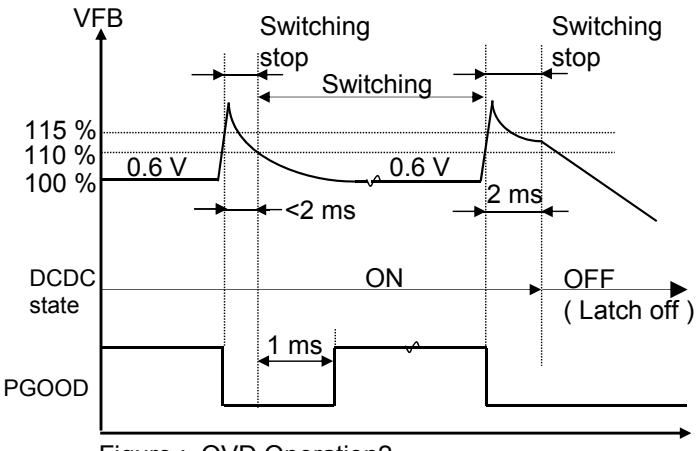
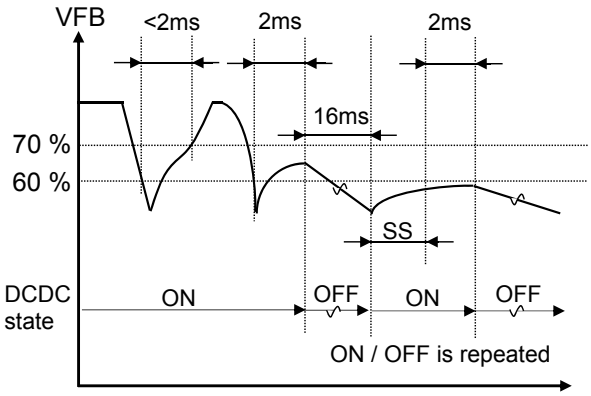


Figure : OVD Operation2
PRTCNT = OPEN / V_{REG} : Latch off case



Note : SS = Soft start time

Figure : SCP Operation1
PRTCNT = L / OPEN : Auto recovery case

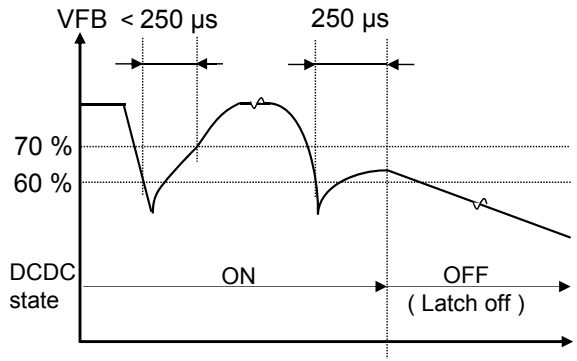


Figure : SCP Operation2
PRTCNT = V_{REG} : Latch off case

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OPERATION (Continued)

1. Protection (Continued)

(5) Output Under Voltage Detection (UVD)

During normal operation, if output voltage drops and VFB pin voltage reaches 85 % of its set value (0.6 V), the internal MOSFET connected to PGOOD pin, will turn on and the voltage of PGOOD will be set to low.

If the output voltage returns to 90 % of its set value (0.6 V) prior to triggering short-circuit-protection, the MOSFET connected to PGOOD pin will turn off and PGOOD voltage will become high again after 1 ms delay.

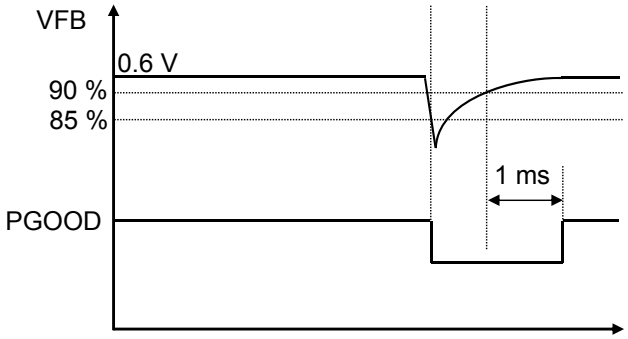


Figure : UVD Operation

(6) Thermal Shut Down (TSD)

When the IC internal temperature becomes more than about 130 °C, TSD operates and DC-DC turns off.

2. Pin Setting

(1) Operating MODE Setting

The IC can operate at two different modes :
Skip (discontinuous) mode and Forced Continuous Conduction Mode (FCCM).
In Skip mode, the IC is working under pulse skipping mechanism to improve efficiency at light load condition.
In FCCM, the IC is working at fixed frequency to avoid EMI issues.
The operating mode can be set by MODE pin as follows.

MODE pin	Mode
L	Skip mode
V_{REG}	FCCM

(2) Switching Frequency Setting

The IC can operate at three different frequencies : 400 kHz, 600kHz and 800 kHz.
The Switching Frequency can be set by FSEL pin as indicated in the table below.

FSEL pin	Frequency [kHz]
L	400
OPEN	600
V_{REG}	800

Switching frequency is recommended to be determined so that the inductor current amplitude becomes less than 40% of the maximum load current.
Inductor current amplitude is calculated by the following equation ;

$$Inductor\ Current\ Amplitude[\mathrm{A}] = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}} \times \frac{1000}{F_{sw}[kHz]}$$

For example, under V_{IN} = 12 V condition and maximum load current is 10 A, switching frequency is recommended to be set as follows depending on V_{OUT}.

V_{OUT} = 1.0V : 400, 600, 800 kHz
V_{OUT} = 1.8V : 400, 600, 800 kHz
V_{OUT} = 3.3V : 600, 800 kHz
V_{OUT} = 5.0V : 800 kHz

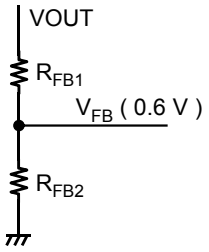
OPERATION (Continued)

3. Output Voltage Setting

(1) Output Voltage setting by external resistor

The Output Voltage can be set by external resistance of FB pin, and its calculation is as follows. Below resistors are recommended for following popular output voltage

$$V_{out} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \times 0.6$$



V_{OUT} [V]	R_{FB1} [Ω]	R_{FB2} [Ω]
5.0	11 k	1.5 k
3.3	4.5 k	1 k
1.8	2 k	1 k
1.2	1 k	1 k
1.0	1 k	1.5 k

VFB comparator threshold is adjusted to ± 1 %, but the actual output voltage accuracy becomes more than ± 1 % due to the influence from the circuits other than VFB comparator.
In the case of VOUT Setting = 1.0 V, the actual output voltage accuracy becomes ± 1.5 %.
(V_{IN} = 12 V, I_{OUT} = 5 A, Fsw = 600 kHz, FCCM).

(2) Built-in Feed Back Resistors for 1.0 V / 3.3 V

NN31000A has built-in feedback resistors for 1.0 V and 3.3 V output voltage.
When the UVLO delay (internal) signal changes from Low to High (UVLO release), depending on the state of FB pin, the output voltage can be configured as follows :

Table : Output voltage setting

VFB voltage [V]	Output voltage [V]
V_{REG}	3.3 V
OPEN	1.0 V
Resistor divider	Adjustable between 0.6 V and 5.5 V

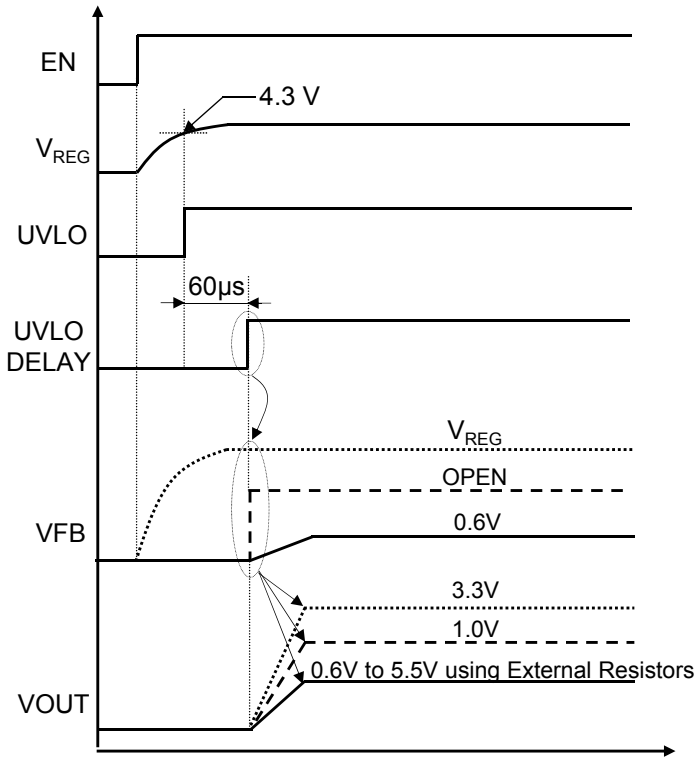


Figure : Timing chart of output voltage setting

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OPERATION (Continued)

4. Soft Start Setting

Soft Start function maintains the smooth control of the output voltage during start up by adjusting soft start time. When the EN pin becomes High, the current (2 μA) begin to charge toward the external capacitor (Css) of SS pin, and the voltage of SS pin increases straightly. Because the voltage of VFB pin is controlled by the voltage of SS pin during start up, the voltage of VFB increase straightly to the regulation voltage (0.6 V) together with the voltage of SS pin and keep the regulation voltage after that. On the other hand, the voltage of SS pin increase to about 2.8 V and keep the voltage. The calculation of Soft Start Time is as follows.

$$Soft\ Start\ Time(s) = \frac{0.6}{2\mu} \times Css$$

When Css is set at 4.7nF, soft-start time is Approximately 1.5 ms in 1.0 V setting.

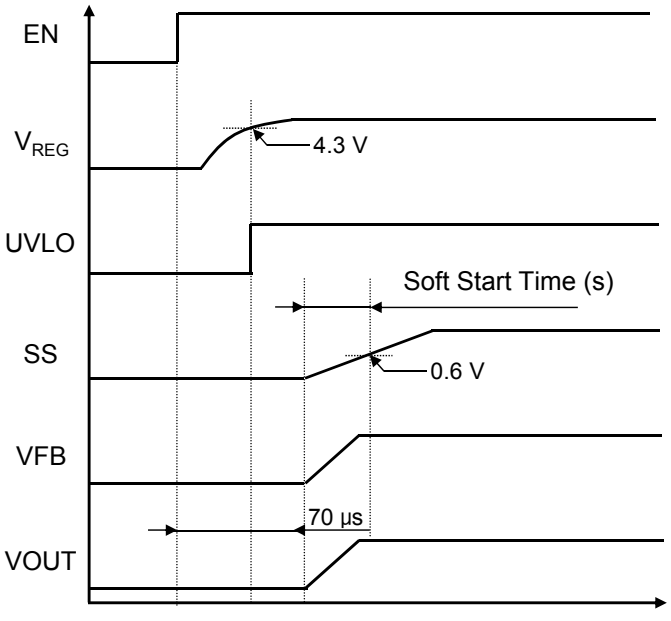

Figure : Soft Start Operation

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OPERATION (Continued)

5. Start Up / Shut Down Settings

The Start up / Shut down is enabled by the EN pin. The EN pin can be set by either applying voltage from an external voltage source or through a resistor connected to the AVIN pin.

Case 1 : Setting up the EN pin using an external voltage source. When an external voltage source is used, the EN pin input voltage (V_{ENH}, V_{ENL}) should satisfy the conditions as defined in the electrical characteristics.

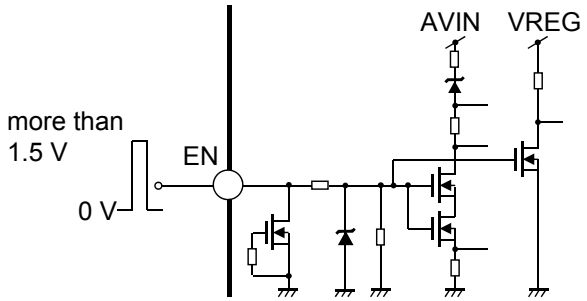

Figure : Internal circuit with EN pin

Case 2 : Setting up the EN pin through a resistor connected to AVIN pin. When setting up the EN pin through a resistor connected to the AVIN pin, refer to the following equation to calculate the optimal resistor settings.

[Equation]

$$\frac{AV_{IN} - V_{dMIN}}{Id} < R_{EN1} < \frac{(AV_{IN} - V_{ENH}) \times R_{EN2MIN}}{V_{ENH}}$$

R_{EN1}	: pull up resistor of EN pin
AV_{IN}	: input voltage
V_{dMIN}	: minimum internal zener diode voltage (5.4 V)
Id	: internal zener diode current (100 µA)
V_{ENH}	: EN pin high level input voltage (1.5 V to 5 V)
R_{EN2MIN}	: minimum pull down resistor (500 kΩ)

[Example (AV_{IN} = 12 V, V_{ENH} = 5 V)]

66 kΩ $< R_{EN1} <$ 700 kΩ

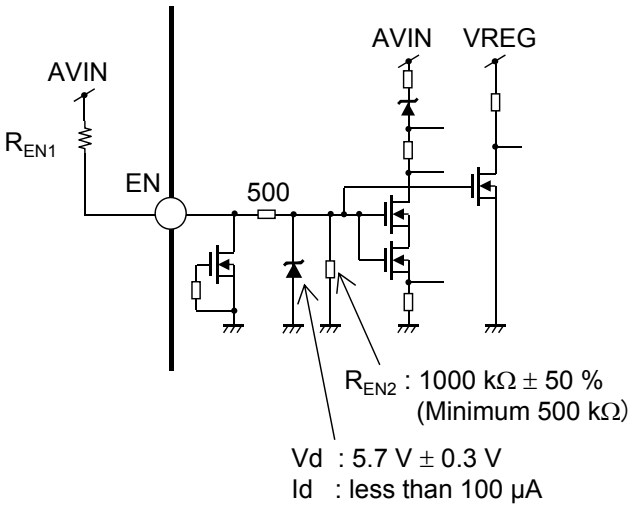

Figure : Internal circuit with EN pin

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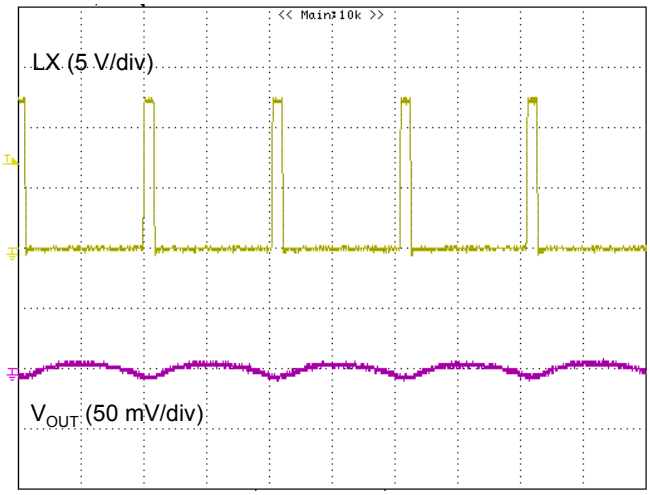
TYPICAL CHARACTERISTICS CURVES

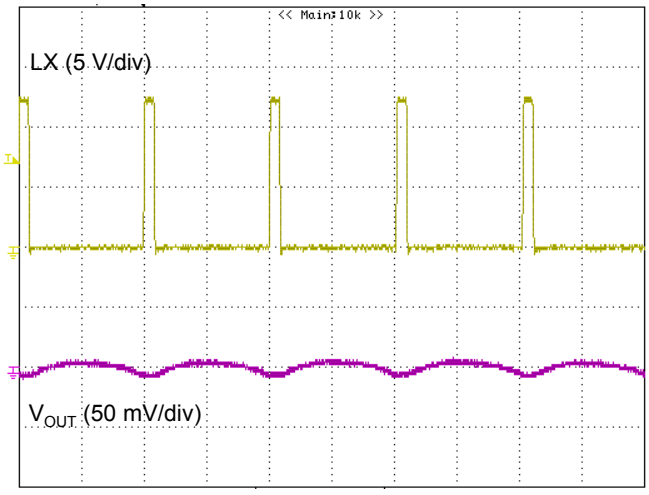
1. Output Ripple Voltage

Condition : V_{IN} = 12 V, V_{OUT} Setting = 1.0 V, Switching Frequency = 600 kHz, FCCM,
C_O = 66 µF (22 µF x 3)

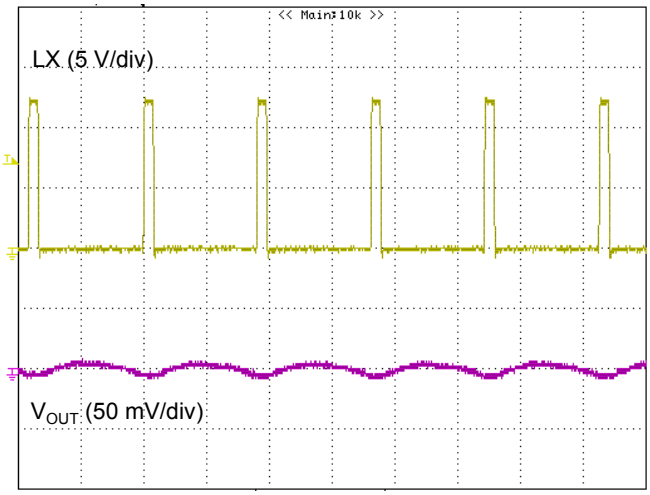
I_{OUT} = 0 A



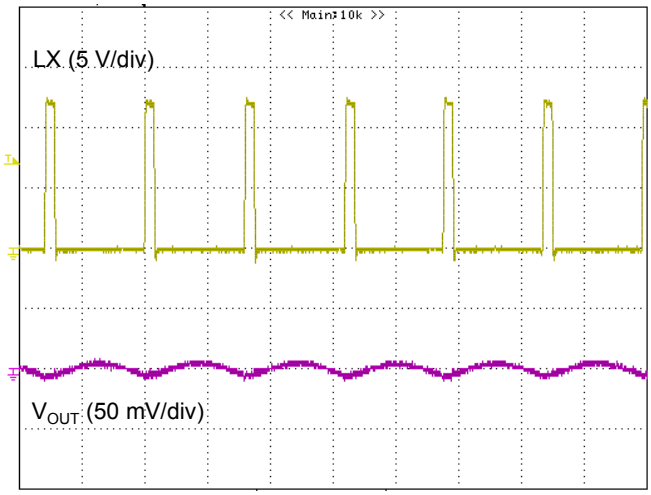
I_{OUT} = 0.1 A



I_{OUT} = 3 A



I_{OUT} = 10 A



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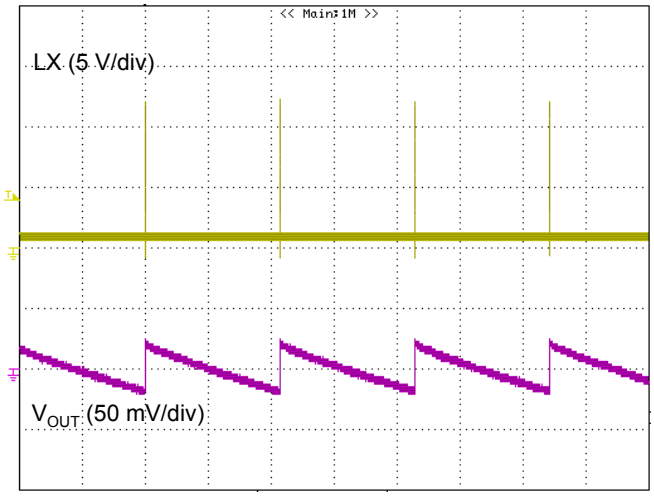
TYPICAL CHARACTERISTICS CURVES (Continued)

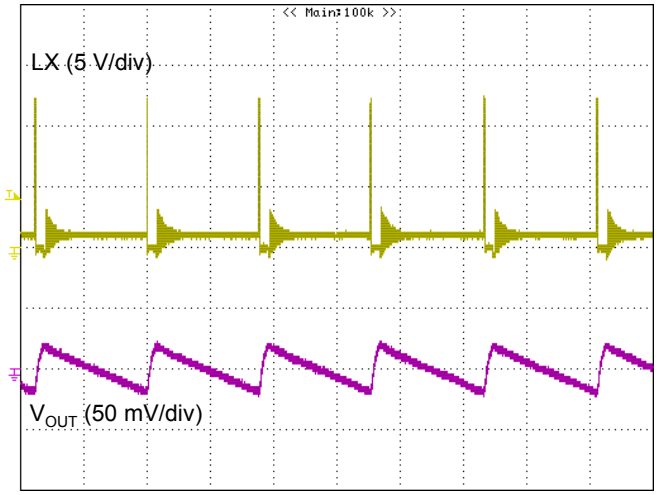
1. Output Ripple Voltage (Continued)

Condition : V_{IN} = 12 V, V_{OUT} Setting = 1.0 V, Switching Frequency = 600 kHz, Skip mode,
C_O = 66 µF (22 µF x 3)

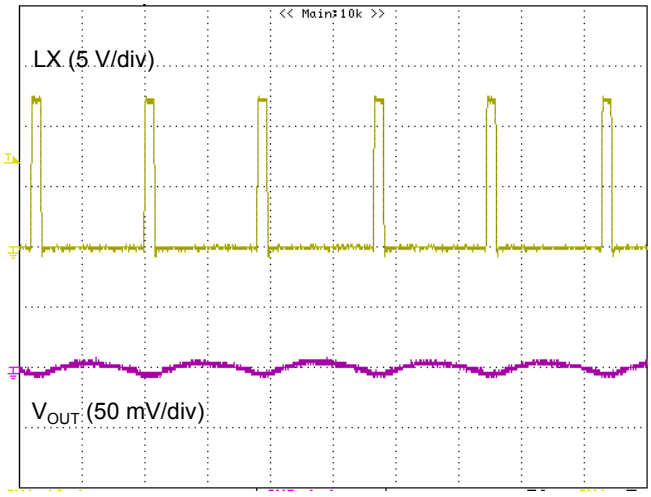
I_{OUT} = 0 A



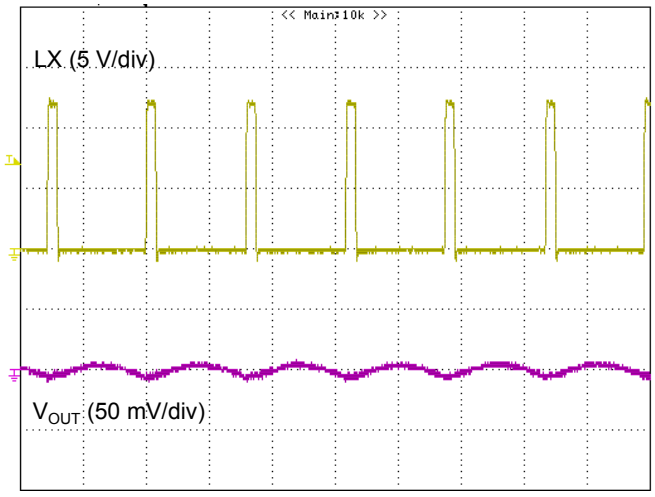
I_{OUT} = 0.1 A



I_{OUT} = 3 A



I_{OUT} = 10 A



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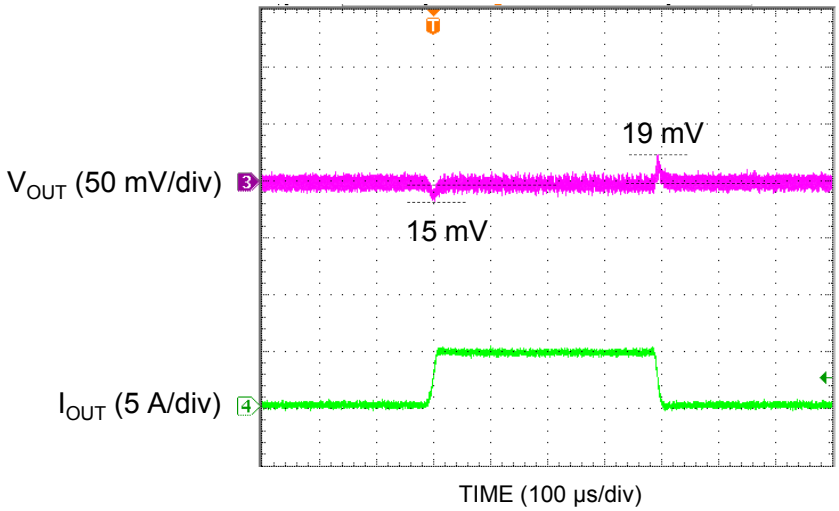
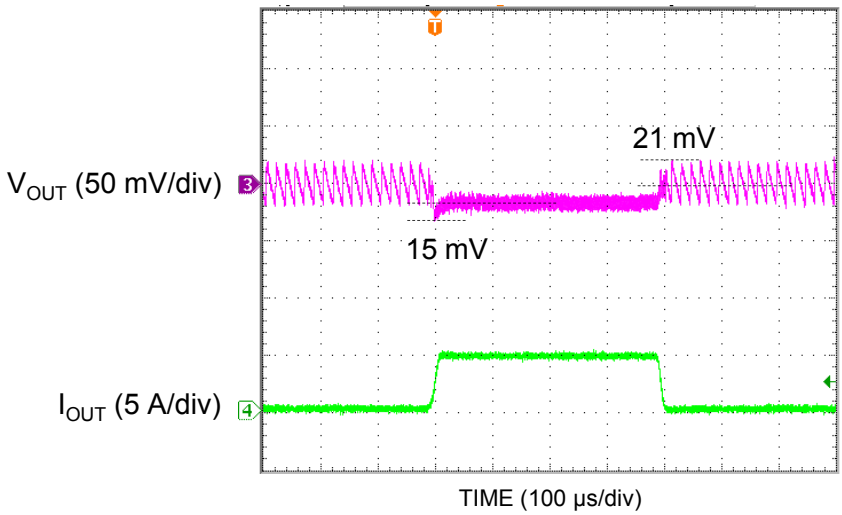
TYPICAL CHARACTERISTICS CURVES (Continued)

2. Load Transient Response

Condition : V_{IN} = 12 V, V_{OUT} Setting = 1.0 V, Switching Frequency = 600 kHz, FCCM,
C_O = 66 µF (22 µF x 3), I_{OUT} = 0.1 A to 5 A (0.5 A / µs)



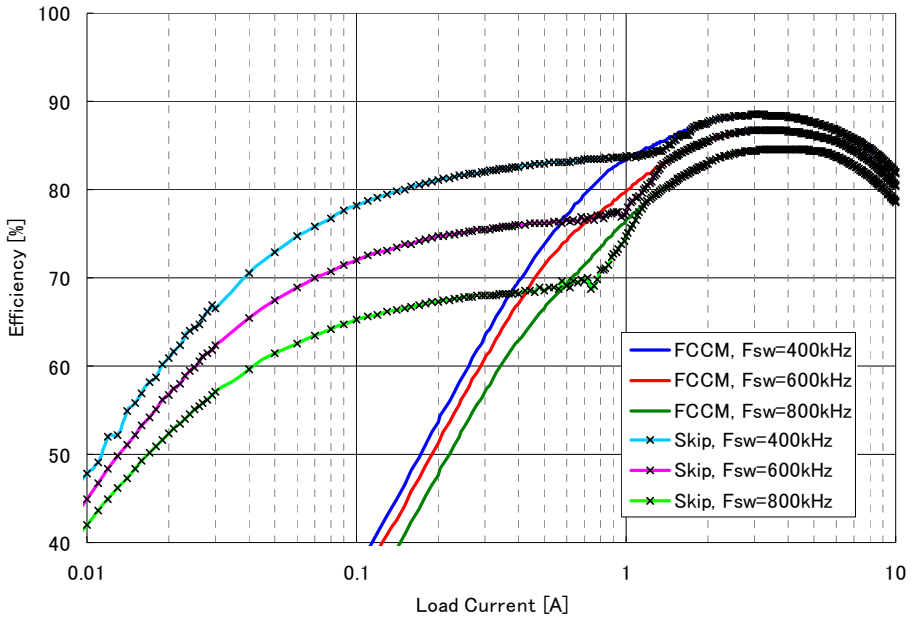
Condition : V_{IN} = 12 V, V_{OUT} Setting = 1.0 V, Switching Frequency = 600 kHz, Skip mode,
C_O = 66 µF (22 µF x 3), I_{OUT} = 0.1 A to 5 A (0.5 A / µs)



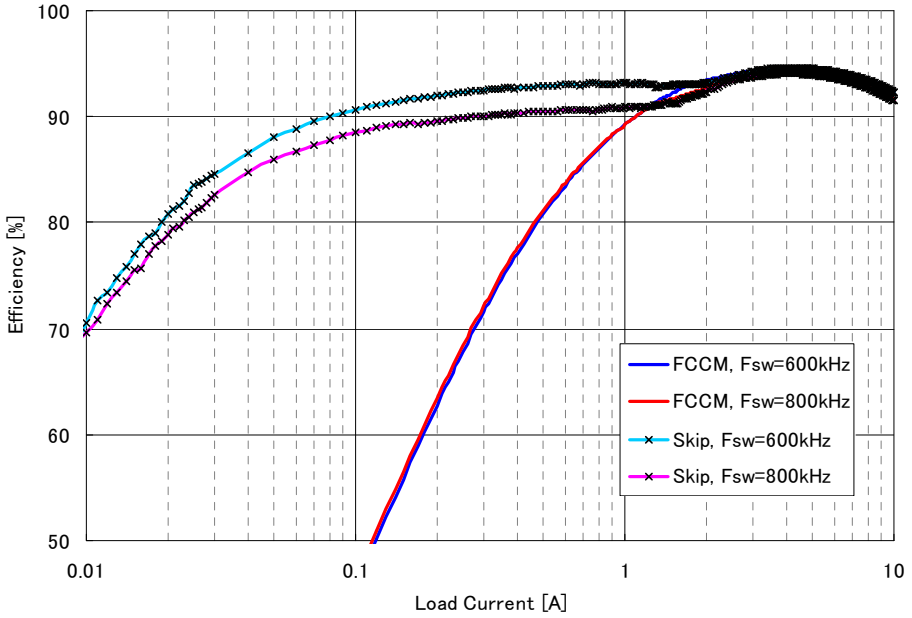
TYPICAL CHARACTERISTICS CURVES (Continued)

3. Efficiency

Condition : V_{IN} = 12 V, V_{OUT} Setting = 1.0 V, Switching Frequency = 400 / 600 / 800 kHz, FCCM / Skip mode, C_O = 66 µF (22 µF x 3)



Condition : V_{IN} = 12 V, V_{OUT} Setting = 3.3 V, Switching Frequency = 600 / 800 kHz, FCCM / Skip mode, C_O = 66 µF (22 µF x 3)



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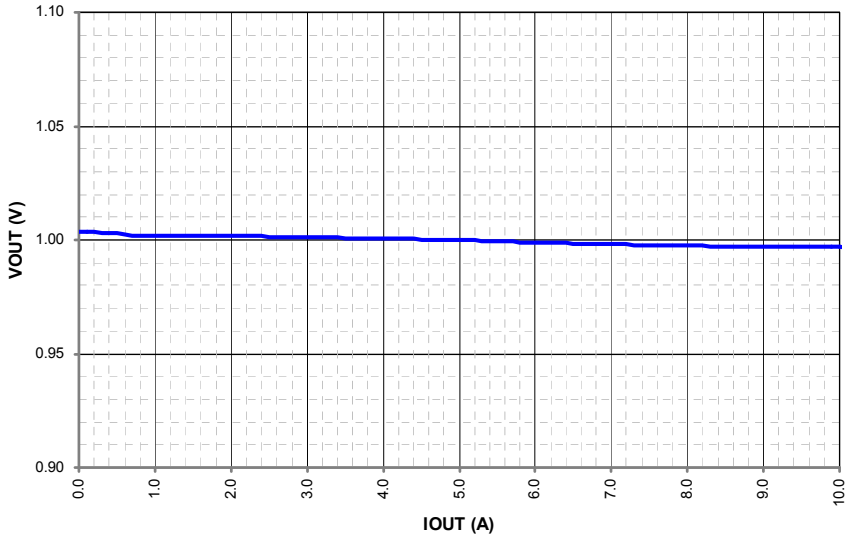
TYPICAL CHARACTERISTICS CURVES (Continued)

4. Load Regulation

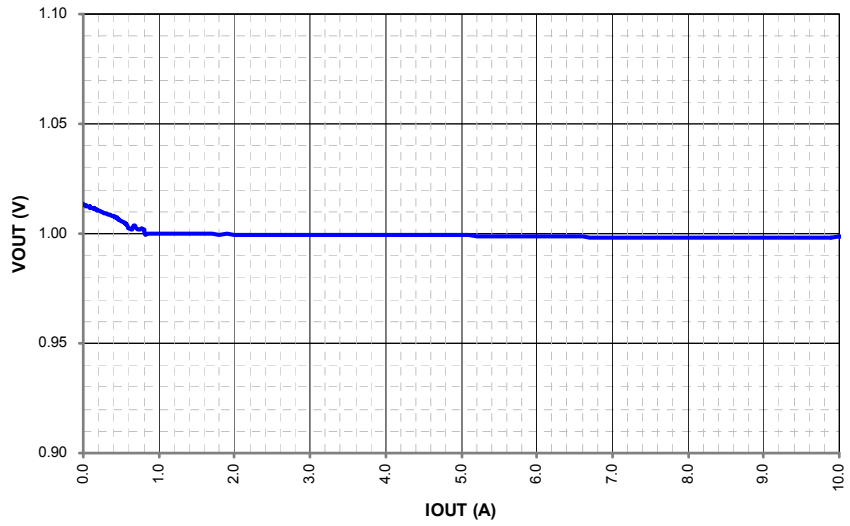
Condition : V_{IN} = 12 V, V_{OUT} Setting = 1.0 V, Switching Frequency = 600 kHz, FCCM,
C_O = 66 µF (22 µF x 3)

DCDC Load REG at FCCM



Condition : V_{IN} = 12 V, V_{OUT} Setting = 1.0 V, Switching Frequency = 600 kHz, Skip mode,
C_O = 66 µF (22 µF x 3)

DCDC Load REG at Skip Mode



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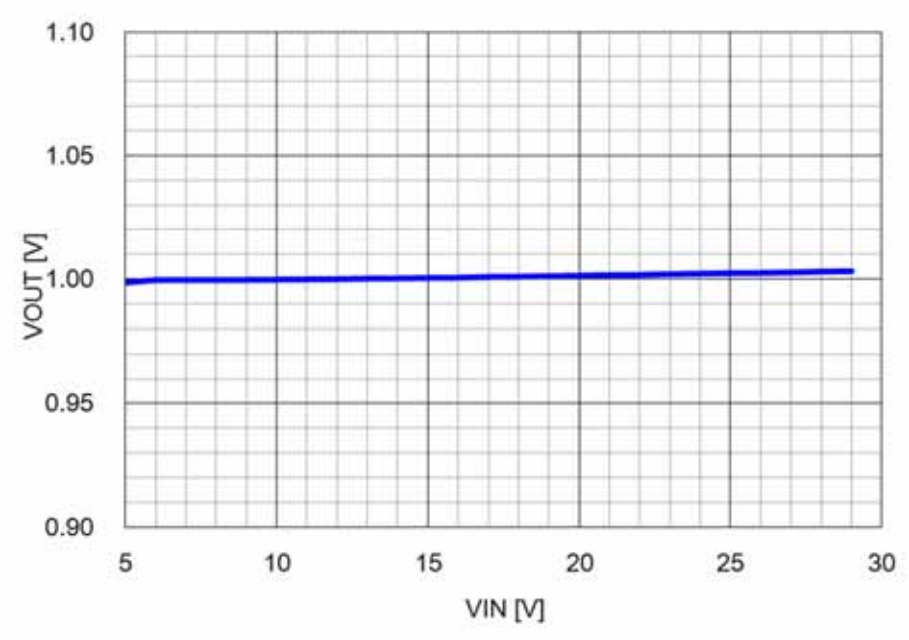
TYPICAL CHARACTERISTICS CURVES (Continued)

5. Line Regulation

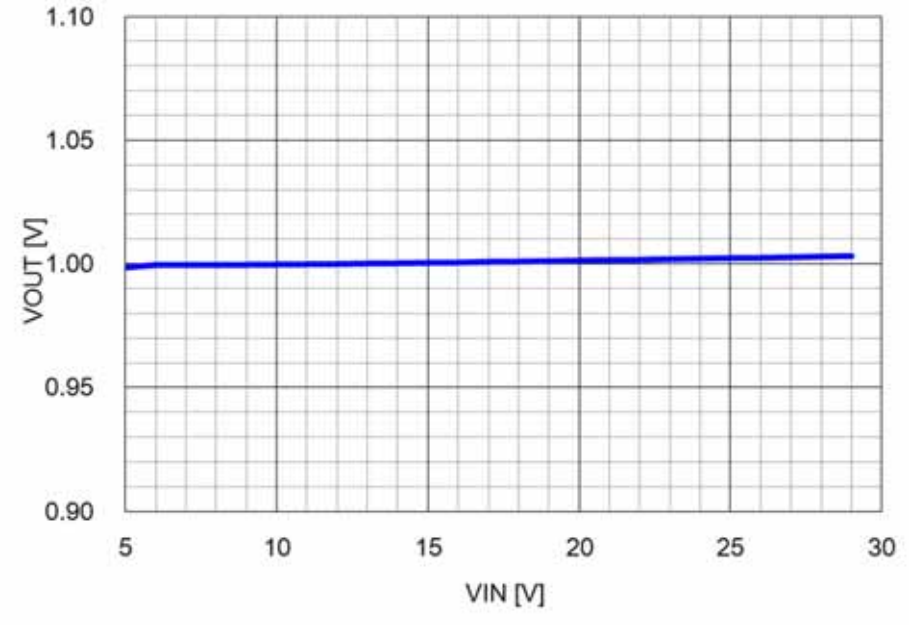
Condition : I_{OUT} = 2 A, V_{OUT} Setting = 1.0 V, Switching Frequency = 600 kHz, FCCM, C_O = 66 µF (22 µF x 3)

Line Regulation FCCM



Condition : I_{OUT} = 2 A, V_{OUT} Setting = 1.0 V, Switching Frequency = 600 kHz, Skip mode, C_O = 66 µF (22 µF x 3)

Line Regulation Skip Mode



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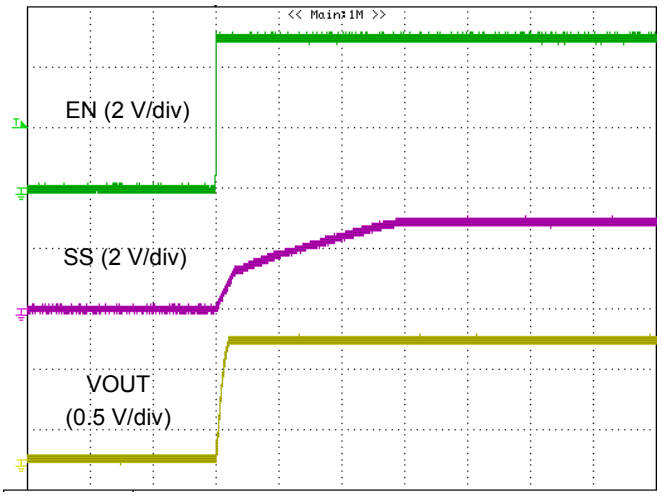
TYPICAL CHARACTERISTICS CURVES (Continued)

6. Start-up

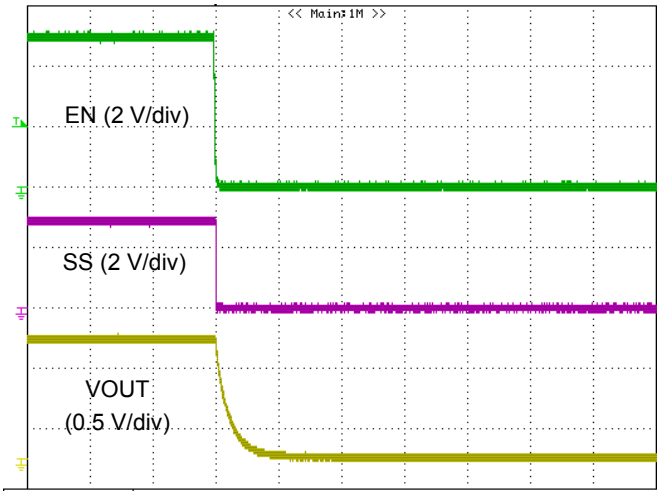
Condition : V_{IN} = 12 V, V_{OUT} Setting = 1.0 V, I_{OUT} = 0 A, Switching Frequency = 600 kHz, FCCM,
C_O = 66 µF (22 µF x 3)

EN = Low to High



TIME (10 ms/div)

EN = High to Low



TIME (10 ms/div)

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