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NOIH2SM1000A

HAS2 Image Sensor

ON Semiconductor®

http://onsemi.com

INTRODUCTION

Scope

This ICD version is generated after qualification campaign closure. This specification details the ratings, physical, geometrical, electrical and electro-optical characteristics, and test- and inspection-data for the High Accuracy Star Tracker (HAS2) CMOS active pixel image sensor (CMOS APS).

The device described in this document is protected by US patent 6,225,670 and others.

Component Type Values

Table 10 on page 9 provides a summary of the type variants of the basic CMOS image sensor. The complete list of specifications for each type variant is given in Detailed Specifications on page 10.

All specifications in Detailed Specifications on page 10 are given at 25 ±3°C, under nominal clocking and bias conditions. Exceptions are noted in the 'Remarks' field.

Maximum Rating

Table 11 on page 9 specifies the maximum ratings. Do not exceed these ratings at any times, during use or storage.

Physical Dimension and Geometrical Information

Figure 4 on page 25 shows the physical dimensions of the assembled component. The geometrical information in Figure 3 on page 10 describes the position of the die in the package.

Pin Assignment

Figure 5 on page 26 contains the pin assignment. The figure contains a schematic drawing and a pin list. A detailed functional description of each pin is available in Pin List on page 36.

Soldering Instructions

Soldering is restricted to manual soldering only. No wave or reflow soldering is allowed. For manual soldering, the following restrictions are applicable:

- Solder 1 pin on each of the four sides of the sensor.
- Cool down for a minimum period of 1 minute before soldering another pin on each of the four sides.
- Repeat soldering of 1 pin on each side, including a 1 minute cool down period.

Handling Precautions

The component is susceptible to damage by electro-static discharge. Therefore, use suitable precautions for protection during all phases of manufacture, testing, packaging, shipment, and any handling. Follow these guidelines:

- Always manipulate devices in an ESD controlled environment.
- Always store the devices in a shielded environment that protects against ESD damage (at least a non-ESD generating tray and a metal bag).
- Always wear a wrist strap when handling the devices and use ESD safe gloves.
- The HAS2 is classified as class 1A (JEDEC classification - [AD03]) device for ESD sensitivity.

For proper handling and storage conditions, refer to the ON Semiconductor application note AN52561.

Limited Warranty

ON Semiconductor's Image Sensor Business Unit warrants that the image sensor products to be delivered hereunder, if properly used and serviced, will conform to Seller's published specifications and will be free from defects in material and workmanship for two (2) years following the date of shipment. If a defect were to manifest itself within two (2) years period from the sale date, ON Semiconductor will either replace the product or give credit for the product.

Return Material Authorization (RMA)

ON Semiconductor packages its image sensor products in a clean room environment under strict handling procedures and ships all image sensor products in ESD-safe, clean-room-approved shipping containers. Products returned to ON Semiconductor for failure analysis should be handled under these same conditions and packed in its original packing materials, or the customer may be liable for the product.

Storage Information

The components must be stored in a dust-free and temperature-, humidity-and ESD-controlled environment.

- Store devices in special ESD-safe trays such that the glass window is never touched.
- Close the trays with EDS-safe rubber bands.
- Seal the trays in an ESD-safe conductive foil in clean room conditions.
- For transport and storage outside a clean room, pack the trays in a second ESD-save bag that is sealed in clean room.

May, 2013 – Rev. 13
Publication Order Number:
NOIH2SM1000A/D

Additional Information

The HAS sensor is subject to the standard European export regulations for dual use products. A Certificate of Conformance will be issued upon request at no additional charge. The CoC refers to this document. Additional screening tests is done on request at additional cost.

The following data is delivered by default with FM sensors:

- Sensor calibration data
- Temperature calibration data
- Certificate of Conformance to this detailed specification
- Visual inspection report
- Bad pixel map

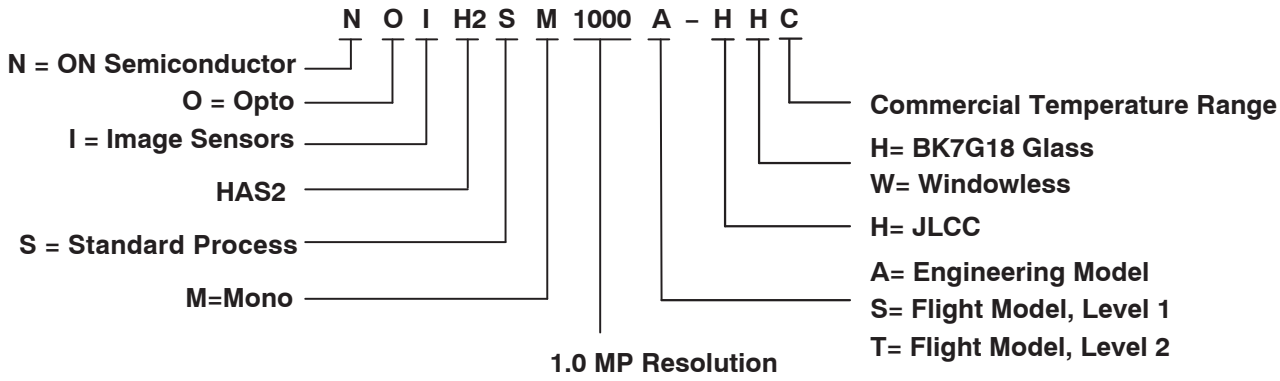
ITAR Information

The NOIH2SM1000A is an ITAR-free component.

Table 1. ORDERING INFORMATION

Marketing Part Number	Description	Package
NOIH2SM1000T-HHC	HAS2 Mono, Flight Model, Level 2	84-pin JLCC
NOIH2SM1000A-HHC	HAS2 Mono, Engineering Model	
NOIH2SM1000S-HHC	HAS2 Mono, Flight Model, Level 1	
NOIH2SM1000A-HWC	HAS2 Mono Windowless, Engineering Model	
NOIH2SM1000S-HWC	HAS2 Mono Windowless, Flight Model, Level 1	

ORDERING CODE DEFINITION



APPLICABLE DOCUMENTS

The following documents form part of this specification:

Table 2. APPLICABLE DOCUMENTS

No.	Reference	Title	Issue	Date
AD01	ESCC Generic Specification 9020	Charge Coupled Devices, Silicon, Photosensitive	2	March 2010
AD02	001-06225 (Note 1)	Electro-optical test methods for CMOS image sensors	E	October, 2008
AD03	JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	B	June, 2000
AD04	APS2-FVD-06-003	Process Identification Document for HAS2	2	February, 2008
AD05	001-49283	Visual Inspection for FM devices	1	January, 2008
AD06	001-49280	HAS2 FM Screening	2	June, 2009

1. This specification will be superseded by the ESCC basic specification 25000, which is currently under development. The current reference is an internal ON Semiconductor procedure and is a confidential document.
2. Lot acceptance and screening are based on ESCC 9020 issue 2. Please note that Lot Acceptance and Screening on page 6 – is valid for the Flight Model Level 1 devices. For more information on Flight Model 1 Windowless devices, please contact imagesensors@onsemi.com

DETAILED INFORMATION

Deviations from Generic Specification

Lot acceptance and screening are based on ESCC 9020 issue 2. See Lot Acceptance and Screening on page 6 for more information.

Mechanical Requirements

Dimension Check

The dimensions of the components specified here is checked and must comply with the specifications and the tolerances indicated in Figure 4 on page 25

Geometrical Characteristics

The geometrical characteristics of the components specified here is checked and must comply with the specifications and tolerances given in Figure 4 on page 25 and Figure 3 on page 10

Weight

The maximum weight of the components specified here is specified in Table 14 on page 10

Materials and Finishes

The materials and finishes is as specified in this document. Where a definite material is not specified, a material which enables the components to meet the performance requirements of this specification must be used. See Note 2.

Case

The case is hermetically sealed and must have a ceramic body and a glass window.

Table 3. CASE

Type	JLCC−84
Material	Black Alumina BA−914
Thermal expansion coefficient	$7.6 \times 10^{-6/K}$
Hermeticity	$< 5 \times 10^{-7}$ atms. cm^3/s
Thermal resistance (Junction to case)	3.633°C/W

Lead Material and Finish

Table 4. LEAD MATERIAL AND FINISH

Lead Material	KOVAR
1e Finish	Nickel, min 2 μm
2nd Finish	Gold, min 1.5 μm

Window

The window material is a BK7G18 glass lid with anti-reflective coating applied on both sides.

The optical quality of the glass must have the specifications in Table 15 on page 11.

The anti reflective coating has a reflection coefficient less than 1.3% absolute and less than 0.8% on average, over a bandwidth from 440 nm to 1100 nm.

Level 2 versus Level 1 differences

HAS2 Level 2 devices are differing from Level 1 devices in Lot Acceptance and Screening on page 6

- 100% screening is applied with burn-in limited to 168 h instead of 240 h as for Level 1.
- Assembly process is based on ESA qualified process (same procedures and materials)
- Devices will be fully tested at room temperature, electrical testing at 85 degrees is limited to power consumption measurements only.
- X/Y dye placement is relaxed to +/- 200 μm.
- Mismatching between odd and even columns in Direct Readout is allowed but shall stay in the limit of 127 LSB.
- The defect and particles specification will be the same as for the Engineering Model - NOIH2SM1000A-HHC – with the exception of the defective columns which are not allowed in the Level 2 devices. Refer to Table 10 “Type Variant Summary” on page 9.
- Endurance testing during wafer LAT is limited to a 1000 h burn in instead of 2000 h and will be performed on 3 un-screened parts instead of 6.
- Prior to endurance testing and total dose testing, a stabilization bake of 48 hrs, followed by a 168 hrs burn-in, shall be performed.
- During wafer LAT, the Electro-optical measurements is limited on 2 parts (1 from endurance testing and 1 from radiation testing) instead of 6.
- For each assembly batch (manufacturing-lot), 2 screened devices will be made available for a DPA test. An assembly batch is defined as a group of parts which have been assembled within a time window of less than one week. The DPA devices can be rejected devices (glass lid cosmetic defects, electrical defects,…) but has to be screened through the same thermal steps as the HAS2 “level2”. The DPA test will be carried out by ON Semiconductor as a customer courtesy.
  Prior to DPA testing, the following tests are performed: Solderability and Resistance to Solvents (marking permeability).

NOTE: As the glass lid removal is a best effort activity, the DPA test cannot be 100% guaranteed.

- Pictures and defect maps are not included in the data pack, but will be made available upon request.
- Assembly lot acceptance testing is not performed.

Data Pack

Each set of devices will have a data pack which will be made available to the customer. The data pack consists of:

- CoC form referring to the applicable specification
- Calibration data
- Screening Report
- Life Test Report and Radiation (Total Dose) Test Report for each wafer lot
- Electrical Test Report
- Spectral response data
- Visual Inspection Report
- DPA Test Report

Marking

General

The marking must consist of lead identification and traceability information.

Lead Identification

An index to pin 1 must be located on the top of the package in the position defined in Figure 4 on page 25. The pin numbering is counter clock-wise, when looking at the top-side of the component.

Traceability Information

Each component must be marked such that complete traceability is maintained.

The component must have a number as follows:

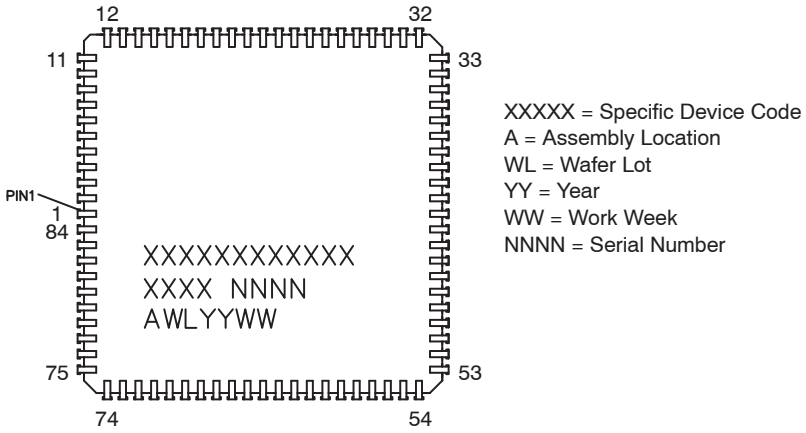


Figure 1. Product Marking

Table 5. PACKAGE MARK DECODER

Orderable Part Number	Package Mark: Line 1	Package Mark: Line 2	Package Mark: Line 3
NOIH2SM1000T-HHC	NOIH2SM1000T	-HHC NNNN	AWLYYWW
NOIH2SM1000A-HHC	NOIH2SM1000A	-HHC NNNN	AWLYYWW
NOIH2SM1000S-HHC	NOIH2SM1000S	-HHC NNNN	AWLYYWW
NOIH2SM1000A-HWC	NOIH2SM1000A	-HWC NNNN	AWLYYWW
NOIH2SM1000S-HWC	NOIH2SM1000S	-HWC NNNN	AWLYYWW
where NNNN- serialized number controlled manually by ON Semiconductor, BELGIUM			
where DD-MM-YYYY represents the lot assembly date			
NOIH2SM1000T-HHC has a Minimum Order Quantity of 10			

Electrical and Electro−optical Measurements

Electrical and Electro−opticalMeasurements at Reference Temperature

The parameters to be measured to verify the electrical and electro-optical specifications are given in Table 18 on page 14 and Table 27 on page 24. Unless otherwise specified, the measurements must be performed at a environmental temperature of 22 ±3°C.

For all measurements, the nominal power supply, bias, and clocking conditions apply. The nominal power supply and bias conditions are given in Table 28 on page 24; the timing diagrams in Figure 35 on page 47 and Figure 37 on page 49.

NOTE: The given bias and power supply settings imply that the devices are measured in ‘soft-reset’ condition.

Electrical and Electro−optical Measurements at High and Low Temperature

Table 19 on page 15 and Table 20 on page 16 list the parameters to be measured to verify electrical and electro-optical specifications. Unless otherwise specified,

the measurements must be performed at –40 (–5 +0) °C and at +85 (+5 –0) °C.

Circuits for Electrical and Electro−optical Measurements

Circuits for performing the electro−optical tests in Table 18 on page 14 and Table 27 on page 24 are shown in Figure 49 on page 59 to Figure 52 on page 59.

Burn−in Test

Parameter Drift Values

The parameter drift values for power burn-in are specified in Table 21 on page 18. Unless otherwise specified, the measurements must be conducted at an environmental temperature of 22 ±3°C and under nominal power supply, bias, and timing conditions.

Do not exceed the parameter drift values. In addition to these drift value requirements, do not exceed the limit values of any parameter, as indicated in Table 18 on page 14

Conditions for High Temperature Reverse Bias Burn-in

Not Applicable

Conditions for Power Burn-in

The conditions for power burn-in is specified in Table 24 on page 20 of this specification.

Electrical Circuits for High Temperature Reverse Bias Burn-in

Not Applicable

Electrical Circuits for Power Burn-in

Circuits to perform the power burn-in test are shown in Figure 48 on page 58 and Figure 49 on page 59 of this specification.

Environmental and Endurance Tests

Electrical and Electro-optical Measurements on Completion of Environmental Test

The parameters to be measured on completion of environmental tests are listed in Table 25 on page 21. Unless otherwise stated, the measurements must be performed at a environmental temperature of 22 ±3°C. Measurements of dark current must be performed at 22 ±1°C and the actual environmental temperature must be reported with the test results.

Electrical and Electro-optical Measurements At Intermediate Point During Endurance Test

The parameters to be measured at intermediate points during endurance test of environmental tests are listed in Table 25 on page 21. Unless otherwise stated, the measurements must be performed at an environmental temperature of 22 ±3°C.

Electrical and electro-optical Measurements on Completion of Endurance Test

The parameters to be measured on completion of endurance tests are listed in Table 25 on page 21. Unless otherwise stated, the measurements must be performed at a environmental temperature of 22 ±3°C.

Conditions for Operating Life Test

The conditions for operating life tests must be as specified in Table 24 on page 20 of this specification.

Electrical Circuits for Operating Life Test

Circuits for performing the operating life test are shown in Figure 49 on page 59 and next ones of this specification.

Conditions for High Temperature Storage Test

The temperature to be applied must be the maximum storage temperature specified in Table 11 on page 9 of this specification.

Total Dose Radiation Test

Application

The total dose radiation test must be performed in accordance with the requirements of ESCC Basic Specification 22900.

Parameter Drift Values

The allowable parameter drift values after total dose irradiation are listed in Table 22 on page 19 . The parameters shown are valid after a total dose of 42 KRad and 168 h / 100°C annealing.

Bias Conditions

Continuous bias must be applied during irradiation testing as shown in Figure 49 on page 59 and next ones of this specification.

Electrical and Electro-optical Measurements

The parameters to be measured, prior to, during and on completion of the irradiation are listed in Table 27 on page 24 of this specification. Only devices that meet the specification in Table 18 on page 14 of this specification must be included in the test samples.

Lot Acceptance and Screening

This section describes the Lot Acceptance Testing (LAT) and screening on the HAS2 FM devices. All tests on device level must be performed on screened devices (see Table 9 on page 7)

Wafer Lot Acceptance

This is the acceptance of the silicon wafer lot. This must be done on every wafer lot that is used for the assembly of flight models.

Table 6.

Test	Test Method	Number of Devices	Test Condition	Test Location
Wafer processing data review	PID	NA	NA	ON Semiconductor
SEM	ESCC 21400	4 naked dies	NA	Test house
Total dose test	ESCC 22900	3 devices	42 krad, not to exceed 3.6 krad/hr	Test house by ON Semiconductor
Endurance test	MIL-STD-883 Method 1005	6 devices	2000h at +125°C	Test house

Before and after total dose test and endurance test:

- Electrical measurements before and after at high, low, and room temperature. See Table 18 on page 14, Table 19 on page 15 and Table 20 on page 16 of this specification.
- Visual inspection before and after
- Detailed electro-optical measurements before and after

Glass Lot Acceptance

Transmission and reflectance curves that are delivered with each lot must be compared with the specifications in Table 15. Three glass lids are chosen randomly from the lot and measured in detail. The results are compared with Figure 5 on page 26.

Package Lot Acceptance

- Five packages are chosen randomly from the lot and measured in detail. The results are compared with Figure 4 on page 25.
- A solderability test is covered in the assembly lot acceptance tests (Table 7)

Table 7. ASSEMBLY LOT ACCEPTANCE

Test	Test Method	Number of Devices	Test Condition	Test Location
Special assembly house in process control				Assembly House
Bond strength test	MIL-STD-883 method 2011	2	D	Assembly House
Assembly house geometrical data review	Review	All		CY
Solder ability	MIL-STD883, method 2003	3	D	Test House
Terminal strength	MIL-STD 883, method 2004			
Marking permanence	ESCC 24800			
Geometrical measurements	PID	All		CY
Temperature cycling	MIL-STD 883, method 1010	5	Condition B 50 cycles –55°C / +125°C	Test House
Moisture resistance	JEDEC Std. Method A101-B		240 h at 85°C / 85%	Test House

Table 7. ASSEMBLY LOT ACCEPTANCE

Test	Test Method	Number of Devices	Test Condition	Test Location
DPA				
Die shear test	MIL-STD-883 method 2019	4	N/A	Test House
Bond pull test	MIL-STD-883 method 2011		All wires	Test House

NOTE: As the glass lid is removed from the package prior to DPA, the results of the DPA cannot be guaranteed.

Before and after the following tests are done:

- Electrical measurements conform to Table 18 on page 14 of this specification
- Detailed visual inspection
- Fine leak test + gross leak test

Fine- and gross-leak tests must be performed using the following methods:

Fine Leak test: MIL-STD-883, Test Method 1014, Condition A

Gross Leak test: MIL-STD-883, Test Method 1014, Condition C

The required leak rate for fine leak testing is 5×10^{-7} atms.cm^3/s

Table 8. PERIODIC TESTING

Test	Test Method	Number of Devices	Test Condition	Test Location
Mechanical shock	MIL-STD 883, method 2002	2	B - 5 shocks, 1500 g – 0.5 ms – ½ sine, 6 axes	Test House
Mechanical vibration	MIL-STD 883, method 2007	2	A - 4 cycles, 20 g 80 to 2000 Hz, 0.06 inch 20 to 80 Hz, 3 axes	Test House
DPA				
Die shear test	MIL-STD-883 method 2019	2	N/A	Test House
Bond pull test	MIL-STD-883 method 2011		All wires	Test House

NOTE: As the glass lid is removed from the package prior to DPA, the results of the DPA cannot be guaranteed.

Periodic testing is required every two years. Before and after the following tests are done:

- Electrical measurements conform to Table 18 on page 14
- Detailed visual inspection
- Fine leak test + gross leak test

Fine- and gross-leak tests must be performed using the following methods:

Fine Leak Test: MIL-STD-883, Test Method 1014, Condition A

Gross Leak Test: MIL-STD-883, Test Method 1014, Condition C

The required leak rate for fine leak testing is 5×10^{7} atms.cm^3/s

Table 9. SCREENING

No.	Test	Test Method	Number of Devices	Test Condition	Test Location
1	HCRT Electrical measurements	001-53958	All	HT +85°C LT –40°C RT +25°C	ON Semiconductor
2	Visual inspection	001-49283 + ICD	All		ON Semiconductor
3	Die placement measurements	Internal proc.	All		ON Semiconductor
4	XRAY	ESCC 20900	All		Test House
5	Stabilization bake	MIL-STD-883 method 1008	All	48h at 125°C	Test House
6	Fine leak test	MIL-STD-883 method 1014	All	A	Test House

Table 9. SCREENING

7	Gross leak test	MIL-STD-883 method 1014	All	C	Test House
8	Temperature cycling	MIL-STD-883 method 1010	All	B - 10 cycles –55°C +125°C	Test House
9	Biased Burn-in	ICD	All	240 h at +125°C	ON Semiconductor
10	Mobile Particle Detection	MIL-STD-883 method 2020	All	A	Test House
11	Fine leak test	MIL-STD-883 method 1014	All	A	Test House
12	Gross leak test	MIL-STD-883 method 1014	All	C	Test House
13	HCRT Electrical measurements	001-53958	All	HT +85°C LT –40°C RT +25°C	ON Semiconductor
14	Final Visual Inspection	001-49283 + ICD	All		ON Semiconductor

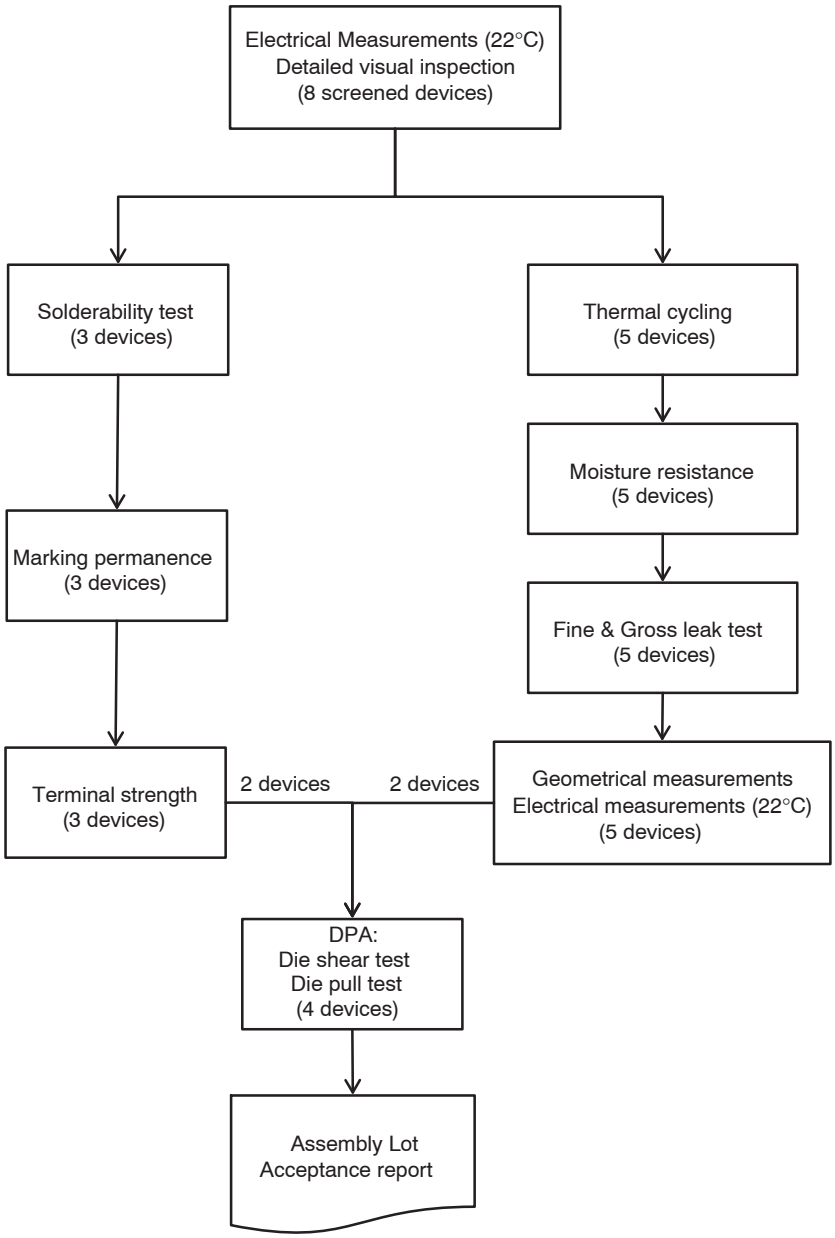


Figure 2. HAS2 Assembly LAT Flow

TABLES AND FIGURES

Specification Tables

Table 10. TYPE VARIANT SUMMARY

HAS2 Type Variants	Engineering Model	Flight Model
Optical quality (see Optical Quality – Definitions on page 67)		
Dead pixels	100	20
Bright pixels in FPN image	50	20
Bad pixels in PRNU image	150	50
Bad columns	5	0
Bad rows	5	0
Bright pixel clusters		
2 adjacent bright pixels	25	2
4 or more adjacent bright pixels	10	0
DSNU defects at 22 dec BOL	1200	1000
DSNU defects at 22 dec EOL	1500	1250
Particle contamination		
Fixed particles outside focal plane	N/A	N/A
Mobile particles > 20 μm	0	0
Fixed particles on focal plane > 20 μm	0	0
Mobile particles > 10 μm and < 20 μm	20	10
Fixed particles on focal plane > 10 μm and < 20 μm		
Particles < 10 μm	N/A	N/A
Wafer lot acceptance (see section Wafer Lot Acceptance on page 6)	NO	Yes
Glass lot acceptance (see section Glass Lot Acceptance on page 6)	NO	Yes
Assembly lot acceptance (Table 7 on page 6)	NO	Yes
Periodic testing (Table 8 on page 7)	NO	Yes
Screening (Table 9 on page 7)	NO	Yes
Calibration data	NO	Yes
Visual Inspection + particle mapping	NO	Yes

Table 11. MAXIMUM RATINGS

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1	Any supply voltage except VDD_RES	−0.5	3.3	+7.0	V	
2	Supply voltage at VDD_RES	−0.5	3.3	+5.0	V	3.3 V for normal operation; up to 5 V for increased full well capacity.
3	Voltage on any input terminal	−0.5	3.3	Vdd + 0.5	V	
4	Soldering temperature	NA	NA	260	°C	Hand soldering only; See Soldering Instructions on page 1
5	Operating temperature	−40	NA	+85	°C	
6	Storage temperature	−55	NA	+125	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Detailed Specifications – All Type Variants

Table 12. GENERAL SPECIFICATIONS

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1	Image sensor format	N/A	1024 x 1024	N/A	pixels	
2	Pixel size	N/A	18	N/A	μm	
3	ADC resolution	N/A	12	N/A	bit	10-bit accuracy at 5 Msamples/sec

Table 13. SILICON PARTICLE CONTAMINATION SPECIFICATIONS

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1	Optical quality: Particle max size	N/A	N/A	20	μm	See Type Variant Summary on page 9

Table 14. MECHANICAL SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units
Die (Refer to Figure 3 “Die Placement” on page 10)	Flatness of image area (Note 1)	NA	7.4	NA	μm
	Flatness of glass lid (Note 2)	NA	90	150	μm
	Mass	7.7	7.85	8.0	g
	Die thickness	−0.01	740	0.01	μm
	Die center, X offset to the center of package	(−50)	0	(+50)	μm
	Die center, Y offset to the center of the package	(−50)	0	(+50)	μm
	Die position, X tilt	(−0.1)	0	(0.1)	deg
	Die position, Y tilt	(−0.1)	0	(0.1)	deg
	Die placement accuracy in package	(−50)		(+50)	μm
	Die rotation accuracy	−1		1	deg
	Optical center referenced from package center (X-dir)	(−50)	+571	(+50)	μm
	Optical center referenced from package center (Y-dir)	(−50)	+109.5	(+50)	μm
	Distance from top of the die surface to top of the glass lid		1.83		mm
	Total Thickness	Refer to Package Diagram (Figure 4 on page 25)			

1. Peak-to-peak at 25 ±3°C. Specified by the foundry over an entire 8-inch wafer.
2. Towards ceramic package.

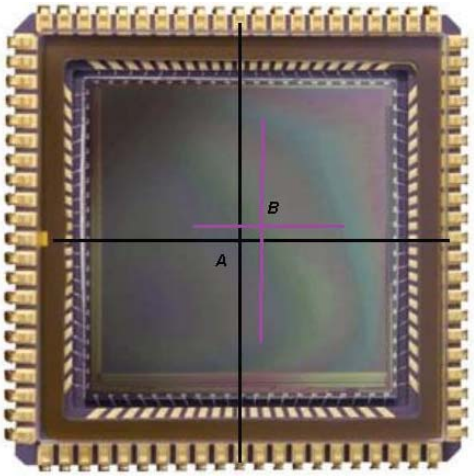


Figure 3. Die Placement

Table 15. GLASS LID SPECIFICATIONS

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1a	XY size	26.7 x 26.7	26.8 x 26.8	26.9 x 26.9	mm	
1b	Thickness	1.4	1.5	1.6	mm	
2a	Spectral range for optical coating of window	440	NA	1100	nm	
2b	Reflection coefficient for window	NA	<0.8	<1.3	%	Over bandwidth indicated in 2a
3	Optical quality: Scratch max width Scratch max number Dig max size Dig max number	N/A	N/A	 10 5 60 25	μm	

Table 16. ENVIRONMENTAL SPECIFICATIONS

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1	Operating temperature	−40	NA	+85	°C	
2	Storage temperature	−55	NA	+125	°C	Lower storage temperatures (up to −80°C) have been tested and the device survives, but this is not a fully qualified temperature.
3	Sensor total dose radiation tolerance	N/A	42	N/A	krad (Si)	Tested for functionality up to 300 krad, 42 krad is guaranteed
4	Sensor SEL threshold with ADC enabled	NA	NA	>110	MeV cm^3 mg^{-1}	Equivalent LET value

Table 17. ELECTRICAL SPECIFICATIONS

No	Characteristic	Min	Typ	Max	Unit	Remarks
1	Total power supply current stand-by	16	18.5	21	mA	
2	Total power supply current, operational	35	37	40	mA	ADC at 5 MHz sampling rate measured
3	Power supply current to ADC, operational: analog + digital	17	19	21	mA	ADC at 5 MHz sampling rate measured
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	
7	Output amplifier voltage range	2.2	2.45	2.6	V	
8	Output amplifier gain setting 0	NA	1	NA	–	Nominal 1 measured reference
9	Output amplifier gain setting 1	1.9	2.1	2.3	–	Nominal 2 relative to setting 0
10	Output amplifier gain setting 2	3.8	4.1	4.4	–	Nominal 4 relative to setting 0
11	Output amplifier gain setting 3	7.2	7.7	8.2	–	Nominal 8 relative to setting 0
12	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
13	Output amplifier offset setting 31	1.30	1.35	1.40	V	
14	Output amplifier offset setting 32	0.43	0.51	0.6	V	
15	Output amplifier offset setting 63	0.80	0.90	1.0	V	
16	ADC ladder network resistance	NA	1.8	NA	kΩ	Typical value

Table 17. ELECTRICAL SPECIFICATIONS

No	Characteristic	Min	Typ	Max	Unit	Remarks
17	ADC differential nonlinearity	NA	7	11	lsb	
18	ADC integral nonlinearity	NA	8	18	lsb	
19	ADC setup time	5	NA	NA	ns	Analog_in stable to CLK_ADC rising
20	ADC hold time	10	NA	NA	ns	Analog_in stable after CLK_ADC rising edge
21	ADC delay time	NA	NA	20	ns	
22	ADC latency	NA	6.5	NA	-	Cycles of CLK_ADC
23	ADC ideal input range	0.85	NA	2.0	V	VLOW_ADC to VHIGH_ADC
24	Saturation voltage output swing	1.20	1.49	NA	V	VDD_RES = 3.3 V
25	Output range	0.8	NA	2.1	V	Measured with PGA in unity gain, offset = 0.8 V, low is dark, high is bright.
26	Linear range of pixel signal swing	40	50 0.75	NA	ke- V	Measured within ±1%
27	Linear range	60	82	NA	ke-	Measured within ±5%
28	Full well charge	90	100	NA	ke-	Measured with VDD_RES = 3.3 V
29	Quantum efficiency x fillfactor	NA	45	NA	%	Measured between 500 nm and 650 nm. Refer to section Spectral Response on page 27 for complete curve.
30	Spectral response	NA	33.3	NA	%	Measured average over 400 nm – 900 nm.
31	Charge to voltage conversion factor	NA	16.9	NA	μV/e-	At pixel
32	Charge to voltage conversion factor	13	14.8	15.6	μV/e-	Measured at output SIGNAL_OUT, unity gain
33a	Temporal noise (soft reset)	NA	55	95	e-	Dark noise, with DR/DS, internal ADC
33b	Temporal noise (hard reset)	N/A	75	125	e-	Dark noise, with DR/DS, internal ADC
33c	Temporal noise (HTS reset)	NA	65	110	e-	Dark noise, with DR/DS, internal ADC
34a	Temporal noise (NDR soft reset)	NA	75	100	e-	
34b	Temporal noise (NDR hard reset)	NA	75	100	e-	
34c	Temporal noise (NDR HTS reset)	NA	70	100	e-	
35	ADC quantization noise	NA	7	NA	e-	
36a	Local fixed pattern noise standard deviation (hard reset)	NA	110	160	e-	With DR/DS
36b	Local fixed pattern noise standard deviation (soft reset)	NA	70	140	e-	With DR/DS
36c	Local fixed pattern noise standard deviation (HTS reset)	NA	95	140	e-	With DR/DS
37a	Global fixed pattern noise standard deviation (hard reset)	NA	115	180	e-	With DR/DS
37b	Global fixed pattern noise standard deviation (soft reset)	NA	90	140	e-	With DR/DS
37c	Global fixed pattern noise standard deviation (HTS reset)	NA	110	180	e-	With DR/DS

Table 17. ELECTRICAL SPECIFICATIONS

No	Characteristic	Min	Typ	Max	Unit	Remarks
37d	Global fixed pattern noise standard deviation (NDR, soft reset)	14	15	18	e-	With NDR/CDS and external ADC
37e	Local Column fixed pattern noise standard deviation (NDR, soft reset)	14	15	18	e-	With NDR/CDS and external ADC
38	Average dark signal	NA	190	400	e-/s	At 25 ±2°C die temp, BOL see “Dark Current vs Temperature Model” on page 31
39	Average dark signal	NA	5550	8730	e-/s	At 25 ±2°C die temp, EOL (25 krad)
40	Dark signal temperature dependency	5	5.8	8	°C	Sensor temperature increase for doubled average dark current.
41	Local dark signal non-uniformity standard deviation	NA	260	400	e-/s	At 25 ±2°C die temp, BOL 96% of BOL average
42	Global dark signal non-uniformity standard deviation	N/A	275	500	e-/s	At 25 ±2°C die temp, BOL 96% of BOL average
43	Local photo response non-uniformity, standard deviation	NA	0.8	1.0	%	Of average response
44	Global photo response non-uniformity, standard deviation	NA	1.8	5	%	Of average response
45	MTF X direction	NA	0.35	NA	NA	At Nyquist measured
46	MTF Y direction	NA	0.35	NA	-	At Nyquist measured
47	Pixel to pixel crosstalk X direction	NA	9.8	NA	%	Of total source signal – see “Pixel−to−Pixel Cross Talk” on page 35 for 2−D plot
48	Pixel to pixel crosstalk Y direction	NA	9.8	NA	%	Of total Source signal – see “Pixel−to−Pixel Cross Talk” on page 35 for 2−D plot
49	Anti-blooming capability	200	1000	NA		Typical
50	Pixel rate	NA	5	10	MHz	
51	Temperature sensor transfer curve	NA	−4.64	NA	mV/°C	BOL
52	Temperature sensor output signal range, Min to Max (typical)	800	NA	1700	mV	BOL
53	Temperature sensor linearity	NA	3	NA	mV	BOL
54	Temperature sensor transfer curve	NA	−4.64	NA	mV/°C	EOL
55	Temperature sensor output signal range, Min to Max (typical)	800	NA	1700	NA	EOL
56a	Image lag (soft reset)	NA	0.54	NA	-	Soft reset
56b	Image lag (hard reset)	NA	−0.2	NA	-	Hard reset
56c	Image lag (HTS reset)	NA	−0.15	NA	-	HTS reset

The following formulas are applicable to convert % Vsat and mV/s into e- and e-/s:

$$FPN[e-] = \frac{FPN[\%Vsat] * \sqrt{Vsat}}{conversion\_gain}$$

$$Dark\_signal[e-/s] = \frac{Dark\_signal[V/s]}{conversion\_gain}$$

$$DSNU[e-] = \frac{DSNU[\%Vsat] * \sqrt{Vsat}}{conversion\_gain}$$

Other Definitions

$$ADC\ Quantization\ Noise = \frac{\frac{Analog\ Range}{ADC\ Resolution}}{\frac{Conversion\ Gain}{\sqrt{ADC\ Resolution}}}$$

- Conversion gain for HAS: 14.8 μV/e-
- Definition for local measurements: 32 x 32 pixels
- Definition for global measurements: Full pixel array

Table 18. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT ROOM TEMPERATURE 22°C

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1	Total power supply current stand-by	16	18.5	21	mA	
2	Total power supply current, operational	35	37	40	mA	ADC at 5 MHz sampling rate
3	Power supply current to ADC, operational	17	19	21	mA	ADC at 5 MHz sampling rate
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	
7	Output impedance digital outputs	NA	NA	400	W	
8	Output impedance analog output	NA	NA	1	kΩ	
9	Output amplifier voltage range	2.2	2.45	2.6	V	
10	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
11	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
12	Output amplifier gain setting 2	3.8	4.1	4.4	-	Nominal 4 relative to setting 0
13	Output amplifier gain setting 3	7.2	7.7	8.2	-	Nominal 8 relative to setting 0
14	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
15	Output amplifier offset setting 31	1.30	1.35	1.40	V	
16	Output amplifier offset setting 32	0.43	0.51	0.6	V	
17	Output amplifier offset setting 63	0.80	0.90	1.0	V	
18	ADC Differential nonlinearity	N/A	7	11	lsb	
19	ADC Integral nonlinearity	N/A	8	18	lsb	
20	Saturation voltage output swing	1.20	1.49	NA	V	VDD_RES = 3.3 V
21	Output range	0.8	NA	2.1	V	PGA in unity gain, offset = 0.8 V, low is dark, high is bright.
22a	Temporal noise (soft reset)	NA	55	95	e-	Dark noise, with DR/DS, internal ADC
22b	Temporal noise (hard reset)	NA	75	125	e-	Dark noise, with DR/DS, internal ADC
22c	Temporal noise (HTS reset)	NA	65	110	e-	Dark noise, with DR/DS, internal ADC
23a	Temporal noise (NDR soft reset)	NA	75	100	e-	
23b	Temporal noise (NDR hard reset)	NA	75	100	e-	
23c	Temporal noise (NDR HTS reset)	NA	70	100	e-	
24	ADC quantization noise	NA	7	NA	e-	
25a	Local fixed pattern noise standard deviation (soft reset)	N/A	70	140	e-	With DR/DS

Table 18. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT ROOM TEMPERATURE 22°C

No.	Characteristic	Min	Typ	Max	Unit	Remarks
25b	Local fixed pattern noise standard deviation (hard reset)	NA	110	160	e-	With DR/DS
25c	Local fixed pattern noise standard deviation (HTS reset)	NA	95	140	e-	With DR/DS
26a	Global fixed pattern noise standard deviation (soft reset)	NA	90	140	e-	With DR/DS
26b	Global fixed pattern noise standard deviation (hard reset)	NA	115	180	e-	With DR/DS
26c	Global fixed pattern noise standard deviation (HTS reset)	NA	110	180	e-	With DR/DS
27	Average dark signal	NA	190	400	e-/s	At 25 ±2°C die temp
28	Local dark signal non-uniformity standard deviation	NA	260	400	e-/s	At 25 ±2°C
29	Global dark signal non-uniformity standard deviation	NA	275	500	e-/s	At 25 ±2°C
30	Local photo response non-uniformity, standard deviation	NA	0.8	1.0	%	Of average response
31	Global photo response non-uniformity, standard deviation	NA	1.8	5	%	Of average response
32a	Image lag (soft reset)	NA	0.54	NA	-	
32b	Image lag (hard reset)	NA	–0.2	NA	-	
32c	Image lag (HTS reset)	NA	–0.15	NA	-	

Table 19. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT HIGH TEMPERATURE +85°C

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1	Total power supply current stand-by	17	20	23	mA	
2	Total power supply current, operational	35	38	41	mA	ADC at 5 MHz sampling rate
3	Power supply current to ADC, operational	17	19	21	mA	ADC at 5 MHz sampling rate
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	
7	Output impedance digital outputs	NA	NA	400	W	
8	Output impedance analog output	NA	NA	1	kΩ	
9	Output amplifier voltage range	2.2	2.45	2.6	V	
10	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
11	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
12	Output amplifier gain setting 2	3.7	4.0	4.3	-	Nominal 4 relative to setting 0
13	Output amplifier gain setting 3	7.0	7.5	8.0	-	Nominal 8 relative to setting 0
14	Output amplifier offset setting 0	0.89	0.94	1.0	V	0 decodes to middle value
15	Output amplifier offset setting 31	1.30	1.36	1.42	V	
16	Output amplifier offset setting 32	0.43	0.53	0.63	V	
17	Output amplifier offset setting 63	0.83	0.93	1.03	V	

Table 19. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT HIGH TEMPERATURE +85°C

No.	Characteristic	Min	Typ	Max	Unit	Remarks
18	ADC Differential nonlinearity	NA	8	11	lsb	
19	ADC Integral nonlinearity	NA	10	18	lsb	
20	Saturation voltage output swing	1.20	1.52	NA	V	VDD_RES = 3.3 V
21	Output range	0.8	NA	2.1	V	PGA in unity gain, offset = 0.8 V, low is dark, high is bright.
22a	Temporal noise (soft reset)	NA	66	110	e-	DR/DS
22b	Temporal noise (hard reset)	NA	85	125	e-	DR/DS
22c	Temporal noise (HTS reset)	NA	73	110	e-	DR/DS
23a	Temporal noise (NDR soft reset)	NA	200	400	e-	
23b	Temporal noise (NDR hard reset)	NA	170	300	e-	
23c	Temporal noise (NDR HTS reset)	NA	65	125	e-	
24	ADC quantization noise	NA	7	NA	e-	
25a	Local fixed pattern noise standard deviation (soft reset)	NA	82	160	e-	With DR/DS
25b	Local fixed pattern noise standard deviation (hard reset)	NA	95	160	e-	With DR/DS
25c	Local fixed pattern noise standard deviation (HTS reset)	NA	100	160	e-	With DR/DS
26a	Global fixed pattern noise standard deviation (soft reset)	NA	80	140	e-	With DR/DS
26b	Global fixed pattern noise standard deviation (hard reset)	NA	97	160	e-	With DR/DS
26c	Global fixed pattern noise standard deviation (HTS reset)	NA	115	300	e-	With DR/DS
27	Average dark signal	NA	41000	60000	e-/s	At +85 ±2°C die temp
28	Local dark signal non-uniformity standard deviation	NA	2800	4000	e-/s	
29	Global dark signal non-uniformity standard deviation	NA	3100	4500	e-/s	
30	Local photo response non-uniformity, standard deviation	NA	0.74	1.0	%	Of average response
31	Global photo response non-uniformity, standard deviation	NA	1.7	5	%	Of average response
32a	Image lag (soft reset)	NA	–0.13	NA	-	Soft reset
32b	Image lag (hard reset)	NA	–0.09	NA	-	Hard reset
32c	Image lag (HTS reset)	NA	–0.12	NA	-	HTS reset

Table 20. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT LOW TEMPERATURE –40°C

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1	Total power supply current stand-by	16	18	21	mA	
2	Total power supply current, operational	35	37	40	mA	ADC at 5 MHz sampling rate
3	Power supply current to ADC, operational	17	19	21	mA	ADC at 5 MHz sampling rate
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	

Table 20. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT LOW TEMPERATURE –40°C

No.	Characteristic	Min	Typ	Max	Unit	Remarks
7	Output impedance digital outputs	NA	NA	400	W	
8	Output impedance analog output	NA	NA	1	kΩ	
9	Output amplifier voltage range	2.2	2.45	2.6	V	
10	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
11	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
12	Output amplifier gain setting 2	3.8	4.1	4.4	-	Nominal 4 relative to setting 0
13	Output amplifier gain setting 3	7.2	7.7	8.2	-	Nominal 8 relative to setting 0
14	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
15	Output amplifier offset setting 31	1.30	1.35	1.40	V	
16	Output amplifier offset setting 32	0.43	0.51	0.6	V	
17	Output amplifier offset setting 63	0.80	0.90	1.0	V	
18	ADC differential nonlinearity	N/A	7	11	lsb	
19	ADC integral nonlinearity	N/A	11	18	lsb	
20	Saturation voltage output swing	1.20	1.49	NA	V	VDD_RES = 3.3 V
21	Output range	0.8	NA	2.1	V	PGA in unity gain, offset = 0.8 V, low is dark, high is bright.
22a	Temporal noise (soft reset)	NA	59	100	e-	DR/DS
22b	Temporal noise (hard reset)	NA	77	125	e-	DR/DS
22c	Temporal noise (HTS reset)	NA	70	125	e-	DR/DS
23a	Temporal noise (NDR soft reset)	NA	80	125	e-	
23b	Temporal noise (NDR hard reset)	NA	80	125	e-	
23c	Temporal noise (NDR HTS reset)	NA	75	125	e-	
24	ADC quantization noise	NA	7	NA	e-	
25a	Local fixed pattern noise standard deviation (soft reset)	NA	70	140	e-	With DR/DS
25b	Local fixed pattern noise standard deviation (hard reset)	NA	90	140	e-	With DR/DS
25c	Local fixed pattern noise standard deviation (HTS reset)	NA	100	160	e-	With DR/DS
26a	Global fixed pattern noise standard deviation (soft reset)	NA	70	140	e-	With DR/DS
26b	Global fixed pattern noise standard deviation (hard reset)	NA	95	140	e-	With DR/DS
26c	Global fixed pattern noise standard deviation (HTS reset)	NA	120	180	e-	With DR/DS
27	Average dark signal	NA	3.3	10	e-/s	
28	Local dark signal non-uniformity standard deviation	NA	6	20	e-/s	
29	Global dark signal non-uniformity standard deviation	NA	8	30	e-/s	
30	Local photo response non-uniformity, standard deviation	NA	0.8	1.0	%	Of average response measured

Table 20. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT LOW TEMPERATURE –40°C

No.	Characteristic	Min	Typ	Max	Unit	Remarks
31	Global photo response non-uniformity, standard deviation	NA	1.8	5	%	Of average response measured
32a	Image lag	NA	0.6	NA	-	Soft reset
32b	Image lag	NA	0.2	NA	-	Hard reset
32c	Image lag	NA	–1.2	NA	-	HTS reset

Table 21. PARAMETER DRIFT VALUES FOR BURN IN

Electrical and Electro-optical Measurements at Room Temperature +22°C

No.	Characteristic	Typical Value	Max Drift	Unit	Remarks
1	Total power supply current stand-by	18.5	2	mA	
2	Total power supply current, operational	37	3	mA	ADC at 5 MHz sampling rate
3	Power supply current to ADC, operational	19	2	mA	ADC at 5 MHz sampling rate
4	Power supply current to image core, operational	15.5	2	mA	
5	Output impedance digital outputs	NA	20	W	
6	Output impedance analog output	NA	20	W	
7	Output amplifier voltage range	2.45	0.3	V	
8	Output amplifier gain setting 0	1	N/A	-	Nominal 1 measured reference
9	Output amplifier gain setting 1	2.1	0.2	-	Nominal 2 relative to setting 0
10	Output amplifier gain setting 2	4.1	0.4	-	Nominal 4 relative to setting 0
11	Output amplifier gain setting 3	7.7	0.6	-	Nominal 8 relative to setting 0
12	Output amplifier offset setting 0	0.93	0.1	V	0 decodes to middle value
13	Output amplifier offset setting 31	1.35	0.1	V	
14	Output amplifier offset setting 32	0.51	0.1	V	
15	Output amplifier offset setting 63	0.90	0.1	V	
16	ADC Differential nonlinearity	7	2	lsb	
17	ADC Integral nonlinearity	8	2	lsb	
18	Saturation voltage output swing	1.49	0.2	V	VDD_RES=3.3 V
19	Output range	NA	0.2	V	PGA in unity gain, offset = 0.8 V, low is dark, high is bright.
20a	Temporal noise (soft reset)	55	+15	e-	Dark noise, with DR/DS, internal ADC
20b	Temporal noise (hard reset)	75	+15	e-	DARK noise, with DR/DS, internal ADC
20c	Temporal noise (HTS reset)	65	+15	e-	Dark noise, with DR/DS, internal ADC
21a	Temporal noise (NDR soft reset)	75	+15	e-	
21b	Temporal noise (NDR hard reset)	75	+15	e-	
21c	Temporal noise (NDR HTS reset)	70	+15	e-	
22	ADC quantization noise	7	NA	e-	
23a	Local fixed pattern noise standard deviation (soft reset)	70	+15	e-	With DR/DS
23b	Local fixed pattern noise standard deviation (hard reset)	110	+15	e-	With DR/DS

Table 21. PARAMETER DRIFT VALUES FOR BURN IN
Electrical and Electro-optical Measurements at Room Temperature +22°C

No.	Characteristic	Typical Value	Max Drift	Unit	Remarks
23c	Local fixed pattern noise standard deviation (HTS reset)	95	+30	e-	With DR/DS
24a	Global fixed pattern noise standard deviation (soft reset)	90	+15	e-	With DR/DS
24b	Global fixed pattern noise standard deviation (hard reset)	115	+15	e-	With DR/DS
24c	Global fixed pattern noise standard deviation (HTS reset)	110	+50	e-	With DR/DS
25	Average dark signal	190	+50	e-/s	At 25 ±2°C die temp
26	Local dark signal non-uniformity standard deviation	260	+50	e-/s	At 25 ±2°C
27	Global dark signal non-uniformity standard deviation	275	+50	e-/s	At 25 ±2°C
28	Local photo response non-uniformity, standard deviation	0.8	+0.1	%	Of average response
29	Global photo response non-uniformity, standard deviation	1.8	+0.3	%	Of average response
30a	Image lag (soft reset)	0.54	NA	-	
30b	Image lag (hard reset)	–0.2	NA	-	
30c	Image lag (HTS reset)	–0.15	NA	-	

Table 22. PARAMETER DRIFT VALUES FOR RADIATION TESTING
Electrical and Electro-optical Measurements at Room Temperature +22°C

No.	Characteristic	Typical Value	Max Drift	Unit	Remarks
1	Total power supply current stand-by	18.5	2	mA	
2	Total power supply current, operational	37	3	mA	ADC at 5 MHz sampling rate
3	Power supply current to ADC, operational	19	2	mA	ADC at 5 MHz sampling rate
4	Power supply current to image core, operational	15.5	2	mA	
5	Output impedance digital outputs	N/A	20	W	
6	Output impedance analog output	N/A	20	W	
7	Output amplifier voltage range	2.45	0.2	V	
8	Output amplifier gain setting 0	1	N/A	-	Nominal 1 measured reference
9	Output amplifier gain setting 1	2.1	0.2	-	Nominal 2 relative to setting 0
10	Output amplifier gain setting 2	4.1	0.3	-	Nominal 4 relative to setting 0
11	Output amplifier gain setting 3	7.7	0.5	-	Nominal 8 relative to setting 0
12	Output amplifier offset setting 0	0.93	0.1	V	0 decodes to middle value
13	Output amplifier offset setting 31	1.35	0.1	V	
14	Output amplifier offset setting 32	0.51	0.1	V	
15	Output amplifier offset setting 63	0.90	0.1	V	
16	ADC differential nonlinearity	7	1	lsb	
17	ADC integral nonlinearity	8	1	lsb	

Table 22. PARAMETER DRIFT VALUES FOR RADIATION TESTING
Electrical and Electro-optical Measurements at Room Temperature +22°C

18	Saturation voltage output swing	1.49	0.2	V	VDD_RES = 3.3 V
19	Output range	N/A	0.2	V	PGA in unity gain, offset = 0.8 V, low is dark, high is bright.
20a	Temporal noise (soft reset)	55	+30	e-	Dark noise, with DR/DS, internal ADC
20b	Temporal noise (hard reset)	75	+30	e-	Dark noise, with DR/DS, internal ADC
20c	Temporal noise (HTS reset)	65	+30	e-	Dark noise, with DR/DS, internal ADC
21a	Temporal noise (NDR soft reset)	75	+40	e-	
21b	Temporal noise (NDR hard reset)	75	+40	e-	
21c	Temporal noise (NDR HTS reset)	70	+40	e-	
22	ADC quantization noise	7	NA	e-	
23a	Local fixed pattern noise standard deviation (soft reset)	70	+200	e-	With DR/DS
23b	Local fixed pattern noise standard deviation (hard reset)	110	+100	e-	With DR/DS
23c	Local fixed pattern noise standard deviation (HTS reset)	95	+100	e-	With DR/DS
24a	Global fixed pattern noise standard deviation (soft reset)	90	+200	e-	With DR/DS
24b	Global fixed pattern noise standard deviation (hard reset)	115	+100	e-	With DR/DS
24c	Global fixed pattern noise standard deviation (HTS reset)	110	+100	e-	With DR/DS
25	Average dark signal	190	+6000	e-/s	At 25 ±2°C die temp
26	Local dark signal non-uniformity standard deviation	260	+1500	e-/s	At 25 ±2°C
27	Global dark signal non-uniformity standard deviation	275	+1500	e-/s	At 25 ±2°C
28	Local photo response non-uniformity, standard deviation	0.8	+0.1	%	Of average response
29	Global photo response non-uniformity, standard deviation	1.8	+0.3	%	Of average response
30a	Image lag (soft reset)	0.54	NA	-	
30b	Image lag (hard reset)	−0.2	NA	-	
30c	Image lag (HTS reset)	−0.15	NA	-	

Table 23. CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN−IN

No.	Characteristics	Symbol	Test Condition	Unit
Not applicable				

Table 24. CONDITIONS FOR POWER BURN−IN AND OPERATING LIFE TESTS

No.	Characteristics	Symbol	Test Condition	Unit
1	Ambient temperature	Tamb	125	°C
2	All power supplies	Vdd	3.3	V
3	Bias conditions		See Figure 49 on page 59 and next ones	
4	Clock frequency		10	MHz

Table 25. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING
Electrical and Electro-optical Measurements at Room Temperature +22°C

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1	Total power supply current stand-by	16	18.5	21	mA	
2	Total power supply current, operational	35	37	40	mA	ADC at 5 MHz sampling rate measured
3	Power supply current to ADC, operational	17	19	21	mA	at 5 MHz
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	
7	Output impedance digital outputs	NA	NA	400	W	
8	Output impedance analog output	NA	NA	1	kΩ	
9	Output amplifier voltage range	2.2	2.45	2.6	V	
10	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
11	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
12	Output amplifier gain setting 2	3.8	4.1	4.4	-	Nominal 4 relative to setting 0
13	Output amplifier gain setting 3	7.2	7.7	8.2	-	Nominal 8 relative to setting 0
14	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
15	Output amplifier offset setting 31	1.30	1.35	1.40	V	
16	Output amplifier offset setting 32	0.43	0.51	0.6	V	
17	Output amplifier offset setting 63	0.80	0.90	1.0	V	
18	ADC Differential nonlinearity	NA	7	11	lsb	
19	ADC Integral nonlinearity	NA	8	18	lsb	
20	Saturation voltage output swing	1.20	1.49	N/A	V	VDD_RES = 3.3 V
21	Output range	0.8	NA	2.1	V	PGA in unity gain, offset = 0.8 V, low is dark, high is bright.
22a	Temporal noise (soft reset)	NA	55	95	e-	DARK noise, with DR/DS, internal ADC
22b	Temporal noise (hard reset)	NA	75	125	e-	Dark noise, with DR/DS, internal ADC
22c	Temporal noise (HTS reset)	NA	65	110	e-	Dark noise, with DR/DS, internal ADC
23a	Temporal noise (NDR soft reset)	NA	75	100	e-	
23b	Temporal noise (NDR hard reset)	NA	75	100	e-	
23c	Temporal noise (NDR HTS reset)	NA	70	100	e-	
24	ADC quantization noise	NA	7	NA	e-	
25a	Local fixed pattern noise standard deviation (soft reset)	NA	70	140	e-	With DR/DS
25b	Local fixed pattern noise standard deviation (hard reset)	NA	110	160	e-	With DR/DS
25c	Local fixed pattern noise standard deviation (HTS reset)	NA	95	140	e-	With DR/DS

Table 25. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING
Electrical and Electro-optical Measurements at Room Temperature +22°C

No.	Characteristic	Min	Typ	Max	Unit	Remarks
26a	Global fixed pattern noise standard deviation (soft reset)	NA	90	140	e-	With DR/DS
26b	Global fixed pattern noise standard deviation (hard reset)	NA	115	180	e-	With DR/DS
26c	Global fixed pattern noise standard deviation (HTS reset)	NA	110	180	e-	With DR/DS
27	Average dark signal	NA	190	400	e-/s	At 25 ±2°C die temp
28	Local dark signal non-uniformity standard deviation	NA	260	400	e-/s	At 25 ±2°C
29	Global dark signal non-uniformity standard deviation	NA	275	500	e-/s	At 25 ±2°C
30	Local photo response non-uniformity, standard deviation	NA	0.8	1.0	%	Of average response
31	Global photo response non-uniformity, standard deviation	NA	1.8	5	%	Of average response
32a	Image lag (soft reset)	NA	0.54	NA	-	
32b	Image lag (hard reset)	NA	–0.2	NA	-	
32c	Image lag (HTS reset)	NA	–0.15	NA	-	

Table 26. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS DURING AND ON COMPLETION OF TOTAL-DOSE IRRADIATION TESTING (50krad)
Electrical and Electro-optical Measurements at Room Temperature +22°C

No.	Characteristic Symbol	Min	Typ	Max	Unit	Remarks
1	Total power supply current stand-by	16	18.5	21	mA	
2	Total power supply current, operational	35	37	40	mA	
3	Power supply current to ADC, operational	17	19	21	mA	ADC at 5 MHz sampling rate
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Output impedance digital outputs	NA	NA	400	W	
6	Output impedance analog output	NA	NA	1	kΩ	
7	Output amplifier voltage range	2.2	2.45	2.6	V	
8	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
9	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
10	Output amplifier gain setting 2	3.8	4.1	4.4	-	Nominal 4 relative to setting 0
11	Output amplifier gain setting 3	7.2	7.7	8.2	-	Nominal 8 relative to setting 0
12	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
13	Output amplifier offset setting 31	1.30	1.35	1.40	V	
14	Output amplifier offset setting 32	0.43	0.51	0.6	V	
15	Output amplifier offset setting 63	0.80	0.90	1.0	V	
16	ADC Differential nonlinearity	N/A	8	11	lsb	
17	ADC Integral nonlinearity	N/A	9	18	lsb	

Table 26. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS DURING AND ON COMPLETION OF TOTAL-DOSE IRRADIATION TESTING (50krad)

Electrical and Electro-optical Measurements at Room Temperature +22°C

No.	Characteristic Symbol	Min	Typ	Max	Unit	Remarks
18	Saturation voltage output swing	1.20	1.49	N/A	V	VDD_RES = 3.3 V
19	Output range	0.8	N/A	2.1	V	PGA in unity gain, offset = 0.8 V, low is dark, high is bright.
20	Temporal noise (soft reset)	NA	55	95	e-	Dark noise, with DR/DS, internal ADC
21	Temporal noise (hard reset)	NA	75	125	e-	Dark noise, with DR/DS, internal ADC
22a	Temporal noise (HTS reset)	NA	65	110	e-	Dark noise, with DR/DS, internal ADC
22b	Temporal noise (NDR soft reset)	NA	75	100	e-	
22c	Temporal noise (NDR hard reset)	NA	75	100	e-	
23a	Temporal noise (NDR HTS reset)	NA	70	100	e-	
23b	ADC quantization noise	NA	7	NA	e-	
23c	Local fixed pattern noise standard deviation (soft reset)	NA	70	350	e-	With DR/DS
24	Local fixed pattern noise standard deviation (hard reset)	NA	110	160	e-	With DR/DS
25a	Local fixed pattern noise standard deviation (HTS reset)	NA	95	200	e-	With DR/DS
25b	Global fixed pattern noise standard deviation (soft reset)	NA	90	350	e-	With DR/DS
25c	Global fixed pattern noise standard deviation (hard reset)	NA	115	180	e-	With DR/DS
26a	Global fixed pattern noise standard deviation (HTS reset)	NA	110	200	e-	With DR/DS
26b	Average dark signal	NA	5550	8730	e-/s	At 25 ±2°C die temp
26c	Local dark signal non-uniformity standard deviation	NA	260	2000	e-/s	At 25 ±2°C
27	Global dark signal non-uniformity standard deviation	NA	275	2000	e-/s	At 25 ±2°C
28	Local photo response non-uniformity, standard deviation	NA	0.8	1.0	%	Of average response
29	Global photo response non-uniformity, standard deviation	NA	1.8	5	%	Of average response
30	Image lag (soft reset)	NA	0.54	NA	-	
31	Image lag (hard reset)	NA	–0.2	NA	-	
32a	Image lag (HTS reset)	NA	–0.15	NA	-	

Table 27. ELECTRO−OPTICAL MEASUREMENTS ON THE OPTICAL BENCH

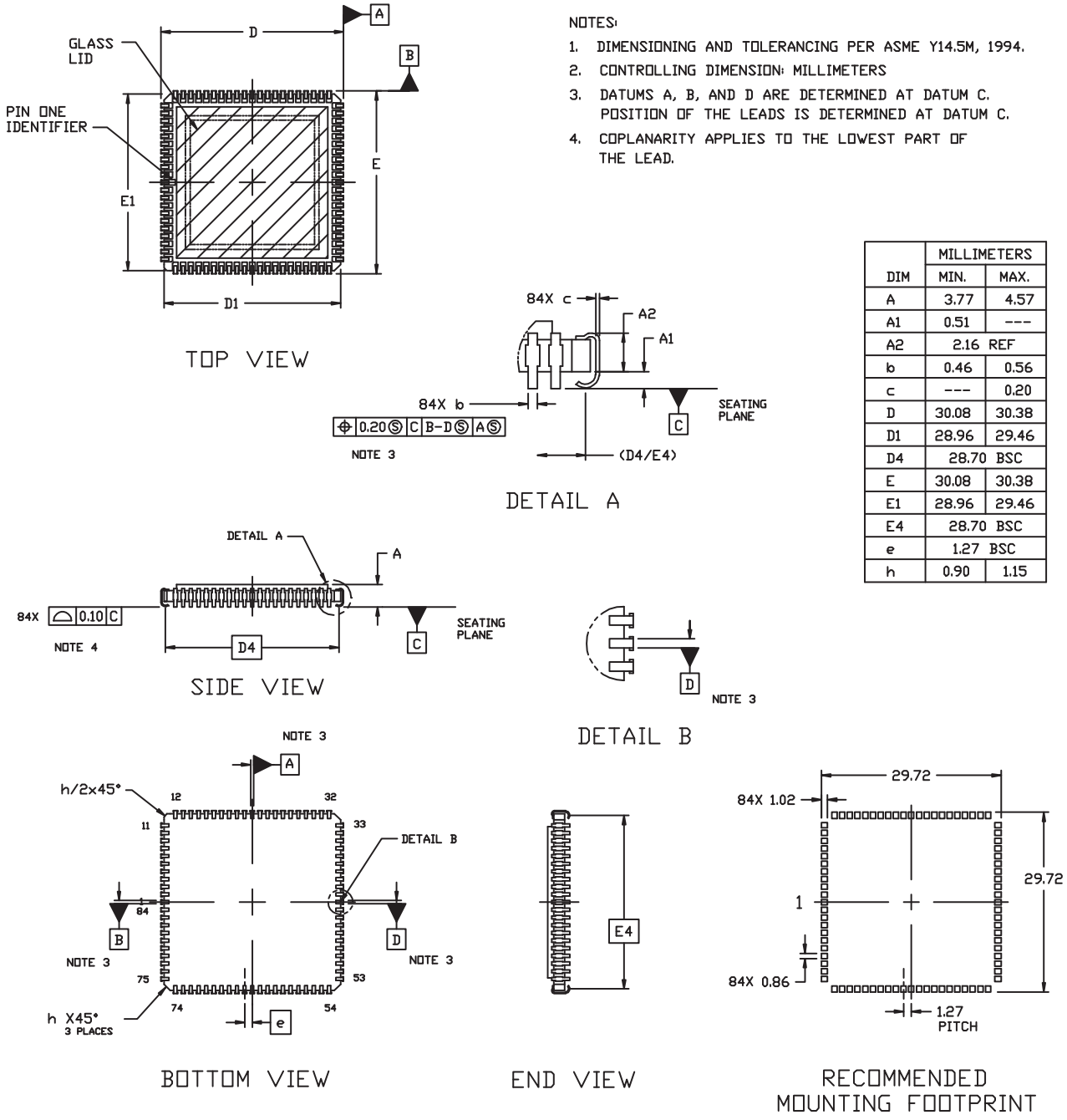
No.	Characteristic Symbol	Min	Typ	Max	Unit	Remarks
1	Linear range of pixel signal swing	40	50 0.75	NA	ke- V	Measured within ±1%
2	Linear range	60	82	NA	ke-	Measured within ±5%
3	Full well charge	90	100	NA	ke-	Measured VDD_RES = 3.3 V
4	Quantum efficiency x Fillfactor	NA	45	NA	%	Measured between 500 nm and 650 nm. See Specification Figures on page 25 for complete curve
5	Spectral Response	NA	33.3	-	%	Measured average over 400 nm − 900 nm.
6	Charge to voltage conversion factor	NA	16.9	-	μV/e-	at pixel
7	Charge to voltage conversion factor	13	14.8	15.6	μV/e-	Measured at output SIGNAL_OUT, unity gain
8	MTF X direction	NA	0.35	NA	-	at Nyquist measured
9	MTF Y direction	NA	0.35	NA	-	at Nyquist measured
10	Pixel to pixel crosstalk X direction	NA	9.8	NA	%	of total source signal − see Specification Figures on page 25 for 2−D plot
11	Pixel to pixel crosstalk Y direction	NA	9.8	NA	%	of total source signal − see Specification Figures on page 25 for 2−D plot
12	Anti-blooming capability	NA	1000	NA	Ke-	predicted value

Table 28. TYPICAL POWER SUPPLY SETTINGS AND SENSOR SETTINGS

Power Supply Settings	
ADC_VLOW	0.85 V
ADC_VHIGH	2.0 V
V_ADC_DIGITAL	3.3 V
V_ADC_ANALOG	3.3 V
VDDD	3.3 V
VDDA	3.3 V
VRES	3.3 V for SR / 4.2 V for HR
VPIX	3.3 V (for HTS switched to 0.75 V)
Sensor Settings	
Read Out Modes	Destructive − Nondestructive
Integration Time	195 μs
Gain Setting	Unity
Offset Setting	0
X Clock Period	100 ns

Specification Figures

JLDCC84
CASE 114AK
ISSUE A



DIM	MILLIMETERS	
	MIN.	MAX.
A	3.77	4.57
A1	0.51	---
A2	2.16 REF	
b	0.46	0.56
c	---	0.20
D	30.08	30.38
D1	28.96	29.46
D4	28.70 BSC	
E	30.08	30.38
E1	28.96	29.46
E4	28.70 BSC	
e	1.27 BSC	
h	0.90	1.15

Figure 4. 84−Pin JLCC Package Diagram