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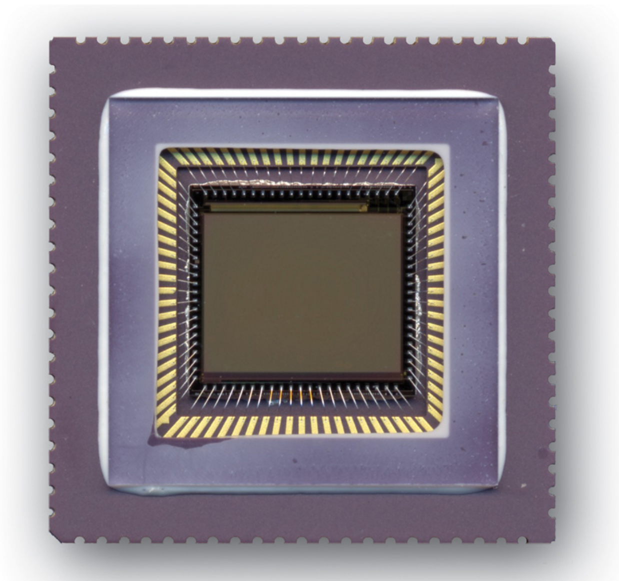
CYII4SM1300AA

IBIS4-1300 1.3 MPxl Rolling Shutter CMOS Image Sensor



Overview

The IBIS4-1300 is a digital CMOS active pixel image sensor with SXGA format.

Due to a patented pixel configuration a 60% fill factor and 50% quantum efficiency are obtained. This is combined with an on-chip double sampling technique to cancel fixed pattern noise.

Features

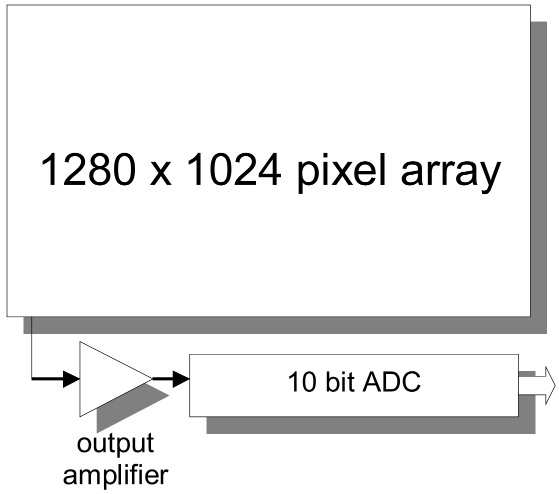
- SXGA resolution: 1280 x 1024 pixels
- High sensitivity 20 $\mu V/e^-$
- High fill factor 60%
- Quantum efficiency > 50% between 500 and 700 nm.
- 20 noise electrons = 50 noise photons
- Dynamic range: 69 dB (2750:1) in single slope operation
- Extended dynamic range mode (80…100 dB) in double slope integration
- On-chip 10 bit, 10 mega Samples/s ADC
- Programmable gain and offset output amplifier
- 4:1 sub sampling viewfinder mode (320x256 pixels)
- Electronic shutter
- 7 x 7 μm^2 pixels
- Low fixed pattern noise (1% Vsat p/p)
- Low dark current: 344 pA/cm^2
- (1055 electrons/s, 1 minute auto saturation)
- RGB or monochrome
- Digital (ADC) gamma correction

Ordering Information

Marketing Part Number	Description	Package
CYII4SM1300AA-QDC	Mono with Glass	84-pin LCC
CYII4SM1300AA-QWC	Mono without Glass	
CYII4SD1300AA-QDC	Color Diagonal with Glass	

Architecture of Image Sensor

Block Diagram



The IBIS4-1300 is an SXGA CMOS image sensor. The chip is composed of 3 modules: an image sensor core, a programmable gain output amplifier, and an on-chip 10 bit ADC.

Figure 1. shows the architecture of the image sensor core.

Figure 1. Architecture of Image Sensor Core

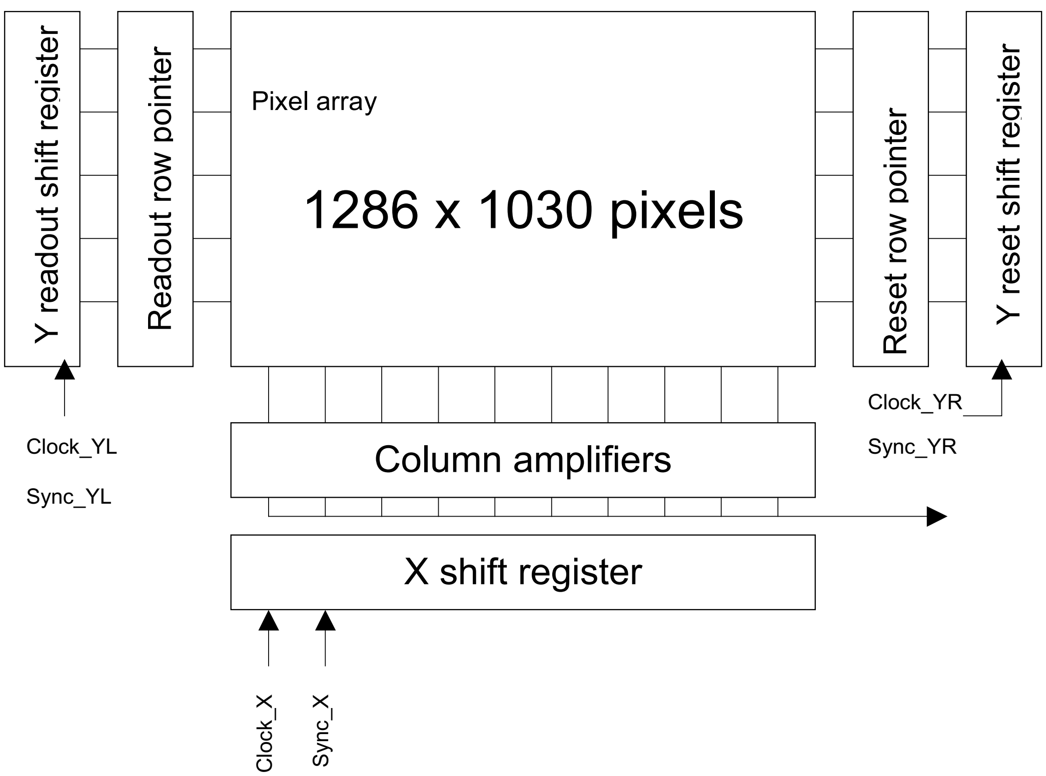
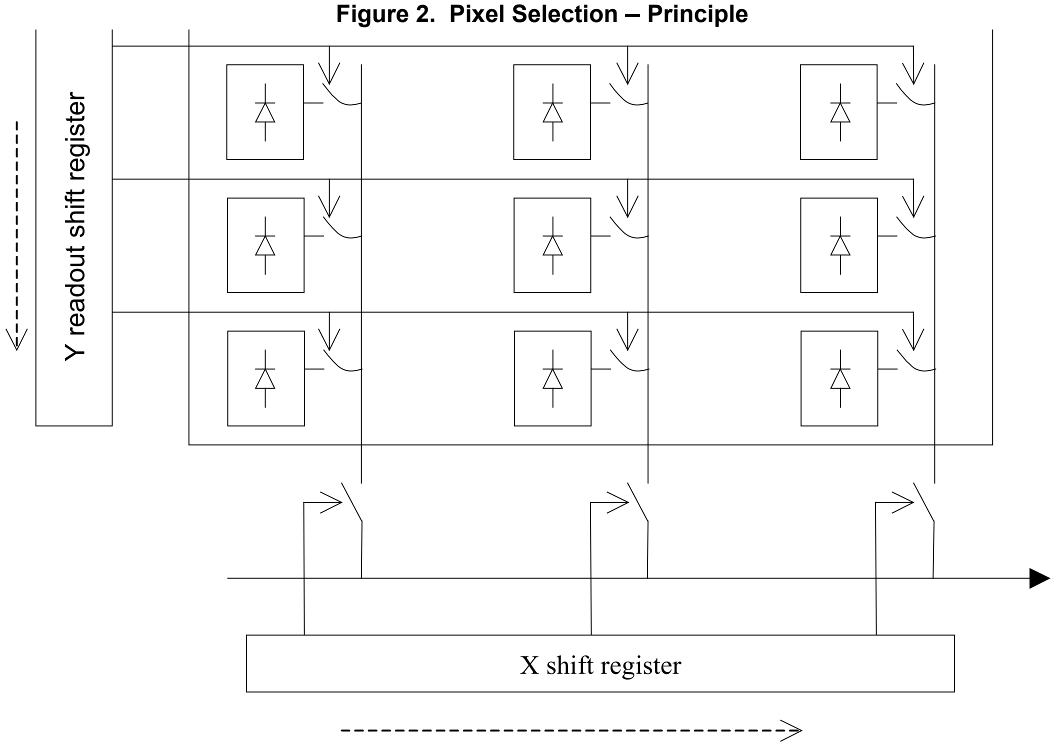


Image Sensor Core – Focal Plane Array

The core of the sensor is the pixel array with 1280 x 1024 (SXGA) active pixels. The name 'active pixels' refers to the amplifying element in each pixel.

This type of pixels offer a high light sensitivity combined with low temporal noise. The actual array size is 1286 x 1030 including the 6 dummy pixels in X and Y. Although the dummy pixels fall outside the SXGA format, their information can be used e.g. for color filter array interpolation.

Figure 2. Pixel Selection – Principle



Next to the pixel array there are two Y shift registers, and one X shift register with the column amplifiers. The shift registers act as pointers to a certain row or column. The Y readout shift register accesses the row (line) of pixels that is currently readout. The X shift register selects a particular pixel of this row. The second Y shift register is used to point at the row of pixels that is reset. The delay between both Y row pointers determines the integration time -thus realizing the electronic shutter.

A clock and a synchronization pulse control the shift registers. On every clock pulse, the pointer shifts one row/column further.

A sync pulse is used to reset and initialize the shift registers to their first position.

The smart column amplifiers compensate the offset variations between individual pixels. To do so, they need a specific pulse pattern on specific control signals before the start of the row readout.

Table 1. summarizes the optical and electrical characteristics of the image sensor. Some specifications are influenced by the output amplifier gain setting (e.g., temporal noise, conversion factor,...). Therefore, all specifications are referred to an output amplifier gain equal to 1.

Table 1. Optical and Electrical Characteristics

Pixel Characteristics	
Pixel structure	3-transistor active pixel
Photodiode	High fill factor photodiode
Pixel size	7 x 7 μm^2
Resolution	1286 x 1030 pixels SXGA plus 6 dummy rows and columns
Pixel rate with on-chip ADC	Nominal 10 MHz (Note 1) (Note 2)
Frame rate with on-chip ADC	About 7 full frames/s at nominal speed
Frame rate with analog output	Up to 23 full frames per second (see table1.1)

Table 1. Optical and Electrical Characteristics (continued)

Pixel Characteristics

Table 1.1. In this table you find achievable values using the analog output.

X pixels	Y pixels	X Freq	X Clock	X Blanking	line time	frame time	frame rate	pixel rate	pixel rate freq
#	#	Hz	sec	sec	sec	sec	per sec	sec	Hz
1286	1030	1,00E+07	1,00E-07	6,25E-06	0,000134850	0,138895500	7,20	1,049E-07	9536522
1286	1030	2,00E+07	5,00E-08	6,25E-06	0,000070550	0,072666500	13,76	5,486E-08	18228207
1286	1030	3,00E+07	3,33E-08	6,25E-06	0,000049117	0,050590167	19,77	3,819E-08	26182559
1286	1030	3,75E+07	2,67E-08	6,25E-06	0,000040543	0,041759633	23,95	3,153E-08	31719148
1286	512	3,75E+07	2,67E-08	6,25E-06	0,000040543	0,020758187	48,17	3,153E-08	31719148

Note
1. The pixel rate can be boosted to 37.5 MHz. This requires a few measures.
   - increase the analog bandwidth by halving the resistor on pin Nbias_oamp
   - increase the ADC speed by the resistors related to the ADC speed (nbiasana1, nbiasana2, pbiasencload)
   - experimentally fine tune the relative occurrence of the ADC clock relative to the X-pixel clock.

Note
2. The pure digital scan speed in X and Y direction is roughly 50 MHz. This is maximum speed for skipping rows and columns.

Light Sensitivity and Detection	
Spectral sensitivity range	400 - 1000 nm
Spectral response * fill factor	0.165 A/W at 700 nm
Quantum efficiency * fill factor	> 30% between 500 and 700 nm
Fill factor	60%
Charge-to-voltage conversion gain	20 $\mu V/e^-$
Output signal amplitude	1.2 V
Full well charge [electrons]	IBIS4-1300: about 90000 saturation, 50000 linear range
Noise equivalent flux at focal plane (700 nm)	1.1e-4 lx*s (at focal plane) 6.3 e-7 s.W/m2
Sensitivity	7 V/lx.s 1260 V.m2/W.s
MTF at Nyquist frequency	0.4-0.5 at 450 nm 0.25-0.35 at 650 nm
Optical cross talk	10% to 1st neighbor 2% to 2nd neighbor
Image Quality	
Temporal noise (dark, short integration time)	20 noise electrons = 50 peak noise photons[3] 400 μV RMS
Dynamic range (analog output, before ADC conversion)	2750:1 69 dB
Dark current	344 pA/cm^2 at 21ºC 19 mV/s 1055 electrons/s
Dark current non-uniformity	Typically 15% RMS of dark current level.
Fixed pattern noise (dark, short integration time)	9.6 mV peak-to-peak 1-2 mV RMS
Photo-response non-uniformity (PRNU)	10% peak-to-peak at ½ of saturation signal
Yield criteria	No missing columns nor rows Less than 100 missing pixels, clusters=<4 pixels

Table 1. Optical and Electrical Characteristics (continued)

Pixel Characteristics	
Anti-blooming	Overexposure suppression > 105
Smear	Absent
Note 3. Peak noise photons are defined as (noise electrons) / (FF*peak QE).	
Features and General Specifications	
Electronic shutter	Rolling curtain type Increment = line time = 135 µs
Viewfinder mode	4 x sub-sampling (320 x 256 pixels)
Digital output	10 bit
Color filter array	Primary colors (Red, Green, Blue) RGB diagonal stripe pattern or Bayer pattern
Die size	10.30 x 9.30 mm^2
Package	84 pins LCC chip carrier 0.460 inch cavity
Supply voltage	5 V stabilized (e.g. from a 7805 regulator)
Power supply feed trough (dVout/dVdd)	< 0.3 for low-frequencies (< 1 MHz) < 0.05 for high frequencies (> 1 MHz)
Power dissipation (continuous operation, 10 MHz, ADC outputs loaded)	Min. 50 mA, Typ. 70 mA, Max. 90 mA

Light Sensitivity

Figure 3. Spectral Response * Fill Factor of IBIS4-1300 Pixels

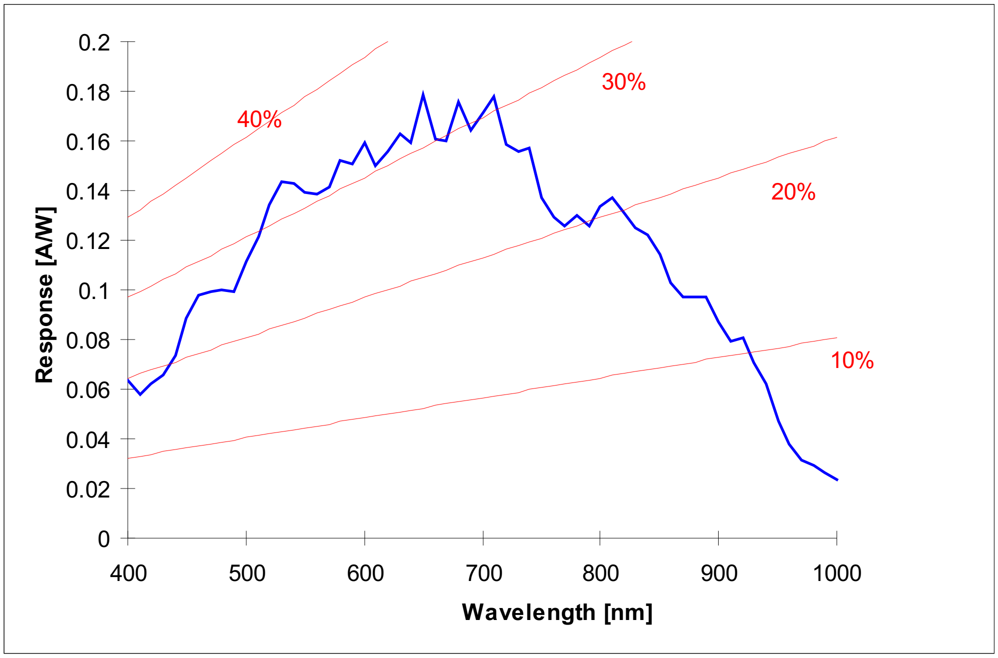
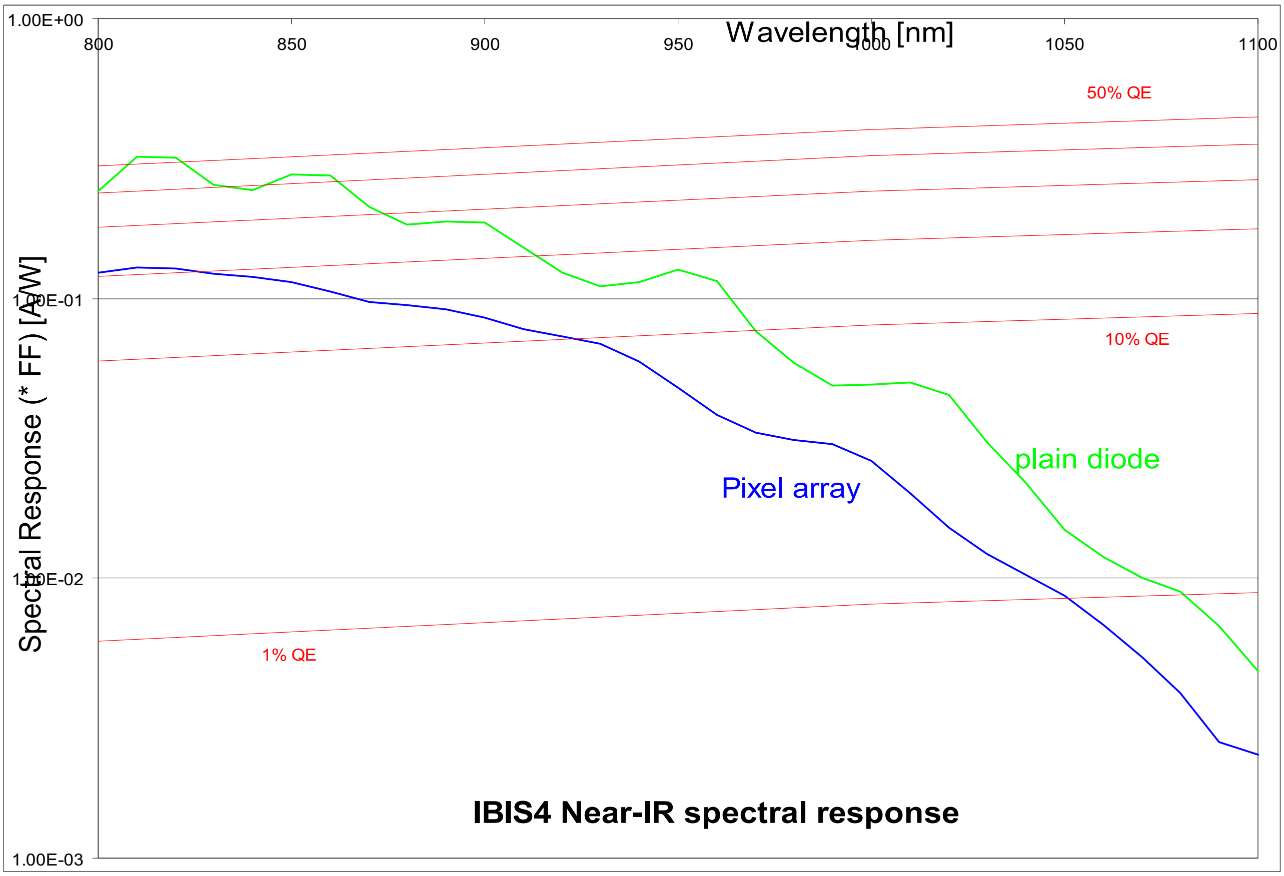


Figure 3. shows the spectral response characteristic. The curve is measured directly on the pixels. It includes effects of non-sensitive areas in the pixel, e.g., interconnection lines. The sensor is light sensitive between 400 and 1000 nm. The peak QE * FF is more than 30% between 500 and 700 nm. In view of a fill factor of 60%, the QE is thus larger than 50% between 500 and 700 nm.

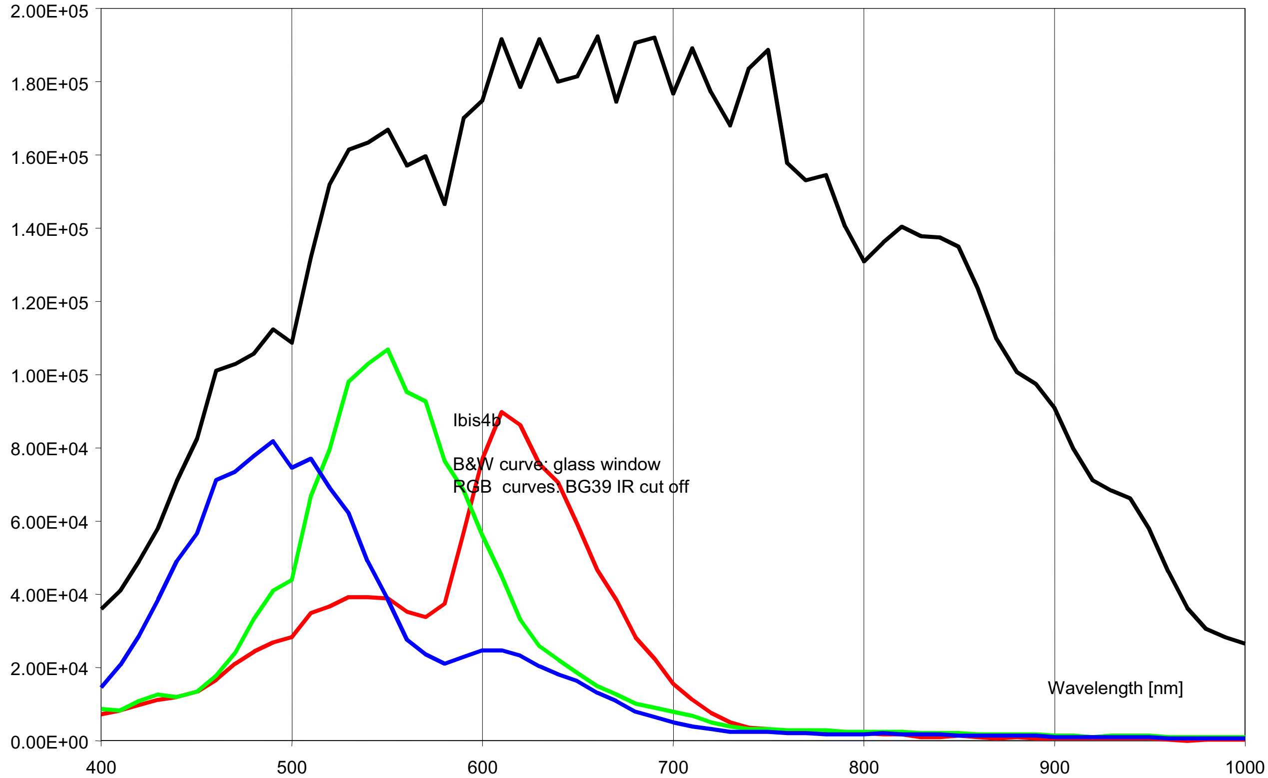
Figure 4. Near Infrared Spectral Response



Calculation of Sensitivity in [V/lx.s]

Pixel area A	49 E-12 m2
Fill factor FF	60%
Spectral response SR	0.22 A/W (average)
FF*SR	0.13 A/W (average over wavelength)
Pixel capacitance Ceff	5E-15 F
Sensitivity = FF*SR*Ceff/A	1.27E+3 [V.W/s.m2]
Conversion to lux: 1W/m2 =	About 180 lux, visible light only About 70 lux, including Near Infrared
Sensitivity in lux units:	7.08 [V/lx.s] visible light only 18 [V/lx.s] if near IR included

Color Sensitivity



Charge Conversion – Conversion of Electrons in an Output Signal

Figure 5. IBIS4-1300 Response Curve – Two Pixels – Lowest Gain Setting (0000)

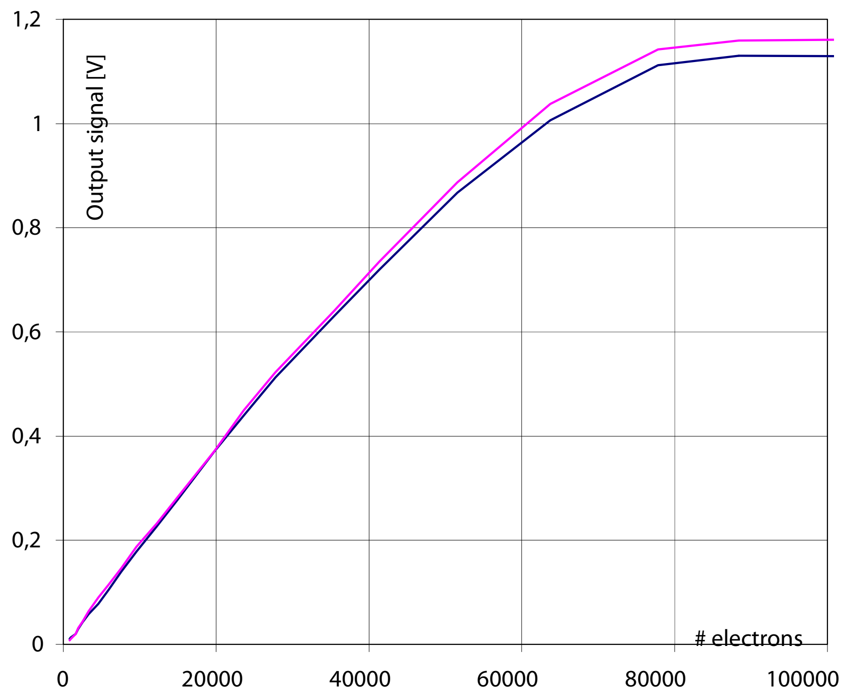


Figure 5. shows the pixel response curve in linear response mode. This curve is the relation between the electrons detected in the pixel and the output signal. This curve was measured with light of 600 nm, with an integration time of 138.75 ms (10 MHz pixel rate), at minimal gain setting 0000. The resulting voltage/electron curve is independent of these parameters. The conversion gain is 18 µV/electron for this gain setting.

Note that the upper part of the curve (near saturation) is actually a logarithmic response, similar to the FUGA1000 sensor.

The level of saturation can be adjusted by the voltage on GND-AB. However, note also that this logarithmic part of the response is not FPN corrected by the on-chip offset correction circuitry.

The signal swing (and thus the dynamic range) is extended by increasing the Vdd_reset (pins 59/79) To 5.5V. This is mode of operation is not further documented.

Table 2. shows the pins of the IC that are related to the image sensor core, describing their functionality.

Table 2. Pins of the Image Sensor Core

Digital Controls		
SYNC_YR\	5	Reset right Y shift register (low active, 0 = sync)
CLK_YR	6	Clock right Y shift register (shifts on falling edge)
EOS_YR\	7	(output) low 1st CLK_YR pulse after last row (low active)
SYNC_X\	28	Reset X shift register (low active, 0 = sync)
CLK_X	29	Clock X shift register (shifts on falling edge)
EOS_X\	8	(output) Low 1st CLK_X pulse after last active column (low active)
SYNC_YL\	36	Reset left Y shift register (low active, 0 = sync)
CLK_YL	37	Clock left Y shift register (shifts on falling edge)
EOS_YL\	38	Low 1st CLK_YL pulse after last row
SHY	30	Parallel Y track & hold (1 = hold, 0 = track) apply pulse pattern - see sensor timing diagram
SIN	35	Column amplifier calibration pulse 1 = calibrate - see sensor timing diagram
SELECT	40	Selects row indicated by left/right shift register high active (1= select row) Apply 5 V DC for normal operation
RESET	41	Resets row indicated by left/right shift register high active (1 = reset) Apply pulse pattern - see timing diagram
L/R\	80	Use left or right register for SELECT and RESET 1 = left / 0 = right - see sensor timing
SUBSMPL	84	Activate viewfinder mode (1:4 sub sampling = 320 x 256 pixels) high active, 1 = sub sampling
Reference Voltages		
DCCON	31	Control voltage for the DCREF voltage generation Connect to ground by default
DCREF	32	Reference voltage (output), to be decoupled to GND Should be about 1.2V, can be adjusted by DCCON
NBIASARRAY	1	1 MegaOhm to VDD and decouple to ground by 100 nF capacitor
PBIAS2	2	1 MegaOhm to ground and decouple to VDD by 100 nF capacitor
PBIAS	3	1 MegaOhm to ground and decouple to VDD by 100 nF capacitor
XMUX_NBIAS	4	100K to VDD and decouple to ground by 100 nF capacitor
GND_AB	54	Anti-blooming drain control voltage ■ Default: connect to ground. The anti blooming is operational but not maximal. ■ Apply about 1 V DC for improved anti-blooming

Table 2. Pins of the Image Sensor Core (continued)

Digital Controls		
Power and Ground		
VDD_RESETL	59	Power supply for left reset line drivers apply 5 V DC (default) or about 4…4.5 V for dual slope mode
VDD_RESETR	79	Power supply for right (default) reset line drivers 5 V DC
VDD_ARRAY	55	Power supply for the pixel array 5 V DC
VDD	11 34 53 77	Power supply of image sensor core & output amplifier 5 V DC
GND	10 33 52 78	Ground of image sensor core & output amplifier

Output Amplifier

The output amplifier stage is user-programmable for gain and offset level. Gain and offset are controlled by 4-bit wide words. Gain settings are on an exponential scale. Offset is controlled by a 4-bit wide DAC, which selects the offset voltage between 2 reference voltages (Vhigh_dac and Vlow_dac) on a linear scale.

The offset setting is independent of the gain setting.

The gain setting is independent of amplifier bandwidth.

The amplifier is designed to match the specifications like the output of the imager array. This signal has a data rate Of 10 MHz and is located between 1.2 and 2.4V. Table 3. Summarizes the specifications of the amplifier.

Table 3. Summary of Output Amplifier Specifications

	Min.	Typ	Max
Gain	1.2 (gain setting 0)	2.7 (setting 4)	16 (setting 15)
Output Signal Range	1 V		4.5 V
Bandwidth (40 pF Load)	12 MHz (gain setting 15)	22 MHz (gain setting 0...8)	33 MHz (gain setting 0)
Output Slew Rate (40 pF Load)	40 V/ µs	50 V/µs	80 V/µs

The range of the output stage input is between 1 and 4V. A lowest gain the sensor outputs a signal in between 1.2 and 2.2V, which fits into the input range of the amplifier. The range of the output signal is between 1 and 4.5V, dependent on the gain and offset settings of the amplifier. This range should fit to the input range of the ADC, external or internal. The on-chip ADC range is between 2 and 4V. A minimal gain setting of "3" seems necessary for the internal ADC, and the offset voltage should be set to the low-reference voltage of the ADC.

Figure 6. Output Amplifier Architecture

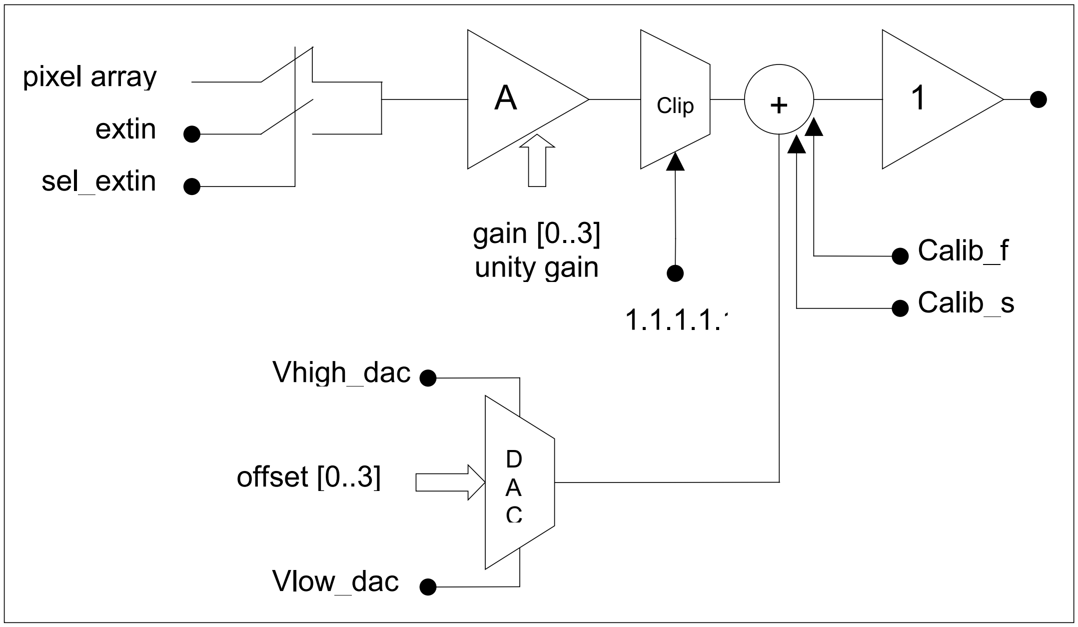


Figure 6. shows the architecture of the output amplifier. First of all, there is a multiplexer which selects either the imager core signal or an external pin EXTIN as the input of the amplifier. EXTIN can be used for evaluation, or to feed alternative data to the output.

SEL_EXTIN controls this switch.

Then, the signal is fed to the first amplifier stage. This stage has an adjustable gain, controlled by a 4-bit word ('gc_bit0...3').

Then, the upper level of the signal must be clipped in some situations (clipping sometimes is necessary when the imager signal is highly saturated, which affects the calibration level. This is visible as black banding at the right side of bright objects in the scene). In order to do this, a voltage should be applied to the 'Clip' pin. The signal is clipped if it is higher than Vclip - Vth,pmos, where Vth,pmos is the PMOS threshold voltage and is typically -1 V. If clipping is not necessary, 5 V should be applied to 'Clip'.

After this, the offset level is added. This offset level is set by a DAC, controlled by a 4-bit word (DAC_bit0...3). The offset level can be calibrated in two modes: fast offset adjustment or slow offset adjustment. This is controlled by 'calib_s' and 'calib_f'. The slow adjustment yields a somewhat cleaner image.

After this, the signal is buffered by a unity feedback amplifier and it leaves the chip. This 2nd amplifier stage determines the maximal readout speed, i.e., the bandwidth and the slew rate of the output signal. The whole amplifier chain is designed for a data rate of 10 Mpix/s (at 40 pF). (It is up to the experimenter to increase this speed by reducing the various setting resistors)

Table 4. shows the IBIS4-1300 pins used by the output amplifier with a short functional description. Power and ground lines are shared between the output amplifier and the image sensor.

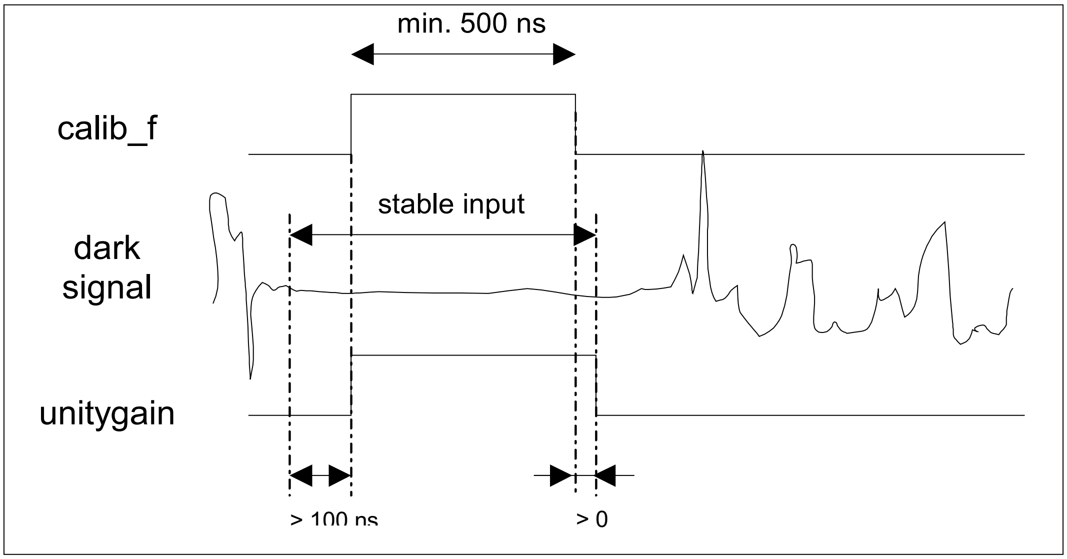
Output Amplifier Offset Level Adjustment

The purpose of this adjustment is to bring the pixel voltage range as good as possible within the ADC range. The offset level of the output signal is controlled by a 4-bit resistive DAC. This DAC selects the offset level on a linear scale between 2 reference voltages. These reference voltages are applied to Vlow_dac and Vhigh_dac.

This offset level is adjusted during the calibration phase. During this phase, the amplifier input should be constant and refers to the 'zero' signal situation. The IBIS4-1300 outputs a dark reference signal after a row has been read out completely. This signal can be used as the 'zero signal' reference. Alternatively one can apply an external reference on pin EXTIN, which is applied to the output amplifier when SEL_EXTIN is 1.

Offset adjustment can be done during row or frame blanking time.

Figure 7. Offset Adjustment: Fast Offset Adjustment Mode



There are 2 modes of offset calibration for the output amplifier: slow and fast adjustment. Figure 7. shows the timing and signal waveforms for fast offset adjustment mode. Closing both 'calib_f' and 'unitygain' operates it. After 'calib_f' is opened again, the offset level is adjusted to the desired value in a single cycle. The signal applied to the output amplifier should be stable just before and during the adjustment phase. The same is true for the DAC output.

The signal applied to the output amplifier can be either:

- The signal generated by the electrical dark reference in the imager core itself, i.e., the pixels named "dark" in Figure 20.
- Apply the reference from outside on the pin EXTIN, controlled by SEL_EXTIN.

If this fast offset adjustment is used, it should be done once each frame, before the readout of the frame starts, e.g., during the blanking time of the first line.

Figure 8. Slow Offset Adjustment Mode

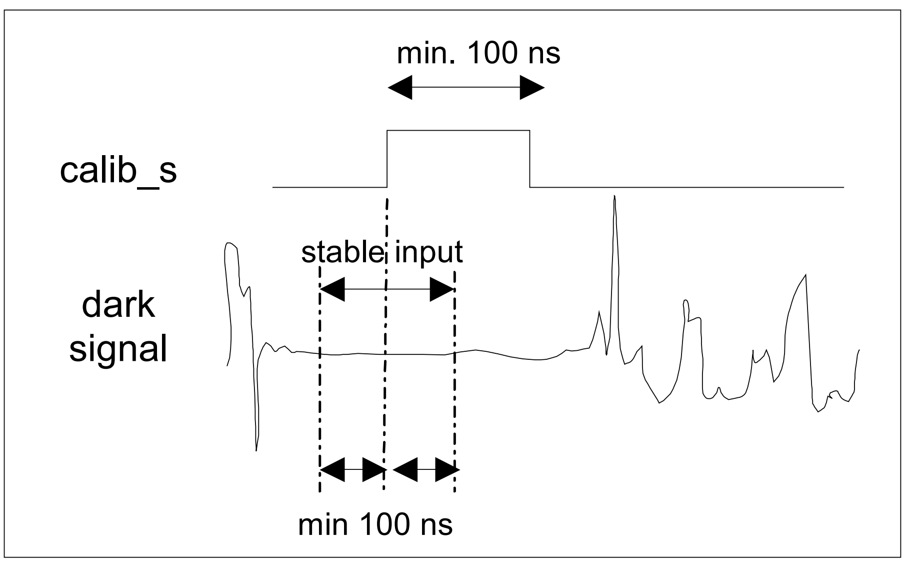


Figure 8. shows the timing and signal waveforms for slow offset adjustment mode. It is operated by pulsing 'calib_s'. The amplifier input signal must be stable and refer to 'dark' signal at the moment when calib_s goes low. The offset is slowly adjusted with a time constant of about 100 of these pulses. One pulse is then generated during each row blanking time.

The baseline is to use the fast calibration once per image. The slow calibration is intended as alternative if, for very slow readout, the offset drifts during the image.

Table 4. Pins Involved in Output Amplifier Circuitry

Name	No.	Function
Analog Signals		
Extin	12	External input of the output amplifier Active if Sel_extin = 1
Output	13	Analog output signal To be connected to the input of the ADC (in_adc, pin 73)
Digital Controls		
Sel_extin	9	1 = external input pin (extin) is applied at the input of the amplifier 0 = output amplifier is connected to the image sensor array
gc_bit0	17	LSB Control bits for output amplifier gain setting Gain adjustment between 1.2 (0000) & 16X (1111) MSB
gc_bit1	18	
gc_bit2	19	
gc_bit3	20	
unitygain	21	1 = output amplifier in unity feedback mode 0 = output amplifier gain controlled by gc_bit0...3
calib_s	16	Slow (or incremental) output offset level adjustment (calibration of output amplifier). Offset adjustment converges after about 100 pulses on calib_s Amplifier input should refer to a 'zero signal' at the moment of the 1->0 transition on calib_s 0 = connect to capacitor (of stage 2) and in- (of stage 1) 1 = connect to DAC output (of stage 2) and out (of stage1)
calib_f	22	Fast (=in 1 cycle) output offset level adjustment (calibration of output amplifier) Offset level is adjusted when both calib_f and unitygain are high Amplifier input should refer to 'zero signal' when calib_f is high 1 = connect DAC output to offset of capacitor 0 = DAC output disconnected
dac_b0	26	LSB Control bits for output offset level adjustment Between Vlow_dac (0000) & Vhigh_dac (1111) MSB
dac_b1	25	
dac_b2	24	
dac_b3	23	
Reference Voltages		
Vlow_dac	14	Low and high references for offset control DAC of the analog output. The range of this resistive division DAC should be about 1V to 2.5V. If the range is not OK, one will notice that it is not possible to adjust the output voltage to the appropriate level of the ADC. As the internal division resistor is about 1.3 Kohm, we suggest to tie Vlow_dac with 1K to GND and Vhigh_dac with 2K7 to VDD.
Vhigh_dac	15	
Nbias_oamp	27	Output amplifier speed/power. Connect with 100 K to VDD and decouple with 100 nF to GND. This setting yields 10 MHz nominal pixel rate. Lowering the resistance does increasing this rate.
Clip	83	Voltage that can be used to clip the output signal Clips output if output signal > 'Vclip - Vth, PMOS' with Vth,PMOS=-1V Default: 5 V (no clipping)

Output Amplifier Gain Control

Figure 9. Output Amplifier DC Gain

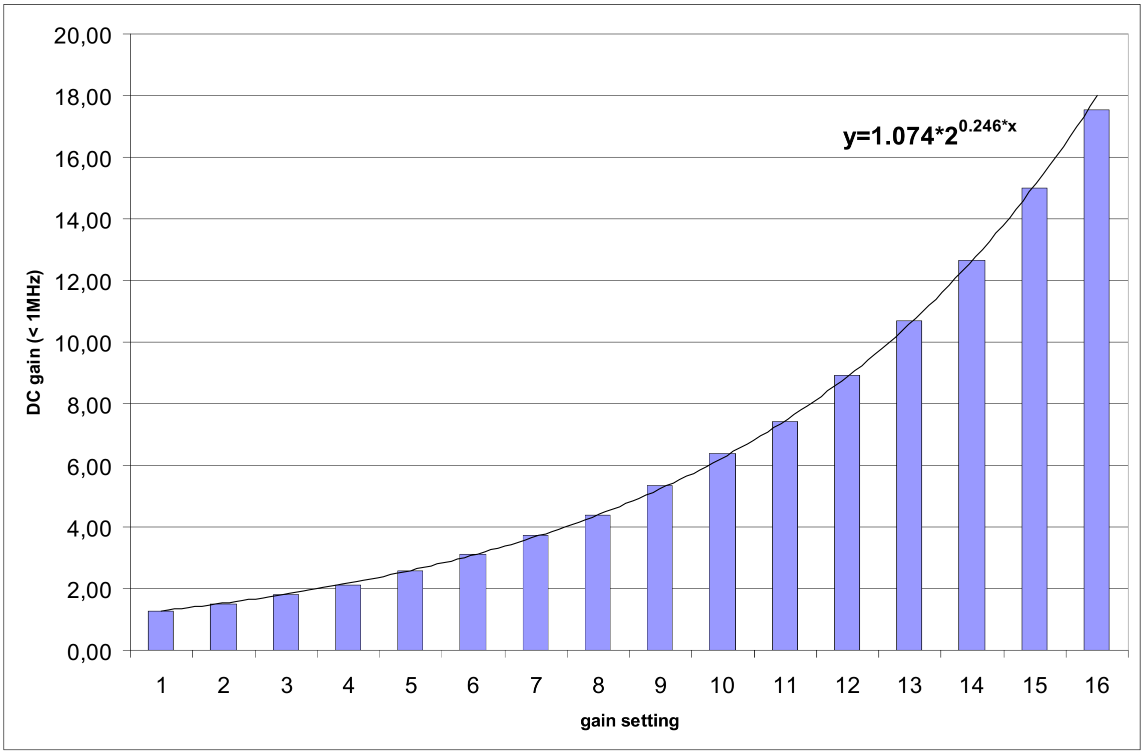


Table 5. DC Gain of Output Amplifier for Different Gain Settings

Gain Setting	DC Gain (<1 MHz)	Gain Setting	DC Gain (<1 MHz)
0000	1.28	1000	5.33
0001	1.51	1001	6.37
0010	1.82	1010	7.41
0011	2.13	1011	8.91
0100	2.60	1100	10.70
0101	3.11	1101	12.65
0110	3.71	1110	15.01
0111	4.40	1111	17.53

The output amplifier gain is controlled by a 4-bit word. In principle, the output amplifier can be configured in unity feedback mode by a permanent high signal on UNITYGAIN, but the purpose of this mode is purely diagnostic. The "normal" gain settings vary on an exponential scale. Figure 9. and Table 5. report all gain settings.

In first approximation, the gain setting is independent of bandwidth, as the amplifier is a 2-stage design. The first stage sets the gain, and the second stage is a unity gain buffer, that determines bandwidth and slew rate. There is however some influence of gain setting on bandwidth. Figure 10. shows the output amplifier bandwidth for all gain settings.

Figure 10. Output Amplifier Bandwidth for Different Gain Settings

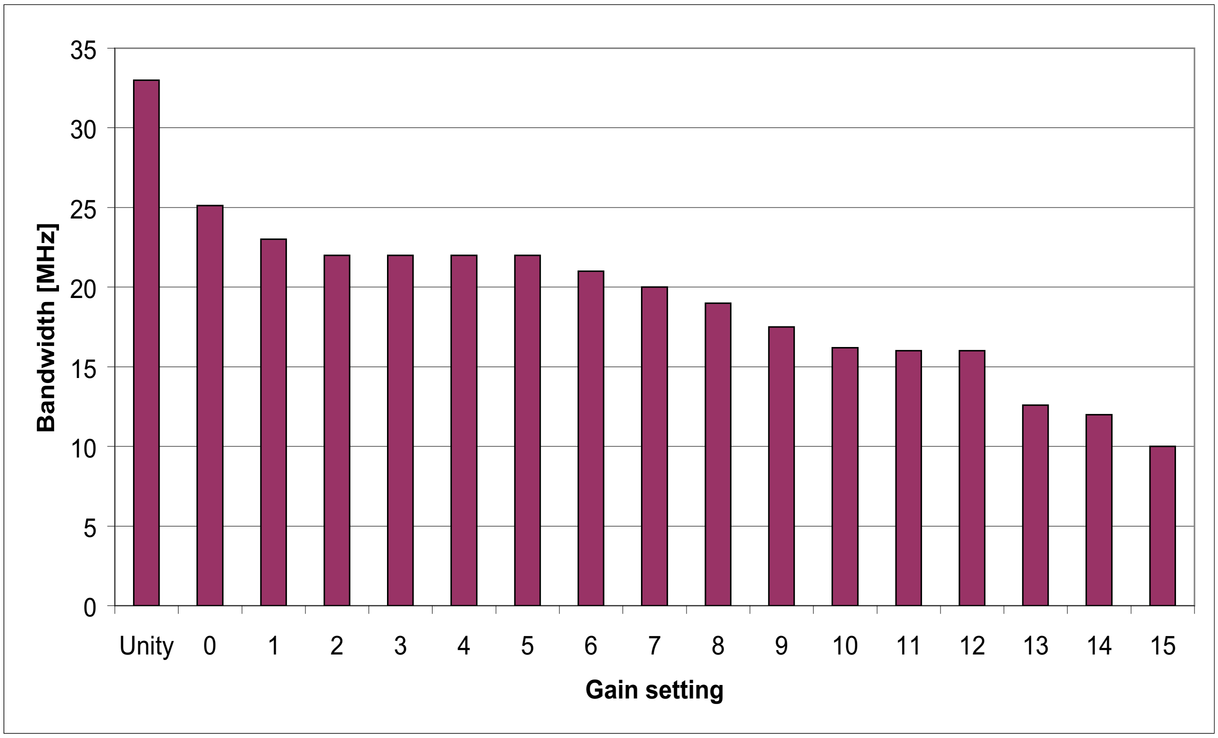


Figure 11. Typical Transfer Characteristic of Output Amplifier (no Clipping, Voffset = 2 V, Input Signal During Offset Adjustment is 1.2 V)

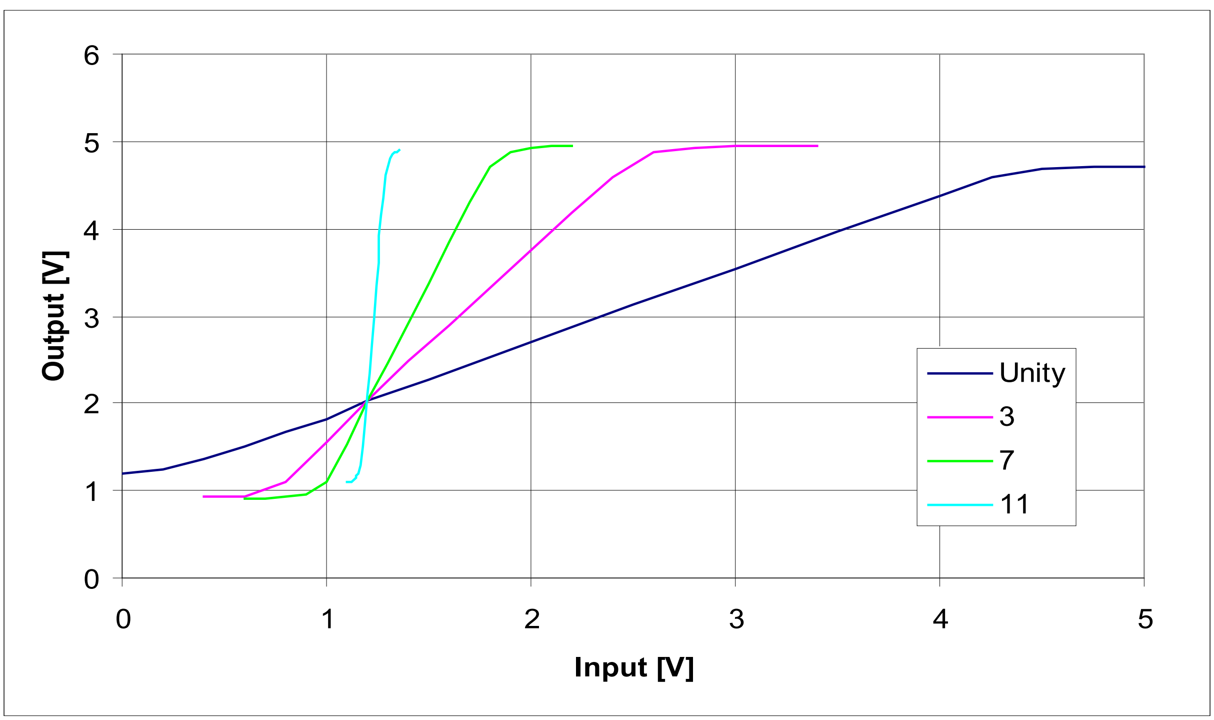
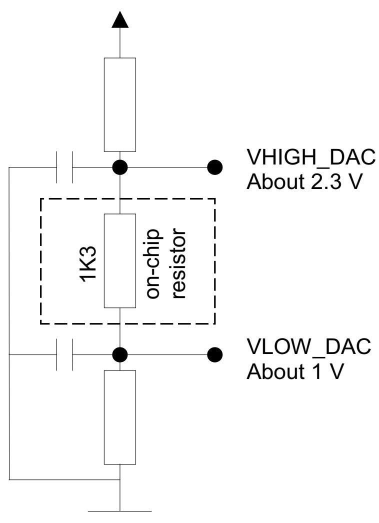


Figure 11. shows the output characteristic curve in a typical case for the imager. The offset voltage is adjusted to 2 V, which corresponds to the low-level voltage of the ADC. Clipping is off, and the input signal is changed between 0 and 5 V. During offset adjustment (when calib_s is switched from 1 -> 0 or when calib_f is on), the input signal is at 1.2 V. This level corresponds to the imager dark reference output. The input signal is transferred to the output by adding a 2V offset and multiplication with the appropriate gain. The input signal of dark pixels (at 1.2 V) corresponds with 2 V at the output. Higher input signals are amplified. The curves for 3 typical gain settings are shown (unity gain, setting 3, 7, and11).

Again, as can be seen on the above figure, the applied input signal during the output amplifier calibration (by 'CALIB_S' or 'CALIB_F') is the reference level to which the signal is amplified. During this calibration, a stable input is required.

Setting of the VLOW_DAC and VHIGH_DAC Reference Voltages

Figure 12. Suggested Circuit for High and Low References of DAC



VLOW_DAC & VHIGH_DAC are the reference voltages for the DAC. They represent the 0000 resp. 1111 code. The internal series resistance is about 1.3 kOhms. They can be connected as in Figure 12., and decoupled to ground.

Analog-to-Digital Converter

The IBIS4-1300 has a 10-bit Flash analog-to-digital converter running nominally at 10 Msamples/s. The ADC is electrically separated from the image sensor. The input of the ADC ("IN_ADC") should be tied externally to the OUTPUT of the output amplifier.

Table 6. ADC Specifications

Input range	2 to 4V
Quantization	10 Bits
Nominal data rate	10 Msamples/s[4]
DNL (linear conversion mode)	
INL (linear conversion mode)	
Input capacitance	< 20 pF
Power dissipation at 10 MHz	107 mA, 535 mW
Delay of digital circuitry (Td, 40 pF load)	< 50 ns after falling edge of clock
Input setup time (Ts) for a stable LSB	< 100 ns before falling edge of clock
Conversion law	Linear / Gamma-corrected

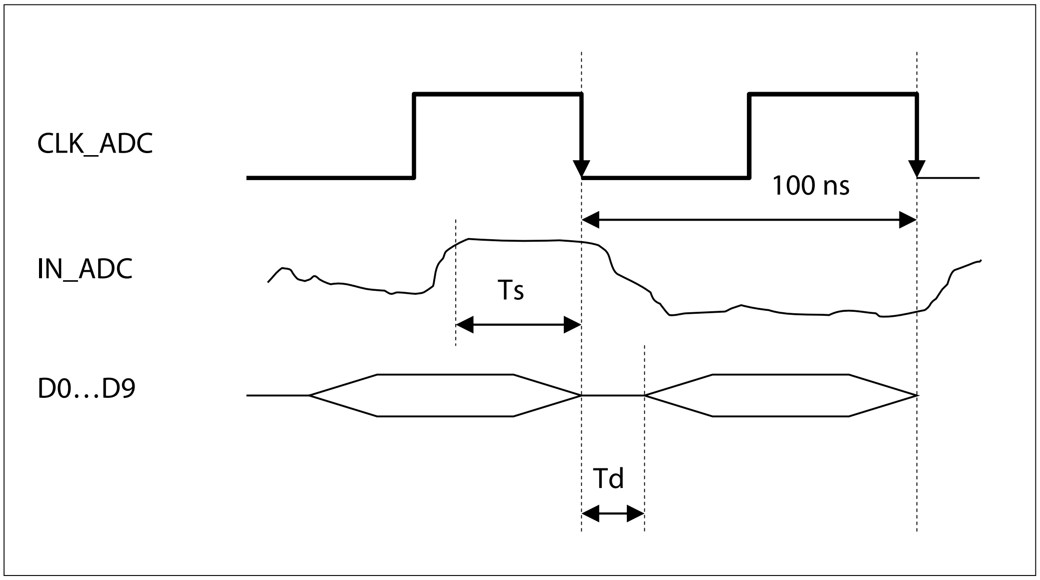
Note

4. Project partners have demonstrated 20 MHz data rate by careful timing and by decreasing some or all of the resistors on NBIAS* and PBIAS*.

ADC Timing

The ADC converts on the falling edge of the CLK_ADC clock. The input signal should be stable during a time Ts before the falling clock edge. The digital output is available Td after the falling clock edge (Figure 13., Ts = 100 ns, Td = 50 ns). These values are the delays to obtain a stable LSB after a half-scale swing of the input signal. For the MSB to become stable, Ts=20 ns is sufficient. For a full scale input swing (which normally doesn't appear with image sensors), Ts is 140 ns for the LSB and 20 ns for the MSB.

Figure 13. ADC Timing



TRI_ADC can be used to put the output bits in a tristate mode (e.g., for bidirectional buses). If this is used, the output signal becomes valid 50 ns after the falling edge on TRI_ADC.

BITINVERT can be used to invert the output word, if necessary (one's complement). When NONLINEAR is high, the ADC conversion is non-linear. The contrast will be higher in dark image regions, and lower in bright areas, similar to gamma correction.

Table 7. ADC Pins

Name	No.	Description
Analog Signals		
IN_ADC	73	Input, connect to sensor's output (pin 13) Input range is between 2 & 4 V (VLOW_ADC & VHIGH_ADC)
Digital Controls		
CLK_ADC	62	ADC Clock ADC converts on falling edge
TRI_ADC	63	Tristate control of ADC digital outputs 1 = tristate; 0 = output
NONLINEAR	67	1 = non-linear analog-digital conversion 0 = linear analog-digital conversion
BITINVERT	39	1 = invert output bits 0 = no inversion of output bits
Digital Output		
DO… D9	51…42	Output bits D0 = LSB, D9 = MSB

Table 7. ADC Pins (continued)

Name	No.	Description
Reference Voltages		
VLOW_ADC	71	Low reference and high reference voltages of ADC should be 2V to 4V. The resistance between VLOW_ADC and VHIGH_ADC is about 1.5 K, thus this range can be approximated by tying LOW with 2K to GND And HIGH with 1K to VDD.
VHIGH_ADC	61	
PBIASDIG1	64	Connect with 100K to GND and decouple to VDD
PBIASENCLOAD	65	Connect with 100K to GND and decouple to VDD
PBIASDIG2	66	Connect with 100K to GND and decouple to VDD
NBIASANA2	69	Connect with 100K to VDD and decouple to GND
NBIASANA	70	Connect with 100K to VDD and decouple to GND
		These resistors determine the analog resp. digital speed /power of the ADC. Both can be increased/decreased by lowering or increasing the resistance values.
Power and Ground		
VDD_DIG	56, 76	Power supply of digital circuits of ADC, + 5 V
VDD_AN	58, 74	Power supply of analog circuits of ADC, + 5 V
GND_DIG	57, 75	Ground of digital ADC circuits
GND_AN	60, 72	Ground of analog ADC circuits

Control of the VLOW_ADC & VHIGH_ADC Reference Voltages

VLOW_ADC and VHIGH_ADC are the reference voltages for a 0 and 1023 code. A 2K-resistor ladder internally connects them. The appropriate 2V and 4V DC voltages can be obtained as in Table 7. pins of the ADC, and decoupled to ground.

Linear and Non-Linear Conversion Mode – "Gamma" Correction

Figure 14. Linear and Non-Linear ADC Conversion Characteristic

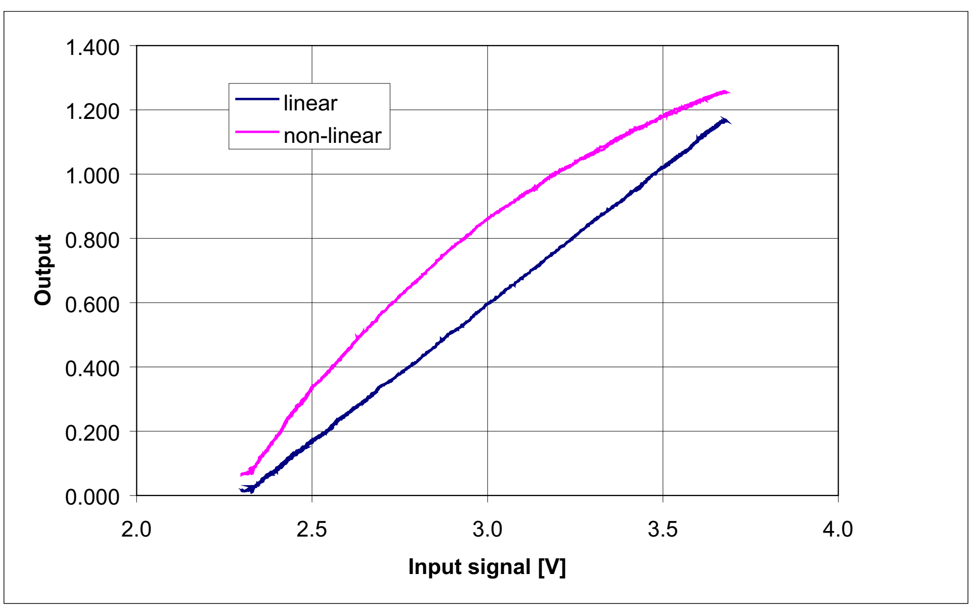


Figure 14. shows the ADC transfer characteristic. For this measurement, the ADC input was connected to a 16-bit DAC. The input voltage was a 100 kHz triangle waveform.

The non-linear ADC conversion is intended for gamma-correction of the images. It increases contrast in dark areas and reduces contrast in bright areas. The non-linear curve is tolerant for external pixel offset error correction. This means that pixel offset variations can be corrected by changing the offset after the non-linear AD conversion. This is so because the non-linear transfer function is

$$H(s) = 1-\exp(-a*s)$$

by design, and neglecting the offset, the relation between the non-linear output (y) and the linear output (x) is exactly:

$$Y = 1024 * (1 - \exp(-x/713)) / (1 - \exp(-1024/713))$$

This law yields an increased accuracy of about a factor 2 near the zero end of the scale. It is thus possible to obtain an effective 11 bit accuracy on a linear scale after post processing by applying the reverse law to the non-linear output:

$$Z = -2 * 713 * \ln(1 - y/(1024/(1-\exp(-1024/713)))) = -1426 * \ln(1-y/1343.5)$$

Then Z is an 11-bit linear output in the range 0...2047.

Operation of the Image Sensor

Set Configuration and Pulse Timing

Figure 15. Typical Operation Mode (Readout of a Frame)

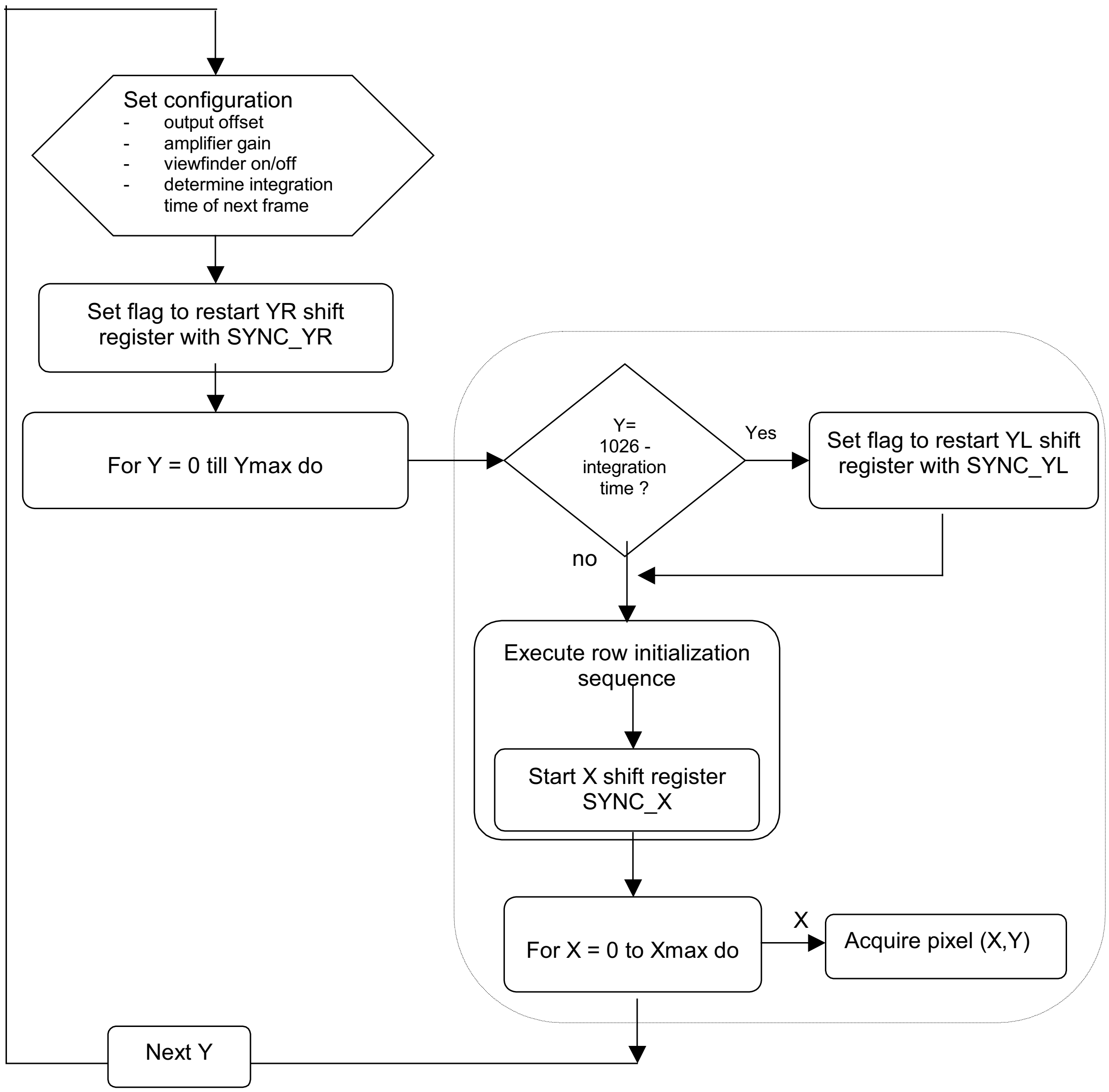


Figure 15. shows a typical operation mode of the image sensor.

At the start of a new frame, the device may be reconfigured. If necessary, the output amplifier gain and offset are adjusted or the device is put in viewfinder mode.

Then, the frame readout shift register is initiated by pulsing "SYNC_YR". This pulse occurs once per frame, normally as a part of the first row blanking sequence.

The readout of a row (line) starts with row blanking initialization sequence. Here several pulses are applied for Y-direction shift, the column amplifier S&H and nulling, and the start (SYNC_X) of the X-direction shift register.

The frame reset shift register is started also once per frame by "SYNC_YL", this pulse occurs once per frame, normally as a part of the row blanking sequence of one particular row. The time delay from the SYNC_YL to SYNC_YR is the integration time. The integration is thus a multiple of the row readout time. The reset shift register always leads the readout shift register. Therefore, the integration time should be determined before the start of the frame readout. The value that is fixed at that moment will be the integration time of the NEXT frame. If the value set for the integration time changes during frame readout, the start pulse might be lost and the next frame might be invalid. We will now discuss all steps in more detail.

Set Configuration

Configuration of the image sensor implies control and adjustment of the following points:

- output amplifier offset level, set by 'dac_bit[0...3]'
- output amplifier gain setting, set by 'gc_bit[0...3]'
- choose the integration time of the next frame
- set/clear viewfinder mode (pin 'subsampl')
- in case when the fast adjustment of the offset level is used, plus 'calib_f' and 'unitygain' as described before in Figure 7. and Figure 8.

Viewfinder Mode Versus Normal Readout

Table 8. Coordinate of Row or Column Selected by Y/X Shift Registers After a # Clock Periods in Viewfinder Mode and Full Image Mode

Clock	Sync	1	2	3	4	5	6	
Viewfinder Mode	None	None	Row 1	Row 5	Row 9	Row 13	Row 17	Y reg.
			Dark	Col. 1	Col. 5	Col. 9	Col. 13	X reg.
Full Image Mode	None	None	Row 1	Row 2	Row 3	Row 4	Row 5	Y reg.
			Dark	Col. 1	Col. 2	Col. 3	Col. 4	X reg.

Clock	258	259	260
Viewfinder Mode	Row 1025	Row 1029	EOS

322	323	324
Col. 1281	Col. 1285	EOS Dark

Clock	1030	1031	1032
Full Image Mode	Row 1029	Row 1030	EOS
	Y Shift Register		

1287	1288	1289
Col. 1285	Col. 1286	EOS Dark
X Shift Register		

In full image readout mode (pin 84, subsmpl = 0), the imager is a 1280 x 1024 SXGA image sensor. There are 3 dummy pixels read at all 4 borders of the image.

In viewfinder mode (subsmpl = 1), the imager acts as a 320 x 256 QVGA image sensor with one dummy pixel at the start of a row/column.

Table 8. shows which column or row is selected after a number of clock pulses.

Start of the Y Shift Registers for Row Readout and Row Reset

The shift registers are put in their initial state by a synchronization- or start pulse. (sync_x, sync_yr, sync_yl). The synchronization signal is low-active and should only be generated when the clock of the shift register is high. After the synchronization pulse, two falling clock edges are needed to skip dummy pixels/lines. On every falling clock edge, the shift register selects a new row for readout or reset. Figure 16. shows this timing.

Figure 16. Timing of Y Shift Registers (for Row Selection)

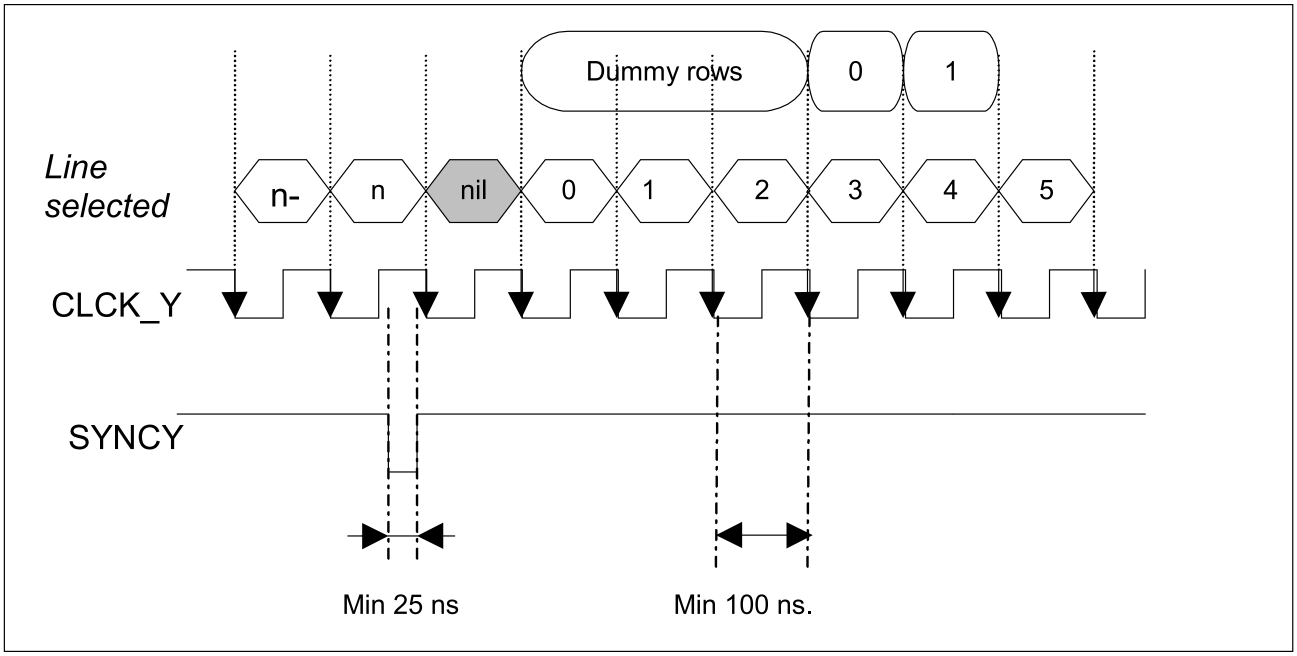
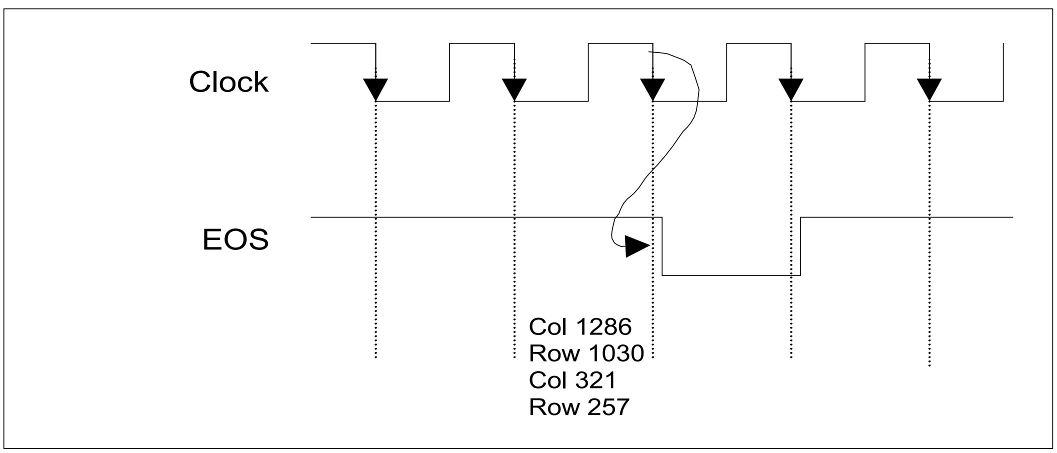


Figure 17. End-of-Scan Pulse



End-of-Scan: EOS_YL, EOS_YR, EOS_X

All three shift registers are equipped with 'end-of-scan' pulses. These pulses are low during the clock period after the last pixel or row has been read out, also in viewfinder mode.

At the EOS_X pulse, the electrical dark reference level is put on the readout bus. This voltage remains on the bus until the SIN pulse goes high. During the row blanking time, this voltage can be used for the offset adjustment of the output amplifier. The SIN high forces the DCREF voltage on the output bus.

We advise not to use the EOS pulses as an input for the row blanking time sequence generation, but to use simple counters instead. If by some reasons the EOS signal is absent or subject to glitches, the system would hang. EOS is intended as diagnostic means.

Row Initialization

During the row blanking time (which occurs at the beginning of every row read), several tasks are executed: selection of a new row, readout of this row by double sampling, reset of a new row, and possibly (slow) offset adjustment of the output amplifier. Therefore, a pulse patterns must be applied to several signals during this time. There is some freedom to make this pattern. The constraints are listed below:

Figure 18. Timing Constraints for Row Readout Initialization (Blanking Time)

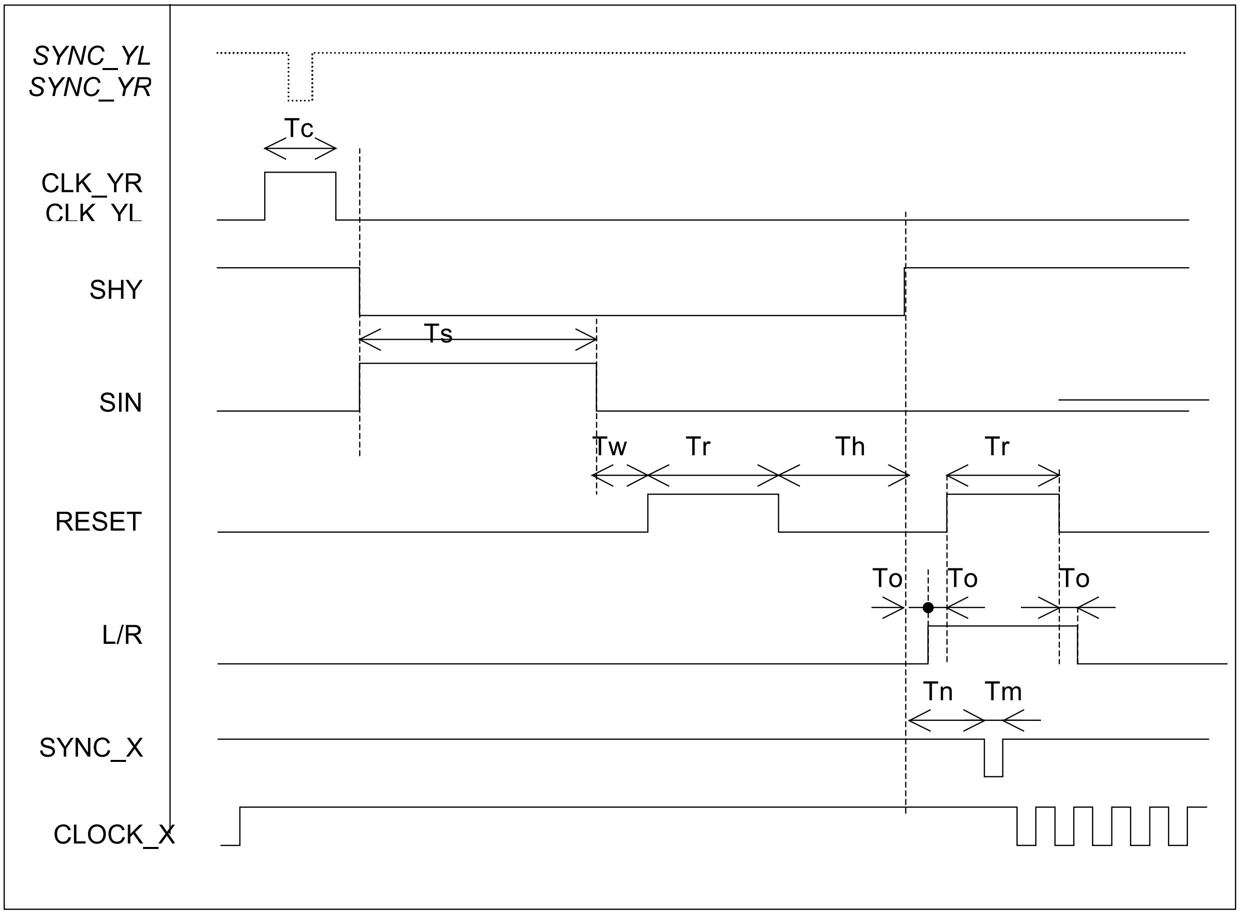


Table 9. Timing Constraints on Row Initialization Pulses Sequence

Ta	Min 0	Delay between falling edge of CLK_Y* and SHY or SIN
Tc	Min 25 ns	CLK_YR & CLK_YL high time
Ts	Typ. 3 µs	On-time of SIN (offset calibration pulse) Delay between selection of new row and end of column amplifier calibration
Tw	Typ. 200 ns	Delay between end SIN and pixel reset
Tr	Typ. 1 µs	On-time of reset pulse
Th	Typ 1 µs	Th + Tr = Delay between pixel reset and column sample & hold
To	Typ 100 ns	Delay between SHY and L/R\ Overlap of L/R\ over 2nd reset pulse
Tm	Min 25 ns	On-time of one of the SYNC pulses. SYNC==low may only occur when the associated CLOCK is high.
Tn	Min. 200 ns	Delay between SHY and start row readout

Figure 18. and Table 9. illustrate the timing constraints of the row initialization/ blanking sequence.

- The EOS_X pulse flags the end of the scanning of previous line, and should be considered as a diagnostic means only. The blanking sequence could start earlier or later.
- The next row (=line) is selected after the falling edge of CLK_YR and CLK_YL,
- The column amplifiers receive the signals on the pixels array columns buses when SHY is low (transparent).
- The SIN pulse (high) forces the column amplifiers in an “offset nulling" state.
- After 3 us, the column amplifiers have reached offset-free equilibrium, and the SIN pulse is brought low again. The pixel's signal level is thus stored in the column amplifier.
- After that the pixels in the selected row (line) are be reset (first pulse on RESET).
- Consequently the reset level is frozen in the column amplifiers when SHY goes high. Both signal level and reset level have now been applied to the column amplifiers. The sample hold (SHY) guarantees that this information will not change anymore during readout of the line.
- Now, the row is ready for readout. A pulse on SYNC_X must be given to start the row readout. SYNC_X initiates the X-direction scanning register. The scanning itself is controlled by CLOCK_X.
- During the beginning of the row readout, or possibly before, the RESET pulse for the electronic shutter (ES) must be given, if the ES is used. This is a pulse on RESET together with a high level on L/R. If the ES is not used, L/R remains low and the second RESET pulse is not generated.

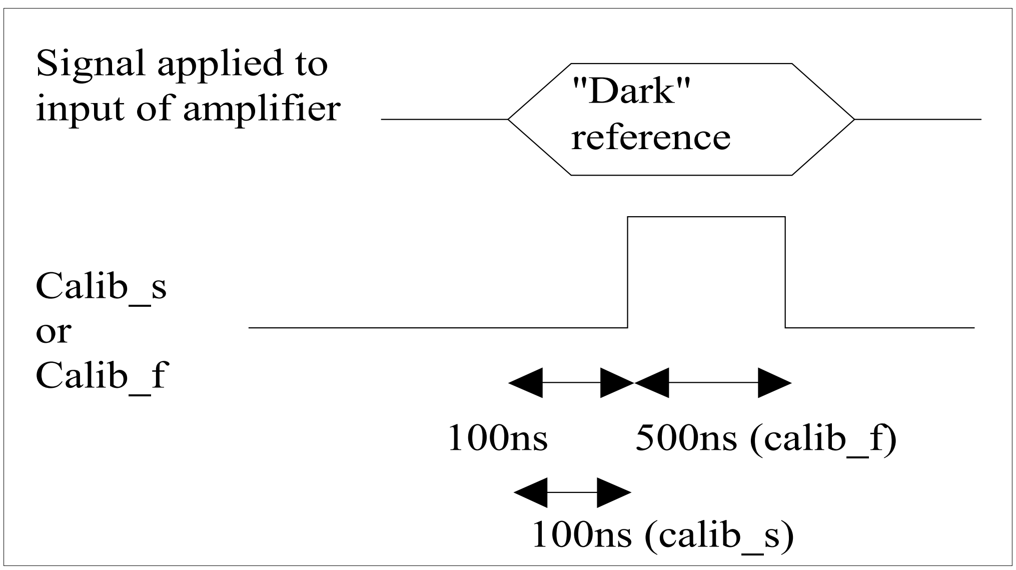
During some or the entire row blanking times, the output amplifier can be calibrated.

If the slow calibration method is used, pulse the 'CALIB_S' pin once per line. The calibration happens on the rising edge of the pulse.

If the fast calibration is used, the 'CALIB_F' should be pulsed during the row blanking time of the first row only. This calibration happens during the time that the pulse is high.

During this calibration, the input applied to the amplifier must be the dark reference, which can either be the built-in electrical dark reference, or an external dark reference on the pin EXTIN.

Figure 19. Pulse on 'CALIB_F'& 'UNITYGAIN' to be Given Once Per Frame, or on CALIB_S Once Per Line



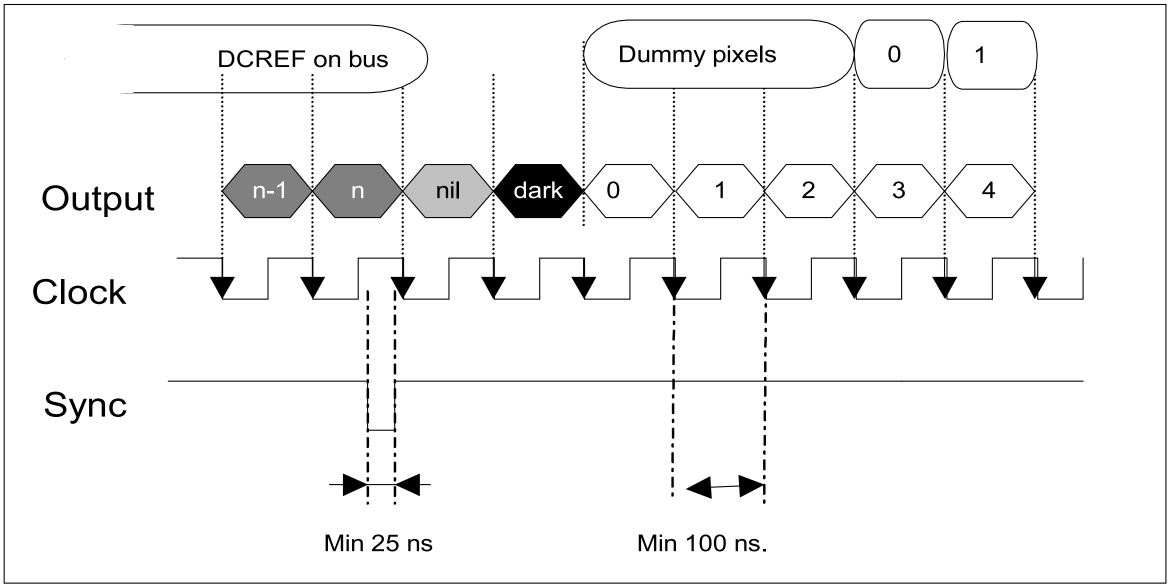
The X-Direction Shift Register

The X shift register behaves like the Y shift registers.

The sequence if initiated by SYNC_X, which should occur when CLOCK_X is high. As CLOCK_X is halted during the blanking time, the SYNC_X pulse could occur anywhere, and be taken equal to some other pulse (e.g. CLOCK_Y).

The first real (dummy) pixel is read out after the 3rd falling edge on the clock. Dummy pixels are perfectly operational pixels, but are added to shield the "real" pixels from the cross talk of the periphery.

Figure 20. Timing of X Shift Register and Pixels Readout



On-Chip Generated Electrical Dark References

The sensor outputs a electrical dark reference level after the 2nd falling edge on the clock (after sync).

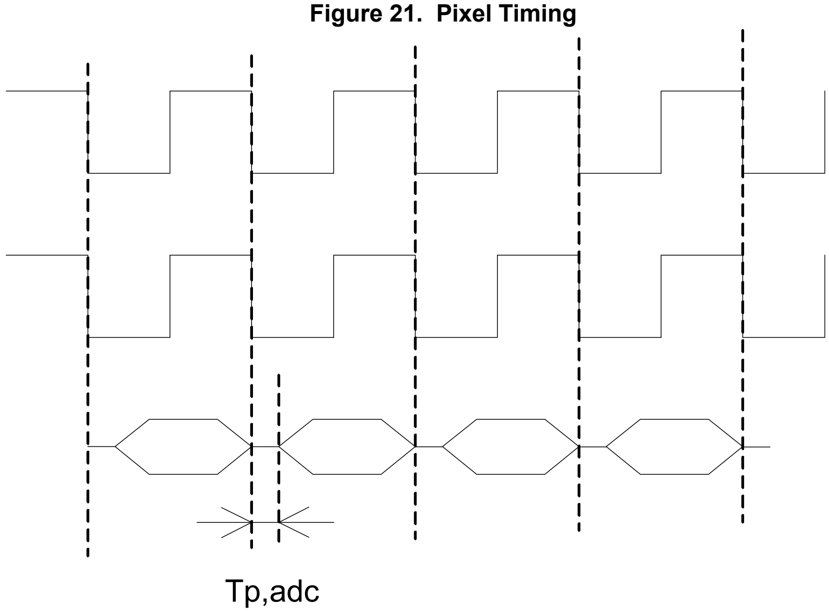
At the end of the row readout, after EOS_X becomes low, the sensor outputs the electrical dark reference voltage also, and it remains present on the on the readout bus until SIN goes high.

Note that if the X-register is reset before the EOS is reached, the dark reference is not put on the bus. Use the dark reference of the beginning of the line instead.

Pixel Readout

The same continuous 10 MHz clock drives CLK_ADC and CLK_X. On the falling edge of CLK_X, a new pixel is selected and propagates to the output amplifier. At the same time, the ADC input is frozen by the falling edge on CLK_ADC. The digital output has a delay of one pixel compared to the analog signal. The digital output becomes valid between 25 to 50 ns after the falling edge on CLK_ADC.

Figure 21. Pixel Timing

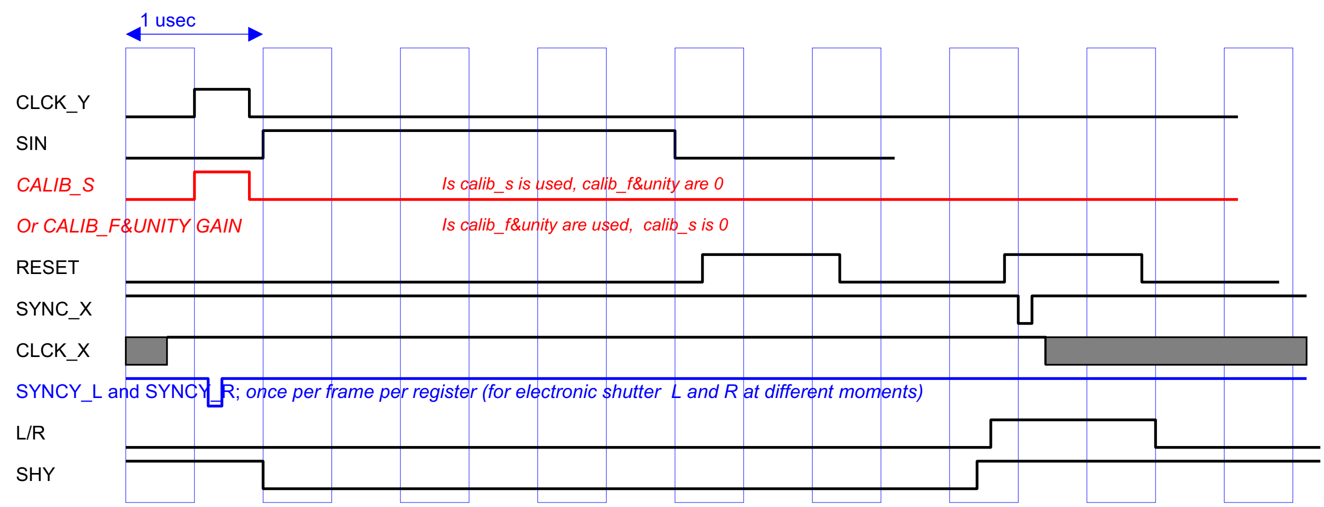


If the end of a row is reached, the sensor outputs an end-of-scan (EOS) pulse during one pulse period. And the electrical black reference level appears at the output for all successive pulses. So, the same 10 MHz clock can drive CLK_X and CLK_ADC.

Example: tIming Used on IBIS4 Breadboard

The next figure is the timing as used in the IBIS4 breadboard version 12 January 2000. In this baseline only CALIB_F is used (pulsing once per frame). CALIB_S (pulse every line) is shown as reference, but is actually not used in the baseline. The UNITY_GAIN pulse is identical to CALIB_F.

Figure 22. Pulse Sequence Used in IBIS4 Breadboard v. January 2000



Illumination Control

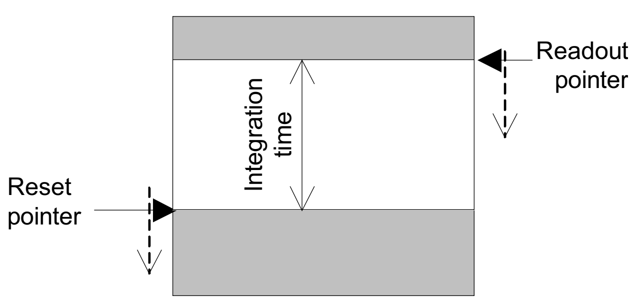
There are two means of controlling the illumination level electrically. For high light levels, there is an electronic shutter. For low light levels, the output signal can be amplified by controlling the output amplifier gain. The offset level of the signal can also be controlled digitally.

"Rolling Curtain" Electronic Shutter

The electronic shutter can reduce the integration time (= exposure time). This is achieved by an additional reset pulse every frame. In this way, the integration time is reduced to a fraction of the frame readout time.

There are two Y shift registers. One of them points at the row that is currently being read out. The other shift register points at the row that is currently being reset. Both pointers are shifted by the same Y-clock and move over the focal plane. The integration time is set by the delay between both pointers.

Figure 23. Schematic Representation of Curtain Type Electronic Shutter



This is a so-called 'rolling curtain'-type shutter. It 'rolls' over the focal plane.

The left and right shift registers can be used both for pointing to the row that is readout or the row that is reset. The shift register that is active for readout or reset is selected by the signal on L/R. In the above timing diagrams, we use the R shift register for readout, and the L shift register for electronic shutter reset. We call them the readout shift register and reset shift register.

The integration time is controlled by the delay between the SYNCY_L and SYNCY_R pulse. The shorter this delay, the shorter the integration time and the smaller the output signal will be.

If the electronic shutter is not used, the L/R signal is not pulsed. The integration time is then equal to the frame readout time.

For proper operation of the ES, the CLOCK_Y must come as an uninterrupted pulse train. Also during the dead time between frames the CLOCK_Y must be clocked. The reason is that each line should see the same elapsed time between the "ES-reset" and the reset of the line being read-out. If the CLOCK_Y is halted, the lines between the two pointers will have a longer effective integration time, and appear brighter.

Gain Control

For low illumination levels, the electronic shutter is not used - or set to its maximal value. Longer integration times can only be obtained by decreasing the frame rate. As an alternative or in complement, one can increase the output amplifier gain.

The gain is controlled by a 4-bit word. Gain values vary between 1.2 and 16, and on an exponential scale, as the F-stops of a lens.

Of course, increasing the signal amplitude by increasing the gain, will also increase the noise level. The apparent increase of sensitivity is at the cost of a lower dynamic range.