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# NOIL1SM0300A

## LUPA300 CMOS Image Sensor



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### Features

- 640(H) x 480(V) Active Pixels (VGA Resolution)
- 9.9  $\mu\text{m}$  x 9.9  $\mu\text{m}$  Square Pixels (Based on the High-Fill Factor Active Pixel Sensor Technology of FillFactory (US patent No. 6,225,670 and others)).
- Optical Format: 1/2 Optical Inch
- Pixel Rate of 80 MHz
- Frame Rate: 250 fps at Full Resolution
- On-Chip 10 bit ADCs
- Global Shutter
- Subsampling (Y Direction)
- Serial Peripheral Interface (SPI)
- Programmable Read Out Direction (X and Y)
- Random Programmable Windowing
- Power Dissipation: 190 mW
- 48-pin LCC Package
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Machine Vision
- Motion Tracking

### Overview

This document describes the interfacing and driving of the LUPA300 image sensor. The pixel size and resolution result in a 6.3 mm x 4.7 mm optical active area (1/2 inch).

This VGA-resolution CMOS active pixel sensor features global shutter and a maximal frame rate of 250 fps in full resolution, where integration during readout is possible. The readout speed can be boosted by means of subsampling and windowed Region Of Interest (ROI) readout. High dynamic range scenes can be captured using the double and multiple slope functionality. User programmable row and column start/stop positions allow windowing. subsampling reduces resolution while maintaining the constant field of view and an increased frame rate. The programmable gain and offset amplifier maps the signal swing to the ADC input range. A 10-bit ADC converts the analog data to a 10-bit digital word stream. The sensor uses a 3-wire Serial-Parallel (SPI) interface. It operates with a 3.3 V and 2.5 V power supply and requires only one master clock for operation up to 80 MHz pixel rate. It is housed in an 48-pin ceramic LCC package.

The sensor is available in a monochrome version or Bayer (RGB) patterned color filter array.

This data sheet allows the user to develop a camera-system based on the described timing and interfacing.

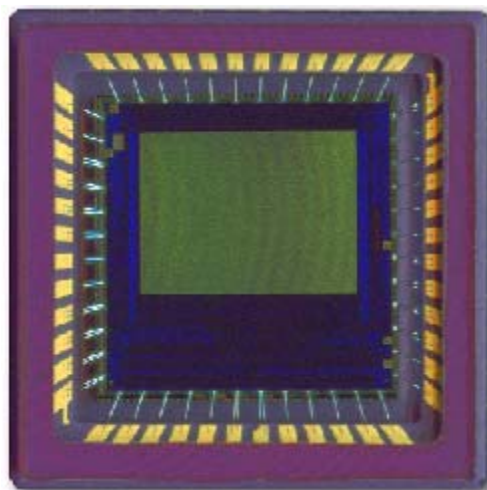


Figure 1. LUPA300 Package Photo

### ORDERING INFORMATION

Marketing Part Number	Description	Package
NOIL1SM0300A-QDC	Mono with Glass	48 pin LCC
NOIL1SE0300A-QDC	Color micro lens with Glass	
NOIL1SM0300A-WWC	Mono Wafer Sales	Wafer Sales



# NOIL1SM0300A

## SPECIFICATIONS

### GENERAL SPECIFICATIONS

Parameter	Specifications
Pixel Architecture	6 transistor pixel
Pixel Size	9.9 $\mu\text{m}$ x 9.9 $\mu\text{m}$
Resolution	640 (H) x 480 (V)
Subsampling	subsampling is possible (only in the Y-direction) Sub-sampling pattern: Y0Y0Y0Y0
Windowing (ROI)	Randomly programmable ROI read out. Implemented as scanning of lines/columns from an uploaded position
Read out direction	Read out direction can be reversed in X and Y
Programmable gain	Range x1 to x16, in 16 steps using 4-bits programming
Programmable offset	256 steps (8 bit)
Digital output	On-chip 10-bit ADCs at 80 Msamples/s
Power dissipation	160 mW not including output load 190 mW with output load of 15 pF
Package type	48 pin LCC
Mass	$\pm 1$ g

### ELECTRO-OPTICAL SPECIFICATIONS

Parameter	Typical Specifications
Optical Format	$\frac{1}{2}$ optical inch
Shutter Type	Pipelined Global shutter
Frame Rate	250 fps
FPN	2.5% RMS <sub>p-p</sub> (Min: 10%, Max: 3.1%)
PRNU	2.5% RMS, Max: 3.1%
Conversion gain	34 $\mu\text{V}/e^-$ at output
Saturation charge	35,000 $e^-$
Sensitivity	3200 V.m <sup>2</sup> /W.s 17 V/lux.s (180 lux = 1 W/m <sup>2</sup> )
Peak QE * FF	45%
Dark current (at 21°C)	300 mV/s
Noise electrons	32 $e^-$
S/N ratio	43 dB
Parasitic sensitivity	1/5000
Dynamic Range	61 dB
Extended dynamic range	Multiple slope (up to 90 dB optical dynamic range)
MTF	60%

**Table 1. RECOMMENDED OPERATING RATINGS** (Notes 1 and 2)

Symbol	Parameter	Min	Max	Units
T <sub>J</sub>	Operating temperature range	-40	70	°C

**Table 2. ABSOLUTE MAXIMUM RATINGS** (Notes 2, 3 and 4)

Symbol	Parameter	Min	Max	Units
V <sub>DD</sub> <sup>[5]</sup>	DC Supply Voltage	-0.5	4.3	V
T <sub>S</sub>	Storage Temperature	-30	+85	°C
%RH	Humidity (Relative)	-	85% at 85°C	
ESD <sup>[3]</sup> & LU <sup>[4]</sup>	ESD & Latch-up	(Notes 3 and 4)		mA

- Operating ratings are conditions in which operation of the device is intended to be functional. All parameters are characterized for DC conditions after thermal equilibrium is established. Unused inputs must always be tied to an appropriate logic level, for example, V<sub>DD</sub> or GND.
- Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- This device does NOT contain circuitry to protect the inputs against damage caused by high static voltages or electric fields. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625-A. Refer to Application Note AN52561.
- The LUPA300 does not have latchup protection.
- V<sub>DD</sub> = V<sub>DDD</sub> = V<sub>DDA</sub> (V<sub>DDD</sub> is supply to digital circuit, V<sub>DDA</sub> to analog circuit).

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## Spectral Response Curve

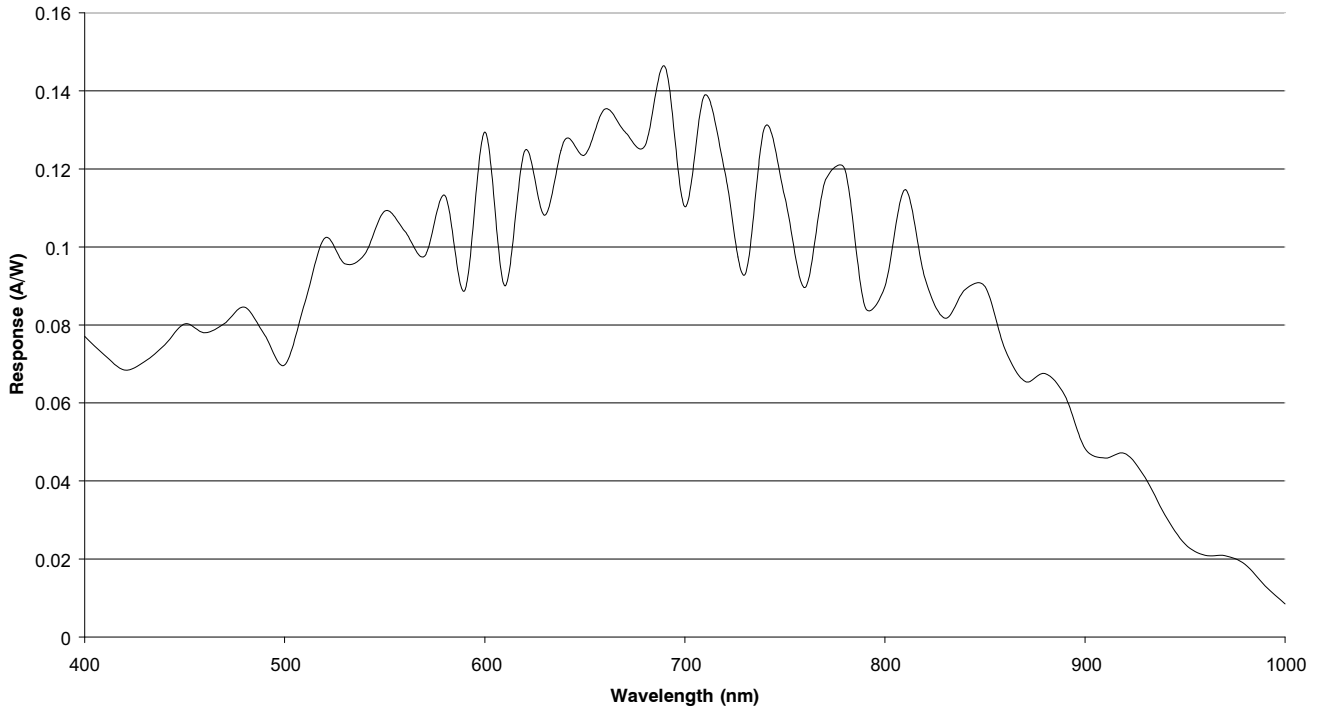


Figure 2. Spectral Response of LUPA300

## Photo-voltaic Response Curve

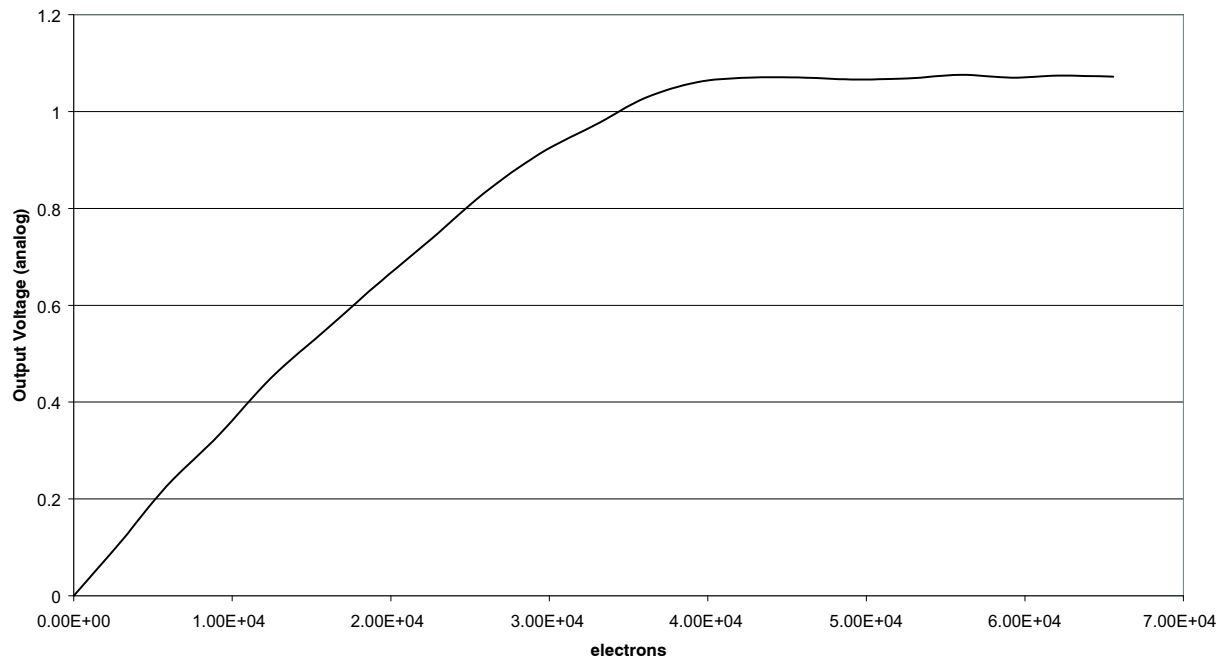


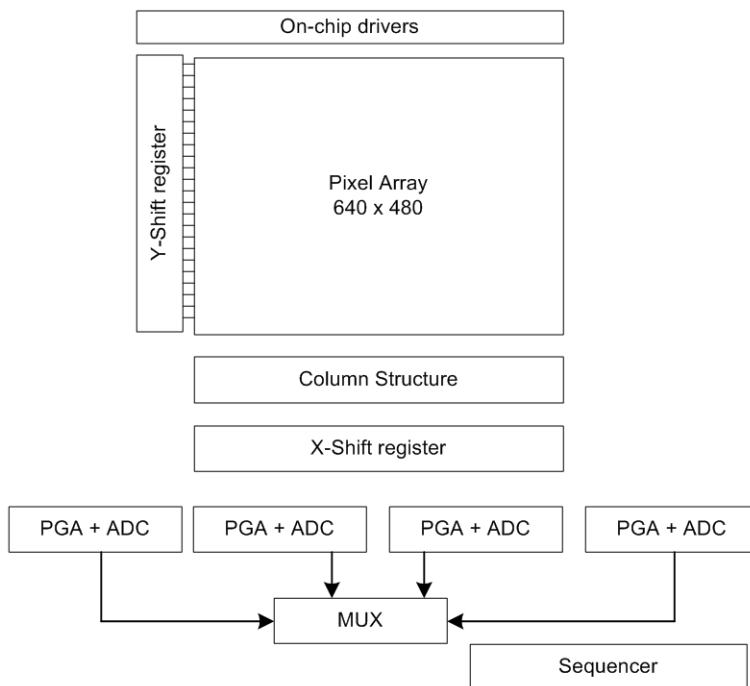
Figure 3. Photo-voltaic Response LUPA300

**SENSOR ARCHITECTURE**

The floor plan of the architecture is shown in Figure 4. The image core consists of a pixel array, an X- and Y-addressing register, pixel array drivers, and column amplifiers. The image sensor of 640 x 480 pixels is read out in progressive scan.

The architecture allows programmable addressing in the x-direction in steps of 8 pixels and in the y-direction in steps of 1 pixel. The starting point of the address is uploadable by means of the Serial Parallel Interface (SPI).

The PGAs amplify the signal from the column and add an offset so the signal fits in the input range of the ADC. The four ADCs then convert the signal to the digital domain. Pixels are selected in a 4 \* 1 kernel. Every ADC samples the signal from one of the 4 selected pixels. Sampling frequency is 20 MHz. The digital outputs of the four ADCs are multiplexed to one output bus operating at 80 MHz.



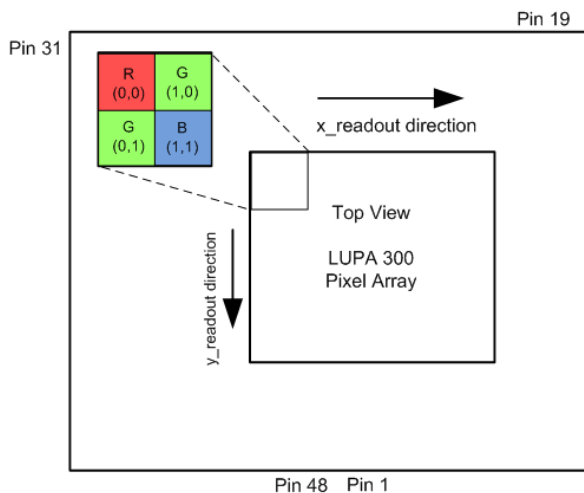
**Figure 4. Floor Plan of the Sensor**

**Pixel Architecture**

The LUPA300 is designed on the 6T pixel architecture.

*Color Filter*

The LUPA300 can also be processed with a Bayer RGB color pattern. Pixel (0,0) has a red filter.



**Figure 5. Color Filter Arrangement on the Pixels**

**Frame Rate and Windowing**

*Frame Rate*

The frame rate depends on the input clock, the Frame Overhead Time (FOT) and the Row Overhead Time (ROT). The frame period is calculated as follows

Frame period = FOT + Nr. Lines \* (ROT + Nr. Pixels \* clock period)

Example: read out of the full resolution at nominal speed (80 MHz pixel rate = 12.5 ns, GRAN<1:0>=10):

Frame period = 7.8 μs + (480 \* (400 ns + 12.5 ns \* 640) = 4.039 ms => 247.6 fps.

In case the sensor operates in subsampling, the ROT is enlarged with 8 clock periods.

**Table 3. FRAME RATE PARAMETERS**

Parameter	Comment	Clarification
FOT	Frame Overhead Time	1200 clock periods for GRAN<1:0> = 11
		624 clock periods for GRAN<1:0> = 10
		336 clock periods for GRAN<1:0> = 01
		192 clock periods for GRAN<1:0> = 00
ROT	Row Overhead Time	48 clock periods for GRAN<1:0> = 11
		32 clock periods for GRAN<1:0> = 10
		24 clock periods for GRAN<1:0> = 01
		20 clock periods for GRAN<1:0> = 00
Nr. Lines	Number of lines read out each frame	
Nr. Pixels	Number of pixels read out each line	
clock period	1/80 MHz = 12.5 ns	

*Windowing*

Windowing is achieved by the SPI interface. The starting point of the x- and y-address is uploadable, as well as the window size. The minimum step size in the x-direction is 8 pixels (only multiples of 8 can be chosen as start/stop addresses). The minimum step size in the y-direction is 1

line (every line can be addressed) in normal mode and 2 lines in subsampling mode.

The window size in the x-direction is uploadable in register NB\_OF\_PIX. The window size in the y-direction is determined by the register FT\_TIMER

**Table 4. FRAME RATE PARAMETERS**

Parameter	Frame Rate (fps)	Frame Readout (us)	Comment
640 x 480	247.5	4038	
640 x 240	488.3	2048	Subsampling
256 x 256	1076	929	Windowing

**Analog to Digital Converter**

The sensor has four 10-bit pipelined ADC on board. The ADCs are nominally operating at 20 Msamples/s. The input range of the ADC is between 0.75 and 1.75V. The analog input signal is sampled at 2.1 ns delay from the rising edge of the ADC clock.

The digital output data appears at the output at 5.5 cycles later. This is at the 6th falling edge succeeding the sample moment. The data is delayed by 3.7 ns with respect to this falling edge. This is illustrated in Figure 6.

**Table 5. ADC PARAMETERS**

Parameter	Specification
Data rate	20 Msamples/s
Input range	0.75 V – 1.75 V
Quantization	10 bit
DNL	Typ. < 0.3 LSB
INL	Typ. < 0.7 LSB

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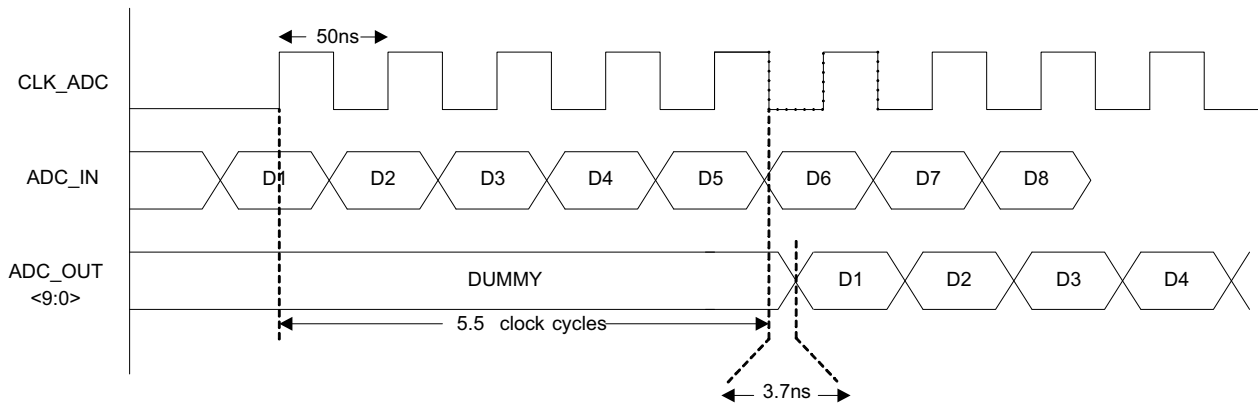


Figure 6. ADC Timing

## Programmable Gain Amplifiers

The programmable gain amplifiers have two functions:

- Adding an offset to the signal to fit it into the range of the ADC. This is controlled by the VBLACK and VOFFSET SPI settings.
- Amplifying the signal after the offset is added.

### Offset Regulation

The purpose of offset regulation is to bring the signal in the input range of the ADC.

After the column amplifiers, the signal from the pixels has a range from 0.1V (bright) to 1.3V (black). The input range of the ADC is from 0.75V to 1.75V. The amount of offset added is controlled by two SPI settings: VBLACK<7:0> and VOFFSET<7:0>. The formula to add offset is:

$$V_{\text{output}} = V_{\text{signal}} + (V_{\text{offset}} - V_{\text{black}})$$

Note that the FPN (fixed pattern noise) of the sensor causes a spread of about 100 mV on the dark level. To allow FPN correction during post processing of the image, this spread on the dark level needs to be covered by the input range of the ADC. This is why the default settings of the SPI are programmed to add an offset of 200 mV. This way the dark level goes from 1.3V to 1.5V and is the FPN information still converted by the ADC. To match the ADC range, it is recommended to program an offset of 340 mV. To match the ADC range, it is recommended to program an offset of 340 mV. To program this offset, the Voffset and Vblack registers can be used. Figure 7 illustrates the operation of the offset regulation with an example. The blue histogram is the histogram of the image taken after the column amplifiers.

Consider as an example that the device has a black level of 1.45V and a swing of 100 mV. With this swing, it fits in the input range of the ADC, but a large part of the range of the ADC is not used in this case. For this reason an offset is added first, to align the black level with the input range of the ADC. In the first step, an offset of 200 mV is added with the default settings of VBLACK and VOFFSET. This results in the red histogram with a average black level of 1.65V. This means that the spread on the black level falls completely inside the range of the ADC. In a second step, the signal is amplified to use the full range of the ADC.

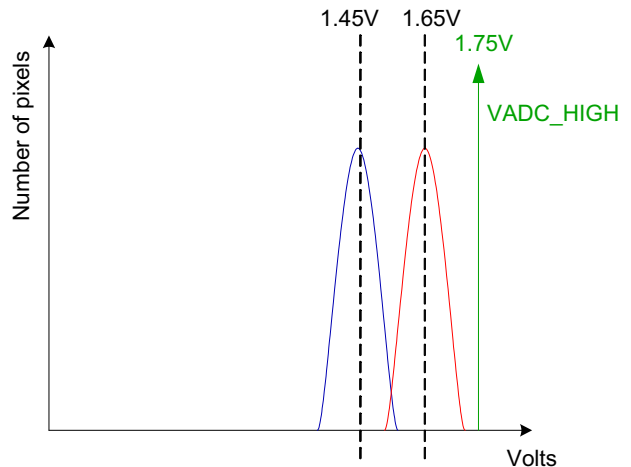


Figure 7. Offset Regulation

*Programmable Gain*

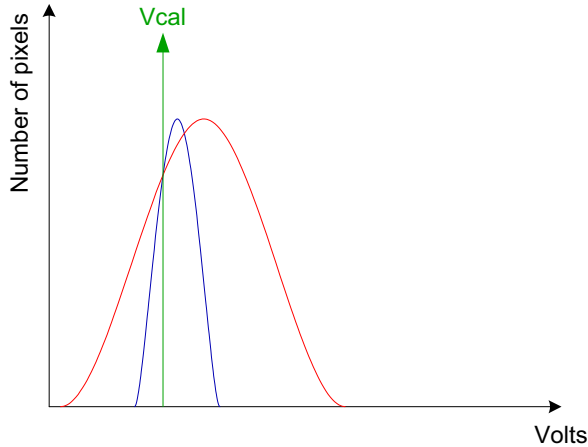
The amplification inside the PGA is controlled by three SPI settings:

The PGA gain selection: 16 gain steps are selectable by means of the GAIN\_PGA<3:0> register. Selection word 0000 corresponds with gain 1.32 and selection word 1111 corresponds with gain 15.5. Table 6 gives the 16 gain settings.

The unity gain selection of the PGA is done by the UNITY\_PGA setting. If this bit is high, the GAIN\_PGA settings are ignored.

The SEL\_UNI setting is used to have more gain steps. If this bit is low, the signal is divided by two before entering the PGA. GAIN\_PGA and UNITY\_PGA settings are applied afterwards. If the SEL\_UNI bit is high, there is a unity feed through to the PGA. This allows having a total gain range of 0.5 to 16 in 32 steps.

The amplification in the PGA is done around a pivoting point, set by Vcal as illustrated in Figure 8. The VCAL<7:0> setting is used to apply the Vcal voltage through an on chip DAC



**Figure 8. Effect on Histogram of PGA (gain = 4)  
(Vcal is the green line)**

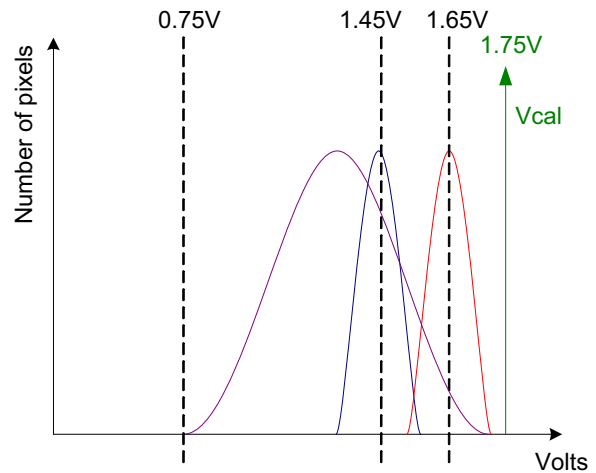
Figure 9 continues on the example in the section, Offset Regulation. The blue histogram is the histogram of the image after the column amplifiers. With offset regulation an offset of 200 mV is added to bring the signal in range of the ADC. The black level of 1.45V is shifted to 1.65V.

The red and blue histograms have a swing of 100 mV. This means the input range of the ADC is not completely used. By amplifying the signal with a factor 10 by the PGA, the full

range of the ADC can be used. In this example, Vcal is set at 1.75V (the maximum input range of the ADC) to make sure the spread on the black level is still inside the range of the ADC after amplification. The result after amplification is the purple histogram.

**Table 6. GAIN SETTINGS**

GAIN_PGA<3:0>	Gain
0000	1.32
0001	1.56
0010	1.85
0011	2.18
0100	2.58
0101	3.05
0110	3.59
0111	4.22
1000	4.9
1001	5.84
1010	6.84
1011	8.02
1100	9.38
1101	11.2
1110	13.12
1111	15.38



**Figure 9. Example of PGA Operation**



## Operation and Signaling

### Power Supplies

Every module on chip such as column amplifiers, output stages, digital modules, and drivers has its own power supply and ground. Off chip the grounds can be combined, but not all power supplies may be combined. This results in several different power supplies, but this is required to reduce electrical cross-talk and to improve shielding, dynamic range, and output swing.

On chip, the ground lines of every module are kept separate to improve shielding and electrical cross-talk between them.

An overview of the supplies is given in Table 7 and Table 8. Table 8 summarizes the supplies related to the pixel array signals, where Table 7 summarizes the supplies related with all other modules.

**Table 7. FRAME RATE PARAMETERS**

Name	DC Current	Peak Current	Typ	Max	Description
V <sub>DDA</sub>	15.7 mA	50 mA	2.5 V	5%	Power supply analog readout module
V <sub>DDD</sub>	6.7 mA	50 mA	2.5 V	2.5 V	Power supply digital modules
V <sub>ADC</sub>	32.7 mA	100 mA	2.5 V	5%	Power supply of ADC circuitry
V <sub>DDO</sub>	3.5 mA	100 mA	2.5 V	5%	Power supply output drivers

**Table 8. OVERVIEW OF THE POWER SUPPLIES RELATED TO PIXEL SIGNALS**

Name	DC Current	Peak Current	Min	Typ	Max	Description
V <sub>PIX</sub>	3 mA	100 mA		2.5 V		Power supply pixel array
V <sub>RES</sub>	1 $\mu$ A	10 mA	3.0 V	3.3 V	3.5 V	Power supply reset drivers
V <sub>RES_DS</sub>	1 $\mu$ A	10 mA		2.8 V		Power supply reset dual slope drivers
V <sub>RES_TS</sub>	1 $\mu$ A	10 mA		2.0 V		Power supply reset triple slope drivers
V <sub>MEM_H</sub>	1 $\mu$ A	1 $\mu$ A	3.0 V	3.3 V	3.5 V	Power supply for memory element in pixel
GND <sub>DRIVERS</sub>				0 V		Ground of the pixel array drivers

The maximum currents mentioned in Table 7 and Table 8 are peak currents. All power supplies should be able to deliver these currents except for V<sub>mem\_I</sub>, which must be able to sink this current.

Note that no power supply filtering on chip is implemented and that noise on these power supplies can

contribute immediately to the noise on the signal. The voltage supplies V<sub>PIX</sub>, V<sub>DDA</sub> and V<sub>ADC</sub> are especially important to be noise free.

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## Biasing

Table 9 summarizes the biasing signals required to drive this image sensor. For optimization reasons of the biasing of

the column amplifiers with respect to power dissipation, several biasing resistors are required. This optimization results in an increase of signal swing and dynamic range.

**Table 9. OVERVIEW OF BIAS SIGNALS**

Signal <sup>[1]</sup>	Comment	Related Module	DC-Level
ADC_BIAS	Connect with 10 kΩ to V <sub>ADC</sub> and decouple with 100n to GND <sub>ADC</sub>	ADC	693 mV
PRECHARGE_BIAS	Connect with 68 kΩ to V <sub>PIX</sub> and decouple with 100 nF to GND <sub>DRIVERS</sub>	Pixel array precharge	567 mV
BIAS_PGA	Biasing of amplifier stage. Connect with 110 kΩ to V <sub>DDA</sub> and decouple with 100 nF to GND <sub>A</sub>	PGA	650 mV
BIAS_FAST	Biasing of columns. Connect with 42 kΩ to V <sub>DDA</sub> and decouple with 100 nF to GND <sub>A</sub>	Column amplifiers	750 mV
BIAS_SLOW	Biasing of columns. Connect with 1.5 MΩ to V <sub>DDA</sub> and decouple with 100 nF to GND <sub>A</sub>	Column amplifiers	450 mV
BIAS_COL	Biasing of imager core. Connect with 500 kΩ to V <sub>DDA</sub> and decouple with 100 nF to GND <sub>A</sub>	Column amplifiers	508 mV

1. Each biasing signal determines the operation of a corresponding module in the sense that it controls speed and dissipation.

## Digital Signals

Depending on the operation mode (master or slave), the pixel array of the image sensor requires different digital

control signals. The function of each of the signals is shown in Table 10.

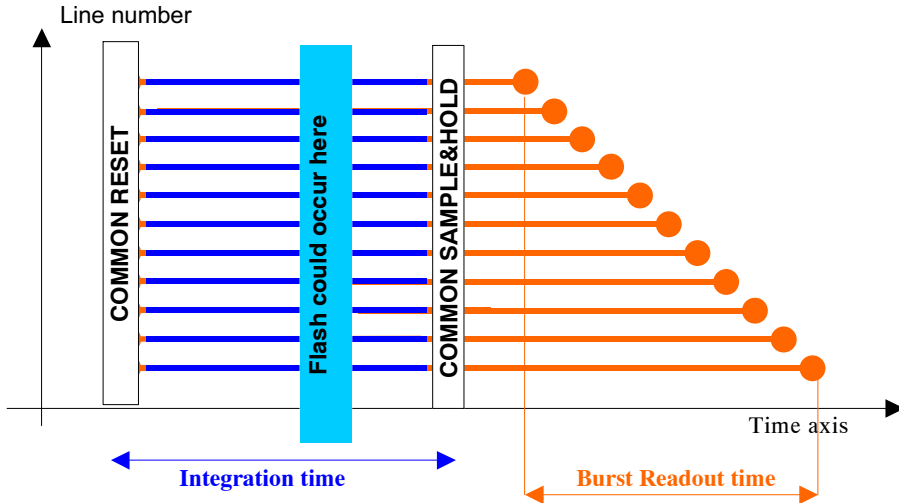
**Table 10. OVERVIEW OF BIAS SIGNALS**

Signal	I/O	Comments
LINE_VALID	Digital output	Indicates when valid data is at the outputs. Active high
FRAME_VALID	Digital output	Indicates when a valid frame is readout. Active high
INT_TIME_3	Digital I/O	In master mode: Output to indicate the triple slope integration time. In slave mode: Input to control the triple slope integration time. Active high
INT_TIME_2	Digital I/O	In master mode: Output to indicate the dual slope integration time. In slave mode: Input to control the dual slope integration time. Active high
INT_TIME_1	Digital I/O	In master mode: Output to indicate the integration time. In slave mode: Input to control integration time. Active high
RESET_N	Digital input	Sequencer reset. Active low
CLK	Digital input	Readout clock (80 MHz), sine or square clock
SPI_ENABLE	Digital input	Enable of the SPI
SPI_CLK	Digital input	Clock of the SPI. (Max. 20 MHz)
SPI_DATA	Digital I/O	Data line of the SPI. Bidirectional pin

**Global Shutter**

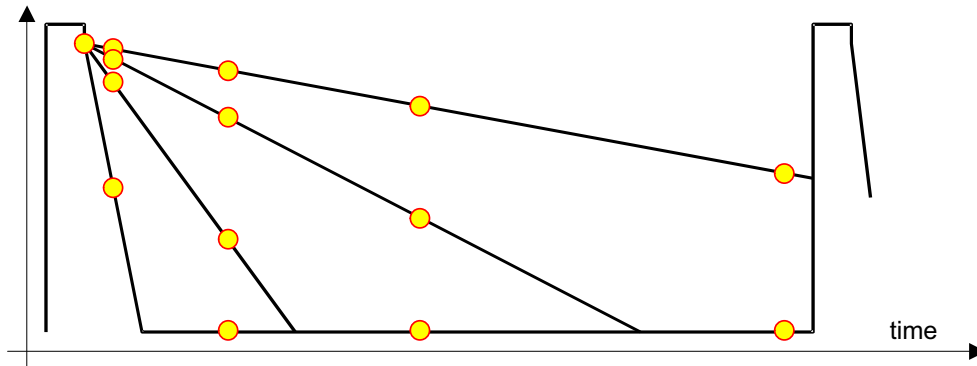
In a global shutter light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 10 shows the integration and read out sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset

simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and read out cycle can occur in parallel or in sequential mode.



**Figure 10. Synchronous Shutter Operation**

**Non Destructive Readout (NDR)**



**Figure 11. Principle of Non Destructive Readout [1]**

The sensor can also be read out in a non destructive way. After a pixel is initially reset, it can be read multiple times, without resetting. The initial reset level and all intermediate signals can be recorded. High light levels saturate the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, one has to use the later or latest

samples. Essentially an active pixel array is read multiple times, and reset only once. The external system intelligence takes care of the interpretation of the data. Table 11 summarizes the advantages and disadvantages of non destructive readout.

NOTE 1: This mode can be activated by setting the NDR SPI register. The NDR SPI register must only be changed during FOT. The NDR bit should be set high during the first Frame Overhead Time after the pixel array is reset; the NDR bit must be set low during the last Frame Overhead Time before the pixel array is being reset.

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**Table 11. ADVANTAGES AND DISADVANTAGES OF NON DESTRUCTIVE READOUT**

Advantages	Disadvantages
Low noise because it is a true CDS.	System memory required to record the reset level and the intermediate samples.
High sensitivity because the conversion capacitance is kept rather low.	Requires multiples readings of each pixel, thus higher data throughput.
High dynamic range because the results includes signal for short and long integrations times.	Requires system level digital calculations.

## Sequencer

The sequencer generates the complete internal timing of the pixel array and the readout. The timing can be controlled by the user through the SPI register settings. The sequencer operates on the same clock as the ADCs. This is a division by 4 of the input clock.

Table 12 shows a list of the internal registers with a short description. In the next section, the registers are explained in more detail.

**Table 12. INTERNAL REGISTERS**

Address	Bits	Name	Description
0 (0000)	10:0	SEQUENCER	Default <10:0>: 00000101001
	1	mastermode	1: master mode; 0: slave mode
	1	ss	1: ss in y; 0: no subsampling
	2	gran	clock granularity
	1	enable_analog_out	1: enabled; 0: disabled
	1	calib_line	1: line calibration; 0 frame calibration
	1	res2_en	1: enable DS; 0: Disable DS
	1	res3_en	1: enable TS; 0: Disable TS
	1	reverse_x	1: readout in reverse x direction 0: readout in normal x direction
	1	reverse_y	1: readout in reverse y direction 0: readout in normal y direction
1	Ndr	1: enable non destructive readout 0: disable non destructive readout	
1 (0001)	7:0	START_X	Start pointer X readout Default <7:0>: 00000000
2 (0010)	8:0	START_Y	Start pointer Y readout Default <8:0>: 00000000
3 (0011)	7:0	NB_PIX	Number of kernels to read out (4 pixel kernel) Default <7:0>: 10100000
4 (0100)	11:0	RES1_LENGTH	Length of reset pulse (in number of lines) Default <11:0>: 00000000010
5 (0101)	11:0	RES2_TIMER	Position of reset DS pulse in number of lines Default <11:0>: 000000000000
6 (0110)	11:0	RES3_TIMER	Position of reset TS pulse in number of lines Default <11:0>: 000000000000
7(0111)	11:0	FT_TIMER	Position of frame transfer in number of lines Default <11:0>: 000111100001
8 (1000)	7:0	VCAL	DAC input for vcal Default <7:0>: 01001010

Table 12. INTERNAL REGISTERS

Address	Bits	Name	Description
9 (1001)	7:0	VBLACK	DAC input for vblack Default <7:0>: 01101011
10 (1010)	7:0	VOFFSET	DAC input for voffset Default <7:0>: 01010101
11 (1011)	11:0	ANA_IN_ADC	Activate analog ADC input Default <11:0>: 000011110000
	4	sel_test_path	Selection of analog test path
	4	sel_path	Selection of normal analog path
	4	bypass_mux	Bypass of digital 4 to 1 mux
12 (1100)	11:0	PGA_SETTING	PGA settings Default <11:0>: 111110110000
	4	gain_pga	Gain settings PGA
	1	unity_pga	PGA unity amplification
	1	sel_uni	Preamplification of 0.5 (0: enabled)
	1	enable_analog_in	Activate analog input
	4	enable_adc	Put separate ADCs in standby
	1	sel_calib_fast	Select fast calibration of PGA
	11:0	CALIB_ADC <11:0>	Calibration word of the ADCs Default: calib_adc<11:0>:101011011111
14 (1110)	11:0	CALIB_ADC <23:12>	calib_adc<23:12>:011011011011
15 (1111)	8:0	CALIB_ADC <32:24>	calib_adc<32:24>:000011011011

*Detailed Description of the Internal Registers*

The registers should only be changed during FOT (when frame valid is low).

These registers should only be changed during RESET\_N is low:

- Mastermode register
- Granularity register

**Sequencer Register <10:0>**

The sequencer register is an 11 bit wide register that controls all of the sequencer settings. It contains several "sub-registers".

*Mastermode (1 bit)*

This bit controls the selection of mastermode/slavemode. The sequencer can operate in two modes: master mode and slave mode. In master mode all the internal timing is controlled by the sequencer, based on the SPI settings. In slave mode the integration timing is directly controlled over three pins, the readout timing is still controlled by the sequencer.

- 1: Master mode (default)
- 0: Slave mode

*Subsampling (1bit)*

This bit enables/disables the subsampling mode. Subsampling is only possible in Y direction and follows this pattern:

- Read one, skip one: Y0Y0Y0Y0...  
By default, the subsampling mode is disabled.

*Clock granularity (2 bits)*

The system clock (80 MHz) is divided several times on chip.

The clock, that drives the "snapshot" or synchronous shutter sequencer, can be programmed using the granularity register. The value of this register depends on the speed of your system clock.

- 11: > 80 MHz
- 10: 40-80 MHz (default)
- 01: 20-40 MHz
- 00: < 20 MHz

*Enable analog out (1 bit)*

This bit enables/disables the analog output amplifier.

- 1: enabled
- 0: disabled (default)

*Calib\_line (1bit)*

This bit sets the calibration method of the PGA. Different calibration modes can be set, at the beginning of the frame and for every subsequent line that is read.

- 1: Calibration is done every line (default)
- 0: Calibration is done every frame (less row fixed pattern noise)



*Res2\_enable (1bit)*

This bit enables/disables the dual slope mode of the device.

1: Dual slope is enabled (configured according to the RES2\_TIMER register)

0: Dual slope is disabled (RES2\_timer register is ignored) - default

*Res3\_enable (1bit)*

This bit enables/disables the triple slope mode of the device.

1: triple slope is enabled (configured according to the RES3\_TIMER register)

0: triple slope is disabled (RES3\_timer register is ignored) - default

*Reverse\_X (1bit)*

The readout direction in X can be reversed by setting this bit through the SPI.

1: Read direction is reversed (from right to left)

0: normal read direction (from left to right) - default

*Reverse\_Y (1bit)*

The readout direction in Y can be reversed by setting this bit through the SPI.

1: Read direction is reversed (from bottom to top)

0: normal read direction (from top to bottom) - default

*Ndr (1 bit)*

This bit enables the non destructive readout mode if desired.

1: ndr enables

0: ndr disables (default)

**Start\_X Register <7:0>**

This register sets the start position of the readout in X direction. In this direction, there are 80 (from 0 to 79) possible start positions (8 pixels are addressed at the same time in one clock cycle). Remember that if you put Start\_X to 0, pixel 0 is being read out. Example:

If you set 23 in the Start\_X register readout only starts from pixel 184 (8x23).

**Start\_Y Register <8:0>**

This register sets the start position of the readout in Y direction. In this direction, there are 480 (from 0 to 479) possible start positions. This means that the start position in Y direction can be set on a line by line basis.

**Nb\_pix <7:0>**

This register sets the number of pixels to read out. The number of pixels to be read out is expressed as a number of kernels in this register (4 pixels per kernel). This means that there are 160 possible values for the register (from 1 to 160). Example:

If you set 37 in the nb\_pix register, 148 (37 x 4) pixels are read out.

**Res1\_length <11:0>**

This register sets the length of the reset pulse (how long it remains high). This length is expressed as a number of lines (res1\_length - 1). The minimum and default value of this register is 2.

The actual time the reset is high is calculated with the following formula:

Reset high = (Res1\_length-1) \* (ROT + Nr. Pixels \* clock period)

**Res2\_timer <11:0>**

This register defines the position of the additional reset pulse to enable the dual slope capability. This is also defined as a number of lines-1.

The actual time on which the additional reset is given is calculated with the following formula:

DS high = (Res2\_timer-1) \* (ROT + Nr. Pixels \* clock period)

**Res3\_timer <11:0>**

This register defines the position of the additional reset pulse to enable the triple slope capability. This is also defined as a number of lines - 1.

The actual time on which the additional reset is given is calculated with the following formula:

TS high = (Res3\_timer-1) \* (ROT + Nr. Pixels \* clock period)

**Ft\_timer <11:0>**

This register sets the position of the frame transfer to the storage node in the pixel. This means that it also defines the end of the integration time. It is also expressed as a the number of lines - 1.

The actual time on which the frame transfer takes place is calculated with the following formula:

FT time = (ft\_timer-1) \* (ROT + Nr. Pixels \* clock period)

**Vcal <7:0>**

This register is the input for the on-chip DAC which generates the Vcal supply used by the PGA.

When the register is "00000000" it sets a Vcal of 2.5V. When the register is 11111111 then it sets a Vcal of 0V. This means that the minimum step you can take with the Vcal register is 9.8 mV/bit (2.5V/256bits).

**Vblack <7:0>**

This register is the input for the on-chip DAC which generates the Vblack supply used by the PGA. When the register is "00000000" it sets a Vblack of 2.5V. When the register is 11111111 then it sets a Vblack of 0V. This means that the minimum step you can take with the Vblack register is 9.8 mV/bit (2.5V/256bits).

**Voffset <7:0>**

This register is the input for the on-chip DAC, which generates the Voffset supply used by the PGA. When the register is "00000000" it sets a Voffset of 2.5V. When the register is 11111111 then it sets a Voffset of 0V. This means that the minimum step you can take with the Voffset register is 9.8 mV/bit (2.5V/256bits).

**Ana\_in\_ADC <11:0>**

This register sets the different paths that can be used as the ADC input (mainly for testing and debugging). The register consists of several "sub-registers".

*Sel\_test\_path (4 bits)*

These bits select the analog test path of the ADC.

0000: No analog test path selected (default)

0001: Path of pixel 1 selected

0010: Path of pixel 2 selected

*Sel\_path (4 bits)*

These bits select the analog path to the ADC.

1111: All paths selected (normal operation) - default

0000: No paths selected (enables ADC to be tested through test paths)

0001: Path of pixel 1 selected

0010: Path of pixel 2 selected

*Bypass\_mux (4 bits)*

These bits enable the possibility to bypass the digital 4 to 1 multiplexer.

0000: no bypass (default)

**PGA\_SETTING <11:0>**

This register defines all parameters to set the PGA. The register consists of different "sub-registers"

*Gain\_pga (4 bits)*

These bits set the gain of the PGA. The following Table 13 gives an overview of the different gain settings.

**Table 13.**

GAIN_PGA<3:0>	Gain
0000	1.32
0001	1.56
0010	1.85
0011	2.18
0100	2.58
0101	3.05
0110	3.59
0111	4.22
1000	4.9
1001	5.84
1010	6.84
1011	8.02
1100	9.38
1101	11.2
1110	13.12
1111	15.38

*Unity\_pga (1 bit)*

This bit sets the PGA in unity amplification.

0: No unity amplification, gain settings apply

1: Unity gain amplification, gain setting are ignored (default)

*Sel\_uni (1 bit)*

This bit selects whether or not the signal gets a 0.5 amplification before the PGA.

0: amplification of 0.5 before PGA

1: Unity feed through (default)

*Enable\_analog\_in (1 bit)*

This bit enables/disables an analog input to the PGA.

0: analog input disabled (default)

1: analog input enabled

*Enable\_adc (4 bits)*

These bits can separately enable/disable the different ADCs.

0000: No ADCs enabled

1111: All ADCs enabled (default)

0001: ADC 1 enabled

0010: ADC 2 enabled

*Sel\_calib\_fast (1 bit)*

Selects the fast/slow calibration of the ADC

0: slow calibration

1: fast calibration

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## 2ADC Calibration Word <32:0>

The calibration word for the ADCs is distributed over three registers (13, 14 and 15). These registers all have their default value and changing this value is not recommended.

The default register values are:

- calib\_adc<11:0>: 101011011111
- calib\_adc<23:12>: 011011011011
- calib\_adc<32:24>: 000011011011

## Data Interface (SPI)

The serial-3-wire interface (or Serial-to-Parallel Interface) uses a serial input to shift the data in the register buffer. When the complete data word is shifted into the register buffer the data word is loaded into the internal register where it is decoded.

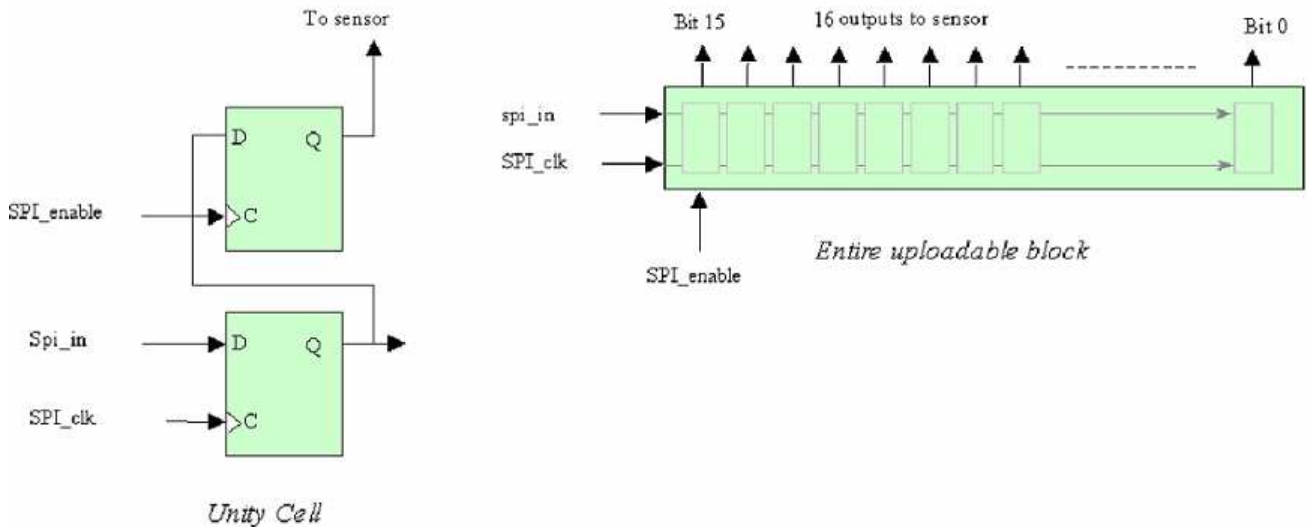


Figure 12. SPI Schematic

The timing of the SPI register is explained in the timing diagram below

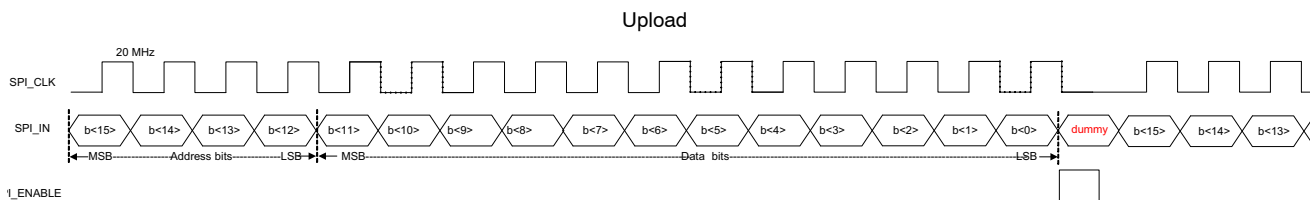


Figure 13. Timing of the SPI

SPI\_IN (15:12): Address bits

SPI\_IN (11:0): Data bits

When SPI\_ENABLE is asserted the parallel data is loaded into the internal registers of the LUPA300. The frequency of

SPI\_CLK is 20 MHz or lower. The SPI bits have a default value that allows the sensor to be read out at full resolution without uploading the SPI bits.

## TIMING AND READOUT OF THE IMAGE SENSOR

The timing of the sensor consists of two parts. The first part is related with the integration time and the control of the pixel. The second part is related to the readout of the image sensor. Integration and readout can be in parallel. In this case, the integration time of frame I is ongoing during readout of frame I-1. Figure 14 shows this parallel timing structure.

The readout of every frame starts with a Frame Overhead Time (FOT) during which the analog value on the pixel diode is transferred to the pixel memory element. After this FOT, the sensor is read out line per line. The readout of every line starts with a Row Overhead Time (ROT) during which

the pixel value is put on the column lines. Then the pixels are selected in groups of 4. So in total 160 kernels of 4 pixels are read out. The internal timing is generated by the sequencer. The sequencer can operate in 2 modes: master mode and slave mode. In master mode all the internal timing is controlled by the sequencer, based on the SPI settings. In slave mode the integration timing is directly controlled over three pins, the readout timing is still controlled by the sequencer. The selection between master and slave mode is done by the MASTERMODE register of the SPI. The sequencer is clocked on the core clock; this is the same clock as the ADCs. The core clock is the input clock divided by 4.

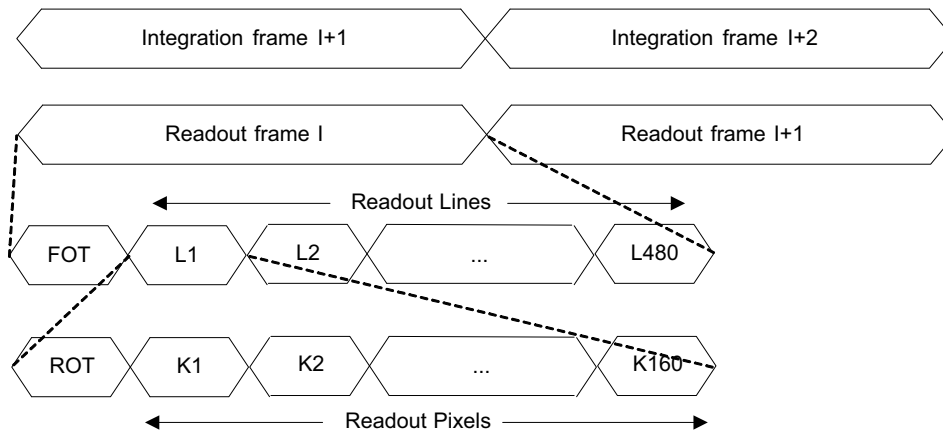


Figure 14. Global Readout Timing

#### Integration Timing in Mastermode

In mastermode the integration time, the dual slope (DS) integration time, and triple slope (TS) integration time are set by the SPI settings. Figure 15 shows the integration timing and the relationship with the SPI registers. The timing concerning integration is expressed in number of lines read out. The timing is controlled by four SPI registers which need to be uploaded with the desired number of lines. This number is then compared with the line counter that keeps track of the number of lines that is read out.

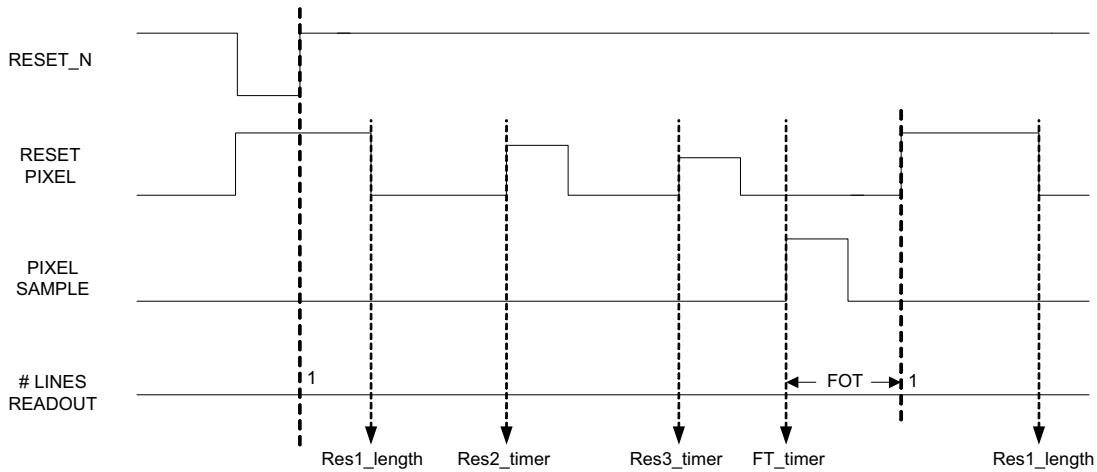
**RES1\_LENGTH <11:0>**: The number of lines read out (minus 1) after which the pixel reset drops and the integration starts.

**RES2\_TIMER <11:0>**: The number of lines read out (minus 1) after which the dual slope reset pulse is given. The length of the pulse is given by the formula:  $4 * (12 * (GRAN <1:0> + 1) + 1)$  (in clock cycles).

**RES3\_TIMER <11:0>**: The number of lines read out (minus 1) after which the triple slope reset pulse is given. The length of the pulse is given by the formula:  $4 * (12 * (GRAN <1:0> + 1) + 1)$  (in clock cycles).

**FT\_TIMER <11:0>**: The number of lines read out (minus 1) after which the Frame Transfer (FT) and the FOT starts. The length of the pulse is given by the formula:  $4 * (12 * (GRAN <1:0> + 1) + 1)$  (in clock cycles).

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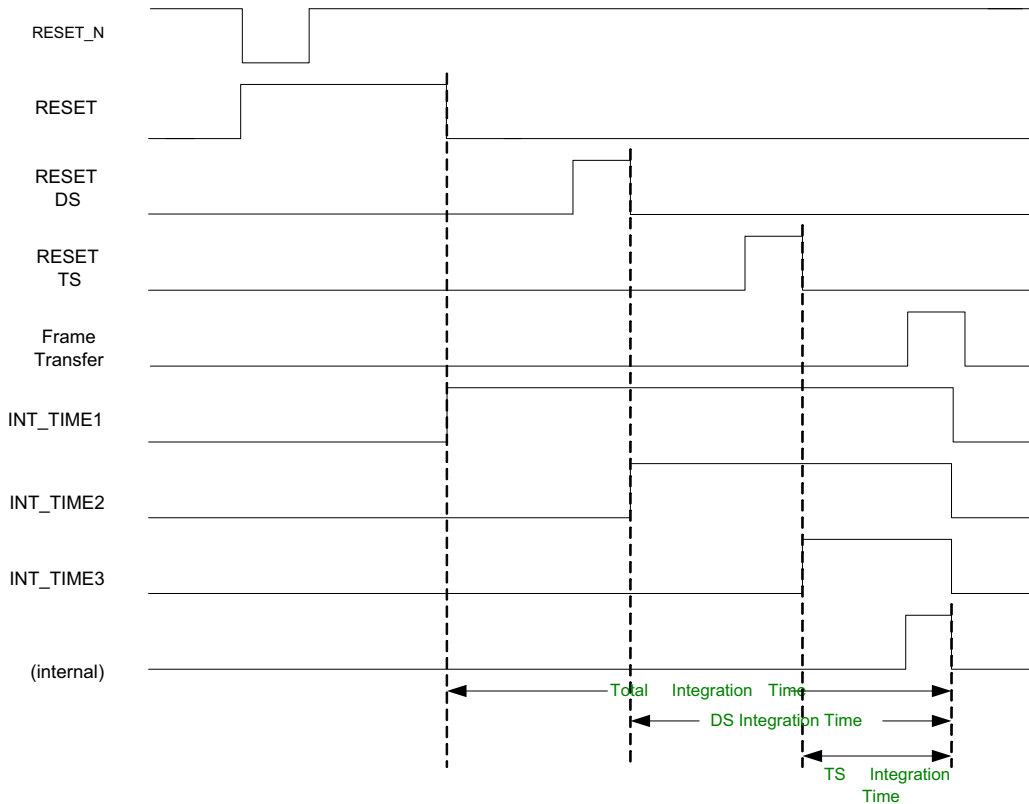


**Figure 15. Integration Timing in Master Mode**

The line counter starts with the value 1 immediately after the rising edge of **RESET\_N** and after the end of the **FOT**. This means that the four integration timing registers must be uploaded with the desired number of lines plus one.

In subsampling mode, the line counter increases with steps of two. In this mode, the counter starts with the value '2' immediately with the rising edge of **RESET\_N**. This means that for correct operation, the four integration timing registers can only be uploaded with an even number of lines if subsampling is enabled.

The length of the integration time, the DS integration time and the TS integration time are indicated by 3 output pins: **INT\_TIME\_1**, **INT\_TIME\_2** and **INT\_TIME\_3**. These outputs are high during the actual integration time. This is from the falling edge of the corresponding reset pulse to the falling edge of the internal pixel sample. Figure 16 illustrates this. The internal pixel sample rises at the moment defined by **FT\_TIMER** (see Figure 15) and the length of the pulse is  $4 * (12 * (\text{GRAN} < 1:0 > + 1) + 2)$ .



**Figure 16. INT\_TIME Timing**

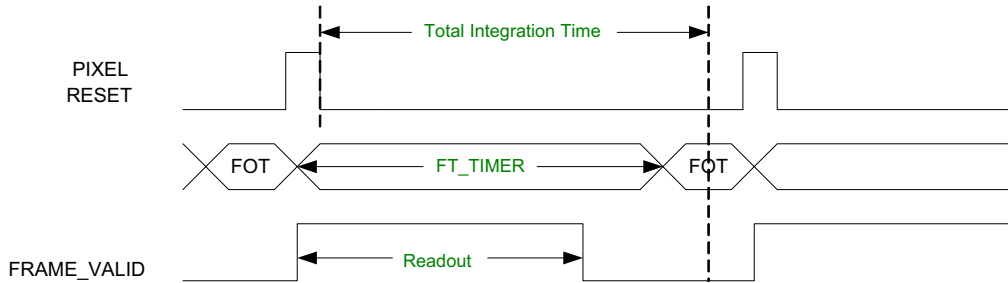


*Readout Time Smaller Than or Equal to Integration Time*

In this situation the RES\_LENGTH register can be uploaded with the smallest possible value, this is the value '2'. The frame rate is determined by the integration time. The readout time is equal to the integration time, the FT\_TIMER register is uploaded with a value equal to the window size to readout plus one. In case the readout time is smaller than the integration time the FT\_TIMER register is uploaded with a value bigger than the window size.

Figure 17 shows this principle. While the sensor is being readout the FRAME\_VALID signal goes high to indicate the time needed to read out the sensor.

When windowing in Y direction is desired in this mode (longer integration time than read out time) the following parameters should be set: The integration time is set by the FT\_TIMER register. The actual windowing in Y is achieved when the surrounding system discards the lines which are not desired for the selected window.

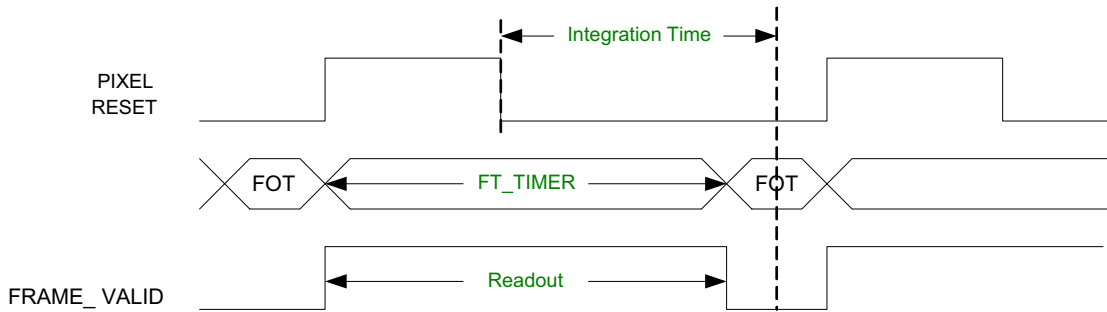


**Figure 17. Readout Time Smaller than Integration Time**

*Readout Time Larger Than Integration Time*

In case the readout time is larger than then integration time, the RES\_LENGTH register needs to be uploaded with a value larger than two to compensate for the larger readout

time. The FT\_TIMER register must be set to the desired window size (in Y). Only the RES\_LENGTH register needs to be changed during operation. Figure 18 shows this example.



**Figure 18. Readout Time Larger than Integration Time**

*Integration Timing in Slave Mode*

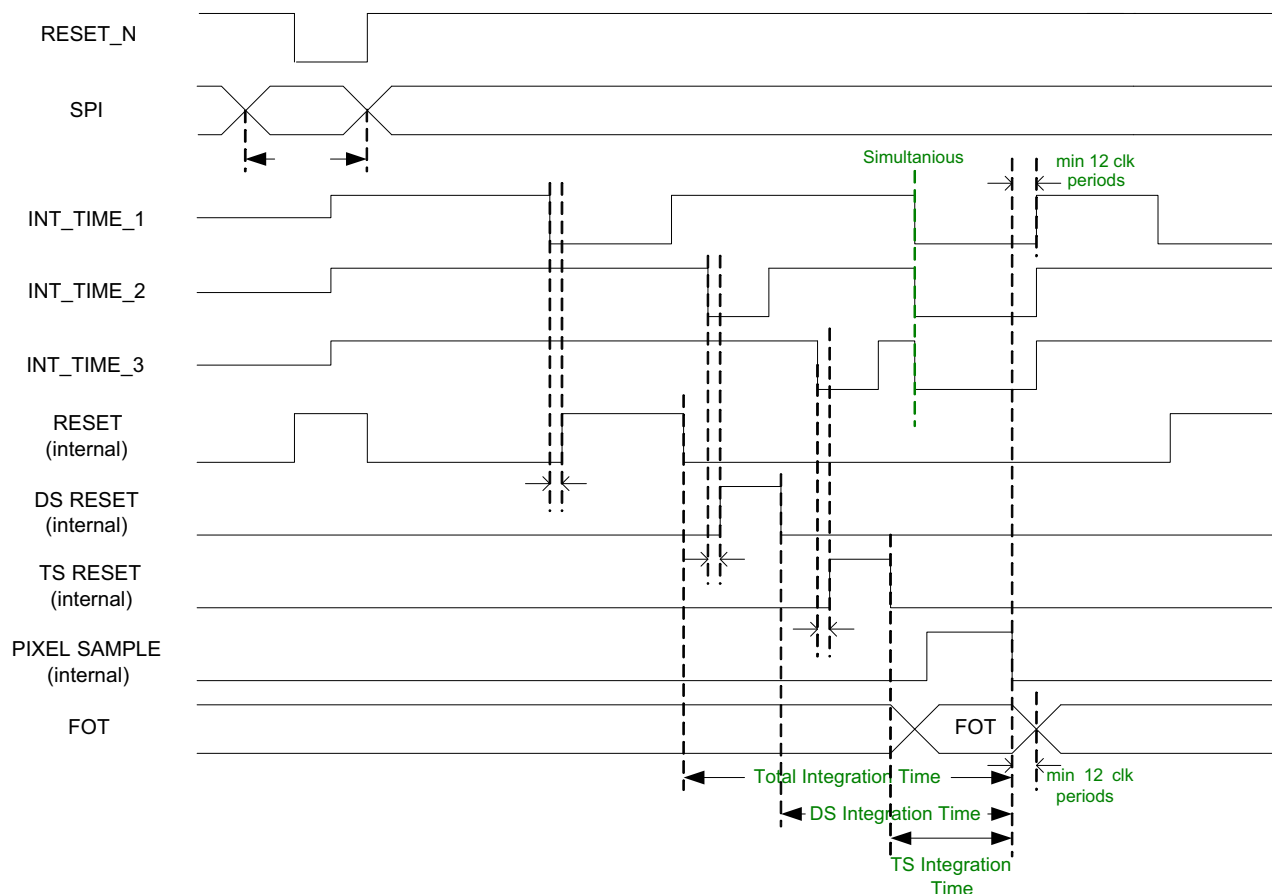
In slave mode, the registers RES\_LENGTH, DS\_TIMER, TS\_TIMER, and FT\_TIMER are ignored. The integration timing is now controlled by the pins INT\_TIME\_1, INT\_TIME\_2 and INT\_TIME\_3, which are now active low input pins.

The relationship between the input pins and the integration timing is illustrated in Figure 19. The pixel is reset as soon as IN\_TIME\_1 is low (active) and INT\_TIME\_2 and INT\_TIME\_3 are high. The integration starts when INT\_TIME\_1 becomes high again and during this integration additional (lower) reset can be given by

activating INT\_TIME\_2 and INT\_TIME\_3 separately. At the end of the desired integration time the frame transfer starts by making all 3 INT\_TIME pins active low simultaneously. There is always a small delay between the applied external signals and the actual internally generated pulses. These delays are also shown in Figure 19.

In case non destructive readout is used, the pulses on the input pins still need to be given. By setting the NDR bit to "1" the internal pixel reset pulses are suppressed but the external pulses are still needed to have the correct timing of the frame transfer.

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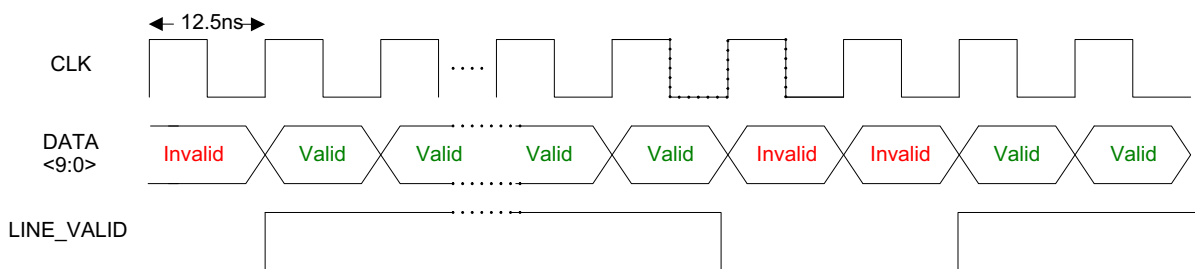
**Figure 19. Integration Timing in Slave Mode**

## Readout Timing

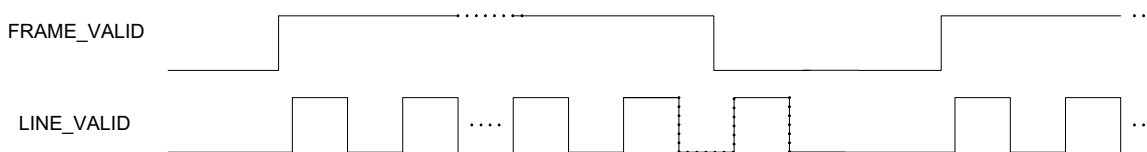
The sensor is readout row by row. The LINE\_VALID signal shows when valid data of a row is at the outputs. FRAME\_VALID shows which LINE\_VALIDs are valid.

LINE\_VALIDs when FRAME\_VALID is low, must be discarded. Figure 20 and Figure 21 illustrate this.

NOTE: The FRAME\_VALID signal automatically goes low after 480 LINE\_VALID pulses in mastermode.



**Figure 20. LINE\_VALID Timing**



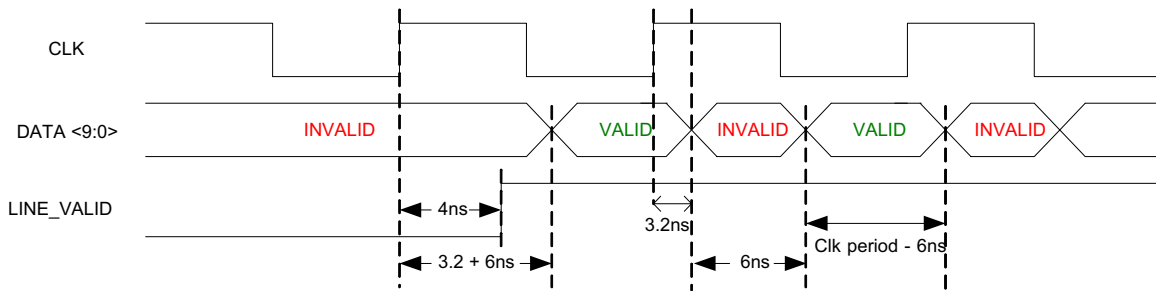
**Figure 21. FRAME\_VALID Timing**

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The data at the output of the sensor is clocked on the rising edge of CLK. There is a delay of 3.2 ns between the rising edge of CLK and a change in DATA<9:0>. After this delay DATA<9:0> needs 6 ns to become stable within 10% of VDDD. This means that DATA<9:0> is stable for a time

equal to the clock period minus 6 ns. Figure 22 illustrates this.

**NOTE:** In slave mode, line valids that occur beyond the desired image window should be discarded by the user's image data acquisition system



**Figure 22. DATA<9.0> Valid Timing**

### Readout Timing in Slave Mode

The start pointer of the window to readout is determined by the START\_X and START\_Y registers (as by readout in master mode). The size of the window in x-direction is also determined by the NB\_OF\_PIX register. The length of the window in y-direction is determined by the externally applied integration timing. The sensor does not know the desired y-size to readout. It therefore reads out all lines starting from START\_Y. The readout of lines continues until the user decides to start the FOT.

Even when the line pointer wants to address non existing rows (row 481 and higher), the sequencer continues to run in normal readout mode. This means that FRAME\_VALID remains high and LINE\_VALID is toggled as if normal lines are readout.

The controller should take care of this and ignore the LINE\_VALIDs that correspond with non existing lines and

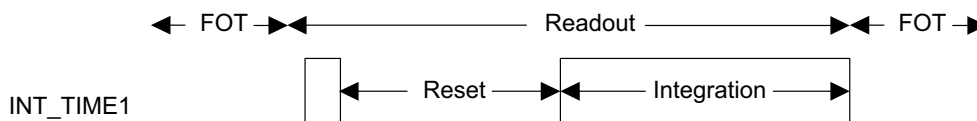
LINE\_VALIDs that correspond with lines that are not inside the desired readout window.

The length of the FOT and ROT is still controlled by the GRAN register as described in this data sheet.

### Readout time longer than integration time

The sensor should be timed according to the formulas and diagram here:

1. INT\_TIME\_1 should be brought high at time  $(read\_t - int\_t)$  and preferably immediately after the falling edge of LINE\_VALID.
2. At time  $read\_t$  all INT\_TIME\_x should simultaneously go low to start the FOT. This is immediately after the falling edge of the last LINE\_VALID of the desired readout window.

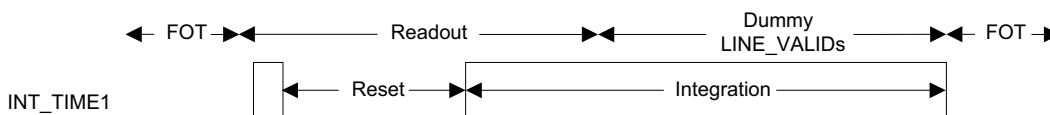


### Readout time shorter than integration time

The sensor should be timed according to the formulas and diagram here:

1. INT\_TIME\_1 should be brought high after a minimum 2  $\mu$ s reset time and preferably immediately after the falling edge of the first LINE\_VALID.

2. At time  $read\_t$  after the last valid LINE\_VALID of the desired window size, all other LINE\_VALIDs should be ignored.
3. After the desired integration length all INT\_TIME\_x should simultaneously go low to start the FOT.

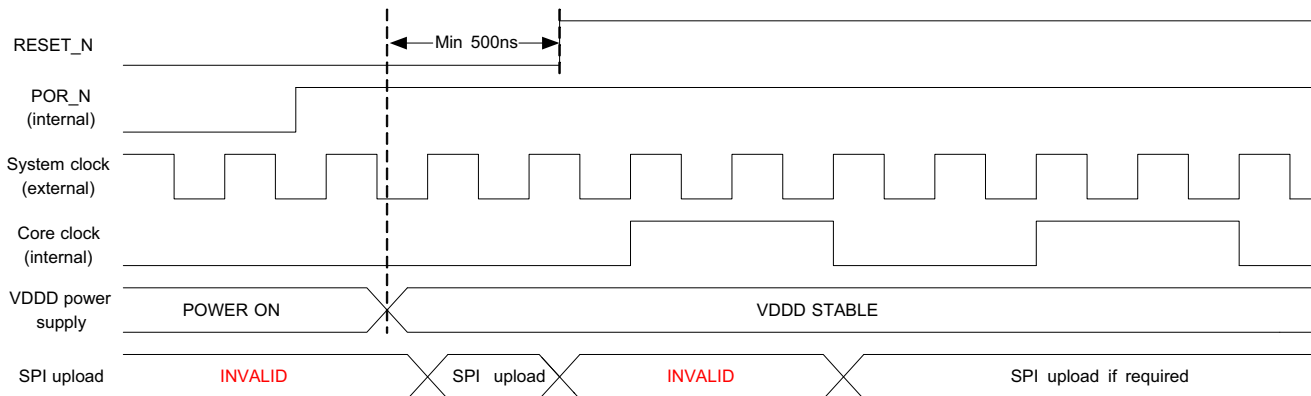


**Startup Timing**

On startup, VDDD should rise together with or before the other supplies. The rise of VDDD should be limited to 1V/100 μs to avoid activation of the on chip ESD protection circuitry.

During the rise of VDDD an on chip POR\_N signal is generated that resets the SPI registers to its default setting. After VDDD is stable the SPI settings can be uploaded to configure the sensor for future readout and light integration. When powering on the VDDD supply, the RESET\_N pin

should be kept low to reset the on chip sequencer and addressing logic. The RESET\_N pin must remain low until all initial SPI settings are uploaded. RESET\_N pin must remain low for at least 500 ns after ALL supplies are stable. The rising edge of RESET\_N starts the on chip clock division. The second rising edge of CLK after the rising edge of RESET\_N, triggers the rising edge of the core clock. Some SPI settings can be uploaded after the core clock has started.

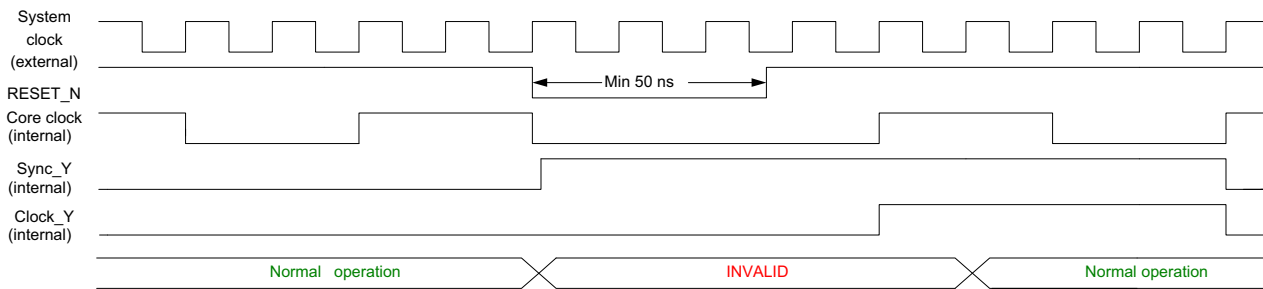


**Figure 23. Startup Timing**

**Sequencer Reset Timing**

By bringing RESET\_N low for at least 50 ns, the on chip sequencer is reset to its initial state. The internal clock division is restarted. The second rising edge of CLK after the

rising edge of RESET\_N the internal clock is restarted. The SPI settings are not affected by RESET\_N. If needed the SPI settings can be changed during a low level of RESET\_N.



**Figure 24. Sequencer Reset Timing**

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## PIN LIST

**Table 14. PINLIST**

Pin No.	Name	Type	Description
1	GND <sub>ADC</sub>	Ground	Ground supply of the ADCs
2	DATA<5>	Output	Databit<5>
3	DATA<6>	Output	Databit<6>
4	DATA<7>	Output	Databit<7>
5	DATA<8>	Output	Databit<8>
6	DATA<9>	Output	Databit<9> (MSB)
7	GND <sub>D</sub>	Ground	Digital ground supply
8	V <sub>DD</sub>	Supply	Digital power supply (2.5V)
9	GND <sub>ADC</sub>	Ground	Ground supply of the ADCs
10	V <sub>ADC</sub>	Supply	Power supply of the ADCs (2.5V)
11	GND <sub>A</sub>	Ground	Ground supply of analog readout circuitry
12	V <sub>DDA</sub>	Supply	Power supply of analog readout circuitry (2.5V)
13	ADC_BIAS	Biasing	Biasing of ADCs. Connect with 10 kΩ to V <sub>ADC</sub> and decouple with 100n to GND <sub>ADC</sub>
14	BIAS4	Biasing	Biasing of amplifier stage. Connect with 110 kΩ to V <sub>DDA</sub> and decouple with 100 nF to GND <sub>A</sub>
15	BIAS3	Biasing	Biasing of columns. Connect with 42 kΩ to V <sub>DDA</sub> and decouple with 100 nF to GND <sub>A</sub>
16	BIAS2	Biasing	Biasing of columns. Connect with 1.5 MΩ to V <sub>DDA</sub> and decouple with 100 nF to GND <sub>A</sub> .
17	BIAS1	Biasing	Biasing of imager core. Connect with 500 kΩ to V <sub>DDA</sub> and decouple with 100 nF to GND <sub>A</sub>
18	VPIX	Supply	Power supply of pixel array (2.5V)
19	SPI_ENABLE	Digital input	Enable of the SPI
20	SPI_CLK	Digital input	Clock of the SPI. (Max. 20 MHz)
21	SPI_DATA	Digital I/O	Data line of the SPI. Bidirectional pin
22	VMEM_H	Supply	Supply of vmem_high of pixelarray (3.3V)
23	GND_DRIVERS	Ground	Ground of pixel array drivers
24	VRESET_1	Supply	Reset supply voltage (typical 3.3V)
25	VRESET_2	Supply	Dual slope reset supply voltage. Connect to other supply or ground when dual slope reset is not used
26	VRESET_3	Supply	Triple slope reset supply voltage. Connect to other supply or ground when triple slope reset is not used
27	PRECHARGE_BIAS	Bias	Connect with 68 kΩ to VPIX and decouple with 100 nF to GND_DRIVERS
28	LINE_VALID	Digital output	Indicates when valid data is at the outputs. Active high
29	FRAME_VALID	Digital output	Indicates when valid frame is readout
30	INT_TIME_3	Digital I/O	In master mode: Output to indicate the triple slope integration time. In slave mode: Input to control the triple slope integration time
31	INT_TIME_2	Digital I/O	In master mode: Output to indicate the dual slope integration time. In slave mode: Input to control the dual slope integration time
32	INT_TIME_1	Digital I/O	In master mode: Output to indicate the integration time In slave mode: Input to control integration time
33	V <sub>DD</sub>	Supply	Digital power supply (2.5V)



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**Table 14. PINLIST**

Pin No.	Name	Type	Description
34	GND <sub>D</sub>	Ground	Digital ground supply
35	V <sub>DDA</sub>	Supply	Power supply of analog readout circuitry (2.5V)
36	GND <sub>A</sub>	Ground	Ground supply of analog readout circuitry
37	RESET_N	Digital input	Sequencer reset, active low
38	CLK	Digital input	Readout clock (80 MHz), sine or square clock
39	V <sub>ADC</sub>	Supply	Power supply of the ADCs (2.5V)
40	GND <sub>ADC</sub>	Ground	Ground supply of the ADCs
41	V <sub>DDO</sub>	Supply	Power supply of the output drivers (2.5V)
42	GND <sub>O</sub>	Ground	Ground supply of the output drivers
43	DATA<0>	Output	Databit<0> (LSB)
44	DATA<1>	Output	Databit<1>
45	DATA<2>	Output	Databit<2>
46	DATA<3>	Output	Databit<3>
47	DATA<4>	Output	Databit<4>
48	V <sub>ADC</sub>	Supply	Power supply of the ADCs (2.5V)

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## PACKAGE DRAWING

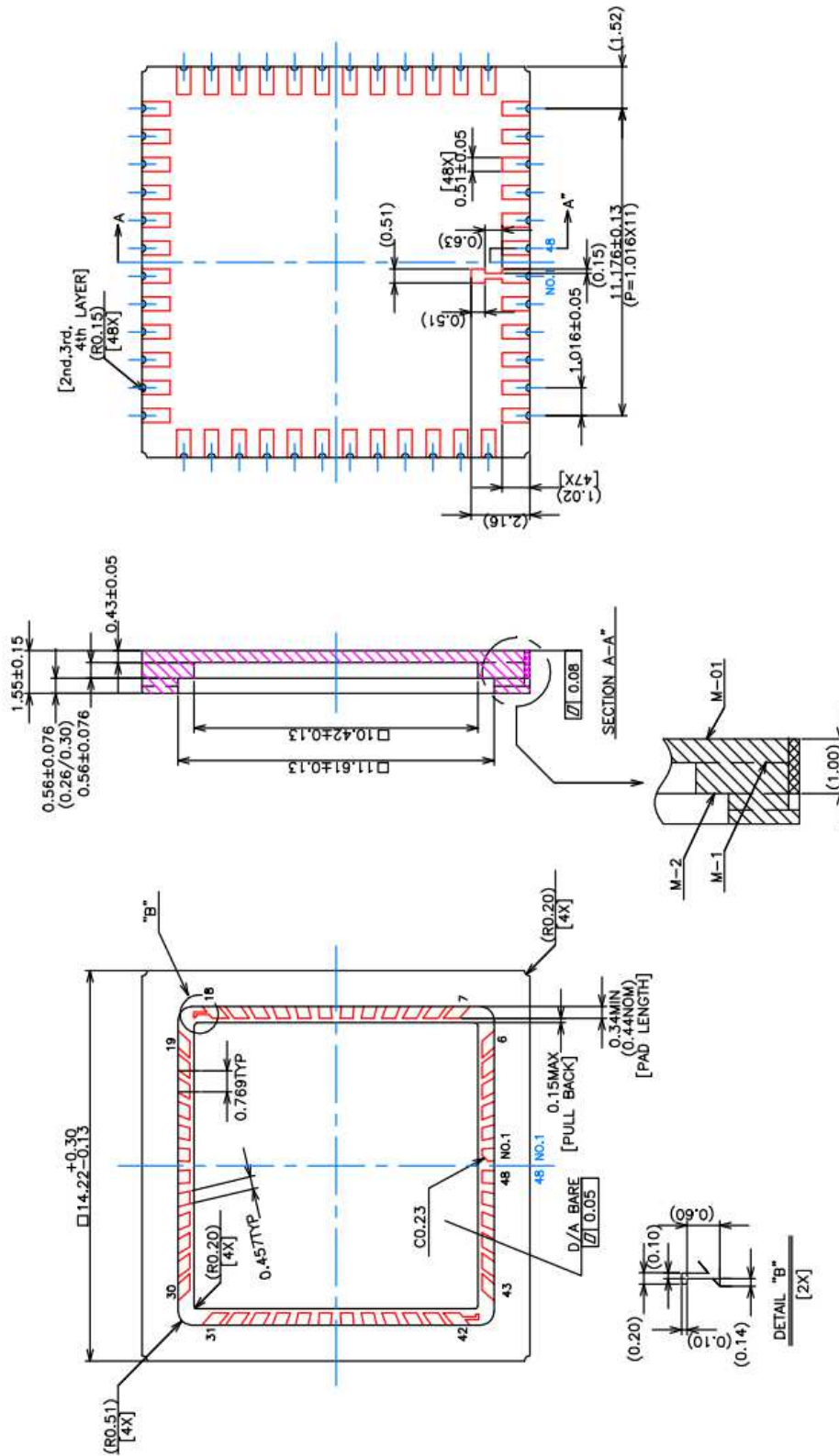


Figure 25. Package Drawing (001-45394)

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## Mechanical Package Specification

Mechanical Specifications		Min	Typ	Max	Units
Die (with Pin 1 to the left center)	Die thickness	-0.01	0.74	0.01	mm
	Die center, X offset to the center of the package	-50	0	50	μm
	Die center, Y offset to the center of the package	-50	0	50	μm
	Die position, X tilt	-1	0	1	deg
	Die position, Y tilt	-1	0	1	deg
	Die placement accuracy in package	-50		50	μm
	Die rotation accuracy	-1		1	deg
	Optical center referenced from package center (X-dir)		6.1		mm
	Optical center referenced from package center (Y-dir)		7.1		mm
	Distance from PCB plane to top of the die surface		1.25		mm
	Distance from top of the die surface to top of the glass lid		1		mm
Glass Lid	Thickness		0.6		mm
	Spectral range for window	400		1000	nm
	Transmission of the glass lid			92	%
Mechanical shock	JESD22-B104C; Condition G			2000	G
Vibration	JESD22-B103B; Condition 1	20		2000	Hz
Mounting Profile	Lead-free Infra-Red (IR) profile for LCC package if no socket is used				