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NOIP1SN025KA, NOIP1SN016KA, NOIP1SN012KA, NOIP1SN010KA

PYTHON 25K/16K/12K/10K Global Shutter CMOS Image Sensors

ON Semiconductor®

www.onsemi.com

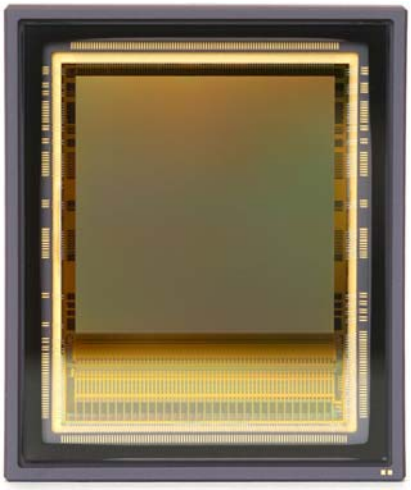


Figure 1. PYTHON XK Photograph

Features

- A Pin-compatible Family with Multiple Resolutions:
  - 25K = 5120 x 5120 Active Pixels
  - 16K = 4096 x 4096 Active Pixels
  - 12K = 4096 x 3072 Active Pixels
  - 10K = 3840 x 2896 Active Pixels
- 4.5 μm x 4.5 μm Low Noise Global Shutter Pixels with In-pixel Correlated Double Sampling (CDS)
- APS−H Optical Format (32.6 mm Diagonal) for 25K
- Monochrome (SN), Color (SE) and NIR (FN)
- Random Programmable Region of Interest (ROI) Readout
- Pipelined and Triggered Global Shutter
- On-chip Fixed Pattern Noise (FPN) Correction
- 10-bit Analog-to-Digital Converter (ADC)
- 32 Low-voltage Differential Signaling (LVDS) High-speed Serial Outputs
- Serial Peripheral Interface (SPI)
- High-speed: 80 Frames per Second (fps) at 25 Mpix
- 4.6 W Power Dissipation at Full Resolution, x32 LVDS Mode
- Operational Range: −40°C to +85°C
- 355-pin μPGA Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Machine Vision
- Motion Monitoring
- Intelligent Traffic Systems (ITS)
- Pick and Place Machines
- Inspection
- Metrology

Description

The PYTHON xK family of CMOS image sensors provide high resolution with very high bandwidth (up to 80 frame per second readout for 25 megapixel readout) in a pin−compatible family of devices.

The high sensitivity 4.5 μm pixels support both pipelined and triggered global shutter readout modes. The sensor also supports correlated double sampling (CDS) readout in global shutter mode, reducing noise and increasing dynamic range.

The sensor is programmed using a four−wire serial peripheral interface. Black level can be calibrated automatically, or adjusted using a user programmable offset. The sensor also supports readout of up to 32 separate regions of interest (ROI) to increase frame rate. Image data is accessed through 32, 16, 8, or 4 LVDS channels, each running at 720 Mbps, and a separate synchronization channel is provided to facilitate image reconstruction.

The PYTHON xK family is packaged in a 355-pin μPGA package and is available in a monochrome, Bayer color, and extended near−infrared (NIR) configurations.

ORDERING INFORMATION

Part Number	Family	Description	Package	Product Status
NOIP1SN025KA-GDI	PYTHON 25K	25 MegaPixel, LVDS mono micro lens	355−pin µPGA	Production
NOIP1SE025KA-GDI		25 MegaPixel, LVDS color micro lens		
NOIP1FN025KA-GDI		25 MegaPixel, LVDS mono micro lens, NIR		
NOIP1SN016KA-GDI	PYTHON 16K	16 MegaPixel, LVDS mono micro lens		
NOIP1SE016KA-GDI		16 MegaPixel, LVDS color micro lens		
NOIP1FN016KA-GDI		16 MegaPixel, LVDS mono micro lens, NIR		
NOIP1SN012KA-GDI	PYTHON 12K	12 MegaPixel, LVDS mono micro lens		
NOIP1SE012KA-GDI		12 MegaPixel, LVDS color micro lens		
NOIP1FN012KA-GDI		12 MegaPixel, LVDS mono micro lens, NIR		
NOIP1SN010KA-GDI	PYTHON 10K	10 MegaPixel, LVDS mono micro lens		
NOIP1SE010KA-GDI		10 MegaPixel, LVDS color micro lens		
NOIP1FN010KA-GDI		10 MegaPixel, LVDS mono micro lens, NIR		

The P1−SN/SE/FN base part is used to reference the mono, color and NIR enhanced versions of the LVDS interface. More details on the part number coding can be found at http://www.onsemi.com/pub_link/Collateral/TND310−D.PDF

Package Mark

Side 1 near Pin 1: **NOIP1xx0RRKA−GDI** where xx denotes mono micro lens (SN) or color micro lens (SE) or NIR mono micro lens (FN), RR is the resolution of the sensor in MP (25, 16, 12 or 10)

Side 2: **AWLYYWW,** where AWL is Production lot traceability, and YYWW is the 4−digit date code

SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	Specification
Pixel Type	Global shutter pixel architecture
Shutter Type	Pipelined and triggered global shutter
Optical Format	25K: APS–H 16K: APS–H 12K: 4/3” 10K: 4/3”
Frame Rate at Full Resolution	80 frames per second @ 25K 120 frames per second @ 16K 160 frames per second @ 12K 175 frames per second @ 10K
Master Clock	360 MHz
Windowing	32 Randomly programmable windows. Normal, sub-sampled and binned readout modes
ADC Resolution (Note 1)	10-bit
LVDS Outputs	32 data + 1 sync + 1 clock
Data Rate	32 x 720 Mbps
Power Consumption	4.6 W
Package Type	355 μPGA
Color	RGB color, mono

1. The ADC is 11-bit, down-scaled to 10-bit. The PYTHON XK uses a larger word-length internally to provide 10-bit on the output.

Table 2. ELECTRO–OPTICAL SPECIFICATIONS

Parameter	Specification
Active Pixels	25K: 5120 (H) x 5120 (V) 16K: 4096 (H) x 4096 (V) 12K: 4096 (H) x 3072 (V) 10K: 3840 (H) x 2896 (V)
Pixel Size	4.5 μm x 4.5 μm
Conversion Gain	0.085 LSB10/e^- , 130 μV/e^-
Temporal Noise	< 14 e^- (Non–Zero ROT, 1x gain)
Responsivity at 550 nm	5.8 V/lux.s
Parasitic Light Sensitivity (PLS)	< 1/5000
Full Well Charge	> 12000 e^-
Quantum Efficiency (QE) x FF	50% at 550 nm
Pixel FPN (Note 2)	< 0.9 LSB10
PRNU (Note 2)	< 1%
MTF	68% @ 535 nm – X–dir & Y–dir 68% @ 535 nm – X–dir & Y–dir (NIR)
PSNL @ 20°C (t_int = 30 ms)	91 LSB10/s, 1100 e^-/s
Dark signal @ 20°C	3.9 e^-/s, 0.33 LSB10/s
Dynamic range	59 dB
Signal-to-Noise Ratio (SNR max)	41 dB

2. Only includes high–frequency component

Table 3. RECOMMENDED OPERATING RATINGS (Note 3)

Symbol	Description	Min	Max	Units
T_J	Operating temperature range	–40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ABSOLUTE MAXIMUM RATINGS (Note 4)

Symbol	Parameter	Min	Max	Units
ABS (1.0 V supply)	ABS rating for 1.0 V supply	–0.5	1.2	V
ABS (1.8 V supply group)	ABS rating for 1.8 V supply group	–0.5	2.2	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	–0.5	4.3	V
ABS (4.2 V supply)	ABS rating for 4.2 V supply	–0.5	4.6	V
ABS (4.5 V supply)	ABS rating for 4.5 V supply	–0.5	5.0	V
T_S (Notes 4 and 5)	ABS storage temperature range	0	150	°C
	ABS storage humidity range at 85°C		85	%RH
Electrostatic discharge (ESD) (Notes 3 and 4)	Human Body Model (HBM): JS−001−2010	2000		V
	Charged Device Model (CDM): JESD22−C101	500		
LU	Latch-up: JESD−78	140		mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Operating ratings are conditions in which operation of the device is intended to be functional.
4. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
5. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

Table 5. ELECTRICAL SPECIFICATIONS

Boldface Limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C (Notes 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Units
Power Supply Parameters					
vdda_33	Analog supply - 3.3 V domain. gnda_33 is connected to substrate	**3.2**	3.3	**3.4**	V
Idda_33	Current consumption from analog supply		910		mA
vddd_33	Digital supply - 3.3 V domain. gndd_33 is connected to substrate	**3.2**	3.3	**3.4**	V
Iddd_33	Current consumption from 3.3 V digital supply		90		mA
vdd_18	Digital supply - 1.8 V domain. gndd_18 is connected to substrate	**1.7**	1.8	**1.9**	V
Idd_18	Current consumption 1.8 V digital supply		540		mA
vdd_pix	Pixel array supply	**3.25**	3.3	**3.35**	V
Idd_pix	Current consumption from pixel supply		115		mA
vdd_resfd	Floating diffusion reset supply		4.2		V
gnd_resfd	Floating diffusion reset ground. Not connected to substrate **Note** This is a sinking power supply with 200 mA range.		0		V
vdd_trans	Pixel transfer supply		3.3		V
gnd_trans	Pixel transfer ground. Not connected to substrate. **Note** This is a sinking power supply with 200 mA range.		0		V

6. All parameters are characterized for DC conditions after thermal equilibrium is established.
7. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high−impedance circuit.
8. Minimum and maximum limits are guaranteed through test and design.
9. Vref_colmux supply should be able to source and sink current

Table 5. ELECTRICAL SPECIFICATIONS

Boldface Limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C (Notes 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Units
vdd_calib	Pixel calibration supply		4.2		V
gnd_calib	Pixel calibration ground. Not connected to substrate		0		V
vdd_sel	Pixel select supply		4.2		V
gnd_sel	Pixel select ground. Not connected to substrate.	0	0	0	V
vdd_casc	Cascode supply		1.0		V
vref_colmux [9]	Column multiplexer reference supply		1.0		V
gnd_colbias	Column biasing ground. Dedicated ground signal for pixel biasing. Connected to substrate		0		V
gnd_colpc	Column precharge ground. Dedicated ground signal for pixel biasing. Not connected to substrate		0		V
Ptot	Total power consumption		4600		mW
Popt	Power consumption at lower pixel rates		Configurable		
I/O - LVDS (EIA/TIA-644): Conforming to standard/additional specifications and deviations listed					
fserdata	Data rate on data channels DDR signaling - 32 data channels, 1 synchronization channel			720	Mbps
fserclock	Clock rate of output clock Clock output for mesochronous signaling			360	MHz
Vicm	LVDS input common mode level	0.3	1.25	2.2	V
Tccsk	Channel to channel skew (training pattern allows per-channel skew correction)			50	ps
LVDS Electrical/Interface					
fin	Input clock rate			360	MHz
tidc	Input clock duty cycle	45	50	55	%
tj	Input clock jitter		20		ps
fspi	SPI clock rate			10	MHz
ratspi	10-bit (32 LVDS channels): ratio: fin/fspi	30			
	10-bit (16 LVDS channels): ratio: fin/fspi	60			
	10-bit (8 LVDS channels): ratio: fin/fspi	120			
	10-bit (4 LVDS channels): ratio: fin/fspi	240			

6. All parameters are characterized for DC conditions after thermal equilibrium is established.
7. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high−impedance circuit.
8. Minimum and maximum limits are guaranteed through test and design.
9. Vref_colmux supply should be able to source and sink current

Table 5. ELECTRICAL SPECIFICATIONS

Boldface Limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C (Notes 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Units
Sensor Requirements					
FOT	Frame overhead time		50		μs
ROT	Row overhead time		1		μs
fpix	Pixel rate (32 channels at 72 Mpix/s)			2304	Mpix/s

Frame Specifications

		Typical		Max	Units
		Non−Zero ROT	Zero ROT		
fps_roi1	Xres x Yres = 5120 x 5120	47	80		fps
fps_roi2	Xres x Yres = 4096 x 4096	65	120		fps
fps_roi3	Xres x Yres = 4096 x 3072	85	160		fps
fps_roi4	Xres x Yres = 3840 x 2896	95	175		fps
fps_roi5	Xres x Yres = 3840 x 2160	125	235		fps
fps_roi6	Xres x Yres = 2880 x 2896	105	175		fps
fps_roi7	Xres x Yres = 2048 x 2048	170	250		fps
fpix	Pixel rate (32 channels at 72 Mpix/s)			2304	Mpix/s

6. All parameters are characterized for DC conditions after thermal equilibrium is established.
7. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high−impedance circuit.
8. Minimum and maximum limits are guaranteed through test and design.
9. Vref_colmux supply should be able to source and sink current

Disclaimer: Image sensor products and specifications are subject to change without notice. Products are warranted to meet the production data sheet and acceptance criteria specifications only.

Color Filter Array

The PYTHON XK color sensor is processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left. Green1 and green2 have a slightly different spectral response due to (optical) cross talk from neighboring pixels. Green1 pixels are located on a green-red row, green2 pixels are located on a blue-green row.

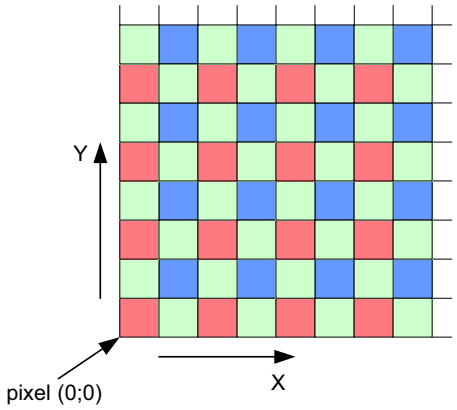


Figure 2. Color Filter Array for the Pixel Array

Quantum Efficiency

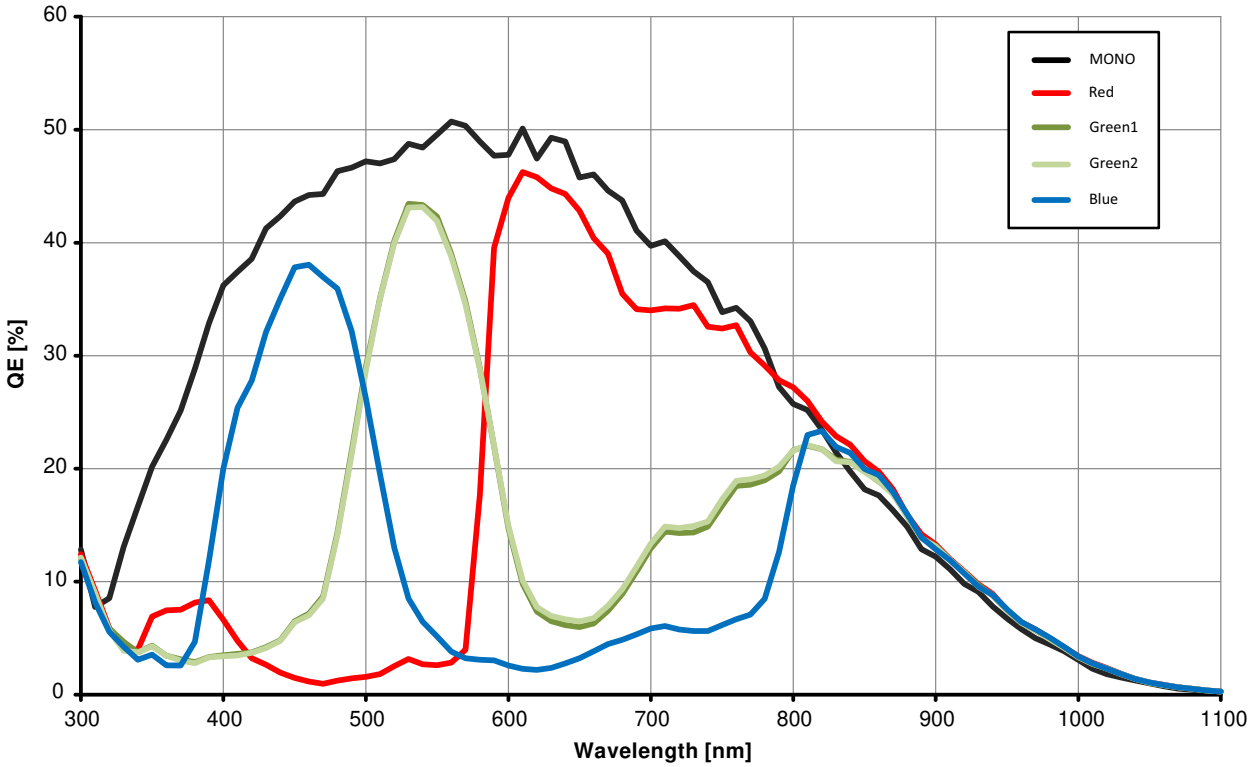


Figure 3. Quantum Efficiency Curve for Mono and Color

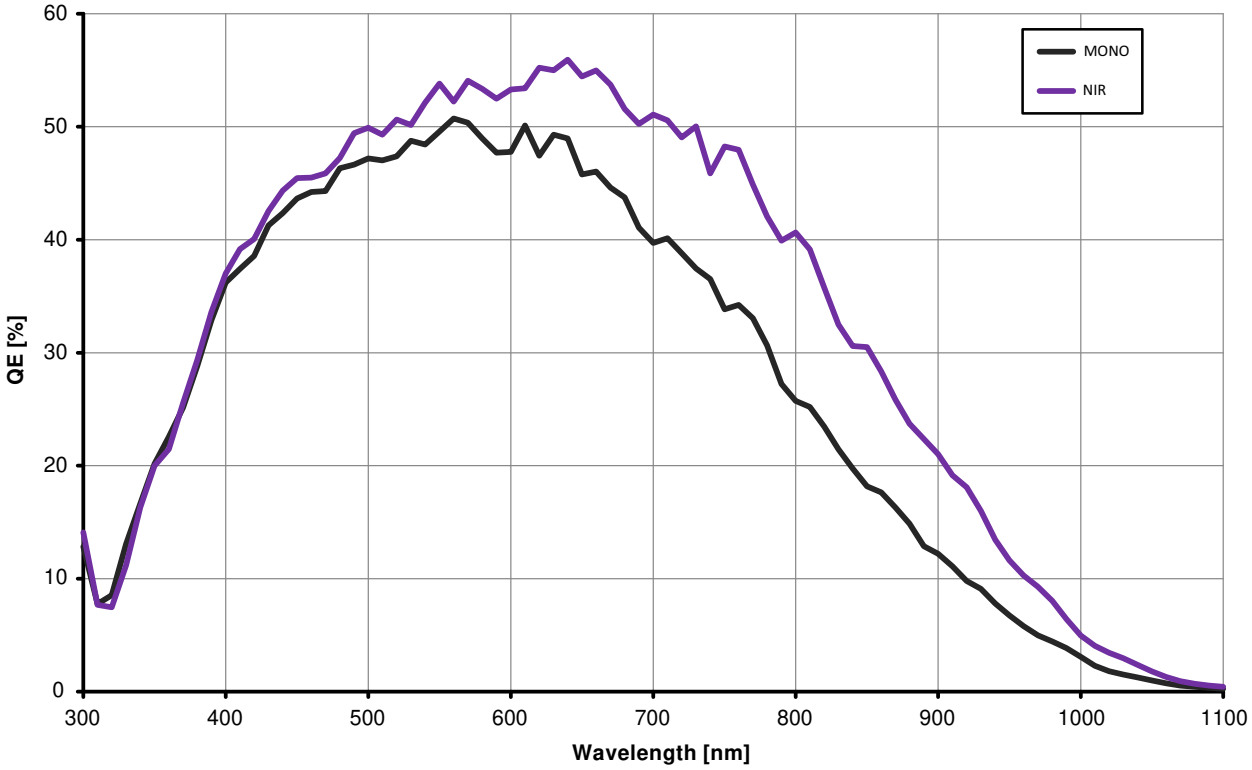


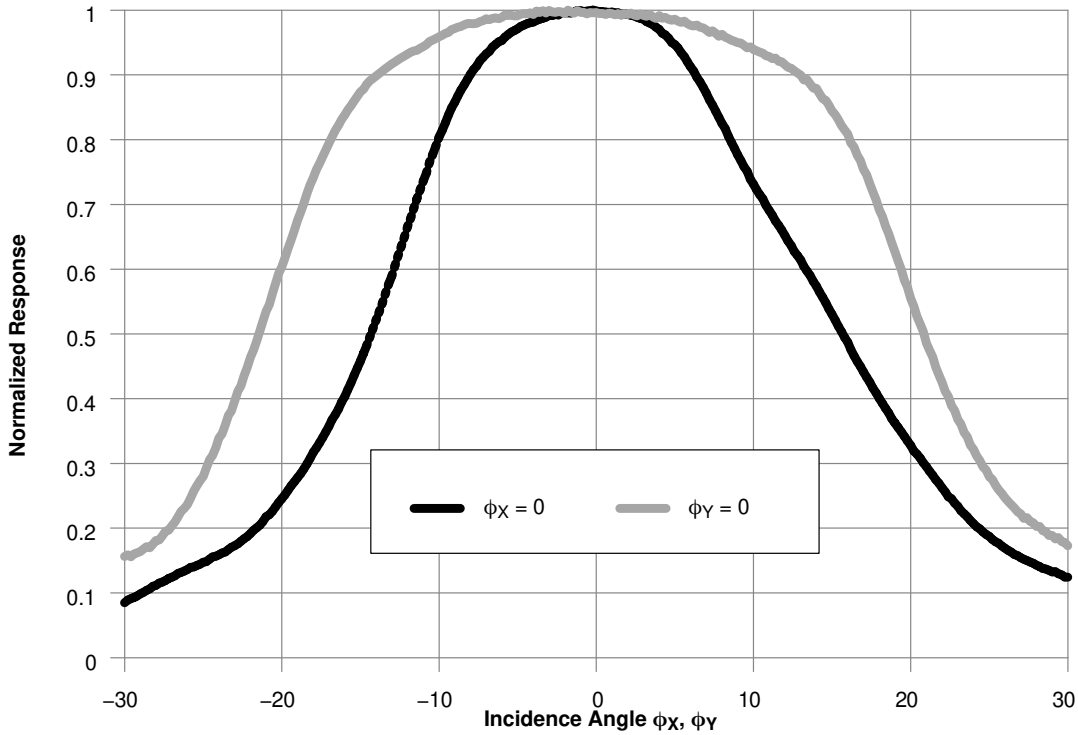
Figure 4. Quantum Efficiency Curve for Standard and NIR Mono

Ray Angle and Microlens Array Information

An array of microlenses is placed over the CMOS pixel array in order to improve the absolute responsivity of the photodiodes. The combined microlens array and pixel array has two important properties:

1. Angular dependency of photoresponse of a pixel
   The photoresponse of a pixel with microlens in the center of the array to a fixed optical power with varied incidence angle is as plotted in Figure 5, where definitions of angles ϕx and ϕy are as described by Figure 6.
2. Microlens shift across array and CRA
   The microlens array is fabricated with a slightly smaller pitch than the array of photodiodes. This difference in pitch creates a varying degree of shift of a pixel's microlens with regards to its photodiode. A shift in microlens position versus photodiode position will cause a tilted angle of peak photoresponse, here denoted Chief Ray Angle (CRA). Microlenses and photodiodes are aligned with 0 shift and CRA in the center of the array, while the shift and CRA increases radially towards its edges, as illustrated by Figure 7.

The purpose of the shifted microlenses is to improve the uniformity of photoresponse when camera lenses with a finite exit pupil distance are used. In the standard version of PYTHONxK, the CRA varies nearly linearly with distance from the center as illustrated in Figure 8, with a corner CRA of approximately 10.6 degrees (for 5120 x 5120 resolution). This edge CRA is matching a lens with exit pupil distance of ~85 mm.



[degrees deviation from normal]
Note that the photoresponse peaks near normal incidence for center pixels.

Figure 5. Center Pixel Photoresponse to a Fixed Optical Power with Incidence Angle Varied Along ϕ_X and ϕ_Y

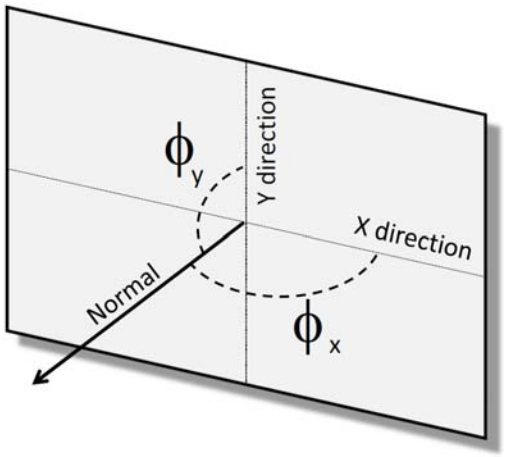
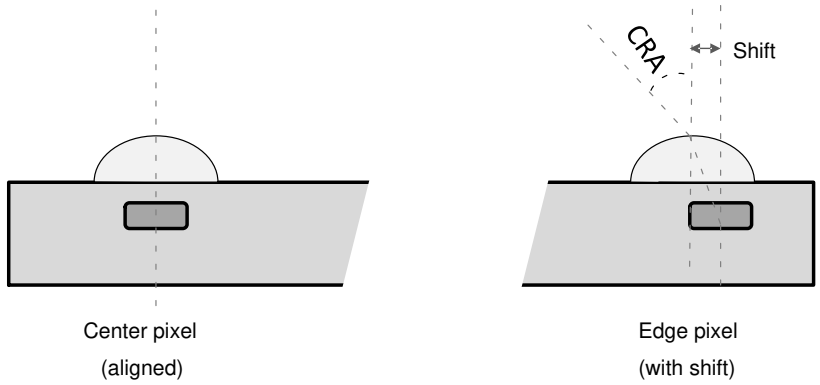


Figure 6. Definition of Angles used in Figure 5.



The center axes of the microlens and the photodiode coincide for the center pixels. For the edge pixels, there is a shift between the axis of the microlens and the photodiode causing a peak response incidence angle (CRA) that deviates from the normal of the pixel array.

Figure 7. Principle of Microlens Shift

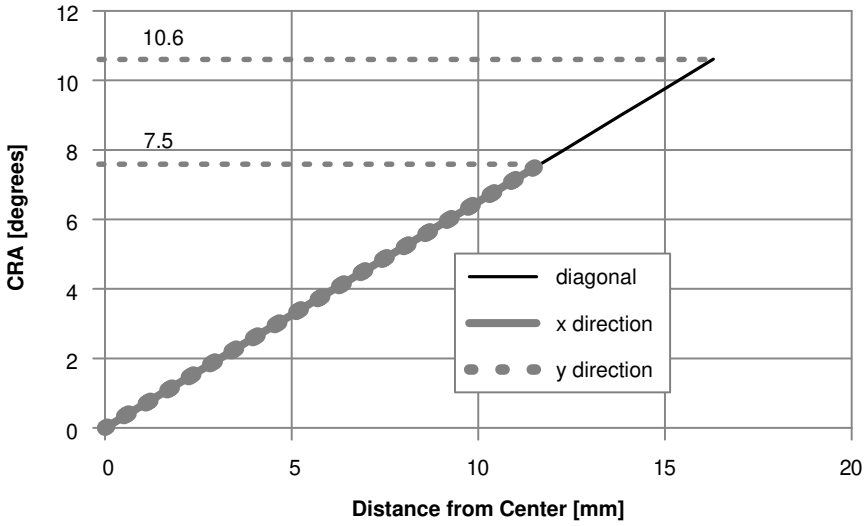


Figure 8. Variation of Peak Responsivity Angle (CRA) as a Function of Distance from the Center of the Array

OVERVIEW

Figure 9 gives an overview of the major functional blocks of the PYTHON sensor.

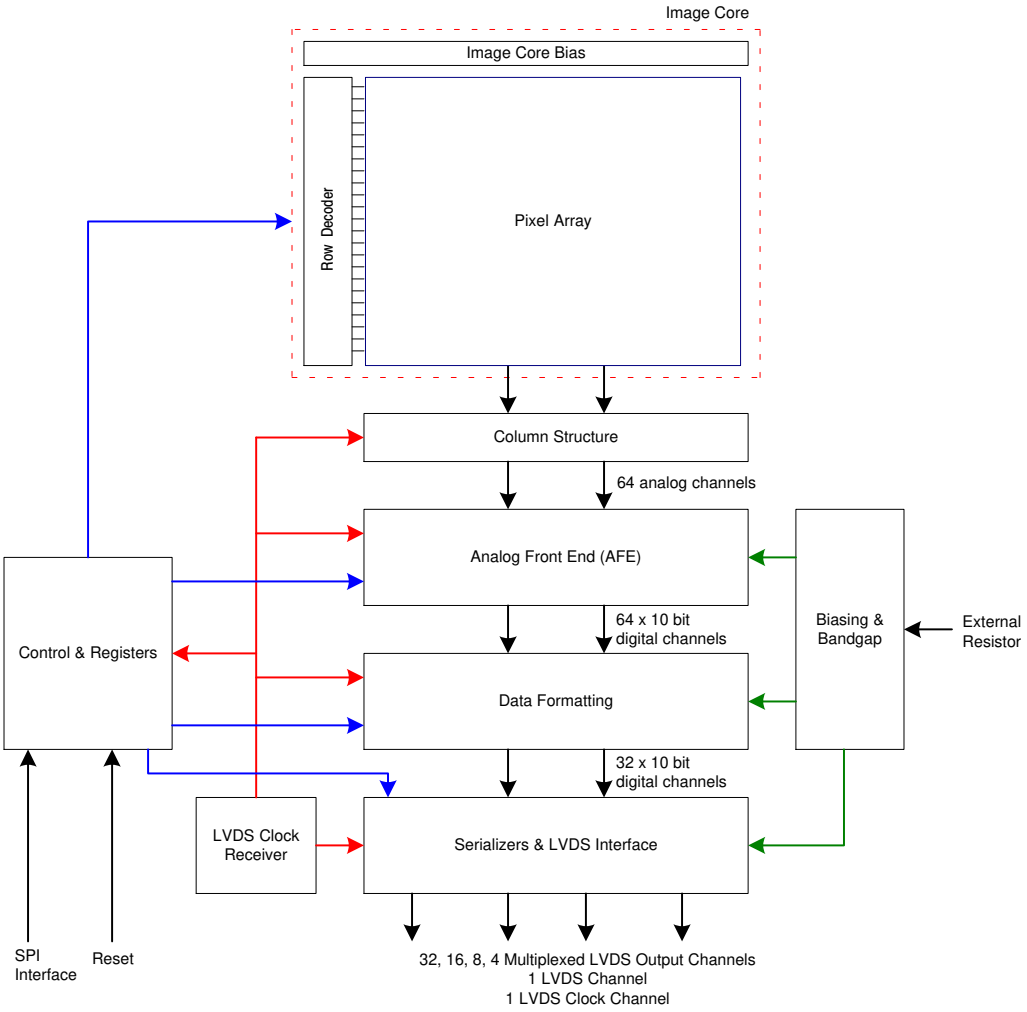


Figure 9. Block Diagram

Image Core

The image core consists of:

- Pixel array
- Address decoders and row drivers
- Pixel biasing

The PYTHON 25MP pixel array contains 5120 (H) x 5120 (V) readable pixels with a pixel pitch of 4.5 µm.

The PYTHON 16MP/12MP/10MP image arrays contain 4224 (H) x 4112 (V) / 4224 (H) x 3088 (V) / 3968 (H) x 2912 (V) readable pixels, inclusive of 8 pixel rows and 64 pixel columns at every side to allow for reprocessing or color reconstruction. The sensor uses in-pixel CDS architecture, which makes it possible to achieve a low noise read out of the pixel array in both global shutter shutter mode with CDS.

The function of the row drivers is to access the image array to reset or read the pixel data. The row drivers are controlled by the on-chip sequencer and can access the pixel array.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 360 MHz. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

The 5120 pixels of one image row are stored in 5120 column sample-and-hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 64 parallel differential outputs operating at a frequency of 36 MHz.

At this stage, the reset signal and integrated signal values are transferred into an FPN-corrected differential signal. A programmable gain of 1x, 2x, or 4x can be applied to the signal at this stage. The column multiplexer also supports a subsampled readout mode (read-1-skip-1 for mono and read-2-skip-2 for color version). Enabling this mode can speed up the frame rate, with a decrease in resolution.

Bias Generator

The bias generator generates all required reference voltages and bias currents that the on-chip blocks use. An external resistor of 47 kΩ, connected between the pins *ibias_master* and *ibias_out* is required for the bias generator to operate properly.

Analog Front End

The AFE contains 64 channels, each containing a PGA and a 10-bit ADC.

For each of the 64 channels, a pipelined 10-bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one LVDS block. A cyclic redundancy check (CRC) code is calculated on the passing data. For each LVDS output channel, one data block is instantiated. An extra data block is foreseen to transmit synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface

The serializer and LVDS interface block receives the formatted (10-bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

The maximum output data bit rate is 720 Mbps per channel.

In addition to the 32 LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system-level image reconstruction.

Sequencer

The sequencer:

- Controls the image core. Starts and stops integration and controls pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

OPERATING MODES

Global Shutter Mode

The PYTHON operates in pipelined or triggered global shutter modes. In this mode, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 10 shows the integration and readout sequence for the global shutter mode. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially. The integration starts at a certain period, relative to the frame start.

Pipelined Global Shutter Mode

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N–1. The readout of every frame starts with a frame overhead time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by the row overhead time (ROT). Figure 11 shows the exposure and readout time line in pipelined global shutter mode.

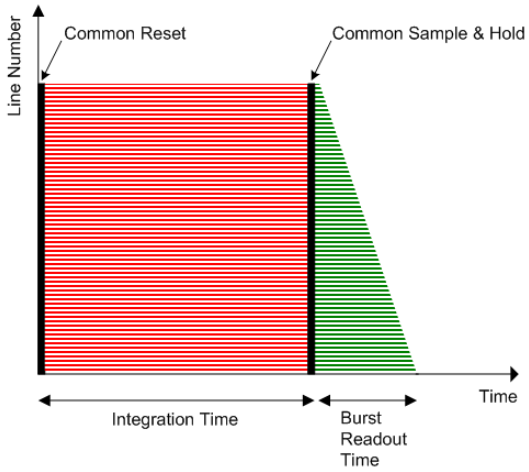


Figure 10. Global Shutter Operation

Master Mode

In this operation mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

Slave Mode

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins.

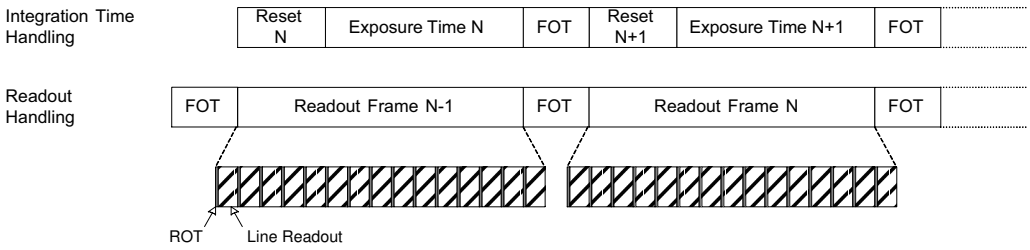


Figure 11. Pipelined Shutter Operation in Master Mode

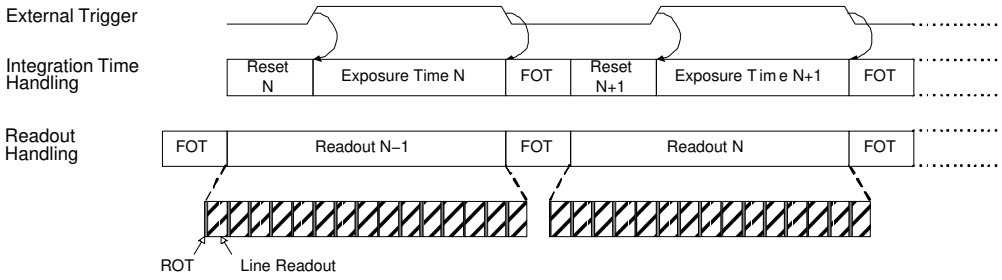


Figure 12. Pipelined Shutter Operation in Slave Mode

Triggered Global Shutter

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences from the pipelined shutter master mode are:

- Upon user action, a single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is user-controlled through an external pin. This mode requires manual intervention for every frame.

  The pixel array is kept in reset state until requested.

The triggered global mode can also be controlled in a master or in a slave mode.

Master Mode

In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is readout sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge. Figure 13 shows the relation between the external trigger signal and the exposure/readout timing. If a rising edge is applied on the external trigger before the exposure time and FOT of the previous frame is complete, it is ignored by the sensor.

Slave Mode

Integration time control is identical to the pipelined shutter slave mode. An external synchronization pin controls the start of integration. When it is de−asserted, the FOT starts. The analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

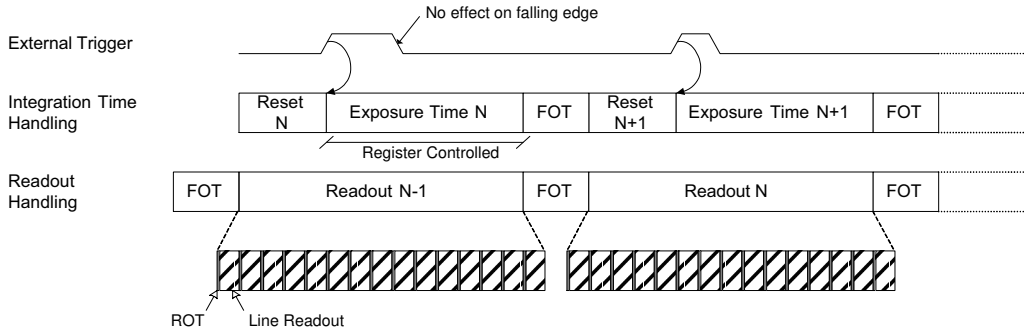


Figure 13. Triggered Shutter Operation in Master Mode

Non−Zero and Zero Row Overhead Time (ROT) Modes

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read out and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value of the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by a Row Overhead Time (ROT) as shown in Figure 14.

In Reduced/Zero ROT operation mode (refer to Figure 15), the row blanking and kernel readout occur in parallel. This mode is called reduced ROT as a part of the ROT is done while the image row is readout. The actual ROT can thus be longer, however the perceived ROT will be shorter (‘overhead’ spent per line is reduced).

This operation mode can be used for two reasons:

- Reduced total line time.
- Lower power due to reduced clock rate.

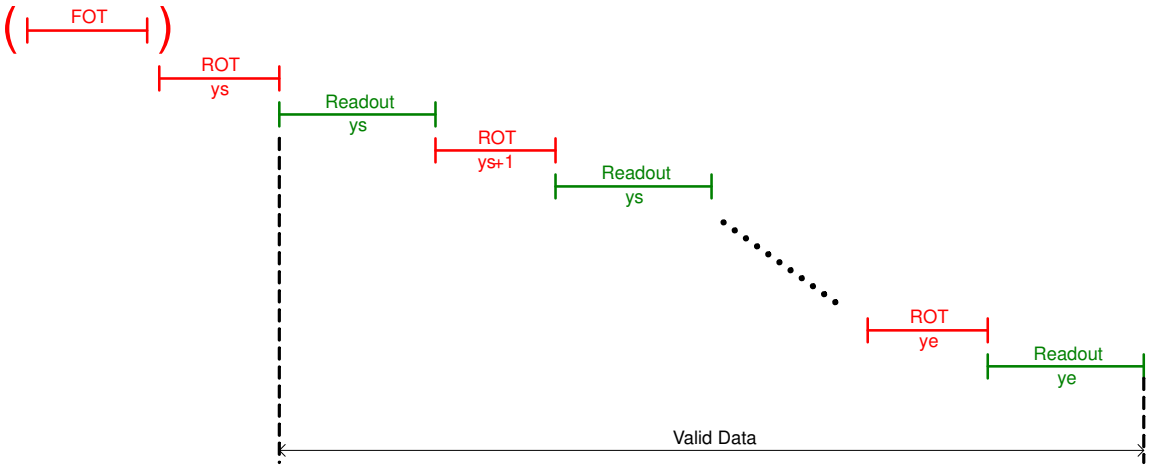


Figure 14. Integration and Readout Sequence of the Sensor Operating in Pipelined Global Shutter Mode with Non−Zero ROT Readout.

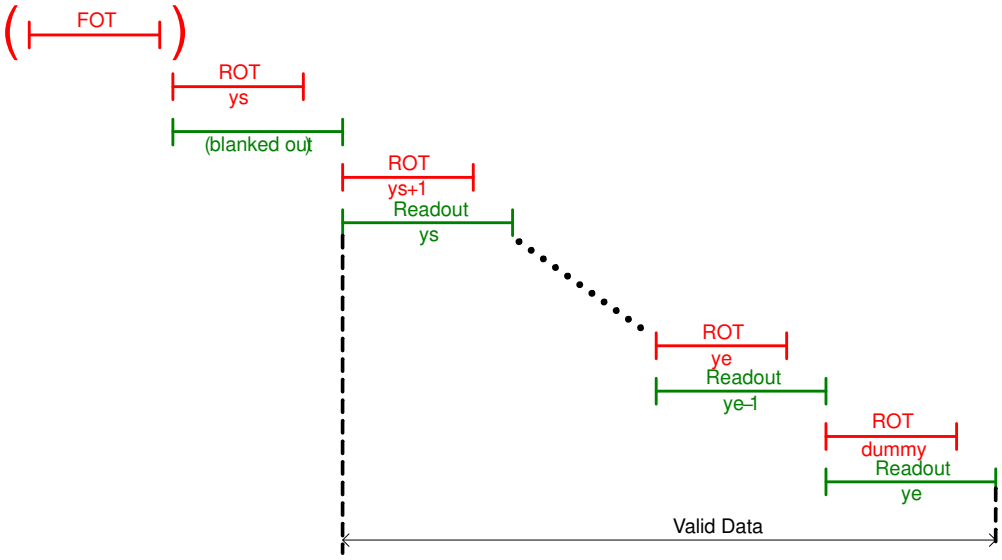


Figure 15. Integration and Readout Sequence of the Sensor operating in Pipelined Global Shutter Mode with Zero ROT Readout.

SENSOR OPERATION

Flowchart

Figure 16 shows the flow chart diagram of the sensor operation. The sensor can be in five different ‘states’. Every state is indicated with an oval circle. These states are:

- Power-Off
- Standby (1)
- Standby (2)
- Idle
- Running

The states above are ordered by power dissipation. Clearly, in ‘power-off’ state the power dissipation will be minimal; in ‘running’ state the power dissipation will be maximal.

On the other hand, the lower the power consumption, the more actions (and time) are required to put the sensor in ‘running’ state and grab images.

This flowchart provides the trade-offs between power saving and enabling time of the sensor.

Next to the ‘states’ a set of ‘user actions’, indicated by arrows, are included in the flow chart diagram. These user actions make it possible to move from one state to another.

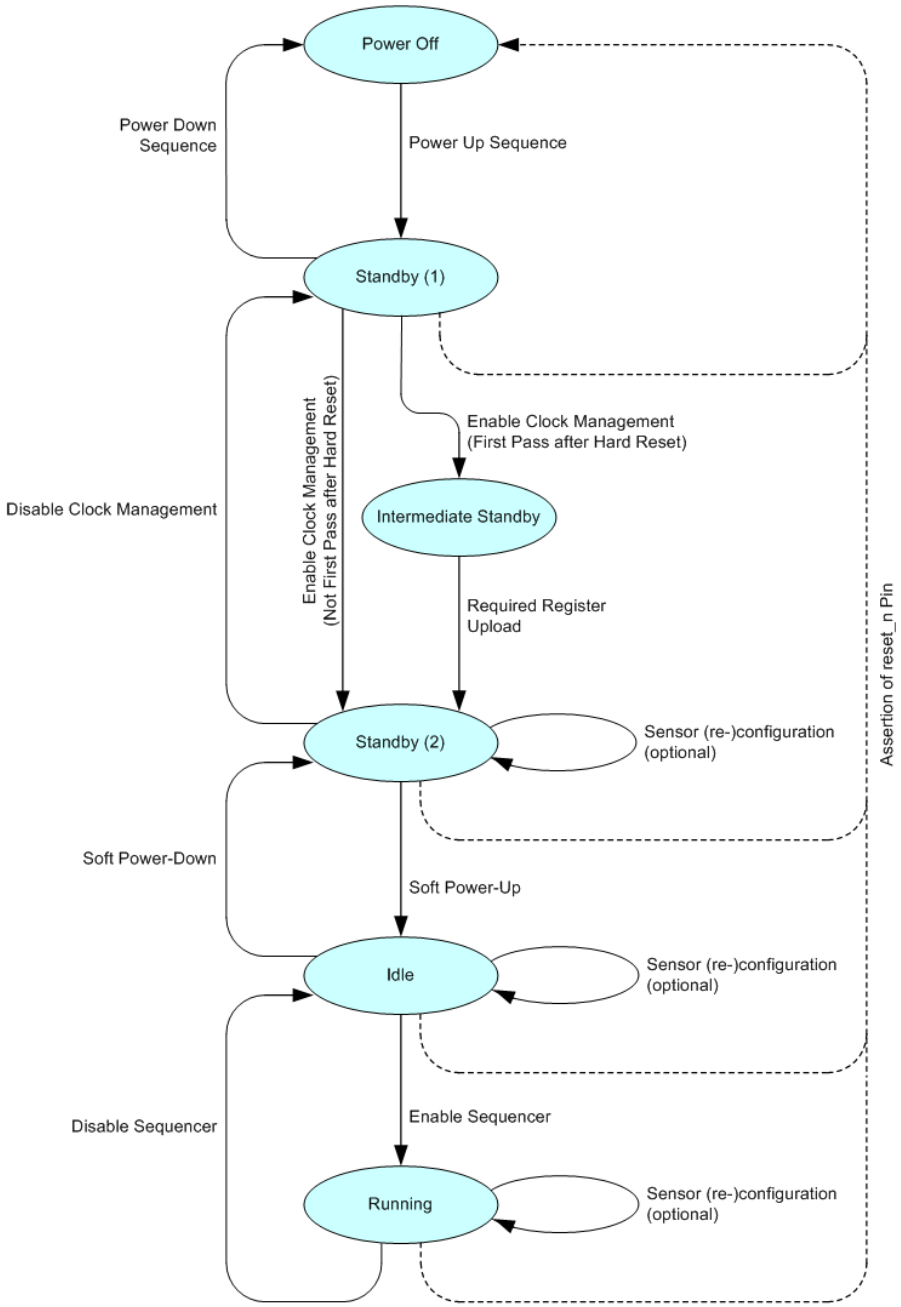


Figure 16. Sensor Operation Flowchart

Sensor States

The sensor can be in five different states:

Power-off

In this state, the sensor is inactive. All power supplies are down and the power dissipation is zero.

Standby (1)

The registers below address 40 can be configured.

Standby (2)

In this standby state all SPI registers are active, meaning that all SPI registers can be accessed for read and write operations. All other blocks are disabled.

Note: An Intermediate Standby state is traversed after a hard reset. In this state the sensor contains the default configurations. Uploads of reserved registers are required to traverse to the Standby (2) state

Idle

In the idle state, all sensor clocks are running and all blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in different global master/slave modes.

User Actions: Power Up Functional Mode Sequences

Power-up Sequence

Figure 17 shows the power-up timing of the sensor. Apply all power supplies in the order shown in the figure. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as a consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. Note that before starting the clock, the LVDS output channel multiplexing (32, 16, 8 or 4), by connecting pins F24/F25 (muxmode0/1), should be set to the correct supply as described in Table 31 and Table 28.

When the clock frequency is stable, the reset_n signal can be de−asserted. After a wait period of 10 μs, the power up sequence is finished and the first SPI upload can be initiated.

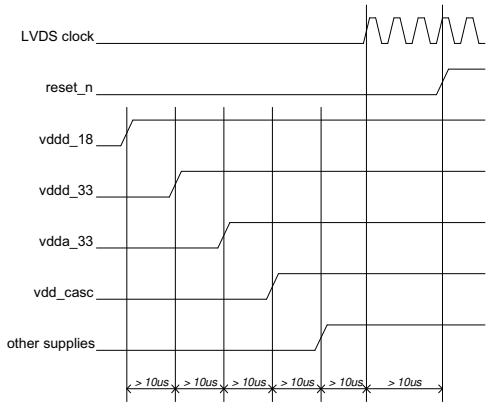


Figure 17. Power−up Procedure

NOTE: vdd_casc should come up prior to vdd_resfd, vdd_trans, vdd_calib and vdd_sel.

Enable Clock Management

The 'Enable Clock Management' action configures the clock management blocks in a pre−defined way. The required uploads are listed in Table 6.

Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD

Upload #	Address	Data	Description
1	2	0x0000	Monochrome
		0x0001	Color
2	34	0x0001	Enable Logic Blocks

Required Register Uploads

In this phase the 'reserved' register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads are listed in Table 7.

Table 7. REQUIRED REGISTER UPLOADS FOR, NON−ZERO ROT, PIPELINED GLOBAL SHUTTER MASTER MODE

Upload #	Address	Data (Non−Zero ROT)
1	41	0x0b5a
2	42	0x1001
3	43	0x018d
4	65	0x88cb
5	66	0x53c7
6	67	0x8567
7	69	0x0488
8	70	0x48ff
9	128	0x360a
10	129	0x0001
11	192	0x000c
12	193*	0x8600
13	194	0x0224
14	197	0x0103
15	204	0x01e4
16	211	0x0e59
17	215	0x0007
18	216	0x7f00
19	219	0x0015
20	220	0x192c
21	224	0x3e07
22	225	0x5ef1
23	227	0x0000
24	237	0xc0a0
25	238	0x8f88
26	384	0xe800
27	385	0xf801
28	386	0xfb1f
29	387	0xfb15
30	388	0xf911
31	389	0xf901
32	390	0xf105
33	391	0xf30f
34	392	0xf201
35	393	0xe001
36	394	0xe021
37	395	0xe061
38	396	0xe265
39	397	0xe061
40	398	0xe041
41	399	0xe001
42	400	0xe406
43	401	0xe005
44	402	0xe20a
45	403	0xe001
46	404	0xe800
47	405	0xe800
48	406	0xec0a
49	407	0xe80a
50	408	0xe800
51	409	0x0030
52	410	0x217b
53	411	0x2071
54	412	0x0071
55	413	0x107f
56	414	0x107f
57	415	0x107f
58	416	0x1075
59	417	0x0071
60	418	0x0036
61	419	0x21bb
62	420	0x20b1
63	421	0x00b1
64	422	0x10bf
65	423	0x10bf
66	424	0x10bf
67	425	0x10b5
68	426	0x00b1
69	427	0x0030
70	428	0x0030
71	429	0x207b
72	430	0x2071
73	431	0x0071
74	432	0x107f
75	433	0x107f
76	434	0x107f
77	435	0x1075
78	436	0x0071

Upload #	Address	Data (Non−Zero ROT)
79	437	0x0036
80	438	0x21bb
81	439	0x20b1
82	440	0x00b1
83	441	0x10bf
84	442	0x10bf
85	443	0x10bf
86	444	0x10b5
87	445	0x00b1
88	446	0x0030
Upload #	**Address**	**Data (Zero ROT)**
12	193*	0x0800

NOTE: Required Uploads for Zero ROT mode are the same as for Non−Zero ROT mode with the exceptions noted.

Soft Power Up

During the soft power-up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power-up uploads are listed in Table 8.

Table 8. SOFT POWER UP REGISTER UPLOADS

Upload #	Address	Data	Description
P1−SN/SE			
1	32	0x2005	Enable Analogue Clock
2	64	0x0001	Enable Biasing Block
3	40	0x0003	Enable Column Multiplexer
4	48	0x0001	Enable Analog Front-End (AFE)
5	68	0x0088	Enable LVDS Bias
6	112	0x0007	Enable LVDS Transmitters

Enable Sequencer

During the ‘Enable Sequencer’-action, the frame grabbing sequencer is enabled. The sensor will start grabbing images in the configured operation mode. Refer to Operating Modes on page 13 for an overview of the possible operation modes.

The ‘Enable Sequencer’ action consists of a set op register uploads. The required uploads are listed in Table 9.

Table 9. ENABLE SEQUENCER REGISTER UPLOADS

Upload #	Address	Data
1	192	0x000D

User Actions: Functional Mode to Power Down Sequences

Disable Sequencer

During the ‘Disable Sequencer’-action, the frame grabbing sequencer is stopped. The sensor will stop grabbing images and returns to the idle mode.

The ‘Disable Sequencer’ action consists of a set op register uploads. The required uploads are listed in Table 10.

Table 10. DISABLE SEQUENCER REGISTER UPLOADS

Upload #	Address	Data
1	192	0x000C

Soft Power Down

During the soft power-down action, the internal blocks are disabled and the sensor is put in standby state in order to reduce the current dissipation. This action exists of a set of register uploads. The soft power-down uploads are listed in Table 11.

Table 11. SOFT POWER DOWN REGISTER UPLOADS

Upload #	Address	Data	Description
P1−SN/SE			
1	112	0x0000	Disable LVDS Transmitters
2	48	0x0000	Disable Analog Front-End (AFE)
3	40	0x0000	Disable Column Multiplexer
4	64	0x0000	Disable Biasing Block
5	32	0x2004	Disable Analogue Clock

Disable Clock Management

The ‘Disable Clock Management’-action stops the internal clocking in order to further decrease the power dissipation. This action exists of a set of register uploads as listed in Table 12.

Table 12. DISABLE SEQUENCER REGISTER UPLOADS

No.	Address	Data	Description
1	34	0x0000	Disable Logic Blocks

Power-down Sequence

The timing diagram of the advised power-down sequence is given in Figure 18. Any other sequence might cause high peak currents.

NOTE: vdd_casc should be powered down after vdd_resfd, vdd_trans, vdd_calib and vdd_sel.

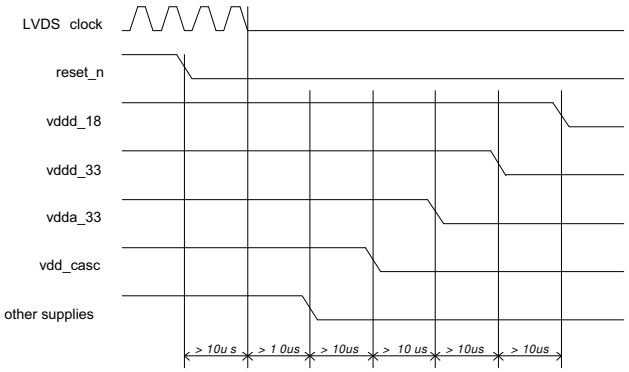


Figure 18. Power−down Sequence

Table 13. SHUTTER/OPERATION MODE CONFIGURATION REGISTERS

Address	Default Value	Description
192 [4]	0x0	Triggered mode selection 0: Normal mode 1: Triggered mode
192 [5]	0x0	Master/Slave selection 0: Master mode 1: Slave mode
192 [7]	0x0	Subsampling mode selection 0: Subsampling disabled 1: Subsampling enabled
192 [8]	0x0	Binning mode selection 0: Binning disabled 1: Binning enabled

Windowing Reconfiguration

The windowing settings can be configured during standby, idle, and running mode.

The required regions of interest (ROI) can be programmed in the roi_configuration registers (addresses 256 up to 351). Registers roi_active0 and roi_active1 are used to activate the desired ROIs.

Default window configuration (after sensor reset) is one window, full frame (window #0).

Exposure/Gain Reconfiguration

The exposure time and gain settings can be configured during standby, idle, and running mode. Refer to Signal Gain Path on page 32 for more information.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers are shown in Table 14. Table 14 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 14. STATIC READOUT PARAMETERS

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64–71	Configure according to recommendation
LVDS	112	Configure according to recommendation
Sequencer mode selection	192	• triggered_mode • slave_mode
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the recommendation

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 15 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the reconfiguration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 15. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

Group	Addresses	Description
Black level configuration	128–129 197[12:8]	Reconfiguration of these registers may have an impact on the black-level calibration algorithm. The effect is a transient number of images with incorrect black level compensation.
Sync codes	129[13] 116–126	Incorrect sync codes may be generated during the frame in which these registers are modified.
Datablock test configurations	144–150	Modification of these registers may generate incorrect test patterns during a transient frame.

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame-related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 16.

Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

Table 16. DYNAMIC READOUT PARAMETERS

Group	Addresses	Description
Subsampling/binning	192[7] 192[8]	Subsampling or binning is synchronized to a new frame start.
ROI configuration	195-196 256–351	An ROI switch is only detected when a new window is selected as the active window (reconfiguration of registers 195, 196, or both). Reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image.
Exposure reconfiguration	199-201	Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to '1' in triggered global mode (master).
Gain reconfiguration	204	Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] gain_lat_comp).

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re-enable the synchronization. The sensor's sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 19 shows a reconfiguration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

When sync_configuration = '1', configurations are synchronized to the frame boundaries (The registers exposure, fr_length, and mult_timer are not used in this mode)

Figure 20 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is deasserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

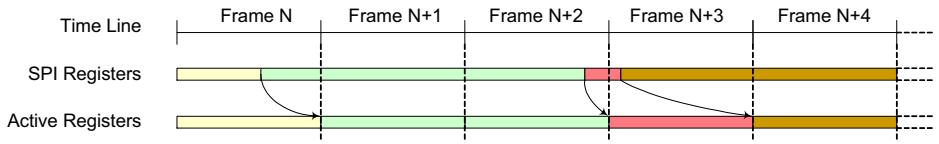


Figure 19. Frame Synchronization of Configurations (no freezing)

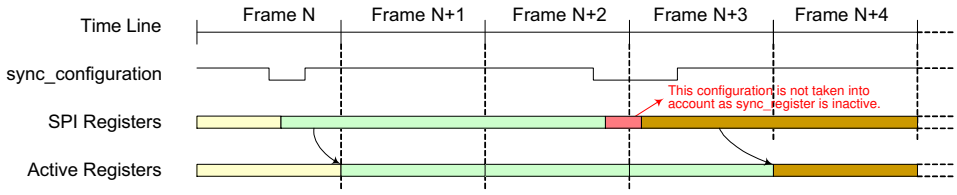


Figure 20. Reconfiguration Using Sync_configuration

NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 17 lists the several sync_configuration possibilities along with the respective registers being frozen.

Table 17. ALTERNATE SYNC CONFIGURATIONS

Group	Affected Registers	Description
sync_black_lines	black_lines	Update of black line configuration is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_exposure	mult_timer fr_length exposure	Update of exposure configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_gain	mux_gainsw afe_gain	Update of gain configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_roi	roi_active0[15:0] roi_active1[15:0] subsampling binning	Update of active ROI configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations. **Note:** The window configurations themselves are not frozen. Re-configuration of active windows is not gated by this setting.

Window Configuration

Global Shutter Mode

Up to 32 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 351. Each window can be activated or deactivated separately using registers 195 and 196. It is possible to reconfigure the inactive windows while acquiring images. Switching between predefined windows is achieved by activation of the respective windows. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is tracked. Switching between the two modes only requires an upload of one (if the total number of windows is smaller than 17) or two (if more than 16 windows are defined) registers.

Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to ‘0’. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to ‘0’ when setting the black level target to ‘0’.

The black level is calibrated for the 64 columns contained in one kernel. This implies 64 black level offsets are generated and applied to the corresponding columns. Configurable parameters for the black-level algorithm are listed in Table 18.

Table 18. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

Group	Addresses	Description
Black Line Generation		
197[7:0]	black_lines	This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 255. **Note:** When the automatic black-level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black-level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations: Each black line contains 80 kernels.
197[12:8]	gate_first_line	A number of black lines are blanked out when a value different from 0 is configured. These blanked out lines are not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm.
Black Value Filtering		
129[0]	auto_blackcal_enable	Internal black-level calibration functionality is enabled when set to ‘1’. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to ‘0’, the automatic black-level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1]. **Note:** Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations.
129[9:1]	blackcal_offset	Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to ‘0’. The sign of the offset is determined by register 129[10] (blackcal_offset_dec). **Note:** All channels use the same offset compensation when automatic black calibration is disabled. The calculated black calibration factors are frozen when this register is set to 0x1FF (all−‘1’) in auto calibration mode. Any value different from 0x1FF re−enables the black calibration algorithm. This freezing option can be used to prevent eventual frame to frame jitter on the black level as the correction factors are recalculated every frame. It is recommended to enable the black calibration regularly to compensate for temperature changes.
129[10]	blackcal_offset_dec	Sign of blackcal_offset. If set to ‘0’, the black calibration offset is added to each pixel. If set to ‘1’, the black calibration offset is subtracted from each pixel. This register is not used when auto_blackcal_enable is set to ‘1’.
128[10:8]	black_samples	The black samples are low-pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate. The effective number of samples taken into account for filtering is $2^{black\_samples}$. **Note:** An error is reported by the device if more samples than available are requested (refer to registers 136 to 139).
Black Level Filtering Monitoring		
136 137 138 139	blackcal_error0 blackcal_error1 blackcal_error2 blackcal_error3	An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation: • Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197). • Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128). • Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift.

NOTE: The maximum number of samples taken into account for black level statistics is half the number of kernels.

Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor's system clock. When the master wants to write or read a sensor's register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 21 shows the communication protocol for read and write accesses of the SPI registers. The PYTHON XK sensor uses 9-bit addresses and 16-bit data words

Data driven by the system is colored blue in Figure 21, while data driven by the sensor is colored yellow. The data in grey indicates high-Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

3. Select the sensor for read or write by pulling down the ss_n line.
4. One SPI clock cycle (100 ns) after selecting the sensor, the 9-bit address is transferred, most significant bit first. The sck clock is passed through to the sensor as indicated in Figure 21. The sensor samples this data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock)
5. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
6. Data transmission:
   - For write commands, the master continues sending the 16-bit data, most significant bit first.
   - For read commands, the sensor returns the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
7. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Note the maximum frequency for the SPI interface needs to scale with the LVDS input clock frequency as described in Table 5.

Consecutive SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

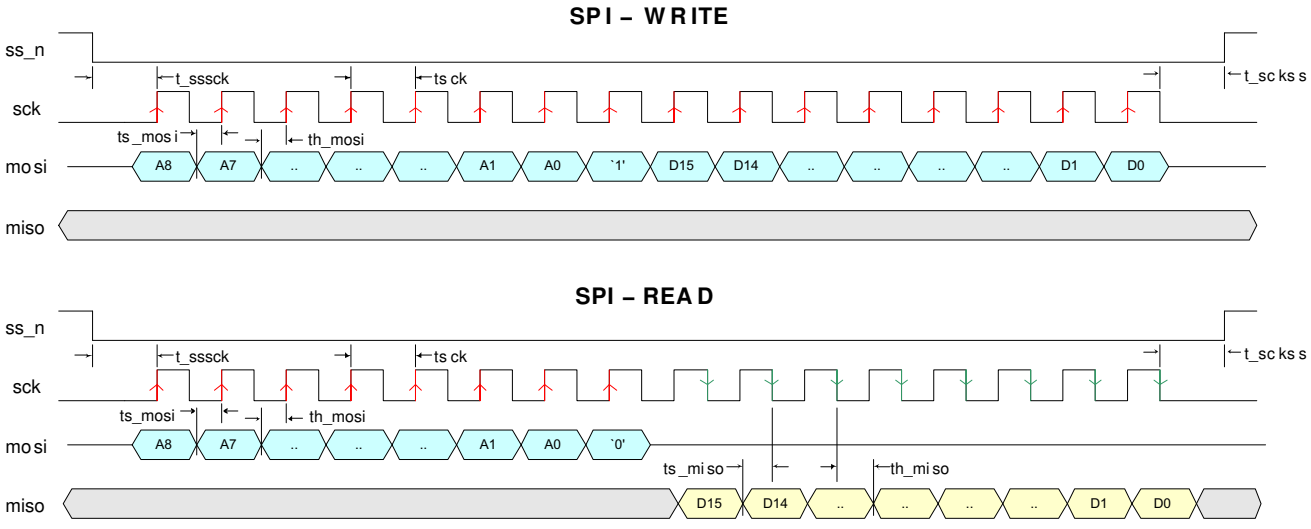


Figure 21. SPI Read and Write Timing Diagram