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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

NOIP1SN1300A

PYTHON 1.3/0.5/0.3 MegaPixels Global Shutter CMOS Image Sensors

ON Semiconductor®

www.onsemi.com

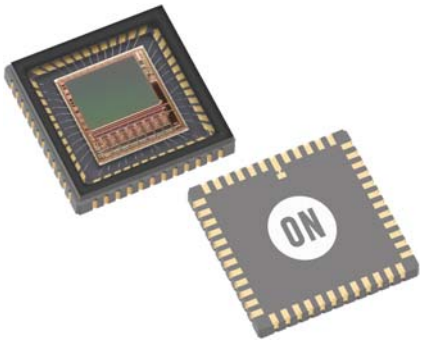


Figure 1. PYTHON 1300

FEATURES

- Size Options:
  - PYTHON 300: 640 x 480 Active Pixels, 1/4” Optical Format
  - PYTHON 500: 800 x 600 Active Pixels, 1/3.6” Optical Format
  - PYTHON 1300: 1280 x 1024 Active Pixels, 1/2” Optical Format
- Data Output Options:
  - P1−SN/SE/FN: 4 LVDS Data Channels
  - P2−SN/SE: 10 bit Parallel
  - P3−SN/SE/FN: 2 LVDS Data Channels
- 4.8 μm x 4.8 μm Low Noise Global Shutter Pixels with In-pixel CDS
- Monochrome (SN), Color (SE) and NIR (FN)
- Zero Row Overhead Time (ZROT) Mode Enabling Higher Frame Rate
- Frame Rate at Full Resolution, 4 LVDS Data Channels (P1−SN/SE/FN only)
  - 210/165 frames per second @ SXGA (ZROT/NROT)
  - 545/385 frames per second @ SVGA (ZROT/NROT)
  - 815/545 frames per second @ VGA (ZROT/NROT)
- Frames Rate at Full Resolution (CMOS)
  - 50/43 Frames per Second @ SXGA (ZROT/NROT)
- On−chip 10−bit Analog−to−Digital Converter (ADC)
- Four/Two/One LVDS High Speed Serial Outputs or Parallel CMOS Output
- Random Programmable Region of Interest (ROI) Readout
- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- High Dynamic Range (HDR) Modes Possible
- Dual Power Supply (3.3 V and 1.8 V)
- −40°C to +85°C Operational Temperature Range
- 48−pin LCC
- Power Dissipation:
  - 620 mW (P1, 4 LVDS, ZROT)
  - 420 mW (P1, P3, 2 LVDS, NROT)
  - 270 mW (P1, P3, 1 LVDS, NROT)
  - 420 mW (P2, ZROT)
- These Devices are Pb−Free and are RoHS Compliant

APPLICATIONS

- Machine Vision
- Motion Monitoring
- Security
- Barcode Scanning (2D)

DESCRIPTION

The PYTHON 300, PYTHON 500, and PYTHON 1300 image sensors utilize high sensitivity 4.8 μm x 4.8 μm pixels that support low noise “pipelined” and “triggered” global shutter readout modes. The sensors support correlated double sampling (CDS) readout, reducing noise and increasing dynamic range.

The image sensors have on−chip programmable gain amplifiers and 10−bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on−chip automatic exposure control loop (AEC) controls these parameters dynamically. The image’s black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to eight regions can be programmed, achieving even higher frame rates.

The image data interface of the P1−SN/SE/FN devices consists of four LVDS lanes, enabling frame rates up to 210 frames per second in Zero ROT mode for the PYTHON 1300. Each channel runs at 720 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receiving end. The P2−SN/SE devices provide a parallel CMOS output interface at reduced frame rate. The P3−SN/SE/FN devices are the same as the P1−SN/SE/FN but with only two of the four LVDS data channels enabled, facilitating frame rates of 90 frames per second in Normal ROT for the PYTHON 1300.

The devices are provided in a 48−pin LCC package and are available in monochrome, Bayer color, and extended near−infrared (NIR) configurations.

ORDERING INFORMATION

Part Number	Description	Package
PYTHON 1300		
NOIP1SN1300A−QDI	1.3 Megapixel, Monochrome, LVDS Output	48−pin LCC
NOIP1SE1300A−QDI	1.3 Megapixel, Bayer Color, LVDS Output	
NOIP1FN1300A−QDI	1.3 Megapixel, Monochrome with enhanced NIR, LVDS Output	
NOIP2SN1300A−QDI	1.3 Megapixel, Monochrome, CMOS (parallel) Output	
NOIP2SE1300A−QDI	1.3 Megapixel, Bayer Color, CMOS (parallel) Output	
NOIP1SN1300A−QTI	1.3 Megapixel, Monochrome, LVDS Output, Protective Foil	
NOIP1SE1300A−QTI	1.3 Megapixel, Bayer Color, LVDS Output, Protective Foil	
NOIP1FN1300A−QTI	1.3 Megapixel, Monochrome with enhanced NIR, LVDS Output, Protective Foil	
NOIP3SN1300A−QDI	1.3 Megapixel, 2 LVDS Outputs, Monochrome	
NOIP3FN1300A−QDI	1.3 Megapixel, 2 LVDS Outputs, NIR enhanced Monochrome	
NOIP3SE1300A−QDI	1.3 Megapixel, 2 LVDS Outputs, Color	
NOIP3SN1300A−QTI	1.3 Megapixel, 2 LVDS Outputs, Monochrome, Protective Foil	
NOIP3FN1300A−QTI	1.3 Megapixel, 2 LVDS Outputs, NIR enhanced Monochrome, Protective Foil	
NOIP3SE1300A−QTI	1.3 Megapixel, 2 LVDS Outputs, Color, Protective Foil	
PYTHON 500		
NOIP1SN0500A−QDI	0.5 Megapixel, Monochrome, LVDS Output	48−pin LCC
NOIP1SE0500A−QDI	0.5 Megapixel, Bayer Color, LVDS Output	
NOIP1FN0500A−QDI	0.5 Megapixel, Monochrome with enhanced NIR, LVDS Output	
NOIP1SN0500A−QTI	0.5 Megapixel, Monochrome, LVDS Output, Protective Foil	
NOIP1SE0500A−QTI	0.5 Megapixel, Bayer Color, LVDS Output, Protective Foil	
NOIP1FN0500A−QTI	0.5 Megapixel, Monochrome with enhanced NIR, LVDS Output, Protective Foil	
PYTHON 300		
NOIP1SN0300A−QDI	0.3 Megapixel, Monochrome, LVDS Output	48−pin LCC
NOIP1SE0300A−QDI	0.3 Megapixel, Bayer Color, LVDS Output	
NOIP1FN0300A−QDI	0.3 Megapixel, Monochrome with enhanced NIR, LVDS Output	
NOIP1SN0300A−QTI	0.3 Megapixel, Monochrome, LVDS Output, Protective Foil	
NOIP1SE0300A−QTI	0.3 Megapixel, Bayer Color, LVDS Output, Protective Foil	
NOIP1FN0300A−QTI	0.3 Megapixel, Monochrome with enhanced NIR, LVDS Output, Protective Foil	

The P1−SN/SE/FN base part references the mono, color and NIR enhanced versions of the 4 LVDS interface; the P2−SN/SE base part references the mono and color versions of the CMOS interface; the P3−SN/SE/FN base part references the mono, color and NIR enhanced version of the 2 LVDS interface. More details on the part number coding can be found at http://www.onsemi.com/pub_link/Collateral/TND310−D.PDF

Production Package Mark

Line 1: NOIP**yxxRRRR**A where y is either “1” for 4 LVDS Outputs, “2” for CMOS Parallel Output, “3” for 2 LVDS Outputs, where xx denotes mono micro lens (SN) or color micro lens (SE) or NIR micro lens (FN)
RRRR is the resolution (1300), (0500) or (0300)
Line 2: **−QDI** (without protective foil), **−QTI** (with protective foil)
Line 3: **AWLYYWW** where AWL is PRODUCTION lot traceability, YYWW is the 4−digit date code

SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	Specification
Pixel type	In−pixel CDS. Global shutter pixel architecture
Shutter type	Pipelined and triggered global shutter
Frame rate Zero ROT/ Normal ROT mode	P1−SN/SE/FN: PYTHON 300: 815/545 fps PYTHON 500: 545/385 fps PYTHON 1300: 210/165 fps P2−SN/SE: 50/43 fps P3−SN/SE/FN: NA/90 fps
Master clock	P1, P3−SN/SE/FN: 72 MHz when PLL is used, 360 MHz (10−bit) / 288 MHz (8−bit) when PLL is not used P2−SN/SE: 72 MHz
Windowing	8 Randomly programmable windows. Normal, sub−sampled and binned readout modes
ADC resolution	10−bit, 8−bit (Note 1)
LVDS outputs	P1−SN/SE/FN: 4/2/1 data + sync + clock P3−SN/SE/FN: 2/1 data + sync + clock
CMOS outputs	P2−SN/SE: 10−bit parallel output, frame_valid, line_valid, clock
Data rate	P1−SN/SE/FN: 4 x 720 Mbps (10−bit) / 4 x 576 Mbps (8−bit) P2−SN/SE: 72 Mhz P3−SN/SE/FN: 2 x 720 Mbps (10−bit)
Power dissipation (10−bit mode)	P1−SN/SE/FN: 620 mW (4 data channels) P1, P3−SN/SE/FN: 420 mW (2 data ch.) P1, P3−SN/SE/FN: 270 mW (1 data ch.) P2−SN/SE: 420 mW
Package type	48−pin LCC

Table 2. ELECTRO−OPTICAL SPECIFICATIONS

Parameter	Specification
Active pixels	PYTHON 300: 640 (H) x 480 (V) PYTHON 500: 800 (H) x 600 (V) PYTHON 1300: 1280 (H) x 1024 (V)
Pixel size	4.8 μm x 4.8 μm
Conversion gain	0.096 LSB10/e^- 140 μV/e^-
Dark temporal noise	< 9 e^- (Normal ROT, 1x gain) < 7 e^- (Normal ROT, 2x gain)
Responsivity at 550 nm	7.7 V/lux.s
Parasitic Light Sensitivity (PLS)	<1/8000
Full Well Charge	10000 e^-
Quantum Efficiency at 550 nm	56%
Pixel FPN	< 1.0 LSB10
PRNU	< 2% or 10 LSB10 on half scale response of 525LSB10
MTF	68% @ 535 nm − X−dir & Y−dir
PSNL at 20°C	120 LSB10/s, 1200 e^-/s
Dark signal at 20°C	5 e^-/s, 0.5 LSB10/s
Dynamic Range	> 60 dB in global shutter mode
Signal to Noise Ratio (SNR max)	40 dB

Table 3. RECOMMENDED OPERATING RATINGS (Note 2)

Symbol	Description	Min	Max	Unit
T_J	Operating temperature range	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ABSOLUTE MAXIMUM RATINGS (Notes 3 and 4)

Symbol	Parameter	Min	Max	Unit
ABS (1.8 V supply group)	ABS rating for 1.8 V supply group	−0.5	2.2	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	−0.5	4.3	V
T_S	ABS storage temperature range	−40	+150	°C
	ABS storage humidity range at 85°C		85	%RH
Electrostatic discharge (ESD)	Human Body Model (HBM): JS−001−2010	2000		V
	Charged Device Model (CDM): JESD22−C101	500		
LU	Latch−up: JESD−78	100		mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The ADC is 11−bit, down−scaled to 10−bit. The PYTHON uses a larger word−length internally to provide 10−bit on the output.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
4. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Unit
Power Supply Parameters – P1 – SN/SE/FN LVDS (ZROT) (NOTE: All ground pins (gnd_18, gnd_33, gnd_colpc) should be connected to an external 0 V ground reference.)					
vdd_33	Supply voltage, 3.3 V	**3.2**	3.3	**3.4**	V
Idd_33	Current consumption 3.3 V supply		140		mA
vdd_18	Supply voltage, 1.8 V	**1.7**	1.8	**1.9**	V
Idd_18	Current consumption 1.8 V supply		80		mA
vdd_pix	Supply voltage, pixel	**3.25**	3.3	**3.35**	V
Idd_pix	Current consumption pixel supply		5		mA
Ptot	Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V P1−SN/SE/FN, 4 LVDS, ZROT		620		mW
Pstby_lp	Power consumption in low power standby mode			50	mW
Popt	Power consumption at lower pixel rates		Configurable		
Power Supply Parameters – P3 – SN/SE/FN LVDS (NROT) (NOTE: All ground pins (gnd_18, gnd_33, gnd_colpc) should be connected to an external 0 V ground reference.)					
vdd_33	Supply voltage, 3.3 V	**3.2**	3.3	**3.4**	V
Idd_33	Current consumption 3.3 V supply (2 / 1 LVDS)		95 / 55		mA
vdd_18	Supply voltage, 1.8 V	**1.7**	1.8	**1.9**	V
Idd_18	Current consumption 1.8 V supply (2 / 1 LVDS)		55 / 45		mA
vdd_pix	Supply voltage, pixel	**3.25**	3.3	**3.35**	V
Idd_pix	Current consumption pixel supply (2 / 1 LVDS)		2 / 1		mA
Ptot	Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V P3−SN/SE/FN, 2 LVDS, NROT P3−SN/SE/FN, 1 LVDS, NROT		 420 270		mW
Pstby_lp	Power consumption in low power standby mode			50	mW
Popt	Power consumption at lower pixel rates		Configurable		
Power Supply Parameters – P2−SN/SE CMOS					
vdd_33	Supply voltage, 3.3 V	**3.2**	3.3	**3.4**	V
Idd_33	Current consumption 3.3 V supply		120		mA
vdd_18	Supply voltage, 1.8 V	**1.7**	1.8	**1.9**	V
Idd_18	Current consumption 1.8 V supply		10		mA
vdd_pix	Supply voltage, pixel	**3.25**	3.3	**3.35**	V
Idd_pix	Current consumption pixel supply		1		mA
Ptot	Total power consumption		420		mW
Pstby_lp	Power consumption in low power standby mode			50	mW
Popt	Power consumption at lower pixel rates		Configurable		
I/O – P1−SN/SE/FN, P3−SN/SE/FN LVDS (EIA/TIA−644): Conforming to standard/additional specifications and deviations listed					
fserdata	Data rate on data channels DDR signaling – 4 data channels, 1 synchronization channel			720	Mbps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Refer to ACSPYTHON1300 available at the Image Sensor Portal for detailed acceptance criteria specifications.
9. For power supply management recommendations, please refer to Application Note AND9158.

Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Unit
fserclock	Clock rate of output clock Clock output for mesochronous signaling			360	MHz
Vicm	LVDS input common mode level	0.3	1.25	1.8	V
Tccsk	Channel to channel skew (Training pattern allows per channel skew correction)			50	ps
I/O − P2−SN/SE CMOS (JEDEC− JESD8C−01): Conforming to standard/additional specifications and deviations listed					
fpardata	Data rate on parallel channels (10−bit)			72	Mbps
Cout	Output load (only capacitive load)			10	pF
tr	Rise time (10% to 90% of input signal)	2.5	4.5	6.5	ns
tf	Fall time (10% to 90% of input signal)	2	3.5	5	ns
Electrical Interface − P1 − SN/SE/FN LVDS					
fin	Input clock rate when PLL used			72	MHz
fin	Input clock when LVDS input used			360	MHz
tidc	Input clock duty cycle when PLL used	45	50	55	%
tj	Input clock jitter			20	ps
ratspi (= fin/fspi)	10−bit (4 LVDS channels), PLL used	6			
	10−bit (2 LVDS channels), PLL used	12			
	10−bit (1 LVDS channel), PLL used	24			
	10−bit (4 LVDS channels), LVDS input used	30			
	10−bit (2 LVDS channels), LVDS input used	60			
	10−bit (1 LVDS channel), LVDS input used	120			
	8−bit (4 LVDS channels), PLL used	6			
	8−bit (2 LVDS channels), PLL used	12			
	8−bit (1 LVDS channel), PLL used	24			
	8−bit (4 LVDS channels), LVDS input used	24			
	8−bit (2 LVDS channels), LVDS input used	48			
	8−bit (1 LVDS channel), LVDS input used	96			
Electrical Interface − P2−SN/SE CMOS					
fin	Input clock rate			72	MHz
tidc	Input clock duty cycle	45	50	55	%
tj	Input clock jitter			20	ps
ratspi (= fin/fspi)	10−bit, PLL bypassed	24			
Electrical Interface − P3 − SN/SE/FN LVDS					
fin	Input clock rate when PLL used			72	MHz
fin	Input clock when LVDS input used			360	MHz
tidc	Input clock duty cycle when PLL used	45	50	55	%
tj	Input clock jitter			20	ps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Refer to ACSPYTHON1300 available at the Image Sensor Portal for detailed acceptance criteria specifications.
9. For power supply management recommendations, please refer to Application Note AND9158.

Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Unit
ratspi (= fin/fspi)	10−bit (2 LVDS channels), PLL used	12			
	10−bit (1 LVDS channel), PLL used	24			
	10−bit (2 LVDS channels), LVDS input used	60			
	10−bit (1 LVDS channel), LVDS input used	120			

Frame Specifications − P1−SN/SE/FN−LVDS (ZROT)

		Maximum			
		Normal ROT	Zero ROT	Max	Units
fps	Frame rate at full resolution	165	210		fps
fps_roi1	Xres x Yres = 1024 x 1024	195	260		fps
fps_roi2	Xres x Yres = 800 x 600	385	545		fps
fps_roi3	Xres x Yres = 640 x 480	545	815		fps
fps_roi4	Xres x Yres = 512 x 512	580	925		fps
fps_roi5	Xres x Yres = 256 x 256	1400	2235		fps
fpix	Pixel rate (4 channels at 72 Mpix/s)			288	Mpix/s

Frame Specifications − P2−SN/SE CMOS

		Maximum			
		Normal ROT	Zero ROT		Units
fps	Frame rate at full resolution	43	50		fps

Frame Specifications − P3−SN/SE/FN LVDS (NROT)

		Maximum			
		2 LVDS	1 LVDS	Max	Units
fps	Frame rate at full resolution	90	45		fps
fps_roi1	Xres x Yres = 1024 x 1024	110	55		fps
fps_roi2	Xres x Yres = 800 x 600	230	120		fps
fps_roi3	Xres x Yres = 640 x 480	340	185		fps
fps_roi4	Xres x Yres = 512 x 512	375	205		fps
fps_roi5	Xres x Yres = 256 x 256	1110	660		fps
fpix	Pixel rate (4 channels at 72 Mpix/s)			144	Mpix/s

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Refer to ACSPYTHON1300 available at the Image Sensor Portal for detailed acceptance criteria specifications.
9. For power supply management recommendations, please refer to Application Note AND9158.

Color Filter Array

The PYTHON color sensors are processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left.

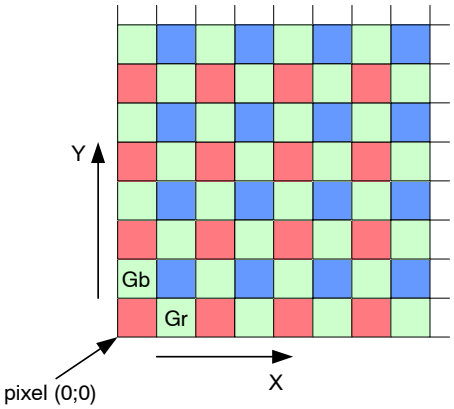


Figure 2. Color Filter Array for the Pixel Array

Quantum Efficiency

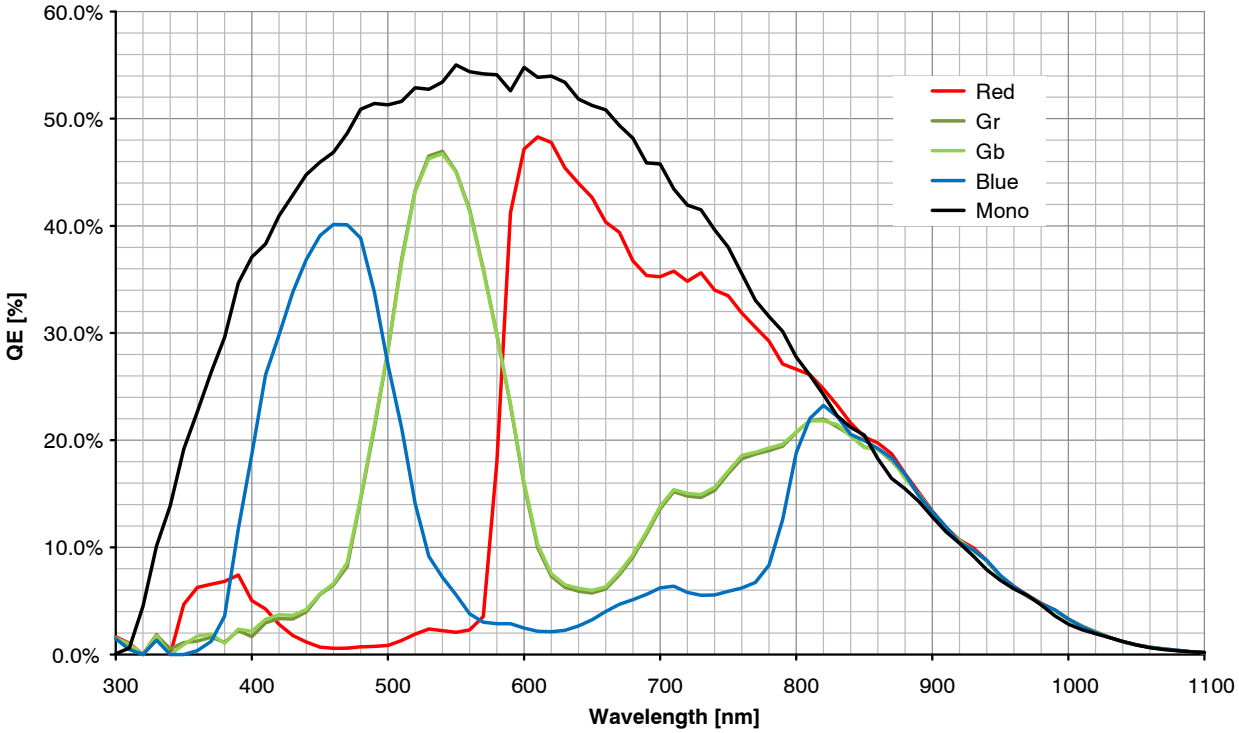


Figure 3. Quantum Efficiency Curve for Mono and Color

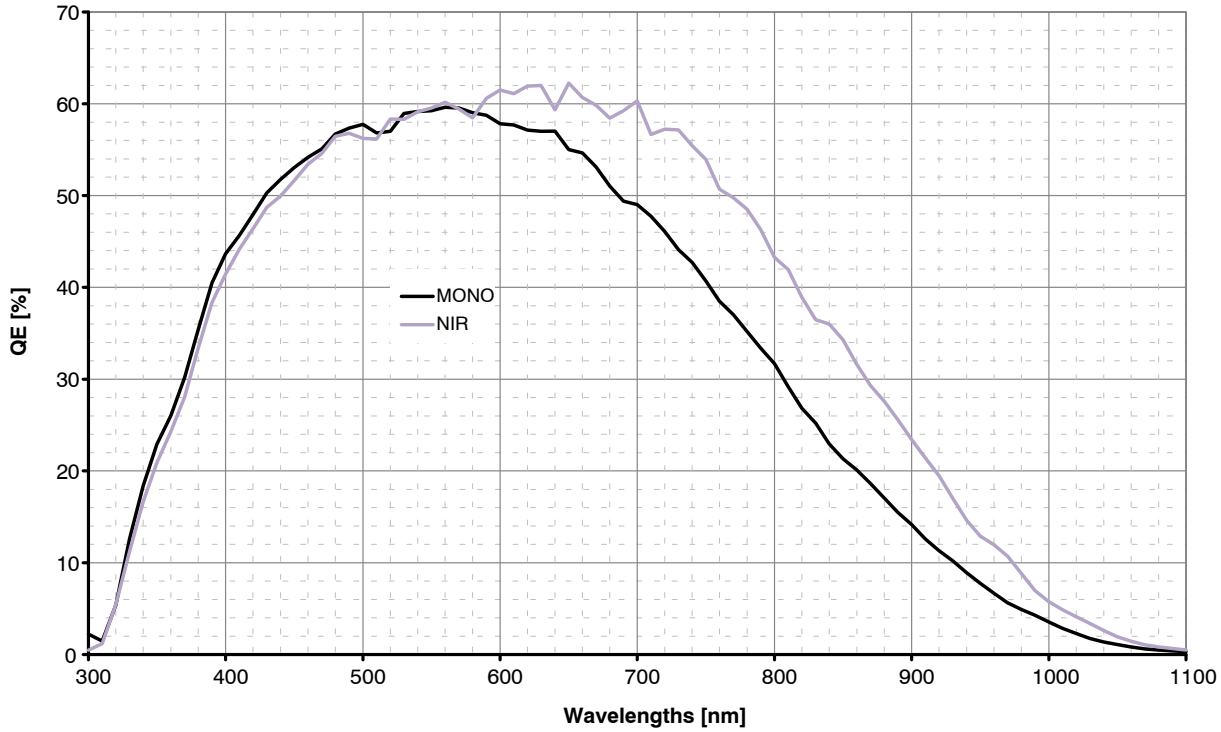


Figure 4. Quantum Efficiency Curve for Standard and NIR Mono

Ray Angle and Microlens Array Information

An array of microlenses is placed over the CMOS pixel array in order to improve the absolute responsivity of the photodiodes. The combined microlens array and pixel array has two important properties:

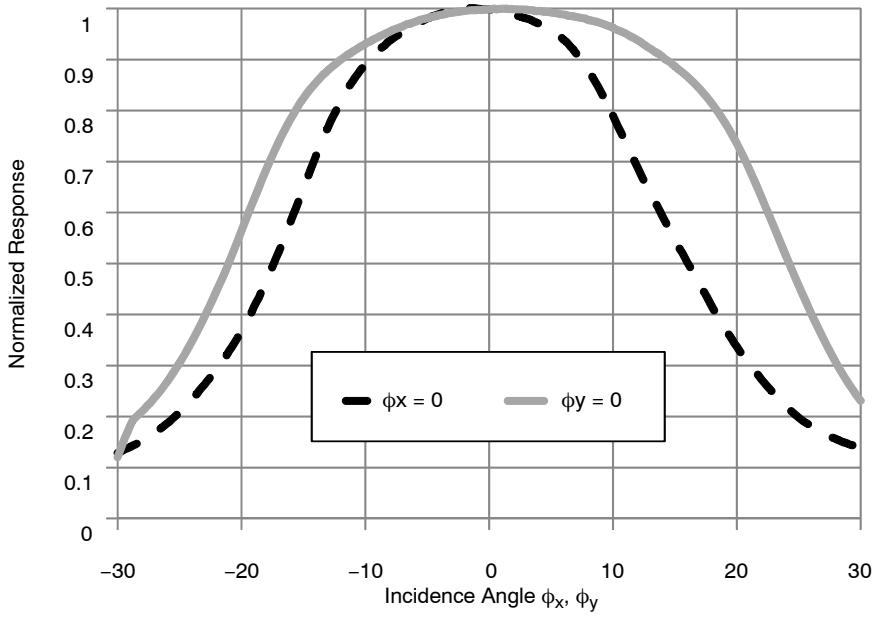
1. Angular dependency of photoresponse of a pixel

The photoresponse of a pixel with microlens in the center of the array to a fixed optical power with varied incidence angle is as plotted in Figure 5, where definitions of angles ϕx and ϕy are as described by Figure 6.

2. Microlens shift across array and CRA

The microlens array is fabricated with a slightly smaller pitch than the array of photodiodes. This difference in pitch creates a varying degree of shift of a pixel's microlens with regards to its photodiode. A shift in microlens position versus photodiode position will cause a tilted angle of peak photoresponse, here denoted Chief Ray Angle (CRA). Microlenses and photodiodes are aligned with 0 shift and CRA in the center of the array, while the shift and CRA increases radially towards its edges, as illustrated by Figure 7.

The purpose of the shifted microlenses is to improve the uniformity of photoresponse when camera lenses with a finite exit pupil distance are used. The CRA varies nearly linearly with distance from the center as illustrated in Figure 8, with a corner CRA of approximately 2.7 degrees. This edge CRA is matching a lens with exit pupil distance of ~ 80 mm.



Note that the photoresponse peaks near normal incidence for center pixels.

Figure 5. Central Pixel Photoresponse to a Fixed Optical Power with Incidence Angle varied along ϕ_x and ϕ_y

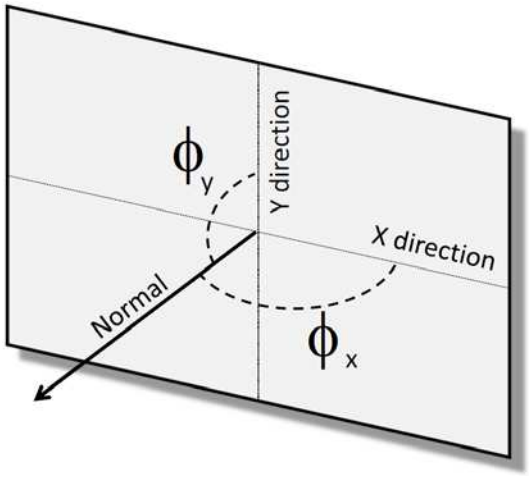
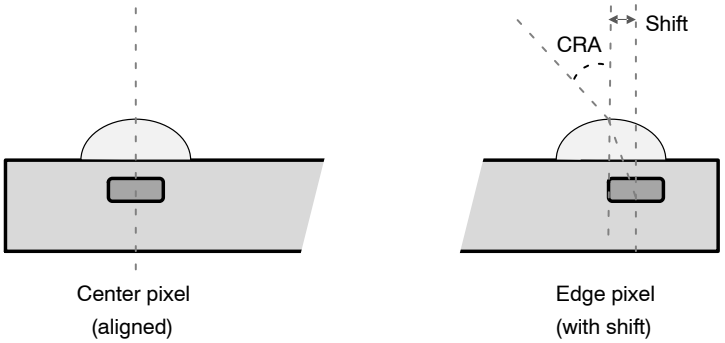


Figure 6. Definition of Angles used in Figure 5.



The center axes of the microlens and the photodiode coincide for the center pixels. For the edge pixels, there is a shift between the axes of the microlens and the photodiode causing a Peak Response Incidence Angle (CRA) that deviates from the normal of the pixel array.

Figure 7. Principles of Microlens Shift

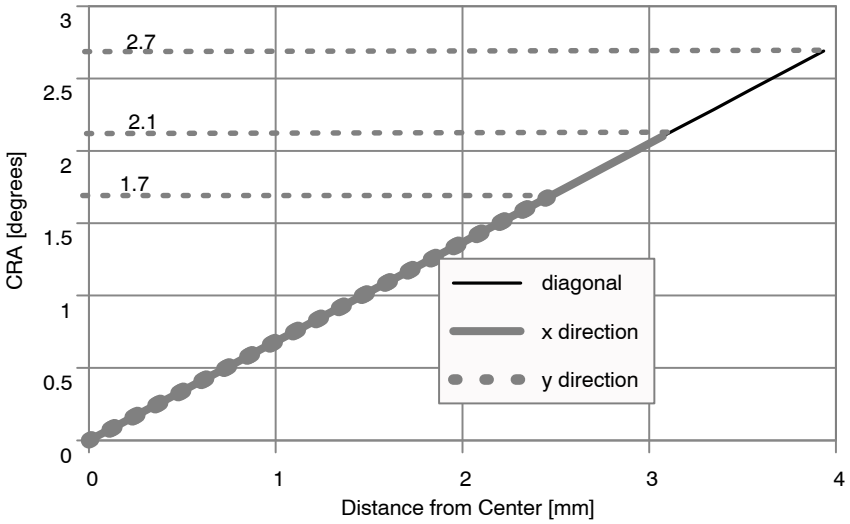
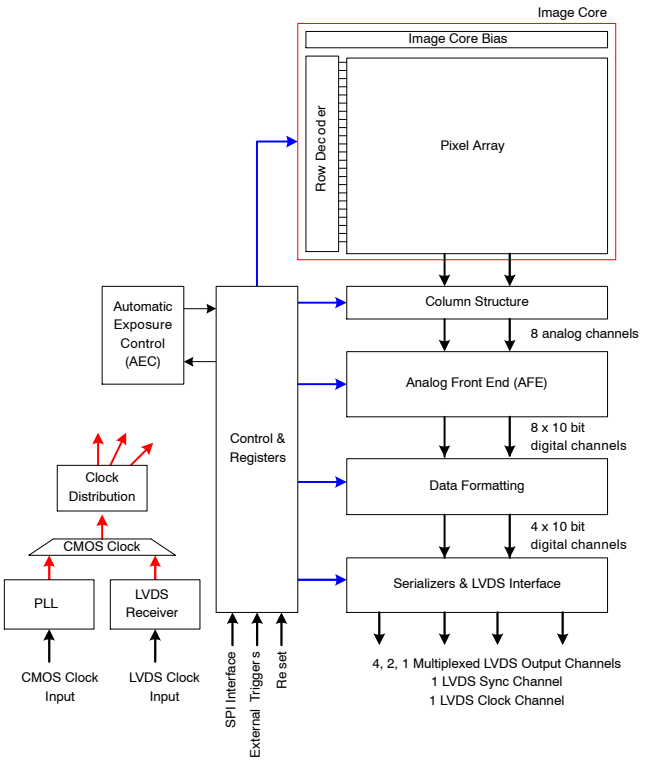


Figure 8. Variation of Peak Responsivity Angle (CRA) as a Function of Distance from the Center of the Array

OVERVIEW

Figures 9 and 10 give an overview of the major functional blocks of the P1−SN/SE/FN, P3−SN/SE/FN and P2−SN/SE sensor respectively.



Note: P3 part only has 2,1 Multiplexed LVDS Output Channels

Figure 9. Block Diagram − P1−SN/SE/FN, P3−SN/SE/FN

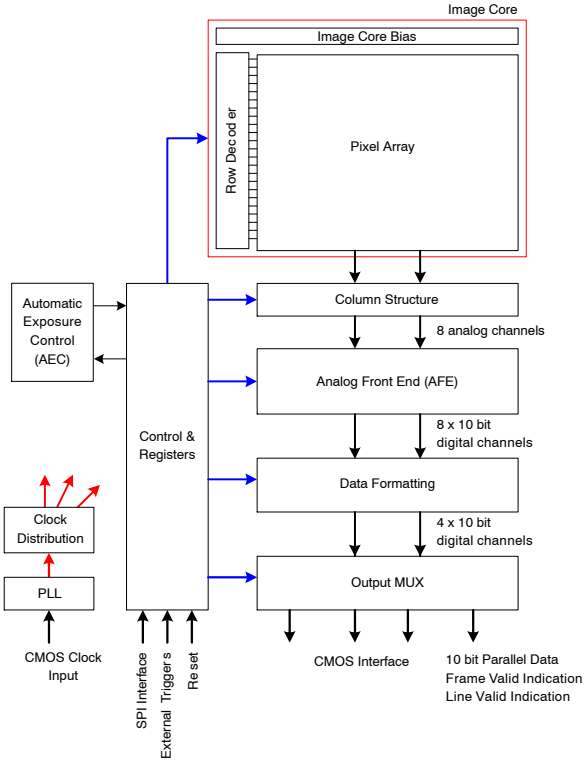


Figure 10. Block Diagram − P2−SN/SE

Image Core

The image core consists of:

- Pixel Array
- Address Decoders and Row Drivers
- Pixel Biasing

The PYTHON 1300 pixel array contains 1280 (H) x 1024 (V) readable pixels with a pixel pitch of 4.8 μm. The PYTHON 300 and PYTHON 500 image arrays contain 672 (H) x 512 (V) and 832 (H) x 632 (V) readable pixels respectively, inclusive of 16 pixel rows and 16 pixel columns at every side to allow for reprocessing or color reconstruction. The sensors use in−pixel CDS architecture, which makes it possible to achieve a low noise read out of the pixel array in global shutter mode with CDS.

The function of the row drivers is to access the image array line by line, or all lines together, to reset or read the pixel data. The row drivers are controlled by the on−chip sequencer and can access the pixel array.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

Phase Locked Loop

The PLL accepts a (low speed) clock and generates the required high speed clock. Optionally this PLL can be bypassed. Typical input clock frequency is 72 MHz.

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 360 MHz in 10−bit mode and 288 MHz in 8−bit mode. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

All pixels of one image row are stored in the column sample−and−hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 8 parallel differential outputs operating at a frequency of 36 MHz. At this stage, the reset signal and integrated signal values are transferred into an FPN−corrected differential signal. A programmable gain of 1x, 2x, or 4x can be applied to the signal. The column

multiplexer also supports read−1−skip−1 and read−2−skip−2 mode. Enabling this mode increases the frame rate, with a decrease in resolution.

Bias Generator

The bias generator generates all required reference voltages and bias currents used on chip. An external resistor of 47 kΩ, connected between pin IBIAS_MASTER and gnd_33, is required for the bias generator to operate properly.

Analog Front End

The AFE contains 8 channels, each containing a PGA and a 10−bit ADC.

For each of the 8 channels, a pipelined 10−bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one data stream. A cyclic redundancy check (CRC) code is calculated on the passing data.

A frame synchronization data block transmits synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface (P1−SN/SE/FN, P3−SN/SE/FN only)

The serializer and LVDS interface block receives the formatted (10−bit or 8−bit) data from the data formatting block. This data is serialized and transmitted by the LVDS 288 MHz output driver.

In 10−bit mode, the maximum output data rate is 720 Mbps per channel. In 8−bit mode, the maximum output data rate is 576 Mbps per channel.

In addition to the LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system−level image reconstruction.

Output MUX (P2−SN/SE)

The output MUX multiplexes the four data channels to one channel and transmits the data words using a 10−bit parallel CMOS interface.

Frame synchronization information is communicated by means of frame and line valid strobes.

Channel Multiplexer

The P1−SN/SE/FN LVDS channel multiplexer provides a 4:2 and 4:1 feature, in addition to utilizing all 4 output channels.

The P3− SN/SE/FN LVDS channel multiplexer provides a 2:1 feature, in addition to utilizing both the output channels.

Sequencer

The sequencer:

- Controls the image core. Starts and stops integration and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

Automatic Exposure Control

The AEC block implements a control system to modulate the exposure of an image. Both integration time and gains are controlled by this block to target a predefined illumination level.

OPERATING MODES

Global Shutter Mode

The PYTHON 300, PYTHON 500, and PYTHON 1300 operate in pipelined or triggered global shuttering modes. In this mode, light integration, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 11 shows the integration and readout sequence for the global shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially. The integration starts at a certain period, relative to the frame start.

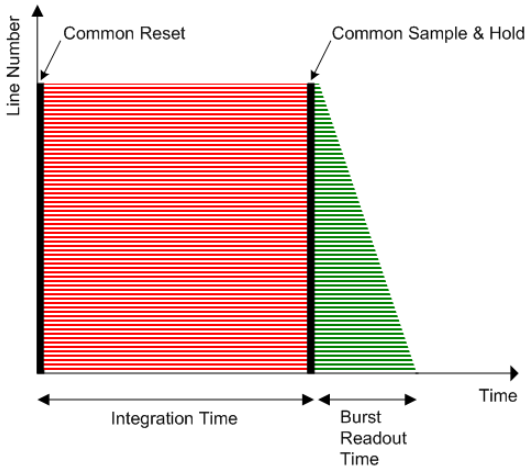


Figure 11. Global Shutter Operation

Pipelined Global Shutter Mode

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line per line and the readout of each line is preceded by the Row Overhead Time (ROT). Figure 12 shows the exposure and readout time line in pipelined global shutter mode.

Master Mode

The PYTHON 300, PYTHON 500, and PYTHON 1300 operate in pipelined or triggered global shuttering modes. In this mode, light, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

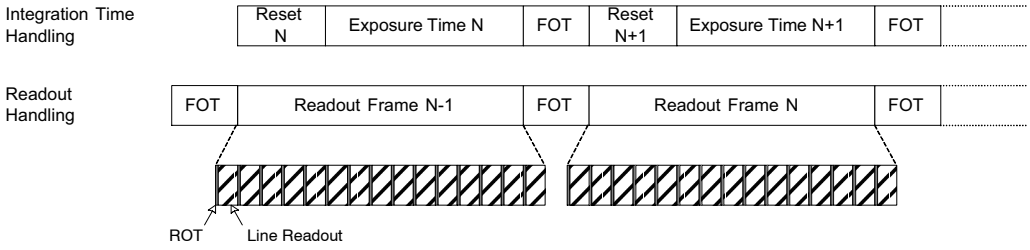


Figure 12. Integration and Readout for Pipelined Shutter

Slave Mode

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins. Figure 13 shows the relation between the external trigger signal and the exposure/readout timing.

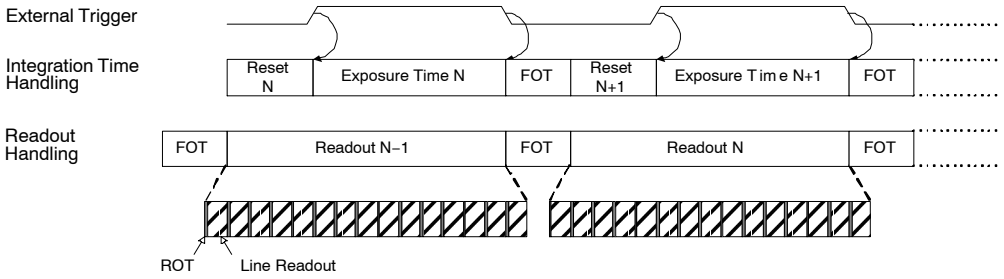


Figure 13. Pipelined Shutter Operated in Slave Mode

Triggered Global Shutter Mode

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences with the pipelined global shutter mode are:

- Upon user action, one single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is under user control through an external pin.

This mode requires manual intervention for every frame. The pixel array is kept in reset state until requested.

The triggered global mode can also be controlled in a master or in a slave mode.

Master Mode

In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is readout sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge. Figure 14 shows the relation between the external trigger signal and the exposure/readout timing.

If a rising edge is applied on the external trigger before the exposure time and FOT of the previous frame is complete, it is ignored by the sensor.

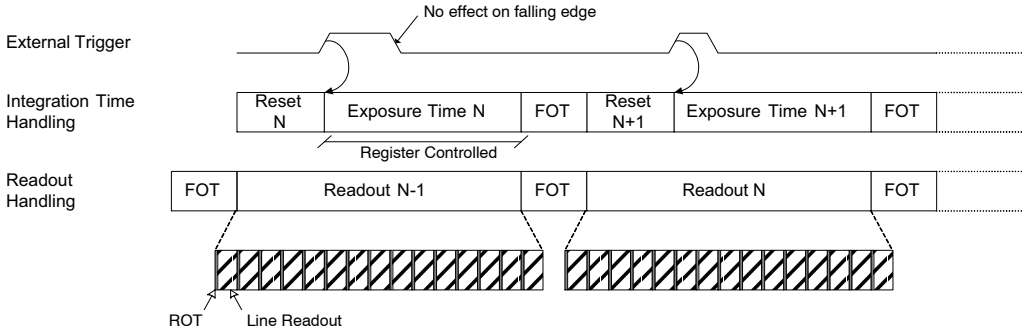


Figure 14. Triggered Shutter Operated in Master Mode

Slave Mode

Integration time control is identical to the pipelined shutter slave mode. An external synchronization pin controls the start of integration. When it is de−asserted, the FOT starts. The analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

Normal and Zero Row Overhead Time (ROT) Modes

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read out and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value of the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by a Row Overhead Time (ROT) as shown in Figure 15.

In Reduced/Zero ROT operation mode (refer to Figure 16), the row blanking and kernel readout occur in parallel. This mode is called reduced ROT as a part of the ROT is done while the image row is readout. The actual ROT can thus be longer, however the perceived ROT will be shorter (‘overhead’ spent per line is reduced). The integration time and gain parameters can be reconfigured without any visible image artifact in Normal ROT mode. Column−level offset corrections are required in Zero ROT mode. Refer to Column−Level Image Correction application note in the PYTHON Developer’s Guide AND9362/D available at the Image Sensor Portal.

This operation mode can be used for two reasons:

- Reduced total line time.
- Lower power due of reduced clock−rate.

NOTE: Zero ROT is not supported on P3−SN/SE/FN devices.

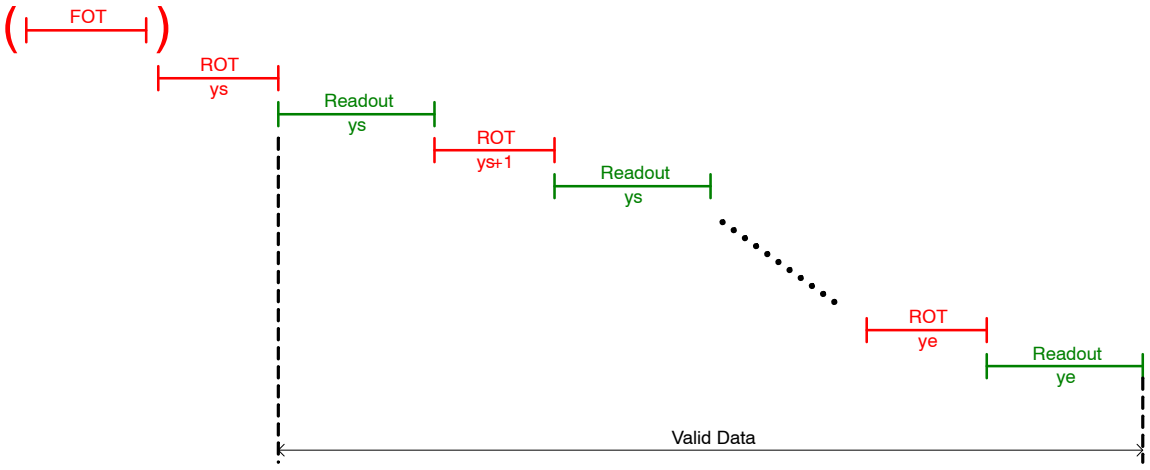


Figure 15. Integration and Readout Sequence of the Sensor Operating in Pipelined Global Shutter Mode with Normal ROT Readout.

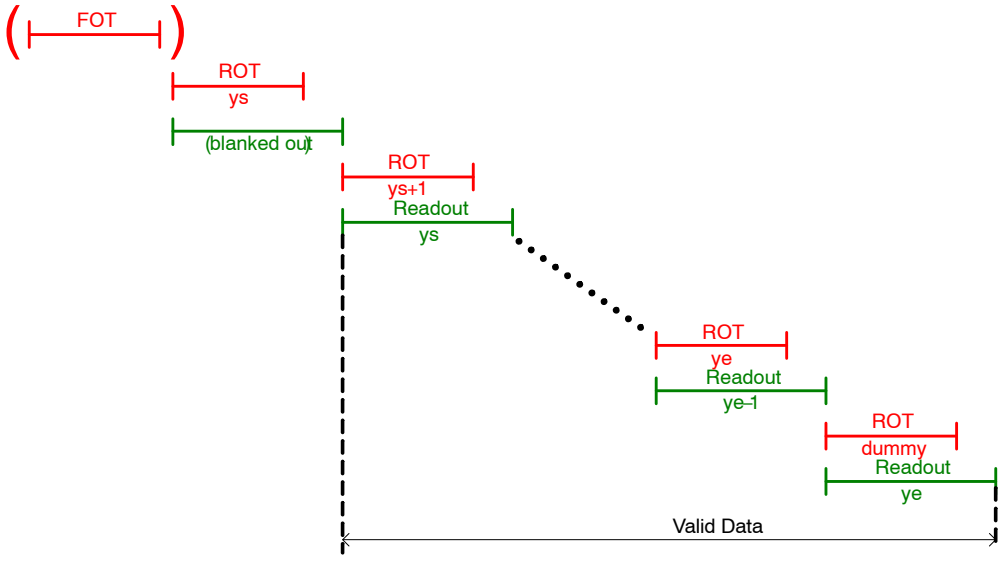


Figure 16. Integration and Readout Sequence of the Sensor Operating in Pipelined Global Shutter Mode with Zero ROT Readout.

SENSOR OPERATION

Flowchart

Figure 17 shows the sensor operation flowchart. The sensor has six different ‘states’. Every state is indicated with the oval circle. These states are Power off, Low power standby, Standby (1), Standby (2), Idle, Running.

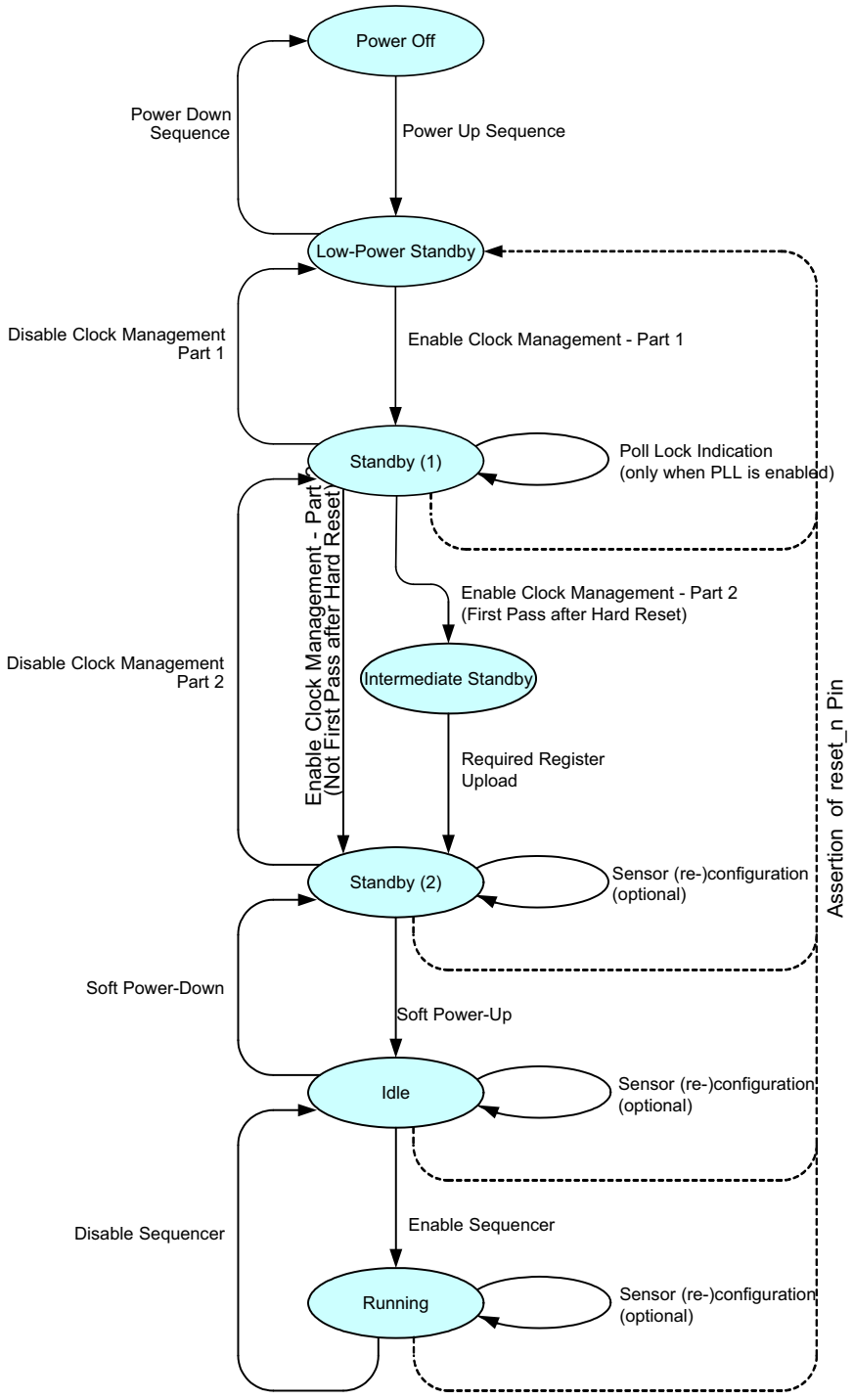


Figure 17. Sensor Operation Flowchart

Sensor States

Low Power Standby

In low power standby state, all power supplies are on, but internally every block is disabled. No internal clock is running (PLL / LVDS clock receiver is disabled).

All register settings are unchanged.

Only a subset of the SPI registers is active for read/write in order to be able to configure clock settings and leave the low power standby state. The only SPI registers that should be touched are the ones required for the ‘Enable Clock Management’ action described in Enable Clock Management − Part 1 on page 18

Standby (1)

In standby state, the PLL/LVDS clock receiver is running, but the derived logic clock signal is not enabled.

Standby (2)

In standby state, the derived logic clock signal is running. All SPI registers are active, meaning that all SPI registers can be accessed for read or write operations. All other blocks are disabled.

Idle

In the idle state, all internal blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in global master/slave modes.

User Actions: Power Up Functional Mode Sequences

Power Up Sequence

Figure 18 shows the power up sequence of the sensor. The figure indicates that the first supply to ramp−up is the vdd_18 supply, followed by vdd_33 and vdd_pix respectively. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. When the clock frequency is stable, the reset_n signal can be de−asserted. After a wait period of 10 µs, the power up sequence is finished and the first SPI upload can be initiated.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

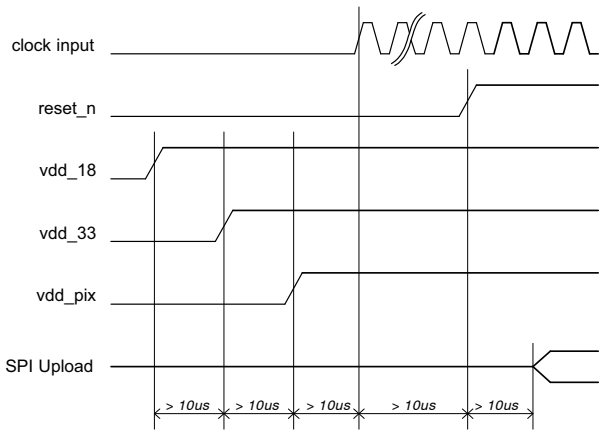


Figure 18. Power Up Sequence

Enable Clock Management − Part 1

The ‘Enable Clock Management’ action configures the clock management blocks and activates the clock generation and distribution circuits in a pre−defined way. First, a set of clock settings must be uploaded through the SPI register. These settings are dependent on the desired operation mode of the sensor.

Table 6 shows the SPI uploads to be executed to configure the sensor for P1−SN/SE/FN, P3−SN/SE/FN 10−bit serial mode, with the PLL, and all available LVDS channels.

Note that the SPI uploads to be executed to configure the sensor for other supported modes (P1−SN/SE/FN 8−bit serial, P2−SN/SE 10−bit parallel, ...) are available to customers under NDA at the ON Semiconductor Image Sensor Portal.

In the serial modes, if the PLL is not used, the LVDS clock input must be running.

In the P2−SN/SE 10−bit parallel mode, the PLL is bypassed. The clk_pll clock is used as sensor clock.

It is important to follow the upload sequence listed in Table 6.

Use of Phase Locked Loop

If PLL is used, the PLL is started after the upload of the SPI registers. The PLL requires (dependent on the settings) some time to generate a stable output clock. A lock detect circuit detects if the clock is stable. When complete, this is flagged in a status register.

NOTE: The lock detect status must not be checked for the P2−SN/SE sensor.

Check the PLL_lock flag 24[0] by reading the SPI register. When the flag is set, the 'Enable Clock Management− Part 2' action can be continued. When PLL is not used, this step can be bypassed as shown in Figure 17 on page 16.

Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD: PART 1

Upload #	Address	Data	Description
P1−SN/SE/FN, P3−SN/SE/FN 10−bit mode with PLL			
1	2	0x0000	Monochrome sensor
		0x0001	Color sensor
2	8	0x0000	Release PLL soft reset
3	16	0x0003	Enable PLL
4	17	0x2113	Configure PLL
5	20	0x0000	Configure clock management
6	26	0x2280	Configure PLL lock detector
7	27	0x3D2D	Configure PLL lock detector
8	32	0x7004	Configure clock management for P1 only
		0x6014	Configure clock management for P3 only
P2−SN/SE 10−bit mode			
1	2	0x0002	Monochrome sensor
		0x0003	Color sensor
2	16	0x0007	Enable PLL bypass mode
3	20	0x0000	Configure clock management
4	32	0x700C	Configure clock management

Enable Clock Management − Part 2

The next step to configure the clock management consists of SPI uploads which enables all internal clock distribution. The required uploads are listed in Table 4. Note that it is important to follow the upload sequence listed in Table 7.

Table 7. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD: PART 2

Upload #	Address	Data	Description
P1−SN/SE/FN, P3−SN/SE/FN 10−bit mode with PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x7006	Enable logic clock for P1 only
		0x6016	Enable logic clock for P3 only
3	34	0x0001	Enable logic blocks
P2−SN/SE 10−bit mode			
1	9	0x0000	Release clock generator soft reset
2	32	0x700E	Enable logic clock
3	34	0x0001	Enable logic blocks

Required Register Upload

In this phase, the ‘reserved’ register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads are listed in Table 8.

Table 8. REQUIRED REGISTER UPLOAD

Upload #	Address	P1−SN/SE/FN 10−bit mode with PLL (4 LVDS ZROT)	Address	P2−SN/SE 10−bit mode (ZROT)	Address	P3−SN/SE/FN 10−bit mode with PLL (2 LVDS NROT)
1	41	0x085F	41	0x085F	41	0x085F
2	42	0x4110	42	0x4110	42	0x4110
3	43	0x0008	43	0x0008	43	0x0008
4	65	0x382B	65	0x382B	65	0x382B
5	66	0x53C8	66	0x53C8	66	0x53C4
6	67	0x0665	67	0x0344	67	0x0645
7	68	0x0085	68	0x0085	68	0x0085
8	69	0x0088	69	0x0088	69	0x0048
9	70	0x1111	70	0x1111	70	0x1111
10	72	0x0010	72	0x0010	72	0x0017
11	128	0x4714	128	0x4714	128	0x4714
12	129	0x8001	129	0xA001	129	0x8001
13	171	0x1002	130	0x0001	171	0x1002
14	175	0x0080	171	0x1002	175	0x0080
15	176	0x00E6	175	0x0080	176	0x00E6
16	177	0x0400	176	0x00E6	177	0x0400
17	192	0x080C	177	0x0400	192	0x0800
18	194	0x0224	192	0x080C	194	0x0224
19	197	0x0306	194	0x0224	197	0x0306
20	204	0x01E1	197	0x0103	204	0x01E3
21	207	0x0000	204	0x01E1	207	0x0000
22	211	0x0E49	207	0x0000	211	0x0E39
23	215	0x111F	211	0x0E49	215	0x111F
24	216	0x7F00	215	0x111F	216	0x7F00
25	219	0x0020	216	0x7F00	219	0x0020
26	220	0x3A28	219	0x0017	220	0x3728
27	221	0x624D	220	0x2C1C	221	0x6245
28	222	0x624D	221	0x623C	222	0x6230
29	224	0x3E5E	222	0x623C	224	0x3E5E
30	227	0x0000	224	0x3E02	227	0x0000
31	250	0x2081	227	0x0000	250	0x2081
32	384	0xC800	250	0x2081	384	0xC800
33	385	0xFB1F	384	0xC800	385	0xFB1F
34	386	0xFB1F	385	0xFB1F	386	0xFB1F
35	387	0xFB12	386	0xFB17	387	0xFB12
36	388	0xF903	387	0xF802	388	0xF903
37	389	0xF802	388	0xF003	389	0xF802
38	390	0xF30F	389	0xF30F	390	0xF30F

Table 8. REQUIRED REGISTER UPLOAD

Upload #	Address	P1−SN/SE/FN 10−bit mode with PLL (4 LVDS ZROT)	Address	P2−SN/SE 10−bit mode (ZROT)	Address	P3−SN/SE/FN 10−bit mode with PLL (2 LVDS NROT)
39	391	0xF30F	390	0xF30F	391	0xF30F
40	392	0xF30F	391	0xF30F	392	0xF30F
41	393	0xF30A	392	0xF101	393	0xF30A
42	394	0xF101	393	0xF005	394	0xF101
43	395	0xF00A	394	0xF247	395	0xF00A
44	396	0xF24B	395	0xF226	396	0xF24B
45	397	0xF226	396	0xF002	397	0xF226
46	398	0xF001	397	0xF402	398	0xF001
47	399	0xF402	398	0xF001	399	0xF402
48	400	0xF001	399	0xF20F	400	0xF001
49	401	0xF402	400	0xF20F	401	0xF402
50	402	0xF001	401	0xF205	402	0xF001
51	403	0xF401	402	0xF002	403	0xF401
52	404	0xF007	403	0xC801	404	0xF007
53	405	0xF20F	404	0xCC01	405	0xF20F
54	406	0xF20F	405	0xC802	406	0xF20F
55	407	0xF202	406	0xC800	407	0xF202
56	408	0xF006	407	0xC800	408	0xF006
57	409	0xEC02	408	0xC801	409	0xEC02
58	410	0xE801	409	0xCC04	410	0xE801
59	411	0xEC02	410	0xC801	411	0xEC02
60	412	0xE801	411	0xC800	412	0xE801
61	413	0xEC02	412	0x0030	413	0xEC02
62	414	0xC801	413	0x0078	414	0xC801
63	415	0xC800	414	0x0072	415	0xC800
64	416	0xC800	415	0x1071	416	0xC800
65	417	0xCC02	416	0x3073	417	0xCC02
66	418	0xC801	417	0x1073	418	0xC801
67	419	0xCC02	418	0x0072	419	0xCC02
68	420	0xC801	419	0x0031	420	0xC801
69	421	0xCC02	420	0x00B1	421	0xCC02
70	422	0xC805	421	0x01B8	422	0xC805
71	423	0xC800	422	0x00B2	423	0xC800
72	424	0x0030	423	0x10B1	424	0x0030
73	425	0x207C	424	0x30B3	425	0x2073
74	426	0x2071	425	0x10B3	426	0x2071
75	427	0x0074	426	0x00B2	427	0x0071
76	428	0x107F	427	0x0030	428	0x1079
77	429	0x1072	428	0x0030	429	0x1072
78	430	0x1074	429	0x0178	430	0x0073

Table 8. REQUIRED REGISTER UPLOAD

Upload #	Address	P1−SN/SE/FN 10−bit mode with PLL (4 LVDS ZROT)	Address	P2−SN/SE 10−bit mode (ZROT)	Address	P3−SN/SE/FN 10−bit mode with PLL (2 LVDS NROT)
79	431	0x0076	430	0x0072	431	0x0031
80	432	0x0031	431	0x1071	432	0x21B6
81	433	0x21BB	432	0x3073	433	0x20B1
82	434	0x20B1	433	0x1073	434	0x00B1
83	435	0x20B1	434	0x0072	435	0x10B9
84	436	0x00B1	435	0x0031	436	0x10B2
85	437	0x10BF	436	0x00B1	437	0x00B1
86	438	0x10B2	437	0x00B8	438	0x0030
87	439	0x10B4	438	0x00B2	439	0x0030
88	440	0x00B1	439	0x10B1	440	0x2176
89	441	0x0030	440	0x30B3	441	0x2071
90	442	0x0030	441	0x10B3	442	0x2071
91	443	0x217B	442	0x00B2	443	0x0071
92	444	0x2071	443	0x0030	444	0x1079
93	445	0x2071			445	0x1072
94	446	0x0074			446	0x0073
95	447	0x107F			447	0x0031
96	448	0x1072			448	0x20B3
97	449	0x1074			449	0x00B1
98	450	0x0076			450	0x10B9
99	451	0x0031			451	0x10B2
100	452	0x20BB			452	0x00B1
101	453	0x20B1			453	0x0030
102	454	0x20B1				
103	455	0x00B1				
104	456	0x10BF				
105	457	0x10B2				
106	458	0x10B4				
107	459	0x00B1				
108	460	0x0030				

NOTE: Register uploads for other supported operation modes can be accessed at the Image Sensor Portal on MyON.

Soft Power Up

During the soft power up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power up uploads are listed in Table 9.

Table 9. SOFT POWER UP REGISTER UPLOAD

Upload #	Address	Data	Description
P1−SN/SE/FN, P3−SN/SE/FN 10−bit mode with PLL (P1 in ZROT, P3 in NROT)			
1	10	0x0000	Release soft reset state
2	32	0x7007	Enable analog clock for P1
		0x6017	Enable analog clock for P3
3	40	0x0003	Enable column multiplexer
4	42	0x4113	Configure image core
5	48	0x0001	Enable AFE
6	64	0x0001	Enable biasing block
7	72	0x0017	Enable charge pump
8	112	0x0007	Enable LVDS transmitters
P2−SN/SE 10−bit mode (ZROT)			
1	10	0x0000	Release soft reset state
2	32	0x700F	Enable analog clock
3	40	0x0003	Enable column multiplexer
4	42	0x4113	Configure image core
5	48	0x0001	Enable AFE
6	64	0x0001	Enable biasing block
7	72	0x0017	Enable charge pump

Enable Sequencer

During the ‘Enable Sequencer’ action, the frame grabbing sequencer is enabled. The sensor starts grabbing images in the configured operation mode. Refer to Sensor States on page 17.

The ‘Enable Sequencer’ action consists of a set of register uploads. The required uploads are listed in Table 10.

Table 10. ENABLE SEQUENCER REGISTER UPLOAD

Upload #	Address	Data	Description
1	192	0x080D	Enable Sequencer for P1 in ZROT
		0x0801	Enable Sequencer for P3 in NROT

User Actions: Functional Modes to Power Down Sequences

Disable Sequencer

During the ‘Disable Sequencer’ action, the frame grabbing sequencer is stopped. The sensor stops grabbing images and returns to the idle mode.

The ‘Disable Sequencer’ action consists of a set of register uploads. as listed in Table 11.

Table 11. DISABLE SEQUENCER REGISTER UPLOAD

Upload #	Address	Data	Description
1	192	0x080C	Disable sequencer for P1 in ZROT
		0x0800	Disable sequencer for P3 in NROT

Soft Power Down

During the soft power down action, the internal blocks are disabled and the sensor is put in standby state to reduce the current dissipation. This action exists of a set of SPI uploads. The soft power down uploads are listed in Table 12.

Table 12. SOFT POWER DOWN REGISTER UPLOAD

Upload #	Address	Data	Description
P1−SN/SE/FN, P3−SN/SE/FN 10−bit mode with PLL (P1 in ZROT, P3 in NROT)			
1	10	0x0999	Soft reset
2	32	0x7006	Disable analog clock for P1
		0x6016	Disable analog clock for P3
3	40	0x0000	Disable column multiplexer
4	42	0x4110	Image core config
5	48	0x0000	Disable AFE
6	64	0x0000	Disable biasing block
7	72	0x0010	Disable charge pump
8	112	0x0000	Disable LVDS transmitters
P2−SN/SE 10−bit mode (ZROT)			
1	10	0x0999	Soft reset
2	32	0x700E	Disable analog clock
3	40	0x0000	Disable column multiplexer
4	42	0x4110	Image core config
5	48	0x0000	Disable AFE
6	64	0x0000	Disable biasing block
7	72	0x0010	Disable charge pump

Disable Clock Management – Part 2

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 13.

Table 13. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD: PART 2

Upload #	Address	Data	Description
P1−SN/SE/FN, P3−SN/SE/FN 10−bit mode with PLL			
1	9	0x0000	Soft reset clock generator
2	32	0x7004	Disable logic clock for P1
		0x6014	Disable logic clock for P3
3	34	0x0000	Disable logic blocks
P2−SN/SE 10−bit mode			
1	9	0x0000	Soft reset clock generator
2	32	0x700C	Disable logic clock
3	34	0x0000	Disable logic blocks

Disable Clock Management – Part 1

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 14.

Table 14. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD: PART 1

Upload #	Address	Data	Description
P1−SN/SE/FN, P3−SN/SE/FN 10−bit mode with PLL			
1	8	0x0099	Soft reset PLL
2	16	0x0000	Disable PLL

Power Down Sequence

Figure 19 illustrates the timing diagram of the preferred power down sequence. It is important that the sensor is in reset before the clock input stops running. Otherwise, the internal PLL becomes unstable and the sensor gets into an unknown state. This can cause high peak currents.

The same applies for the ramp down of the power supplies. The preferred order to ramp down the supplies is first vdd_pix, second vdd_33, and finally vdd_18. Any other sequence can cause high peak currents.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

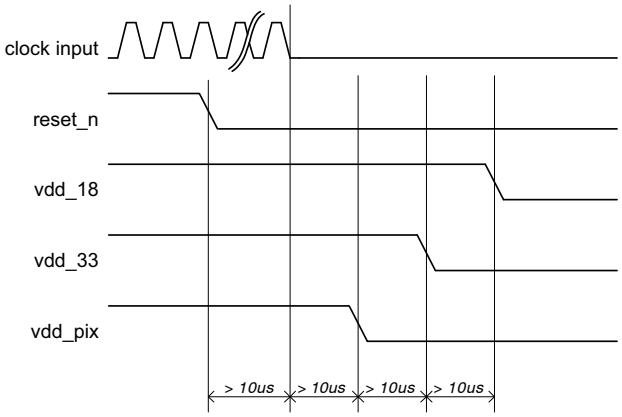


Figure 19. Power Down Sequence

Sensor Reconfiguration

During the standby, idle, or running state several sensor parameters can be reconfigured.

- Frame Rate and Exposure Time: Frame rate and exposure time changes can occur during standby, idle, and running states by modifying registers 199 to 203. Refer to page 30−32 for more information.
- Signal Path Gain: Signal path gain changes can occur during standby, idle, and running states by modifying registers 204/205. Refer to page 37 for more information.
- Windowing: Changes with respect to windowing can occur during standby, idle, and running states. Refer to Multiple Window Readout on page 32 for more information.
- Subsampling: Changes of the subsampling mode can occur during standby, idle, and running states by modifying register 192. Refer to Subsampling on page 33 for more information.
- Shutter Mode: The shutter mode can only be changed during standby or idle mode by modifying register 192. Reconfiguring the shutter mode during running state is not supported.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 15 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 15. STATIC READOUT PARAMETERS

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64–71	Configure according to recommendation
LVDS	112	Configure according to recommendation
Sequencer mode selection	192 [6:1]	Operation modes are: • triggered_mode • slave_mode
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the recommendation

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 16 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the reconfiguration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed.

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 16. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

Group	Addresses	Description
Black level configuration	128–129 197[12:8]	Reconfiguration of these registers may have an impact on the black−level calibration algorithm. The effect is a transient number of images with incorrect black level compensation.
Sync codes	129[13] 116–126	Incorrect sync codes may be generated during the frame in which these registers are modified.
Datablock test configurations	144, 146–150	Modification of these registers may generate incorrect test patterns during a transient frame.