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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# NOIP1SN5000A

# PYTHON 5.0/2.0 MegaPixels Global Shutter CMOS Image Sensors

ON Semiconductor®

www.onsemi.com

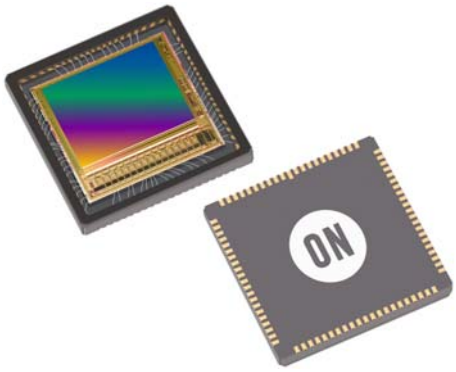

**Figure 1. PYTHON 5000**

### Features

- Data Output Options
  - P1−SN/SE/FN: 8 LVDS Data Channels
  - P3−SN/SE: 4 LVDS Data Channels
- Size Options
  - PYTHON 2000: 1920 x 1200 Active Pixels, 2/3” Optical Format
  - PYTHON 5000: 2592 x 2048 Active Pixels, 1” Optical Format
- 4.8 μm x 4.8 μm Low Noise Global Shutter Pixels with In-pixel CDS
- Monochrome (SN), Color (SE) and NIR (FN)
- Zero Row Overhead Time Mode Enabling Higher Frame Rate
- Frame Rate at Full Resolution, 8 LVDS Data Channels (P1−SN/SE/FN only)
  - 100/85 frames per second @ 5 MP (Zero ROT/Non−Zero ROT)
  - 230/180 frames per second @ 2 MP (Zero ROT/Non−Zero ROT)
  - 255/200 frames per second @ Full HD (Zero ROT/Non−Zero ROT)
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- Eight/Four/Two/One LVDS High Speed Serial Outputs
- Random Programmable Region of Interest (ROI) Readout
- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- High Dynamic Range (HDR) Modes Possible
- Dual Power Supply (3.3 V and 1.8 V)
- −40°C to +85°C Operational Temperature Range
- 84-pin LCC and 128−pad LGA
- Power Dissipation
  - 1.45 W (P1−SN/SE/FN, 8 LVDS, NZROT)
  - 915 mW (P1−SN/SE/FN, P3−SN/SE, 4 LVDS, NZROT)
  - 520 mW (P1−SN/SE/FN, P3−SN/SE, 2 LVDS, NZROT)
  - 370 mW (P1−SN/SE/FN, P3−SN/SE, 1 LVDS, NZROT)
- These Devices are Pb−Free and are RoHS Compliant

### Applications

- Machine Vision
- Motion Monitoring
- Security
- Intelligent Traffic Systems (ITS)

### Description

The PYTHON 2000 and PYTHON 5000 image sensors utilize high sensitivity 4.8 μm x 4.8 μm pixels that support low noise “pipelined” and “triggered” global shutter readout modes. The sensors support correlated double sampling (CDS) readout, reducing noise and increasing dynamic range.

The sensor has on-chip programmable gain amplifiers and 10-bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on-chip automatic exposure control loop (AEC) controls these parameters dynamically. The image’s black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to sixteen regions can be programmed, achieving even higher frame rates.

The image data interface of the P1−SN/SE/FN devices consists of eight LVDS lanes, facilitating frame rates up to 100 frames per second in Zero ROT mode for the PYTHON 5000. Each channel runs at 720 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receiving end.

The P3−SN/SE devices are the same as the P1−SN/SE/FN but with only four of the eight LVDS data channels enabled, facilitating frame rates of 45 frames per second in Non Zero ROT (NZROT) for the PYTHON 5000.

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## ORDERING INFORMATION

| Part Number | Description | Package |
|---|---|---|
| **PYTHON 5000** | | |
| NOIP1SN5000A−QDI | 5 MegaPixel, Monochrome | 84−pin LCC |
| NOIP1SE5000A−QDI | 5 MegaPixel, Bayer Color | |
| NOIP1FN5000A−QDI | 5 MegaPixel, Monochrome with enhanced NIR | |
| NOIP1SN5000A−QTI | 5 MegaPixel, Monochrome, Protective Film | |
| NOIP1SE5000A−QTI | 5 MegaPixel, Bayer Color, Protective Film | |
| NOIP1FN5000A−QTI | 5 MegaPixel, Monochrome with enhanced NIR, Protective Film | |
| NOIP3SN5000A−QDI | 5 MegaPixel, 4 LVDS Outputs, Monochrome | |
| NOIP3SE5000A−QDI | 5 MegaPixel, 4 LVDS Outputs, Bayer Color | |
| NOIP3SN5000A−QTI | 5 MegaPixel, 4 LVDS Outputs, Monochrome, Protective Film | |
| NOIP3SE5000A−QTI | 5 MegaPixel, 4 LVDS Outputs, Bayer Color, Protective Film | |
| NOIP1SN5000A−LTI | 5 MegaPixel, Monochrome, Protective Film | 128−pad LGA |
| NOIP1SE5000A−LTI | 5 MegaPixel, Bayer Color, Protective Film | |
| NOIP1FN5000A−LTI | 5 MegaPixel, Monochrome with enhanced NIR, Protective Film | |
| NOIP3SN5000A−LTI | 5 MegaPixel, 4 LVDS Outputs, Monochrome, Protective Film | |
| NOIP3SE5000A−LTI | 5 MegaPixel, 4 LVDS Outputs, Bayer Color, Protective Film | |
| **PYTHON 2000** | | |
| NOIP1SN2000A−QDI | 2 MegaPixel, Monochrome | 84−pin LCC |
| NOIP1SE2000A−QDI | 2 MegaPixel, Bayer Color | |
| NOIP1FN2000A−QDI | 2 MegaPixel, Monochrome with enhanced NIR | |
| NOIP1SN2000A−QTI | 2 MegaPixel, Monochrome, Protective Film | |
| NOIP1SE2000A−QTI | 2 MegaPixel, Bayer Color, Protective Film | |
| NOIP1FN2000A−QTI | 2 MegaPixel, Monochrome with enhanced NIR, Protective Film | |
| NOIP1SN2000A−LTI | 2 MegaPixel, Monochrome, Protective Film | 128−pad LGA |
| NOIP1SE2000A−LTI | 2 MegaPixel, Bayer Color, Protective Film | |
| NOIP1FN2000A−LTI | 2 MegaPixel, Monochrome with enhanced NIR, Protective Film | |

The P1−SN/SE/FN base part references the mono, color and NIR enhanced versions of the 8 LVDS interface; the P3−SN/SE base part references the mono and color version of the 4 LVDS interface. More details on the part number coding can be found at http://www.onsemi.com/pub_link/Collateral/TND310−D.PDF

### Package Mark for LCC−84 Pin Package

Line 1: NOIP**yxx RRRR**A where y is either “1” for 8 LVDS Outputs, “3” for 4 LVDS Outputs.
where xx denotes mono micro lens (SN) or color micro lens (SE) or NIR micro lens (FN)
RRRR is the resolution (5000), (2000)
Line 2: **−QDI** (LCC−84 without protective film), **−QTI** (LCC−84 with protective film)
Line 3: **AWLYYWW** where AWL is PRODUCTION lot traceability, YYWW is the 4−digit date code

### Package Mark for LGA−128 Pad Package

Package Side 1: NOIP**yxxRRRR**A**−LTI** where y is either “1” for 8 LVDS Outputs, “3” for 4 LVDS Outputs.
where xx denotes mono micro lens (SN) or color micro lens (SE)
RRRR is the resolution (5000), (2000)
**−LTI** (LGA−128 with protective film)
Package Side 2: **AWLYYWW** where AWL is PRODUCTION lot traceability, YYWW is the 4−digit date code

## SPECIFICATIONS

### Key Specifications

**Table 1. GENERAL SPECIFICATIONS** (Note 1)

| Parameter | Specification |
|---|---|
| Pixel Type | In−pixel CDS. Global shutter pixel architecture |
| Shutter Type | Pipelined and triggered global shutter |
| Frame Rate Zero ROT/ Non−Zero ROT Mode | P1−SN/SE/FN:<br>PYTHON 2000: 230/180 fps<br>PYTHON 5000: 100/85 fps<br>P3−SN/SE: NA/45 fps |
| Master Clock | P1−SN/SE/FN, P3−SN/SE:<br>72 MHz when PLL is used,<br>360 MHz (10-bit) / 288 MHz (8-bit) when PLL is not used |
| Windowing | 16 Randomly programmable windows. Normal, sub-sampled and binned readout modes |
| ADC Resolution (Note 1) | 10-bit, 8-bit |
| LVDS Outputs | P1−SN/SE/FN: 8/4/2/1 data + sync + clock<br>P3−SN/SE: 4/2/1 data + sync + clock |
| Data Rate | P1−SN/SE/FN:<br>8 x 720 Mbps (10-bit) /<br>8 x 576 Mbps (8-bit)<br>P3−SN/SE/FN:<br>4 x 720 Mbps (10−bit) |
| Power Dissipation (10−bit mode) | P1−SN/SE/FN:<br>1.45 W (8 data channels)<br>P1−SN/SE/FN, P3−SN/SE:<br>915 mW (4 data channels)<br>P1−SN/SE/FN, P3−SN/SE:<br>520 mW (2 data channels)<br>P1−SN/SE/FN, P3−SN/SE:<br>370 mW (1 data channel) |
| Package Type | 84-pin LCC, 128-pad LGA |

**Table 2. NOMINAL ELECTRO−OPTICAL SPECIFICATIONS**

| Parameter | Specification |
|---|---|
| Active Pixels | PYTHON 5000: 2592 (H) x 2048 (V)<br>PYTHON 2000: 1984 (H) x 1264 (V) |
| Pixel Size | 4.8 μm x 4.8 μm |
| Conversion Gain | 0.096 LSB10/$e^-$, 140 μV/$e^-$ |
| Temporal Noise | < 10.7 $e^-$ (Non−Zero ROT, 1x gain)<br>< 9.4 $e^-$ (Non−Zero ROT, 2x gain) |
| Responsivity at 550 nm | 7.5 V/lux.s |
| Parasitic Light Sensitivity (PLS) | <1/5000 |
| Full Well Charge | 10000 $e^-$ |
| Quantum Efficiency at 550 nm | 57% |
| Pixel FPN | < 1.55 LSB10 (Non−Zero ROT)<br>< 1.35 (Zero−ROT) |
| PRNU | < 10 LSB10 on half scale response of 525 LSB10 |
| MTF | 66% @ 535 nm − X-dir & Y-dir |
| Pixel Storage Node Leakage (PSNL) @ 20°C (t_int = 30 ms) | 300 LSB10/s, 2800 $e^-$/s |
| Dark Signal @ 20°C | 9.3 $e^-$/s, 1.0 LSB10/s |
| Dark Current Doubling Temperature | 5.2°C |
| Dynamic Range | 60 dB |
| Signal to Noise Ratio (SNR max) | 40 dB |

**Table 3. RECOMMENDED OPERATING RATINGS** (Note 2)

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_J$ | Operating junction temperature range | −40 | 85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 4. ABSOLUTE MAXIMUM RATINGS** (Notes 3 and 4)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| ABS (1.8 V supply group) | ABS rating for 1.8 V supply group | −0.5 | 2.2 | V |
| ABS (3.3 V supply group) | ABS rating for 3.3 V supply group | −0.5 | 4.3 | V |
| $T_S$ | ABS storage temperature range | −40 | +150 | °C |
| | ABS storage humidity range at 85°C | | 85 | %RH |
| Electrostatic discharge (ESD) | Human Body Model (HBM): JS−001−2012 | 2000 | | V |
| | Charged Device Model (CDM): EIA/JESD22−C101, Class C1 | 500 | | |
| LU | Latch−up: JESD−78 | 100 | | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The ADC is 11−bit, down−scaled to 10−bit. The PYTHON uses a larger word−length internally to provide 10−bit on the output.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
4. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

## Table 5. ELECTRICAL SPECIFICATIONS

**Boldface limits apply for $T_J = T_{MIN}$ to $T_{MAX}$**, all other limits $T_J$ = +30°C. (Notes 5, 6, 7, 8 and 9)

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Power Supply Parameters – P1 – SN/SE/FN (ZROT)** (Note: All ground pins (gnd_18, gnd_33 and gnd_colpc) should be connected to an external 0 V ground reference.) | | | | | |
| vdd_33 | Supply voltage, 3.3 V | **3.2** | 3.3 | **3.4** | V |
| Idd_33 | Current consumption 3.3 V supply | | 355 | | mA |
| vdd_18 | Supply voltage, 1.8 V | **1.7** | 1.8 | **1.9** | V |
| Idd_18 | Current consumption 1.8 V supply | | 140 | | mA |
| vdd_pix | Supply voltage, pixel | **3.25** | 3.3 | **3.35** | V |
| Idd_pix | Current consumption pixel supply | | 10 | | mA |
| Ptot | Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V | | 1.45 | | W |
| Pstby_lp | Power consumption in low power standby mode | | | 50 | mW |
| Popt | Power consumption at lower pixel rates | | Configurable | | |
| **Power Supply Parameters – P3 – SN/SE (NZROT)** (Note: All ground pins (gnd_18, gnd_33 and gnd_colpc) should be connected to an external 0 V ground reference.) | | | | | |
| vdd_33 | Supply voltage, 3.3 V | **3.2** | 3.3 | **3.4** | V |
| Idd_33 | Current consumption 3.3 V supply (4/2/1 LVDS) | | 215 | | mA |
| vdd_18 | Supply voltage, 1.8 V | **1.7** | 1.8 | **1.9** | V |
| Idd_18 | Current consumption 1.8 V supply (4/2/1 LVDS) | | 105 | | mA |
| vdd_pix | Supply voltage, pixel | **3.25** | 3.3 | **3.35** | V |
| Idd_pix | Current consumption pixel supply (4/2/1 LVDS) | | 5 | | mA |
| Ptot | Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V<br>4 LVDS, NZROT<br>2 LVDS, NZROT<br>1 LVDS, NZROT | | <br>915<br>520<br>370 | | mW |
| Pstby_lp | Power consumption in low power standby mode | | | 50 | mW |
| Popt | Power consumption at lower pixel rates | | Configurable | | |
| **I/O – P1–SN/SE/FN, P3–SN/SE (EIA/TIA–644): Conforming to standard/additional specifications and deviations listed** | | | | | |
| fserdata | Data rate on data channels<br>DDR signaling – 4 data channels, 1 synchronization channel | | | 720 | Mbps |
| fserclock | Clock rate of output clock<br>Clock output for mesochronous signaling | | | 360 | MHz |
| Vicm | LVDS input common mode level | 0.3 | 1.25 | 1.8 | V |
| Tccsk | Channel to channel skew (Training pattern should be used to correct per channel skew) | | | 50 | ps |
| **Clock Specifications – P1–SN/SE/FN, P3–SN/SE** | | | | | |
| fin | Input clock rate when PLL used | | | 72 | MHz |
| fin | Input clock when LVDS input used | | | 360 | MHz |
| tidc | Input clock duty cycle when PLL used | 45 | 50 | 55 | % |
| tj | Input clock jitter | | | 20 | ps |
| fspi | SPI clock rate when PLL used | | | 10 | MHz |
| ratspi (=fin/fspi) | 10–bit (8 LVDS channels), PLL used – P1–SN/SE/FN only | 6 | | | |
| | 10–bit (4 LVDS channels), PLL used | 12 | | | |
| | 10–bit (2 LVDS channels), PLL used | 24 | | | |
| | 10–bit (1 LVDS channel), PLL used | 48 | | | |
| | 10–bit (8 LVDS channels), LVDS input used | 30 | | | |
| | 10–bit (4 LVDS channels), LVDS input used | 60 | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Refer to ACSPYTHON5000 available at CISP extranet for detailed acceptance criteria specifications.
9. For power supply management recommendations, please refer to Application Note AND9158.

**Table 5. ELECTRICAL SPECIFICATIONS**

**Boldface limits apply for $T_J = T_{MIN}$ to $T_{MAX}$**, all other limits $T_J$ = +30°C. (Notes 5, 6, 7, 8 and 9)

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Clock Specifications – P1–SN/SE/FN, P3–SN/SE** | | | | | |
| ratspi (=fin/fspi) | 10–bit (2 LVDS channels), LVDS input used | 120 | | | |
| | 10–bit (1 LVDS channel), LVDS input used | 240 | | | |
| | 8–bit (8 LVDS channels), PLL used | 6 | | | |
| | 8–bit (4 LVDS channels), PLL used | 12 | | | |
| | 8–bit (2 LVDS channels), PLL used | 24 | | | |
| | 8–bit (1 LVDS channel), PLL used | 48 | | | |
| | 8–bit (8 LVDS channels), LVDS input used | 24 | | | |
| | 8–bit (4 LVDS channels), LVDS input used | 48 | | | |
| | 8–bit (2 LVDS channels), LVDS input used | 96 | | | |
| | 8–bit (1 LVDS channel), LVDS input used | 192 | | | |

**Frame Specifications – P1–SN/SE/FN**

| | | Maximum | | | |
|---|---|---|---|---|---|
| | | Non–Zero ROT | Zero ROT | | Units |
| fps_roi1 | Xres x Yres = 2592 x 2048 | 85 | 100 | | fps |
| fps_roi2 | Xres x Yres = 2048 x 2048 | 100 | 130 | | fps |
| fps_roi3 | Xres x Yres = 1920 x 1200 | 180 | 230 | | fps |
| fps_roi4 | Xres x Yres = 1920 x 1080 | 200 | 255 | | fps |
| fps_roi5 | Xres x Yres = 1600 x 1200 | 205 | 275 | | fps |
| fps_roi6 | Xres x Yres = 1024 x 1024 | 395 | 480 | | fps |
| fps_roi7 | Xres x Yres = 1280 x 720 | 390 | 550 | | fps |
| fps_roi8 | Xres x Yres = 800 x 600 | 620 | 985 | | fps |
| fps_roi9 | Xres x Yres = 640 x 480 | 855 | 1450 | | fps |
| fps_roi10 | Xres x Yres = 512 x 512 | 890 | 1555 | | fps |
| fps_roi11 | Xres x Yres = 256 x 256 | 2065 | 2830 | | fps |
| fps_roi12 | Xres x Yres = 544 x 20 | 7980 | 10345 | | fps |
| fpix | Pixel rate (8 channels at 72 Mpix/s) | 576 | 576 | | Mpix/s |

**Frame Specifications – P3–SN/SE**

| | | Maximum (Non–Zero ROT) | | | |
|---|---|---|---|---|---|
| | | 4 LVDS | 2 LVDS | 1 LVDS | Units |
| fps_roi1 | Xres x Yres = 2592 x 2048 | 45 | 25 | 10 | fps |
| fps_roi2 | Xres x Yres = 2048 x 2048 | 55 | 30 | 15 | fps |
| fps_roi3 | Xres x Yres = 1920 x 1200 | 100 | 55 | 25 | fps |
| fps_roi4 | Xres x Yres = 1920 x 1080 | 110 | 60 | 30 | fps |
| fps_roi5 | Xres x Yres = 1600 x 1200 | 115 | 60 | 30 | fps |
| fps_roi6 | Xres x Yres = 1024 x 1024 | 195 | 105 | 55 | fps |
| fps_roi7 | Xres x Yres = 1280 x 720 | 230 | 125 | 65 | fps |
| fps_roi8 | Xres x Yres = 800 x 600 | 385 | 220 | 115 | fps |
| fps_roi9 | Xres x Yres = 640 x 480 | 550 | 320 | 175 | fps |
| fps_roi10 | Xres x Yres = 512 x 512 | 590 | 350 | 190 | fps |
| fps_roi11 | Xres x Yres = 256 x 256 | 1590 | 990 | 580 | fps |
| fps_roi12 | Xres x Yres = 544 x 20 | 6260 | 4340 | 2690 | fps |
| fpix | Pixel rate (8 channels at 72 Mpix/s) | 288 | 144 | 72 | Mpix/s |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Refer to ACSPYTHON5000 available at CISP extranet for detailed acceptance criteria specifications.
9. For power supply management recommendations, please refer to Application Note AND9158.

### Color Filter Array

The PYTHON color sensors are processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left.

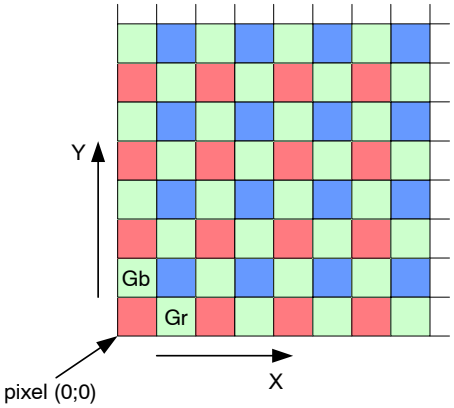



**Figure 2. Color Filter Array for the Pixel Array**

### Quantum Efficiency

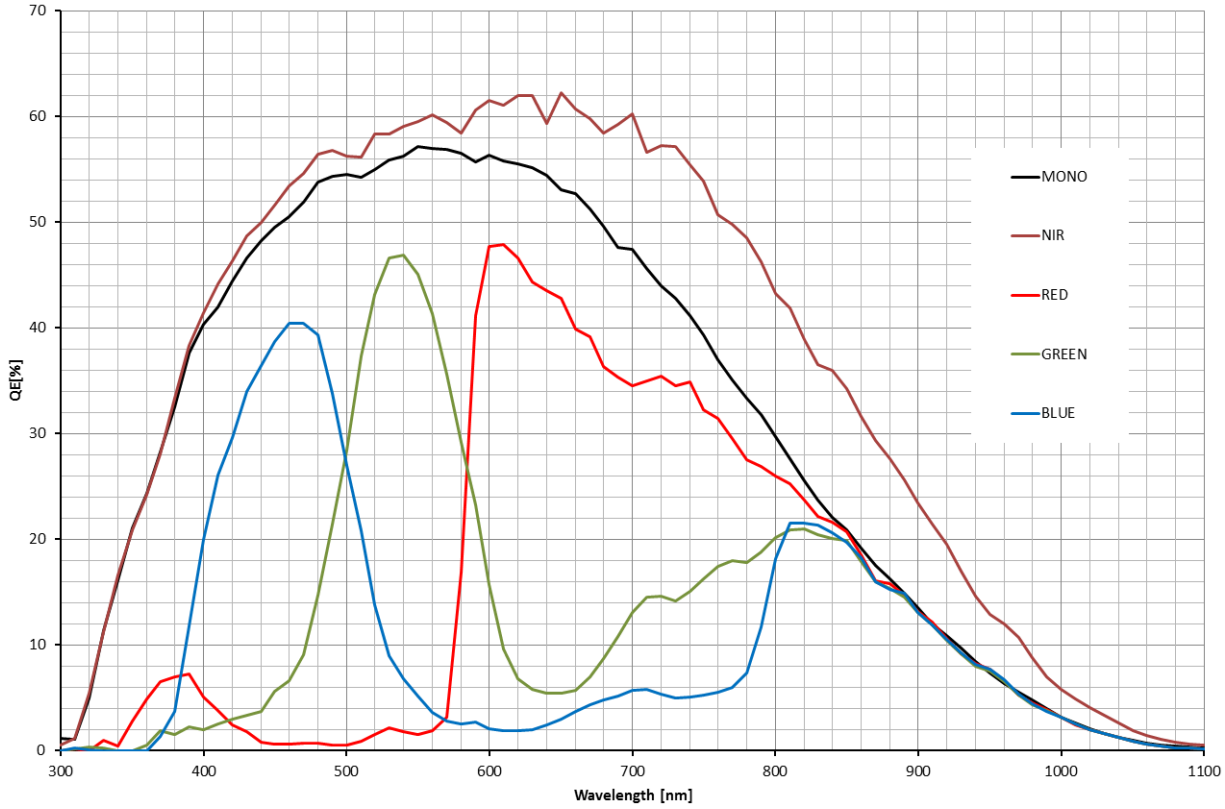



**Figure 3. Quantum Efficiency Curves**

### Ray Angle and Microlens Array Information

An array of microlenses is placed over the CMOS pixel array in order to improve the absolute responsivity of the photodiodes. The combined microlens array and pixel array has two important properties:

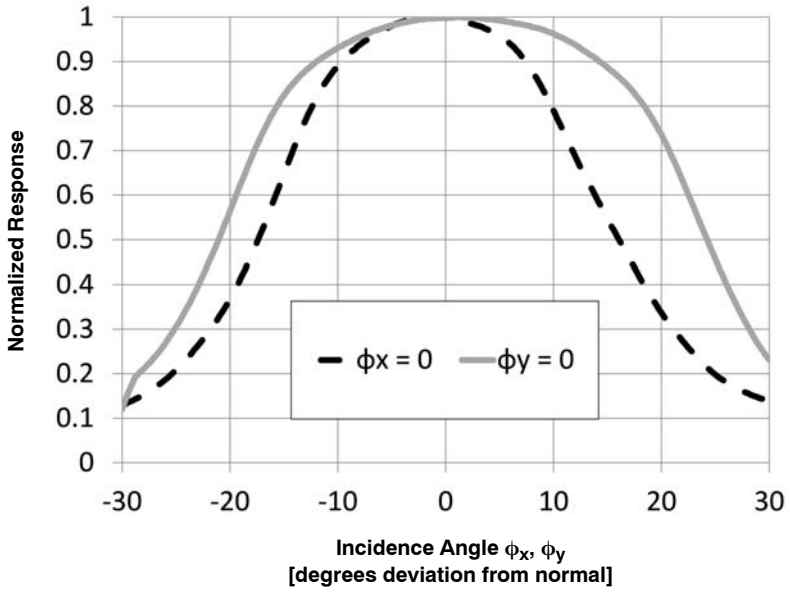
*Angular Dependency of Photoresponse of a Pixel*

The photoresponse of a pixel with microlens in the center of the array to a fixed optical power with varied incidence angle is as plotted in Figure 4, where definitions of angles ϕx and ϕy are as described by Figure 5.

*Microlens Shift across Array and CRA*

The microlens array is fabricated with a slightly smaller pitch than the array of photodiodes. This difference in pitch creates a varying degree of shift of a pixel's microlens with regards to its photodiode. A shift in microlens position versus photodiode position will cause a tilted angle of peak photoresponse, here denoted Chief Ray Angle (CRA). Microlenses and photodiodes are aligned with 0 shift and CRA in the center of the array, while the shift and CRA increases radially towards its edges, as illustrated by Figure 6.

The purpose of the shifted microlenses is to improve the uniformity of photoresponse when camera lenses with a finite exit pupil distance are used. In the standard version of Python 5000, the CRA varies nearly linearly with distance from the center as illustrated in Figure 7, with a corner CRA of approximately 5.4 degrees. This edge CRA is matching a lens with exit pupil distance of ~80 mm.




Note that the Photoresponse Peaks near Normal Incidence for Center Pixels

**Figure 4. Center Pixel Photoresponse to a Fixed Optical Power with Incidence Angle Varied along ϕx and ϕy**

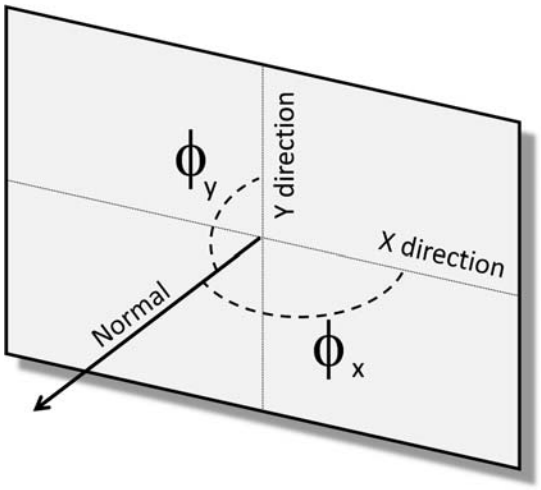
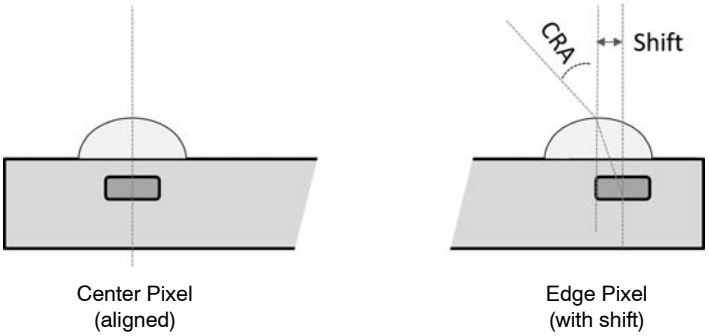



**Figure 5. Definition of Angles Used in Figure 4**




The center axes of the microlens and the photodiode coincide for the center pixels. For the edge pixels, there is a shift between the axes of the microlens and the photodiode causing a Peak Response Incidence Angle (CRA) that deviates from the normal of the pixel array.

**Figure 6. Principle of Microlens Shift**

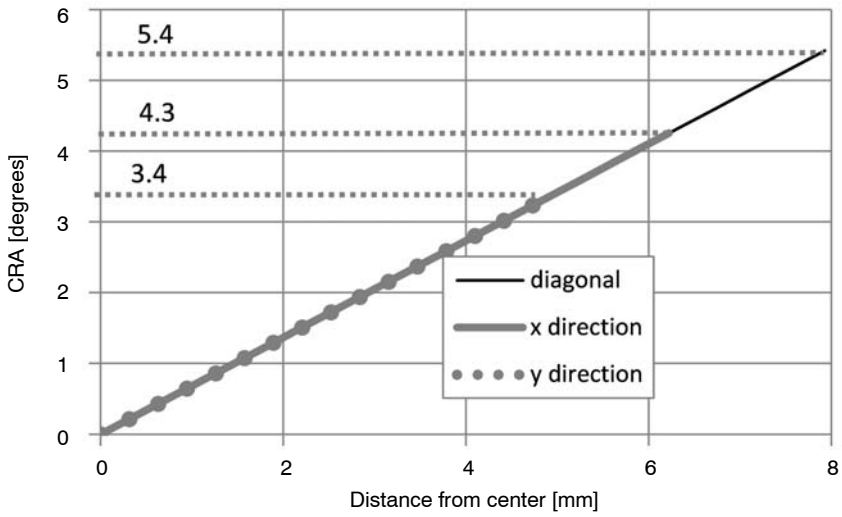



**Figure 7. Variation of Peak Responsivity Angle (CRA)**

## OVERVIEW

Figures 8 gives an overview of the major functional blocks of the PYTHON sensor.

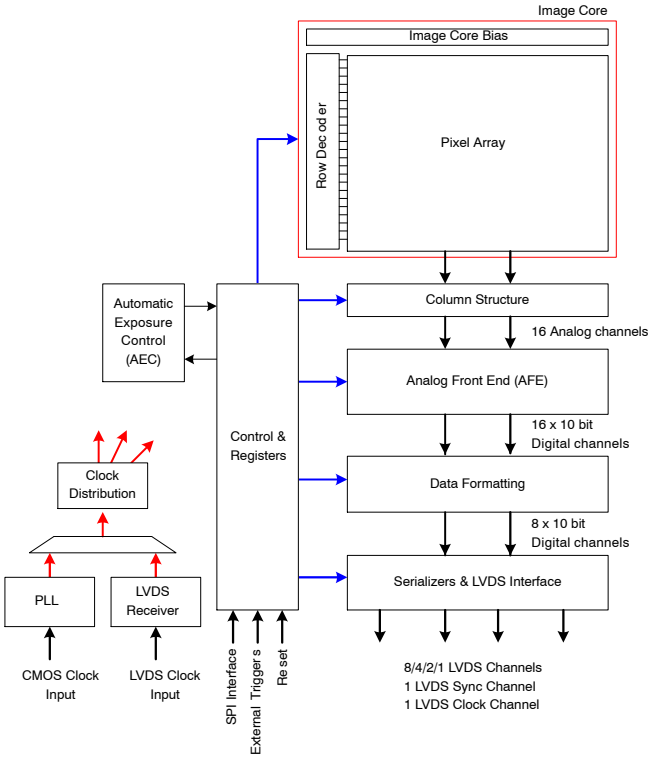



**Figure 8. Block Diagram**

### Image Core

The image core consists of:

- Pixel Array
- Address Decoders and Row Drivers
- Pixel Biasing

The PYTHON 5000 pixel array contains 2592 (H) x 2048 (V) readable pixels with a pixel pitch of 4.8 μm.

The PYTHON 2000 image array contains 1984 (H) x 1264 (V) readable pixels, inclusive of 32 pixels on each side to allow for reprocessing or color reconstruction.

The sensors use in−pixel CDS architecture, which makes it possible to achieve a low noise read out of the pixel array in global shutter mode with the function of the row drivers is to access the image array to reset or read the pixel data. The row drivers are controlled by the on−chip sequencer and can access the pixel array.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

### Phase Locked Loop

The PLL accepts a (low speed) clock and generates the required high speed clock. Optionally this PLL can be bypassed. Typical input clock frequency is 72 MHz.

### LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 360 MHz in 10−bit mode and 288 MHz in 8−bit mode. The clock input needs to be terminated with a 100 Ω resistor.

### Column Multiplexer

All pixels of one image row are stored in the column sample−and−hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 16 parallel differential outputs operating at a frequency of 36 MHz. At this stage, the reset signal and integrated signal values are transferred into an FPN−corrected differential signal. A programmable gain of 1x, 2x, or 4x can be applied to the signal. The column multiplexer also supports read−1−skip−1 and read−2−skip−2 mode. Enabling this mode increases the frame rate, with a decrease in resolution.

### Bias Generator

The bias generator generates all required reference voltages and bias currents used on chip. An external resistor of 47 kΩ, connected between pin IBIAS_MASTER and gnd_33, is required for the bias generator to operate properly.

### Analog Front End

The AFE contains 16 channels, each containing a PGA and a 10−bit ADC.

For each of the 16 channels, a pipelined 10−bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

### Data Formatting

The data block receives data from two ADCs and multiplexes this data to one data stream. A cyclic redundancy check (CRC) code is calculated on the passing data.

A frame synchronization data block transmits synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

### Serializer and LVDS Interface

The serializer and LVDS interface block receives the formatted (10−bit or 8−bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

In 10−bit mode, the maximum output data rate is 720 Mbps per channel. In 8−bit mode, the maximum output data rate is 576 Mbps per channel.

In addition to the LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system−level image reconstruction.

### Channel Multiplexer

The P1−SN/SE/FN LVDS channel multiplexer provides a 8:4, 8:2 and 8:1 feature, in addition to utilizing all 8 output channels.

The P3−SN/SE LVDS channel multiplexer provides a 4:2 and 4:1 feature, in addition to utilizing all 4 output channels.

### Sequencer

The sequencer:

- Controls the image core. Starts and stops integration and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

### Automatic Exposure Control

The AEC block implements a control system to modulate the exposure of an image. Both integration time and gains are controlled by this block to target a predefined illumination level.

## OPERATING MODES

### Global Shutter Mode

The PYTHON 2000 and PYTHON 5000 operates in pipelined or triggered global shutter modes. In this mode, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 9 shows the integration and readout sequence for the global shutter mode. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially. The integration starts at a certain period, relative to the frame start.

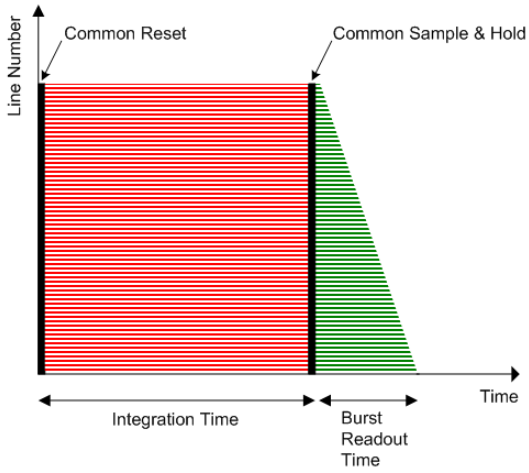



**Figure 9. Global Shutter Operation**

### *Pipelined Global Shutter Mode*

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line per line and the readout of each line is preceded by the Row Overhead Time (ROT). Figure 10 shows the exposure and readout time line in pipelined global shutter mode.

*Master Mode*

The PYTHON 2000 and PYTHON 5000 operate in pipelined or triggered global shuttering modes. In this mode, light, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

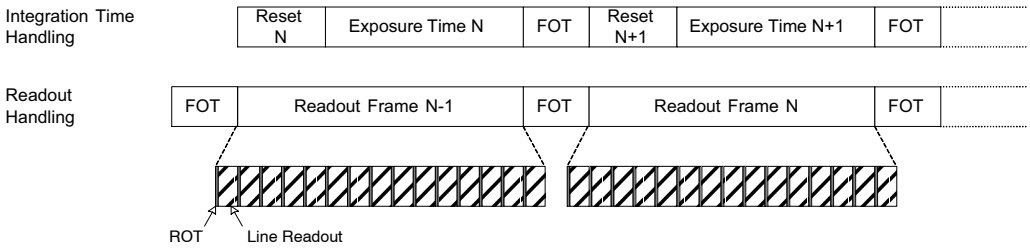



**Figure 10. Pipelined Shutter Operation in Master Mode**

*Slave Mode*

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins. Figure 11 shows the relation between the external trigger signal and the exposure/readout timing.

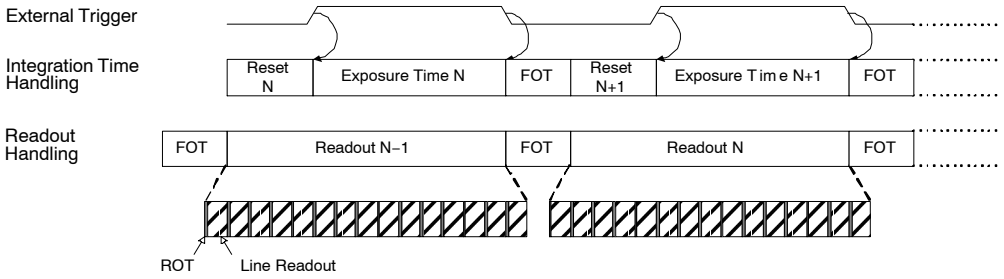



**Figure 11. Pipelined Shutter Operation in Slave Mode**

***Triggered Global Shutter Mode***

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences with the pipelined global shutter mode are:

- Upon user action, one single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is under user control through an external pin.

This mode requires manual intervention for every frame. The pixel array is kept in reset state until requested.

The triggered global shutter mode can also be controlled in a master or in a slave mode.

*Master Mode*

In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is readout sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge. Figure 12 shows the relation between the external trigger signal and the exposure/readout timing.

If a rising edge is applied on the external trigger before the exposure time and FOT of the previous frame is complete, it is ignored by the sensor.

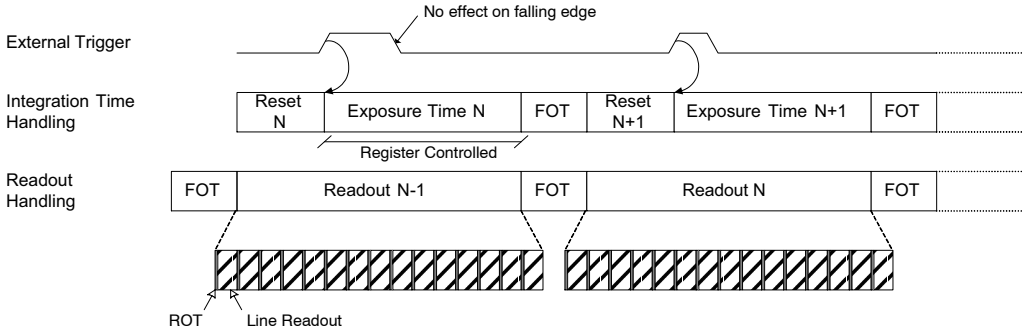



**Figure 12. Triggered Shutter Operation in Master Mode**

*Slave Mode*

Integration time control is identical to the pipelined shutter slave mode. An external synchronization pin controls the start of integration. When it is de−asserted, the FOT starts. The analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

### Non−Zero and Zero Row Overhead Time (ROT) Modes

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read out and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value of the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by a Row Overhead Time (ROT) as shown in Figure 13.

In Reduced/Zero ROT operation mode (refer to Figure 14), the row blanking and kernel readout occur in parallel. This mode is called reduced ROT as a part of the ROT is done while the image row is readout. The actual ROT can thus be longer, however the perceived ROT will be shorter (‘overhead’ spent per line is reduced).

The integration time and gain parameters can be reconfigured without any visible image artifact in Normal ROT mode. Column−level offset corrections are required in Zero ROT mode. Refer to Column−Level Image Correction application note in the PYTHON Developer’s Guide AND9362/D available at the Image Sensor Portal.

This operation mode can be used for two reasons:

- Reduced total line time.
- Lower power due to reduced clock−rate.

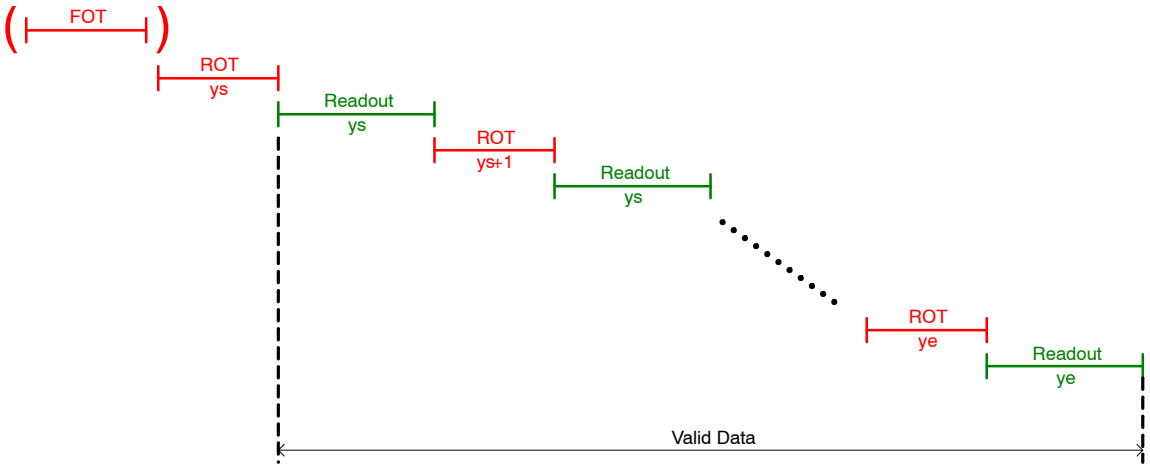



**Figure 13. Integration and Readout Sequence of the Sensor Operating in Pipelined Global Shutter Mode with Non−Zero ROT Readout.**

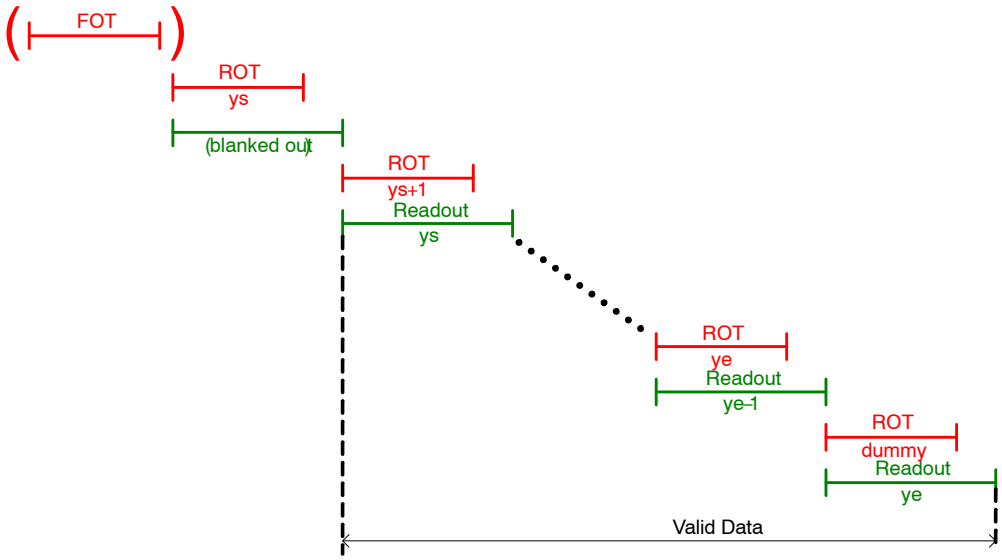



**Figure 14. Integration and Readout Sequence of the Sensor operating in Pipelined Global Shutter Mode with Zero ROT Readout.**

## SENSOR OPERATION

### Flowchart

Figure 15 shows the sensor operation flowchart. The sensor has six different ‘states’. Every state is indicated with the oval circle. These states are Power off, Low power standby, Standby (1), Standby (2), Idle, Running.

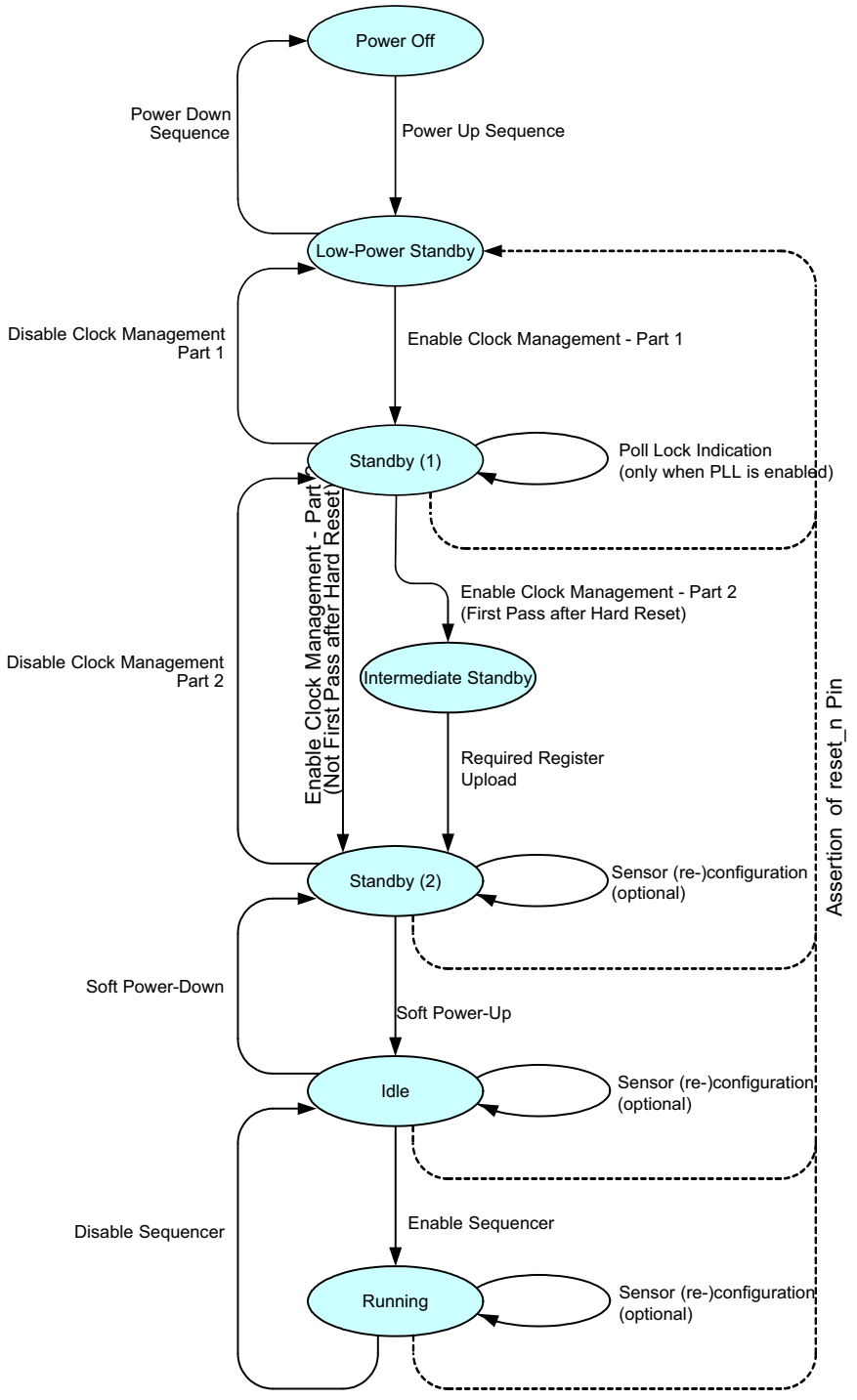



**Figure 15. Sensor Operation Flowchart**

## Sensor States

### *Low Power Standby*

In low power standby state, all power supplies are on, but internally every block is disabled. No internal clock is running (PLL / LVDS clock receiver is disabled).

All register settings are set to their default values (see Table 37).

Only a subset of the SPI registers is active for read/write in order to be able to configure clock settings and leave the low power standby state. The only SPI registers that should be touched are the ones required for the ‘Enable Clock Management’ action described in Enable Clock Management − Part 1 on page 16

### *Standby (1)*

In standby state, the PLL/LVDS clock receiver is running, but the derived logic clock signal is not enabled.

### *Standby (2)*

In standby state, the derived logic clock signal is running. All SPI registers are active, meaning that all SPI registers can be accessed for read or write operations. All other blocks are disabled.

### *Idle*

In the idle state, all internal blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

### *Running*

In running state, the sensor is enabled and grabbing images. The sensor can be operated in global master/slave modes.

## User Actions: Power Up Functional Mode Sequences

### *Power Up Sequence*

Figure 16 shows the power up sequence of the sensor. The figure indicates that the first supply to ramp−up is the vdd_18 supply, followed by vdd_33 and vdd_pix respectively. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. When the clock frequency is stable, the reset_n signal can be de−asserted. After a wait period of 10 μs, the power up sequence is finished and the first SPI upload can be initiated.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

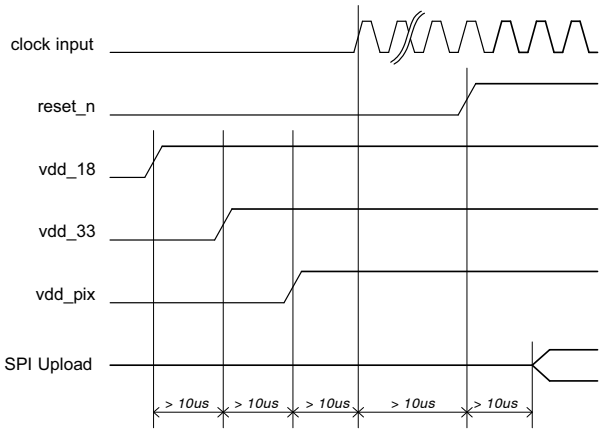



**Figure 16. Power Up Sequence**

### *Enable Clock Management − Part 1*

The ‘Enable Clock Management’ action configures the clock management blocks and activates the clock generation and distribution circuits in a pre−defined way. First, a set of clock settings must be uploaded through the SPI register. These settings are dependent on the desired operation mode of the sensor.

Table 6 shows the SPI uploads to be executed to configure the sensor for P1−SN/SE/FN, P3−SN/SE 10−bit serial mode, with the PLL, and all available LVDS channels.

Note that the SPI uploads to be executed to configure the sensor for other supported modes (P1−SN/SE/FN 8−bit serial,...) are available to customers under NDA at the ON Semiconductor Image Sensor Portal.

If the PLL is not used, the LVDS clock input must be running.

It is important to follow the upload sequence listed in Table 6.

### *Use of Phase Locked Loop*

If PLL is used, the PLL is started after the upload of the SPI registers. The PLL requires (dependent on the settings) some time to generate a stable output clock. A lock detect circuit detects if the clock is stable. When complete, this is flagged in a status register.

Check the PLL_lock flag 24[0] by reading the SPI register. When the flag is set, the ‘Enable Clock Management− Part 2’ action can be continued. When PLL is not used, this step can be bypassed as shown in Figure 15 on page 14.

**Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD − PART 1**

| Upload # | Address | Data | Description |
|---|---|---|---|
| **P1−SN/SE/FN, P3−SN/SE 10−bit mode with PLL** | | | |
| 1 | 2 | 0x0000 | Monochrome sensor |
| | | 0x0001 | Color sensor |
| 2 | 32 | 0x7004 | Configure clock management P1−SN/SE/FN only |
| | | 0x7014 | Configure clock management P3−SN/SE only |
| 3 | 20 | 0x0000 | Configure clock management |
| 4 | 17 | 0x2113 | Configure PLL |
| 5 | 26 | 0x2280 | Configure PLL lock detector |
| 6 | 27 | 0x3D2D | Configure PLL lock detector |
| 7 | 8 | 0x0000 | Release PLL soft reset |
| 8 | 16 | 0x0003 | Enable PLL |

### *Enable Clock Management − Part 2*

The next step to configure the clock management consists of SPI uploads which enables all internal clock distribution. The required uploads are listed in Table 7. Note that it is important to follow the upload sequence listed in Table 7.

**Table 7. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD − PART 2**

| Upload # | Address | Data | Description |
|---|---|---|---|
| **P1−SN/SE/FN, P3−SN/SE 10−bit mode with PLL** | | | |
| 1 | 9 | 0x0000 | Release clock generator soft reset |
| 2 | 32 | 0x7006 | Enable logic clock for P1−SN/SE/FN only |
| | | 0x7016 | Enable logic clock for P3−SN/SE only |
| 3 | 34 | 0x0001 | Enable logic block |

### *Required Register Upload*

In this phase, the ‘reserved’ register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads are listed in Table 8.

**Table 8. REQUIRED REGISTER UPLOADS**

| Up-load # | Ad-dress | P1−SN/SE/FN 10−bit mode with PLL (8 LVDS NZROT) | P3−SN/SE 10−bit mode with PLL (4 LVDS NZROT) |
|---|---|---|---|
| 1 | 41 | 0x0854 | 0x0854 |
| 2 | 42 | 0x0200 | 0x0200 |
| 3 | 43 | 0x000C | 0x000C |
| 4 | 65 | 0x48CB | 0x48CB |
| 5 | 66 | 0x53C8 | 0x53C4 |
| 6 | 67 | 0x8688 | 0x4544 |
| 7 | 68 | 0x0085 | 0x0085 |
| 8 | 69 | 0x0888 | 0x0848 |
| 9 | 70 | 0x4411 | 0x4411 |
| 10 | 71 | 0x9788 | 0x9788 |
| 11 | 72 | 0x3330 | 0x3330 |
| 12 | 128 | 0x4714 | 0x4714 |
| 13 | 129 | 0x8001 | 0x8001 |
| 14 | 171 | 0x1002 | 0x1002 |
| 15 | 175 | 0x0080 | 0x0080 |
| 16 | 176 | 0x00E6 | 0x00E6 |
| 17 | 177 | 0x0400 | 0x0400 |
| 18 | 192 | 0x000C | 0x000C |
| 19 | 193 | 0x4E00 | 0x2C00 |
| 20 | 194 | 0x02E4 | 0x02E4 |
| 21 | 197 | 0x0104 | 0x0104 |
| 22 | 199 | 0x0196 | 0x0174 |
| 23 | 200 | 0x0804 | 0x0804 |
| 24 | 201 | 0x00B1 | 0x0060 |
| 25 | 204 | 0x01E1 | 0x01E1 |
| 26 | 207 | 0x0000 | 0x0000 |
| 27 | 208 | 0xA100 | 0xA100 |
| 28 | 211 | 0x0E49 | 0x0E39 |
| 29 | 215 | 0x111F | 0x111F |
| 30 | 216 | 0x7F00 | 0x7F00 |
| 31 | 219 | 0x0020 | 0x0020 |
| 32 | 220 | 0x2434 | 0x2432 |
| 33 | 224 | 0x3E17 | 0x3E17 |

| Upload # | Address | P1−SN/SE/FN 10−bit mode with PLL (8 LVDS NZROT) | P3−SN/SE 10−bit mode with PLL (4 LVDS NZROT) |
|---|---|---|---|
| 34 | 227 | 0x0000 | 0x0000 |
| 35 | 250 | 0x2081 | 0x2081 |
| 36 | 256 | 0xA100 | 0xA100 |
| 37 | 257 | 0x0000 | 0x0000 |
| 38 | 258 | 0x07FF | 0x07FF |
| 39 | 384 | 0xC800 | 0xC800 |
| 40 | 385 | 0xFB1F | 0xFB1F |
| 41 | 386 | 0xFB1F | 0xFB1F |
| 42 | 387 | 0xFB12 | 0xFB12 |
| 43 | 388 | 0xF912 | 0xF912 |
| 44 | 389 | 0xF902 | 0xF902 |
| 45 | 390 | 0xF804 | 0xF804 |
| 46 | 391 | 0xF008 | 0xF008 |
| 47 | 392 | 0xF102 | 0xF102 |
| 48 | 393 | 0xF30F | 0xF30F |
| 49 | 394 | 0xF30F | 0xF30F |
| 50 | 395 | 0xF30F | 0xF30F |
| 51 | 396 | 0xF30F | 0xF30F |
| 52 | 397 | 0xF30F | 0xF30F |
| 53 | 398 | 0xF30F | 0xF30F |
| 54 | 399 | 0xF102 | 0xF102 |
| 55 | 400 | 0xF008 | 0xF008 |
| 56 | 401 | 0xF24A | 0xF24A |
| 57 | 402 | 0xF264 | 0xF264 |
| 58 | 403 | 0xF226 | 0xF226 |
| 59 | 404 | 0xF021 | 0xF021 |
| 60 | 405 | 0xF002 | 0xF002 |
| 61 | 406 | 0xF40A | 0xF40A |
| 62 | 407 | 0xF005 | 0xF005 |
| 63 | 408 | 0xF20F | 0xF20F |
| 64 | 409 | 0xF20F | 0xF20F |
| 65 | 410 | 0xF20F | 0xF20F |
| 66 | 411 | 0xF20F | 0xF20F |
| 67 | 412 | 0xF005 | 0xF005 |
| 68 | 413 | 0xEC05 | 0xEC05 |
| 69 | 414 | 0xC801 | 0xC801 |
| 70 | 415 | 0xC800 | 0xC800 |
| 71 | 416 | 0xC800 | 0xC800 |
| 72 | 417 | 0xCC0A | 0xCC0A |
| 73 | 418 | 0xC806 | 0xC806 |
| 74 | 419 | 0xC800 | 0xC800 |
| 75 | 420 | 0x0030 | 0x0030 |
| 76 | 421 | 0x2179 | 0x2175 |
| 77 | 422 | 0x2071 | 0x2071 |
| 78 | 423 | 0x0071 | 0x0071 |
| 79 | 424 | 0x107F | 0x107C |
| 80 | 425 | 0x1079 | 0x0071 |
| 81 | 426 | 0x0071 | 0x0031 |
| 82 | 427 | 0x0031 | 0x01B2 |
| 83 | 428 | 0x01B4 | 0x21B5 |
| 84 | 429 | 0x21B9 | 0x20B1 |
| 85 | 430 | 0x20B1 | 0x00B1 |
| 86 | 431 | 0x00B1 | 0x10BC |
| 87 | 432 | 0x10BF | 0x00B1 |
| 88 | 433 | 0x10B9 | 0x0030 |
| 89 | 434 | 0x00B1 | 0x0030 |
| 90 | 435 | 0x0030 | 0x2075 |
| 91 | 436 | 0x0030 | 0x2071 |
| 92 | 437 | 0x2079 | 0x0071 |
| 93 | 438 | 0x2071 | 0x107C |
| 94 | 439 | 0x0071 | 0x0071 |
| 95 | 440 | 0x107F | 0x0031 |
| 96 | 441 | 0x1079 | 0x01B2 |
| 97 | 442 | 0x0071 | 0x21B5 |
| 98 | 443 | 0x0031 | 0x20B1 |
| 99 | 444 | 0x01B4 | 0x00B1 |
| 100 | 445 | 0x21B9 | 0x10BC |
| 101 | 446 | 0x20B1 | 0x00B1 |
| 102 | 447 | 0x00B1 | 0x0030 |
| 103 | 448 | 0x10BF | |
| 104 | 449 | 0x10B9 | |
| 105 | 450 | 0x00B1 | |
| 106 | 451 | 0x0030 | |

NOTE: Register uploads for other supported operation modes can be accessed at the Image Sensor Portal on MyON.

### *Soft Power Up*

During the soft power up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power up uploads are listed in Table 9.

**Table 9. SOFT POWER UP REGISTER UPLOADS**

| Upload # | Address | Data | Description |
|---|---|---|---|
| **P1−SN/SE/FN, P3−SN/SE 10−bit mode with PLL (P1−SN/SE/FN in ZROT, P3−SN/SE in NZROT)** | | | |
| 1 | 10 | 0x0000 | Release soft reset state |
| 2 | 32 | 0x7007 | Enable analogue clock P1−SN/SE/FN only |
| | | 0x7017 | Enable analogue clock P3−SN/SE only |
| 3 | 64 | 0x0001 | Enable biasing clock |
| 4 | 40 | 0x0003 | Enable column multiplexer |
| 5 | 48 | 0x0001 | Enable AFE |
| 6 | 68 | 0x0085 | Enable LVDS bias |
| 7 | 72 | 0x3337 | Enable charge pump |
| 8 | 112 | 0x0007 | Enable LVDS transmitters |

### *Enable Sequencer*

During the ‘Enable Sequencer’ action, the frame grabbing sequencer is enabled. The sensor starts grabbing images in the configured operation mode. Refer to Sensor States on page 15.

The ‘Enable Sequencer’ action consists of a set of register uploads. The required uploads are listed in Table 10.

**Table 10. ENABLE SEQUENCER REGISTER UPLOADS**

| Upload # | Address | Data |
|---|---|---|
| 1 | 192 | 0x080D |

## User Actions: Functional Modes to Power Down Sequences

### *Disable Sequencer*

During the ‘Disable Sequencer’ action, the frame grabbing sequencer is stopped. The sensor stops grabbing images and returns to the idle mode.

The ‘Disable Sequencer’ action consists of a set of register uploads. as listed in Table 11.

**Table 11. DISABLE SEQUENCER REGISTER UPLOAD**

| Upload # | Address | Data |
|---|---|---|
| 1 | 192 | 0x080C |

### *Soft Power Down*

During the soft power down action, the internal blocks are disabled and the sensor is put in standby state to reduce the current dissipation. This action exists of a set of SPI uploads. The soft power down uploads are listed in Table 12.

**Table 12. SOFT POWER DOWN REGISTER UPLOADS**

| Upload # | Address | Data | Description |
|---|---|---|---|
| **P1−SN/SE/FN, P3−SN/SE 10−bit mode with PLL (P1−SN/SE/FN in ZROT, P3−SN/SE in NZROT)** | | | |
| 1 | 112 | 0x0000 | Disable LVDS transmitters |
| 2 | 72 | 0x3330 | Disable charge pump |
| 3 | 48 | 0x0000 | Disable AFE |
| 4 | 40 | 0x0000 | Disable column multiplexer |
| 5 | 64 | 0x0000 | Disable biasing clock |
| 6 | 32 | 0x7006 | Disable analogue clock P1−SN/SE/FN only |
| | | 0x7016 | Disable analogue clock P3−SN/SE only |
| 7 | 10 | 0x0999 | Soft reset |

### *Disable Clock Management – Part 2*

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 13.

**Table 13. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2**

| Upload # | Address | Data | Description |
|---|---|---|---|
| **P1−SN/SE/FN, P3−SN/SE 10−bit mode with PLL** | | | |
| 1 | 32 | 0x7004 | Disable logic clock P1−SN/SE/FN only |
| | | 0x7014 | Disable logic clock P3−SN/SE only |
| 2 | 34 | 0x0000 | Disable logic blocks |
| 3 | 9 | 0x0009 | Soft reset clock generator |

### *Disable Clock Management – Part 1*

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 14.

**Table 14. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 1**

| Upload # | Address | Data | Description |
|---|---|---|---|
| **P1−SN/SE/FN, P3−SN/SE 10−bit mode with PLL** | | | |
| 1 | 8 | 0x0099 | Soft reset PLL |
| 2 | 16 | 0x0000 | Disable PLL |

### *Power Down Sequence*

Figure 17 illustrates the timing diagram of the preferred power down sequence. It is important that the sensor is in reset before the clock input stops running. Otherwise, the internal PLL becomes unstable and the sensor gets into an unknown state. This can cause high peak currents.

The same applies for the ramp down of the power supplies. The preferred order to ramp down the supplies is first vdd_pix, second vdd_33, and finally vdd_18. Any other sequence can cause high peak currents.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

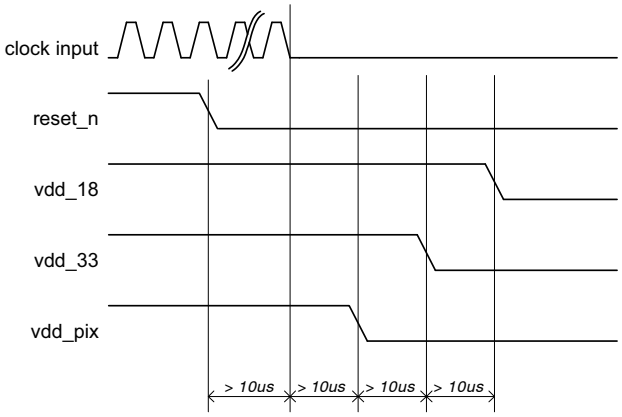



**Figure 17. Power Down Sequence**

### Sensor Reconfiguration

During the standby, idle, or running state several sensor parameters can be reconfigured.

- Frame Rate and Exposure Time: Frame rate and exposure time changes can occur during standby, idle, and running states by modifying registers 199 to 203. Refer to page 30−32 for more information.
- Signal Path Gain: Signal path gain changes can occur during standby, idle, and running states by modifying registers 204/205. Refer to page 37 for more information.
- Windowing: Changes with respect to windowing can occur during standby, idle, and running states. Refer to Multiple Window Readout on page 28 for more information.
- Subsampling: Changes of the subsampling mode can occur during standby, idle, and running states by modifying register 192. Refer to Subsampling on page 29 for more information.
- Shutter Mode: The shutter mode can only be changed during standby or idle mode by modifying register 192. Reconfiguring the shutter mode during running state is not supported.

### Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

#### *Static Readout Parameters*

Some registers are only modified when the sensor is not acquiring images. reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 15 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

**Table 15. STATIC READOUT PARAMETERS**

| Group | Addresses | Description |
|---|---|---|
| Clock generator | 32 | Configure according to recommendation |
| Image core | 40 | Configure according to recommendation |
| AFE | 48 | Configure according to recommendation |
| Bias | 64–71 | Configure according to recommendation |
| Charge Pump | 72 | Configure according to recommendation |
| LVDS | 112 | Configure according to recommendation |
| Sequencer mode selection | 192 [6:1] | Operation modes are: • triggered_mode<br>• slave_mode |
| All reserved registers | | Keep reserved registers to their default state, unless otherwise described in the recommendation |

#### *Dynamic Configuration Potentially Causing Image Artifacts*

The category of registers as shown in Table 16 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the reconfiguration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed.

The effect is transient in nature and the new configuration is applied after the transient effect.

**Table 16. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS**

| Group | Addresses | Description |
|---|---|---|
| Black level configuration | 128–129<br>197[12:8] | Reconfiguration of these registers may have an impact on the black−level calibration algorithm. The effect is a transient number of images with incorrect black level compensation. |
| Sync codes | 129[13]<br>116–126 | Incorrect sync codes may be generated during the frame in which these registers are modified. |
| Datablock test configurations | 144, 146–150 | Modification of these registers may generate incorrect test patterns during a transient frame. |

### *Dynamic Readout Parameters*

It is possible to reconfigure the sensor while it is acquiring images. Frame related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 17. Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

**Table 17. DYNAMIC READOUT PARAMETERS**

| Group | Addresses | Description |
|---|---|---|
| Subsampling/binning | 192[7]<br>192[8] | Subsampling or binning is synchronized to a new frame start. |
| ROI configuration | 195<br>256–303 | A ROI switch is only detected when a new window is selected as the active window (reconfiguration of register 195). reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image. |
| Exposure reconfiguration | 199–203 | Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to '1' in triggered global mode (master). |
| Gain reconfiguration | 204 | Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] – gain_lat_comp). |

### *Freezing Active Configurations*

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re−enable the synchronization. The sensor's sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 18 shows a reconfiguration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

Figure 19 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is de−asserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

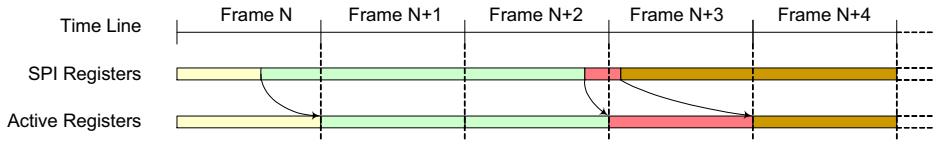



**Figure 18. Frame Synchronization of Configurations (no freezing)**

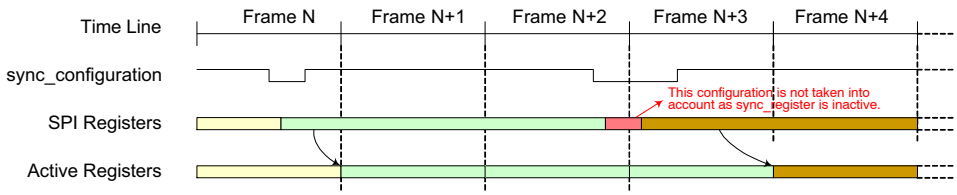



**Figure 19. reconfiguration Using Sync_configuration**

NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 18 lists the several sync_configuration possibilities along with the respective registers being frozen.

**Table 18. ALTERNATE SYNC CONFIGURATIONS**

| Group | Affected Registers | Description |
|---|---|---|
| sync_black_lines | black_lines | Update of black line configuration is not synchronized at start of frame when ‘0’.<br>The sensor continues with its previous configurations. |
| sync_exposure | mult_timer<br>fr_length<br>exposure | Update of exposure configurations is not synchronized at start of frame when ‘0’.<br>The sensor continues with its previous configurations. |
| sync_gain | mux_gainsw<br>afe_gain | Update of gain configurations is not synchronized at start of frame when ‘0’.<br>The sensor continues with its previous configurations. |
| sync_roi | roi_active0[15:0]<br>subsampling<br>binning | Update of active ROI configurations is not synchronized at start of frame when ‘0’.<br>The sensor continues with its previous configurations.<br>**Note:** The window configurations themselves are not frozen. reconfiguration of active windows is not gated by this setting. |

## Window Configuration

### *Global Shutter Mode*

Up to 16 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 303. Each window can be activated or deactivated separately using register 195. It is possible to reconfigure the inactive windows while the sensor is acquiring images.

Switching between predefined windows is achieved by activation of the respective windows. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is tracked. Switching between the two modes only requires an upload of one register.

### *Black Calibration*

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to ‘0’. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to ‘0’ when setting the black level target to ‘0’.

The black level is calibrated for the 16 columns contained in one kernel. This implies 16 black level offsets are generated and applied to the corresponding columns. Configurable parameters for the black−level algorithm are listed in Table 19.

**Table 19. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM**

| Address | Register Name | Description |
|---|---|---|
| **Black Line Generation** | | |
| 197[7:0] | black_lines | This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 255.<br>**Note:** When the automatic black−level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black−level filtering.<br>The number of black pixels generated per line is dependent on the operation mode and window configurations:<br>Each black line contains 162 kernels. |
| 197[12:8] | gate_first_line | A number of black lines are blanked out when a value different from 0 is configured. These blanked out lines are not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm. |
| **Black Value Filtering** | | |
| 129[0] | auto_blackcal_enable | Internal black−level calibration functionality is enabled when set to ‘1’. Required black level offset compensation is calculated on the black samples and applied to all image pixels.<br>When set to ‘0’, the automatic black−level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1].<br>**Note:** Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations. |
| 129[9:1] | blackcal_offset | Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to ‘0’. The sign of the offset is determined by register 129[10] (blackcal_offset_dec).<br>**Note:** All channels use the same offset compensation when automatic black calibration is disabled. |
| 129[10] | blackcal_offset_dec | Sign of blackcal_offset. If set to ‘0’, the black calibration offset is added to each pixel. If set to ‘1’, the black calibration offset is subtracted from each pixel.<br>This register is not used when auto_blackcal_enable is set to ‘1’. |

**Table 19. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM**

| Address | Register Name | Description |
|---|---|---|
| **Black Line Generation** | | |
| 128[10:8] | black_samples | The black samples are low−pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate.<br>The effective number of samples taken into account for filtering is 2^ black_samples.<br>**Note:** An error is reported by the device if more samples than available are requested (refer to register 136). |
| **Black Level Filtering Monitoring** | | |
| 136 | blackcal_error0 | An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation:<br>• Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197).<br>• Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128).<br>• Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift. |

NOTE: The maximum number of samples taken into account for black level statistics is half the number of kernels.

### Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor's system clock. When the master wants to write or read a sensor's register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 20 shows the communication protocol for read and write accesses of the SPI registers. The PYTHON sensor uses 9−bit addresses and 16−bit data words.

Data driven by the system is colored blue in Figure 16, while data driven by the sensor is colored yellow. The data in grey indicates high−Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

1. Select the sensor for read or write by pulling down the ss_n line.
2. One SPI clock cycle after selecting the sensor, the 9−bit address is transferred, most significant bit first. The sck clock is passed through to the sensor as indicated in Figure 20. The sensor samples this address data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock).
3. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
4. Data transmission:
   - For write commands, the master continues sending the 16−bit data, most significant bit first.
   - For read commands, the sensor returns the data on the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
5. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Note that the maximum frequency for the SPI interface scales with the input clock frequency, bit depth and LVDS output multiplexing as described in Table 5.

Consecutive SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

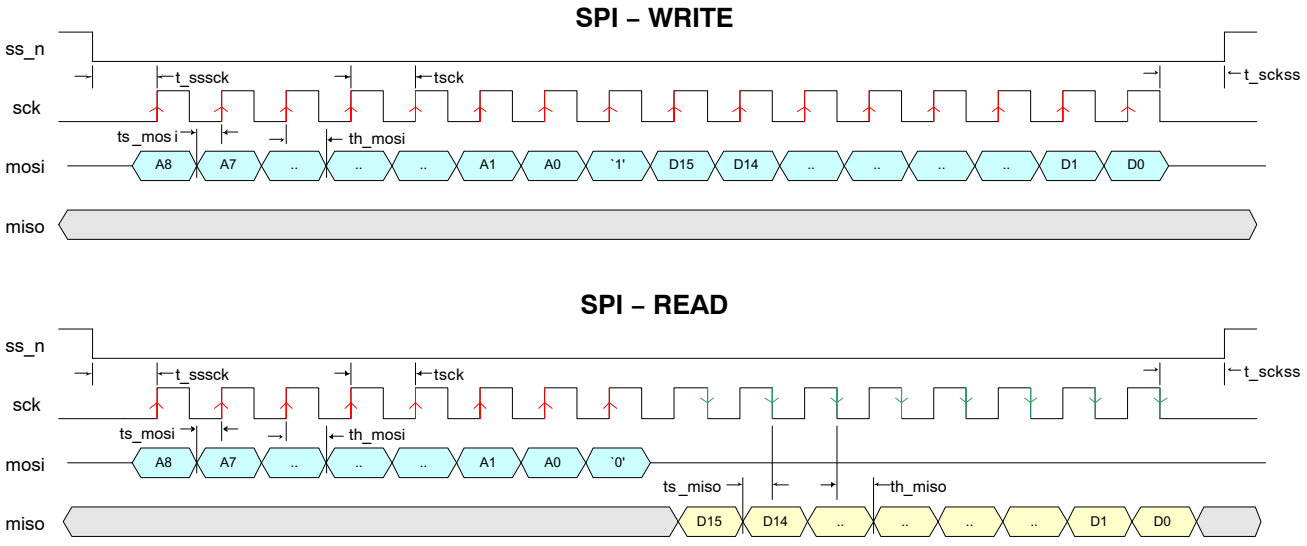



**Figure 20. SPI Read and Write Timing Diagram**

**Table 20. SPI TIMING REQUIREMENTS**

| Group | Addresses | Description | Units |
|---|---|---|---|
| tsck | sck clock period | 100 (*) | ns |
| tsssck | ss_n low to sck rising edge | tsck | ns |
| tsckss | sck falling edge to ss_n high | tsck | ns |
| ts_mosi | Required setup time for mosi | 20 | ns |
| th_mosi | Required hold time for mosi | 20 | ns |
| ts_miso | Setup time for miso | tsck/2−10 | ns |
| th_miso | Hold time for miso | tsck/2−20 | ns |
| tspi | Minimal time between two consecutive SPI accesses (not shown in figure) | 2 x tsck | ns |

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as $1/f_{SPI}$. See text for more information on SPI clock frequency restrictions.