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NOIV1SN025KA

VITA 25K Image Sensor

ON Semiconductor®

www.onsemi.com

Features

- 5120 x 5120 Active Pixels
- 4.5 μm x 4.5 μm Square Pixels
- 35 mm Optical Format
- Monochrome (SN) or Color (SE)
- 53 Frames per Second (fps) at Full Resolution
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 32 Low-voltage Differential Signaling (LVDS) High-speed Serial Outputs
- Random Programmable Region of Interest (ROI) Readout
- Pipelined and Triggered Global Shutter, Rolling Shutter
- On-chip Fixed Pattern Noise (FPN) Correction
- Serial Peripheral Interface (SPI)
- Operational Range: −40°C to +85°C
- 355-pin μPGA Package
- 3.4 W Power Dissipation
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Machine Vision
- Motion Monitoring
- Intelligent Traffic Systems (ITS)
- Pick and Place Machines
- Inspection
- Metrology

Figure 1. VITA 25K Photograph

Description

The VITA 25K is a 5120 x 5120 CMOS image sensor delivering high resolution images at frame rates up to 53 frames per second. The high sensitivity 4.5 μm x 4.5 μm pixels support pipelined and triggered global shutter readout modes and can also be operated in a low noise rolling shutter mode. In rolling shutter mode, the sensor supports correlated double sampling readout, reducing noise and increasing the dynamic range.

The sensor has on-chip programmable gain amplifiers and 10-bit A/D converters. The image's black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to 32 regions can be programmed, achieving even higher frame rates.

The image data interface consists of 32 LVDS lanes. Each channel runs at 620 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receive end.

The VITA 25K is packaged in a ceramic 355-pin μPGA package and is available in a monochrome, color and windowless versions.

Contact your local ON Semiconductor office for more information.

ORDERING INFORMATION

Part Number	Family	Description	Package	Product Status
NOIV1SN025KA−GDC	VITA 25K	25 MegaPixel, Monochrome, no Protective Tape	355−pin μPGA	Production
NOIV1SE025KA−GDC		25 MegaPixel, Color, no Protective Tape		
NOIV1SN025KA−GWC		25 MegaPixel, Monochrome, Windowless		
NOIV1SE025KA−GWC		25 MegaPixel, Color, Windowless		
NOIV1SN025KA−GTI		25 MegaPixel, Monochrome, Protective Tape		
NOIV1SE025KA−GTI		25 MegaPixel, Color, Protective Tape		

The V1 − SN/SE base part is used to reference the mono and color enhanced versions of the LVDS interface. More details on the part number coding can be found at http://www.onsemi.com/pub_link/Collateral/TND310−D.PDF

Package Mark

Following is the VITA 25K production package mark:

Side 1 near Pin 1: **NOIV1S * 025KA−GDC**, where N = mono micro lens, E = color micro lens

Side 2: **AWLYYWW, NNNN** where AWLYYWW is the lot traceability, and NNNN is the serial number

Windowless Devices

The windowless devices are assembled in the same package as the windowed devices with the exception that the windowless devices are delivered with the glass lid (referenced in Figure 37 and Figure 39), *taped on* to the package. The glass lid is taped to the package in a clean room environment, soon after the wire bonding process, to maintain silicon integrity and wire dressing. The windowless devices are tested according to the Standard Acceptance Criteria and are electro optically identical to production devices WITH GLASS LID. Please note the RMA policy on Page 73 for windowless devices.

Please contact your local sales office for entering a windowless order.

CONTENTS

SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	Specification
Active pixels	5120 (H) x 5120 (V)
Pixel size	4.5 μm x 4.5 μm
Pixel type	Global shutter pixel architecture
Shutter type	Pipelined and triggered global shutter, rolling shutter
Master clock	310 MHz (10-bit) 248 MHz (8-bit)
Windowing features	32 Randomly programmable windows. Normal, sub-sampled and binned readout modes
ADC resolution	10-bit, 8-bit
Number of LVDS outputs	32 data + 1 sync + 1 clock
Data rate	32 x 620 Mbps (10-bit) 32 x 496 Mbps (8-bit)
Power dissipation	3.4 W
Package type	355 μPGA
Color	RGB color, mono

Table 2. ELECTRO−OPTICAL SPECIFICATIONS [1]

Parameter	Specification
Frame rate	53 fps at full resolution
Optical format	35 mm
Conversion gain	0.0644 LSB10/e^- , 81.5 μV/e^-
Dark noise	2.13 LSB10, 34e^- in global shutter 1.42 LSB10, 23e^- in rolling shutter
Responsivity at 550 nm	18 LSB10 /nJ/cm^2, 3.4 V/lux.s
Parasitic Light Sensitivity (PLS)	<1/900 at 550 nm
Full well charge	22000 e^-
Quantum efficiency (QE) x FF	50% at 550 nm
Pixel FPN	0.5% of RMS of maximum swing rolling shutter: 1.0 LSB10 global shutter: 2.0 LSB10
Row FPN	rolling & global shutter: 0.2 LSB10
Column FPN	rolling & global shutter: 1.0 LSB10
Dynamic range	56.2 dB in global shutter mode 59.6 dB in rolling shutter mode
Signal-to-Noise Ratio (SNR)	43.4 dB in global and rolling shutter mode
Dark signal	14 e^-/s, 0.9 LSB10/s at +30°C

Table 3. RECOMMENDED OPERATING RATINGS (Note 2)

Symbol	Description	Min	Max	Units
T_J	Operating temperature range	−40	+85	°C

Table 4. ABSOLUTE MAXIMUM RATINGS (Note 3)

Symbol	Parameter	Min	Max	Units
ABS (1.0 V supply)	ABS rating for 1.0 V supply	−0.5	1.2	V
ABS (1.8 V supply group)	ABS rating for 1.8 V supply group	−0.5	2.2	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	−0.5	4.3	V
ABS (4.2 V supply)	ABS rating for 4.2 V supply	−0.5	4.6	V
ABS (4.5 V supply)	ABS rating for 4.5 V supply	−0.5	5.0	V
T_S (Notes 3 and 4)	ABS storage temperature range	0	150	°C
	ABS storage humidity range at 85°C		85	%RH
Electrostatic discharge (ESD) (Notes 2 and 3)	Human Body Model (HBM): JS−001−2010	2000		V
	Charged Device Model (CDM): JESD22−C101	500		
LU	Latch-up: JESD−78	140		mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The ADC is 11-bit, down-scaled to 10-bit. The VITA 25K uses a larger word-length internally to provide 10-bit on the output.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
4. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

Electrical Specifications

Power Supply Ratings

Table 5. POWER SUPPLY RATINGS

Limits in bold apply for for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C [5], [6], [7], [8]

Parameter	Description	Min	Typ	Max	Units
Power Supply Parameters					
vdda_33	Analog supply - 3.3 V domain. gnda_33 is connected to substrate	**3**	3.3	**3.6**	V
Idda_33	Current consumption from analog supply	675	725	775	mA
vddd_33	Digital supply - 3.3 V domain. gndd_33 is connected to substrate	**3**	3.3	**3.6**	V
Iddd_33	Current consumption from 3.3 V digital supply	65	85	105	mA
vdd_18	Digital supply - 1.8 V domain. gndd_18 is connected to substrate	**1.6**	1.8	**2**	V
Idd_18	Current consumption 1.8 V digital supply	240	310	380	mA
vdd_pix	Pixel array supply	**3**	3.3	**3.6**	V
Idd_pix	Current consumption from pixel supply	25	35	45	mA
vdd_resfd	Floating diffusion reset supply	3.3	4.5	4.6	V
gnd_resfd	Floating diffusion reset ground. Not connected to substrate	0	0	1.0	V
vdd_respd	Photo diode reset supply	3.3	4.2	4.6	V
gnd_respd	Photo diode reset ground. Not connected to substrate. **Note** This is a sinking power supply with 200 mA range.	0	0	1.0	V
vdd_trans	Pixel transfer supply	3.3	4.2	4.6	V
gnd_trans	Pixel transfer ground. Not connected to substrate	0	0	1.0	V
vdd_sel	Pixel select supply	3.0	3.3	3.6	V
gnd_sel	Pixel select ground. Not connected to substrate.	0	0	0	V
vdd_casc	Cascode supply	0.9	1.0	1.1	V
vref_colmux [8]	Column multiplexer reference supply	–	1.0	–	V
gnd_colbias	Column biasing ground. Dedicated ground signal for pixel biasing. Connected to substrate	–	0	–	V
gnd_colpc	Column precharge ground. Dedicated ground signal for pixel biasing. Not connected to substrate	–	0	–	V
Ptot	Total power consumption	3000	3400	3800	mW
Pstby	Power consumption in standby mode	–	–	50	mW
Popt	Power consumption at lower pixel rates		Configurable		
I/O - LVDS (EIA/TIA-644): Conforming to standard/additional specifications and deviations listed					
fserdata	Data rate on data channels in 10-bit mode DDR signaling - 32 data channels, 1 synchronization channel			620	Mbps
fserdata	Data rate on data channels in 8-bit mode DDR signaling - 32 data channels, 1 synchronization channel			496	Mbps
fserclock	Clock rate of output clock in 10-bit mode Clock output for mesochronous signaling			310	MHz
fserclock	Clock rate of output clock in 8-bit mode Clock output for mesochronous signaling			248	MHz
Vicm	LVDS input common mode level	0.3	1.25	2.2	V
Tccsk	Channel to channel skew (training pattern allows per-channel skew correction)			50	ps
LVDS Electrical/Interface					
fin	Input clock rate for 10-bit mode			310	MHz
fin	Input clock rate for 8-bit mode			248	MHz

Table 5. POWER SUPPLY RATINGS

Limits in bold apply for for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C [5], [6], [7], [8]

Parameter	Description	Min	Typ	Max	Units
tidc	Input clock duty cycle	40	50	60	%
tj	Input clock jitter		20		ps
fspi	SPI clock rate			10	MHz
ratspi	10-bit: ratio: Fin/fspi	30			
	8-bit: ratio: Fin/fspi	24			
Sensor Requirements					
fps	Frame rate at full resolution (global shutter)			53	fps
fps_roi1	Xres x Yres = 1920 x 1080			440	fps
fps_roi2	Xres x Yres = 1024 x 1024			590	fps
fps_roi3	Xres x Yres = 640 x 480			1380	fps
fps_roi4	Xres x Yres = 512 x 512			1360	fps
fps_roi5	Xres x Yres = 256 x 256			2750	fps
FOT	Frame overhead time		50		µs
ROT	Row overhead time		1		µs
fpix	Pixel rate (32 channels at 62 Mpix/s)			1984	Mpix/s

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high−impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Vref_colmux supply should be able to source and sink current

Disclaimer: Image sensor products and specifications are subject to change without notice. Products are warranted to meet the production data sheet and acceptance criteria specifications only.

Power Distribution Network

A power distribution network (PDN) is designed to ensure proper power management to the VITA 25K sensor. Table 6 provides the recommended power supplies for the VITA 25K power management. Please refer to the AN65466 for recommended linear regulator selection, decoupling capacitor network and BOM for the power distribution network.

Table 6. RECOMMENDED POWER SUPPLIES FOR VITA 25K

Category	Power Supply	Source/Sink Stage	Min Rating (V)	Typ Rating (V)	Max Rating (V)	Max DC Current (mA)	Peak Currents at Allowable pk−pk Ripples
Digital	VDDD_18	Sourcing	1.6	1.8	2	380	2 A at 200 mV
	VDDD_33	Sourcing	3	3.3	3.6	105	0.6 A at 200 mV
	VDD_sel	Sourcing	3	3.3	3.6	0	1 mA at 20 mV
Analog	VDDA_33	Sourcing	3	3.3	3.6	775	1.5 A at 50 mV
	VDD_pix	Sourcing	3	3.3	3.6	45	700 mA at 100 mV
	VDD_respd	Sourcing	3.3	4.2	4.6	7	300 mA at 20 mV
	VDD_trans	Sourcing	3.3	4.2	4.6	7	
	VDD_resfd	Sourcing	3.3	4.5	4.6	7	
	VDD_casc	Sourcing	0.9	1	1.1	0	6 mA at 300 mV
	Vref_colmux	Sourcing & Sinking		1		0	0.35 A at 0.5 mV
	gnd_respd	Sinking	0	0	1	30 mA sinking at 0.4 V	200 mA at 20 mV

9. Combining power supplies:
   - VDD_sel can be combined with either VDDD_33 or VDDA_33
   - VDD_respd and VDD_trans can be grouped together as VDD_42
   - gnd_respd is be designed to be a 7 mA sinking supply, but can be tied to ground with no impact to image quality

Color Filter Array

The VITA 25K color sensor is processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left. Green1 and green2 have a slightly different spectral response due to (optical) cross talk from neighboring pixels. Green1 pixels are located on a green-red row, green2 pixels are located on a blue-green row.

Figure 3 depicts the spectral response for the mono and color devices. Figure 4 shows the photovoltaic response for the VITA 25K.

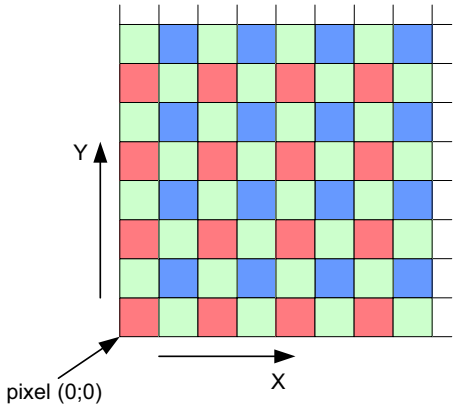

Figure 2. Color Filter Array for the Pixel Array

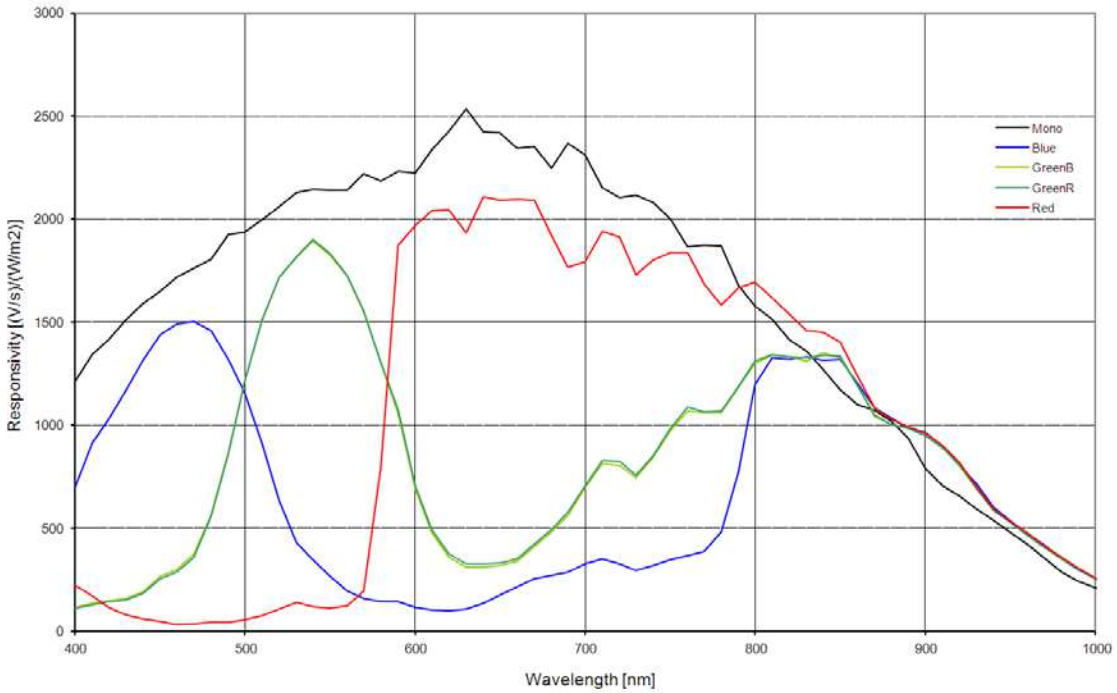

Figure 3. Mono and Color Spectral Response with Micro Lens

Note that green pixels on a Green−Red (Green 1) and Green−Blue (Green 2) row have similar responsivity to wavelength trend as is depicted by the legend “Green”.

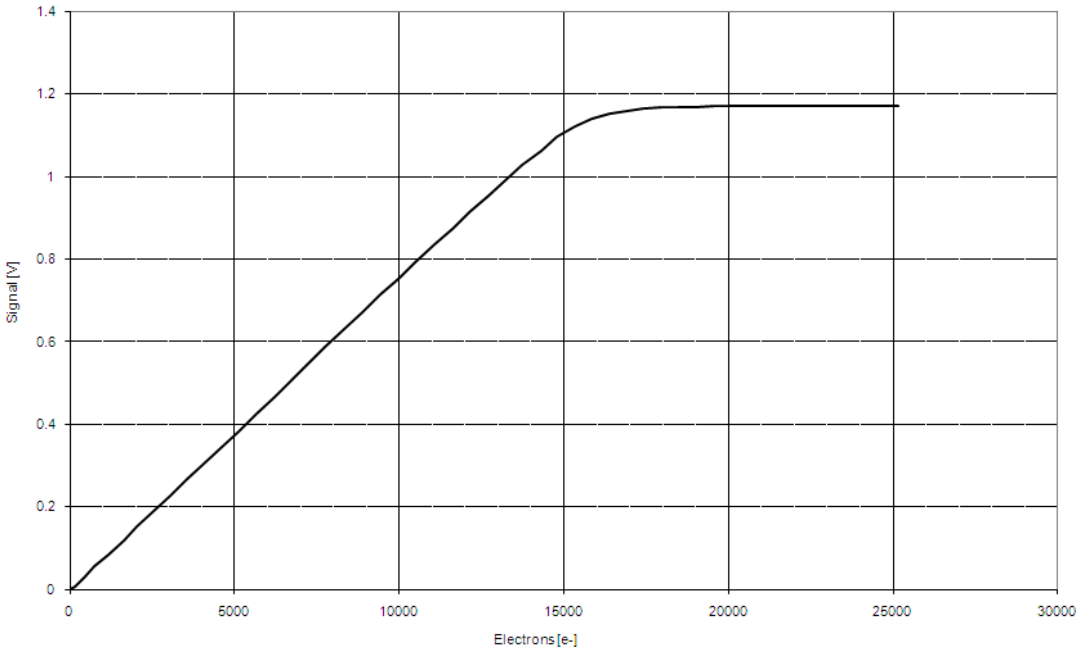

Figure 4. Typical Photovoltaic Response

OVERVIEW

Figure 5 gives an overview of all functional blocks in the image sensor. The system clock is received by the LVDS clock receiver block and distributed to other blocks. The sequencer defines the sensor timing and controls the image core. The sequencer is started either autonomously (master mode) or on assertion of an external trigger (slave mode). The image core contains all pixels and readout circuits. The column structure selects pixels for readout and performs correlated double sampling (CDS) or double sampling (DS). The data comes out sequentially and is fed into the analog front end (AFE) block. The programmable gain amplifier (PGA) of the AFE adds the offset and gain. The output is a fully differential analog signal that goes to the ADC, where the analog signal is converted to a 10-bit data stream. Depending on the operating mode, eight or ten bits are fed into the data formatting block. This block adds synchronization information to the data stream based on the frame timing. The data then goes to the low voltage serial (LVDS) interface block that sends the data out through the I/O ring.

On-chip programmability is controlled through the Serial Peripheral Interface (SPI). See Register Map on page 43 for register details. A bias block generates bias currents and voltages for all analog blocks on the chip. By controlling the bias current, the speed-versus-power of each block can be tuned. All biasing programmability is contained in the bias block.

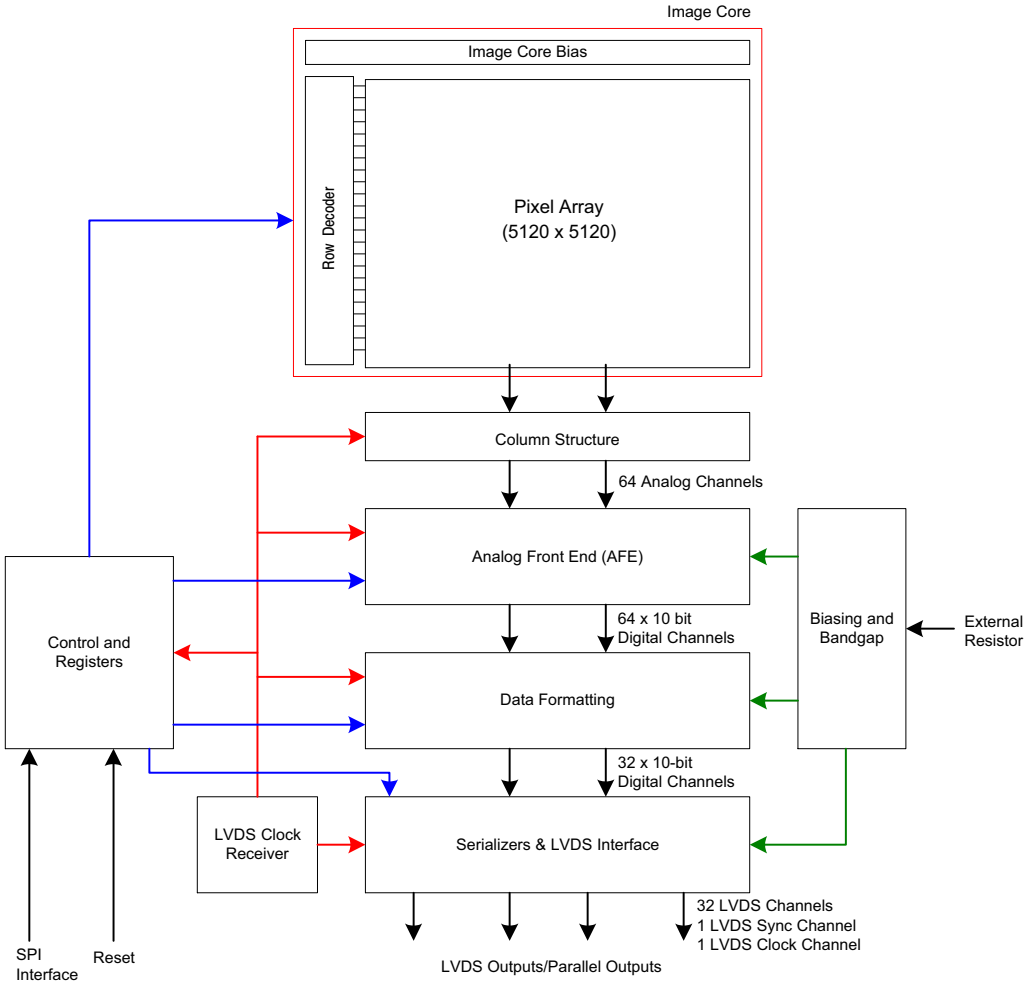

Figure 5. Block Diagram

Image Core

The image core consists of:

- Pixel array
- Address decoders and row drivers
- Pixel biasing

The pixel array contains 5120 x 5120 readable pixels with a pixel pitch of 4.5 μm. Four dummy pixel rows and columns are placed at every side of the pixel array to eliminate possible edge effects. The sensor uses a 5T pixel architecture, which makes it possible to read out the pixel

array in global shutter mode with DS, or rolling shutter mode with CDS.

The function of the row drivers is to access the image array line by line, or all lines together, to reset or read the pixel data. The row drivers are controlled by the on-chip sequencer and can access the pixel array in global and rolling shutter modes.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

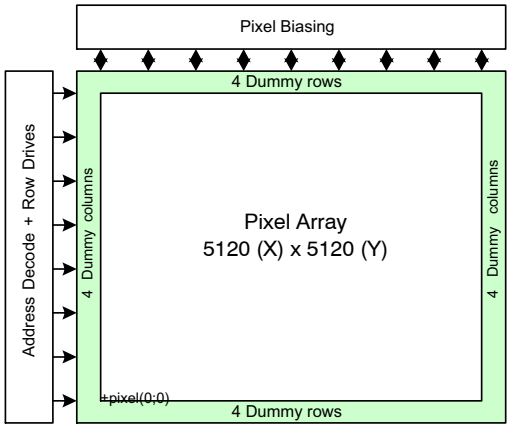

Figure 6. Image Core Diagram

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 310 MHz in 10-bit mode and 248 MHz in 8-bit mode. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

The 5120 pixels of one image row are stored in 5120 column sample-and-hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 64 parallel differential outputs operating at a frequency of 31 MHz.

At this stage, the reset signal and integrated signal values are transferred into an FPN-corrected differential signal. A programmable gain of 1x, 2x, or 4x can be applied to the signal at this stage. The column multiplexer also supports a subsampled readout mode (read-1-skip-1 for mono and read-2-skip-2 for color version). Enabling this mode can speed up the frame rate, with a decrease in resolution.

Bias Generator

The bias generator generates all required reference voltages and bias currents that the on-chip blocks use. An external resistor of 47 kΩ, connected between the pins *ibias_master* and *gnda_33* is required for the bias generator to operate properly.

Analog Front End

The AFE contains 64 channels, each containing a PGA and a 10-bit ADC. The PGA can be programmed to apply a gain of 1x, 1.39x, 1.94x, and 2.72x to the image signal. Together with the gain applied in the column multiplexer, a total signal gain of 10x can be achieved.

For each of the 64 channels, a pipelined 10-bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one LVDS block. A cyclic redundancy check (CRC) code is calculated on the passing data. For each LVDS output channel, one data block is instantiated. An extra data block is foreseen to transmit synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface

The serializer and LVDS interface block receives the formatted (10-bit or 8-bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

In 10-bit mode, the maximum output data bit rate is 620 Mbps per channel. In 8-bit mode, the maximum output data bit rate is 496 Mbps per channel.

In addition to the 32 LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system-level image reconstruction.

Sequencer

The sequencer is responsible for the following tasks:

- Controls the image core. Starts and stops integration in rolling and global shutter modes and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

OPERATING MODES

This sensor supports multiple operation modes. The following list provides an overview.

- Global Shutter mode
  - ♦ Pipelined global shutter mode
    - Master mode
    - Slave mode
  - ♦ Triggered global shutter
    - Master mode
    - Slave mode
- Rolling shutter mode
- Multiple windowing readout
  - ♦ Flexible window configuration
  - ♦ Processing multiple windows in Global Shutter mode
- Subsampling and binning
  - ♦ Pixel binning
  - ♦ Subsampling

Global Shutter Mode

In a global shutter mode, light integration takes place on all pixels in sync, although subsequent readout is sequential, as shown in Figure 7. Figure 8 shows the integration and readout sequence for the global shutter. All pixels are light sensitive at the same time. The whole pixel core is reset simultaneously and, after the integration time, all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. The integration and readout can occur in parallel or sequentially.

The integration starts at a certain period, relative to the frame start.

Pipelined Global Shutter Mode

In pipelined shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N–1. The readout of every frame starts with a frame overhead time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by the row overhead time (ROT).

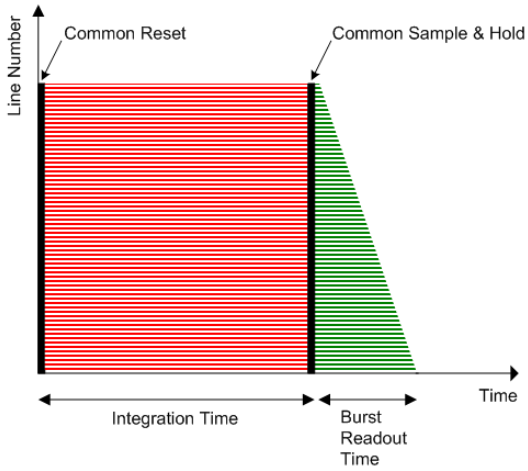

Figure 7. Global Shutter Operation

Master Mode

In this operation mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

Slave Mode

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins.

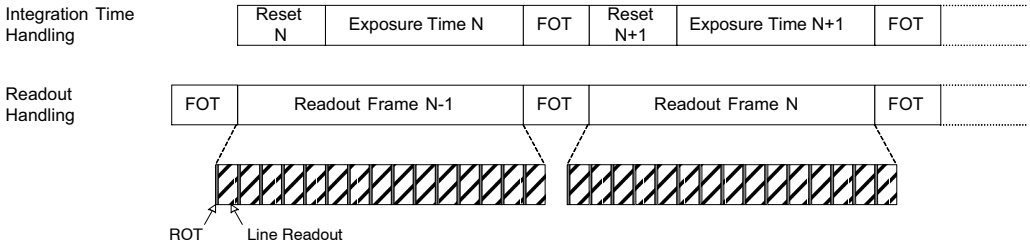

Figure 8. Integration and Readout for Pipelined Shutter

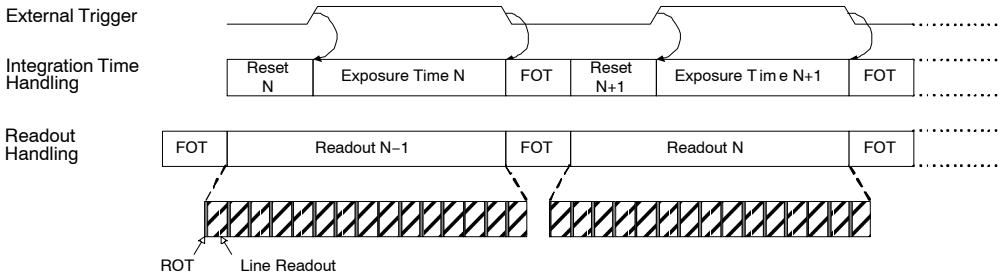

Figure 9. Pipelined Shutter Operated in Slave Mode

Triggered Global Shutter

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences from the pipelined shutter master mode are:

- Upon user action, a single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is user-controlled through an external pin.

The triggered global mode can also be controlled in a master or in a slave mode.

Master Mode

As shown in Figure 10, in the master mode a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is read out sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge.

Slave Mode

Integration time control is identical to the pipelined shutter slave mode, in which both integration time and readout requests are controlled by an external trigger. An external synchronization pin controls the start of integration. The moment it is deasserted, the FOT starts. At this time, the analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

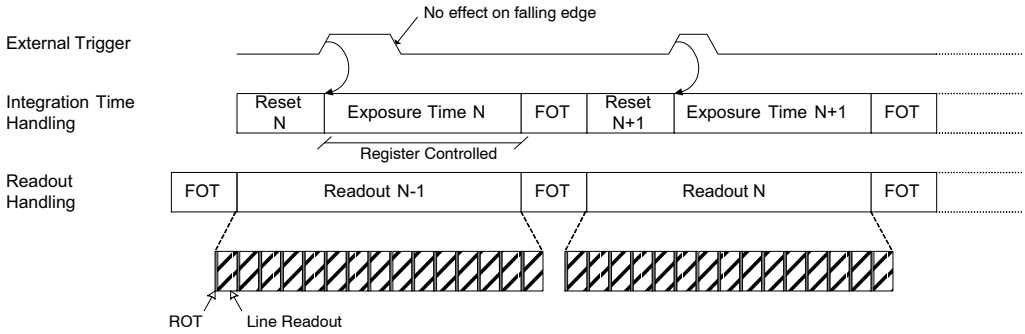

Figure 10. Triggered Shutter Operated in Master Mode

Rolling Shutter Mode

The sensor also supports the rolling shutter mode. The shutter mechanism is an electronic rolling shutter and the sensor operates in streaming mode similar to a video. This mechanism is controlled by the on-chip sequencer logic. There are two Y pointers, as indicated in Figure 11. One of them points to the row that is to be reset for rolling shutter operation and the other points to the row to be read out. Functionally, a row is reset first and selected for readout later. The time elapsed between these two operations is the exposure time.

Figure 11 schematically indicates the relative shift of the integration times of different lines during rolling shutter operation. Each row is read and reset sequentially, as described in the previous paragraph. Each row in a particular frame is integrated for the same time, but all lines in a frame 'see' a different stare time. Therefore, fast horizontal moving objects in the field of view give rise to motion artifacts in the image; this is an unavoidable property of a rolling shutter.

In rolling shutter mode, a second pointer indicates the rows that need to be reset for the rolling shutter mechanism. The distance between the reset pointer and the readout pointer determines the integration time.

The VITA 25K supports dynamic exposure time updates without artifacts or interrupting the image data stream.

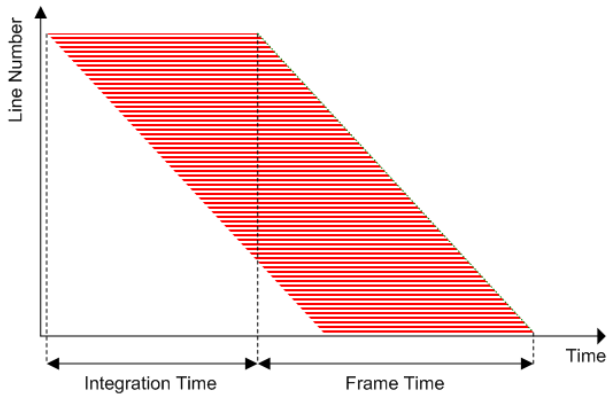

Figure 11. Rolling Shutter Operation

SENSOR OPERATION

Operation Flowchart

Figure 12 shows the flow chart diagram of the sensor operation. The sensor can be in five different ‘states’. Every state is indicated with the oval circle. These states are:

- Power-Off
- Standby (1)
- Standby (2)
- Idle
- Running

The states above are ordered by power dissipation. Clearly, in ‘power-off’ state the power dissipation will be minimal; in ‘running’ state the power dissipation will be maximal.

On the other hand, the lower the power consumption, the more actions (and time) are required to put the sensor in ‘running’ state and grabbing images.

This flowchart provides the trade-offs between power saving and enabling time of the sensor.

Next to the ‘states’ a set of ‘user actions’, indicated by arrows, are included in the flow chart diagram. These user actions make it possible to move from one state to another.

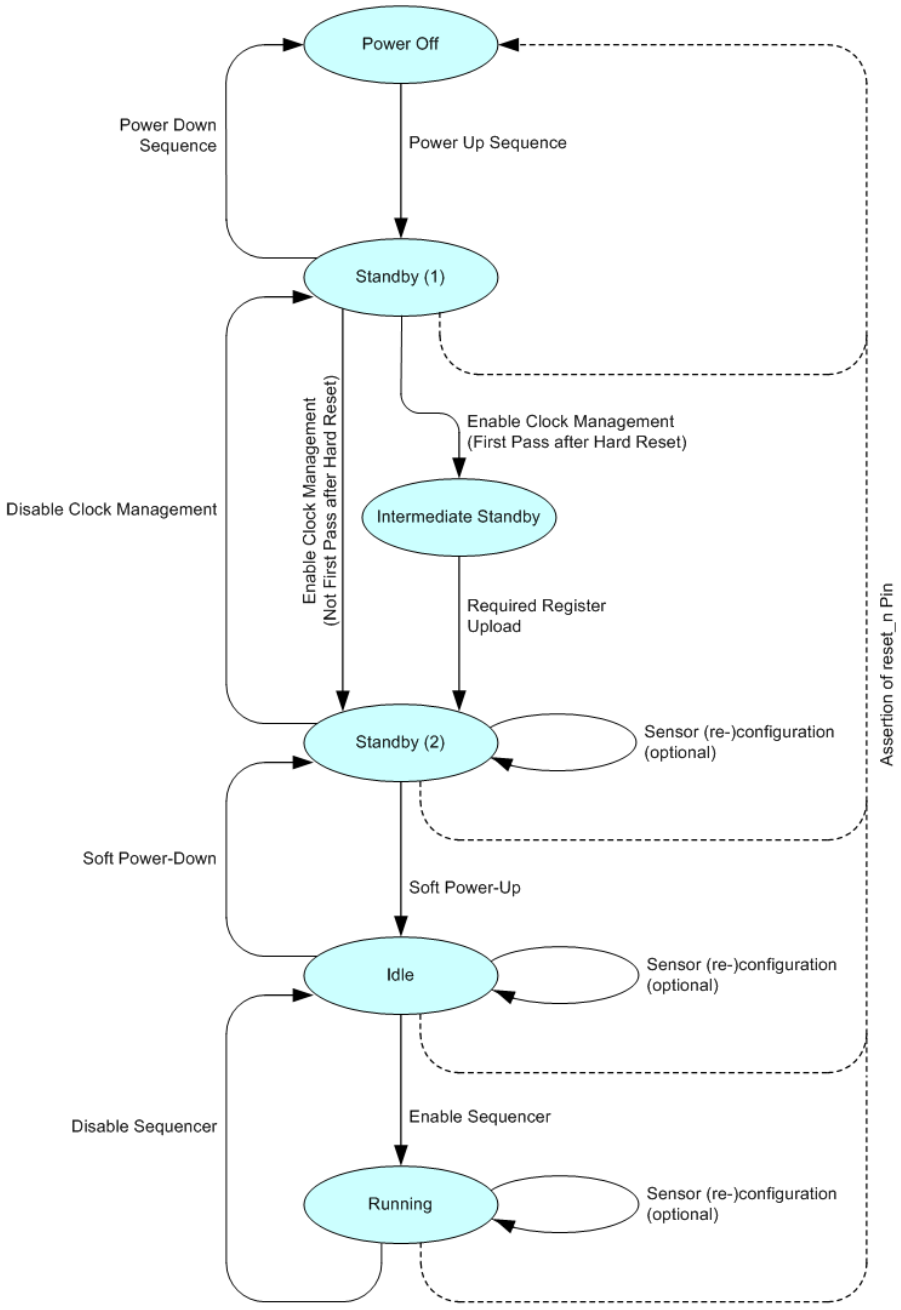

Figure 12. VITA 25K Sensor Operation Flow

The sensor can be in five different states:

Power-off

In this state, the sensor is inactive. All power supplies are down and the power dissipation is zero.

Standby (1)

The registers below address 40 can be configured.

Standby (2)

In this standby state all SPI registers are active, meaning that all SPI registers can be accessed for read and write operations. All other blocks are disabled.

Note: An Intermediate Standby state is traversed after a hard reset. In this state the sensor contains the default configurations. Uploads of reserved registers are required to traverse to the Standby (2) state

Idle

In the idle state, all sensor clocks are running and all blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in different rolling/global master/slave modes.

User Actions: Functional Mode to Power Up Sequences

To ‘travel’ between the five possible states, a set of actions is defined. Except for the power-up and power-down sequences, all actions consist of a set of SPI uploads.

The “Sensor reconfiguration actions” indicated in Figure 12 are used to reconfigure the operation modes of the sensor. The sensor state itself is not altered.

Power-up Sequence

Figure 13 shows the power-up timing of the sensor. Apply all power supplies in the order shown in the figure. It is important to comply with the described sequence. Any othyer supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up

When all the supplies are stable, enable the sensor clock signal; then deassert the reset_n signal. After leaving the hard-reset mode, the sensor enters the standby (1) state. To go to the standby (2) mode, the sensor requires the reconfiguration of some registers. This reconfiguration can be applied 10 μs after the hard reset is released.

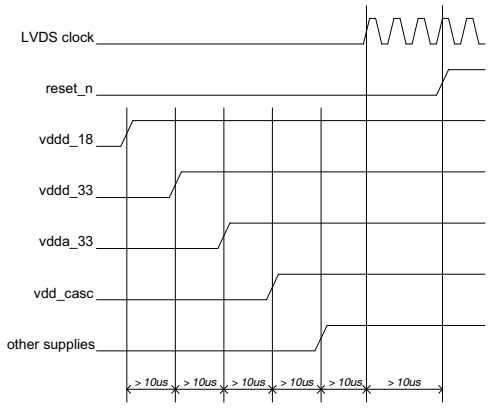

Figure 13. Power−up Procedure

NOTE: vdd_casc should come up prior to vdd_respd, vdd_resfd, and vdd_trans.

The required input clock frequency depends on the word depth mode of the sensor. This is possible in the following mode:

- 8-bit
- 10-bit

The input clock frequencies to achieve a frame rate of 53 frames/s are listed in Table 7.

Table 7. CLOCK FREQUENCY OVERVIEW

Parameter	8−bit Mode	10−bit Mode
Input Clock Frequency	248 MHz	310 MHz

Enable Clock Management

The next step consists of SPI uploads which configures the internal clock distribution. The required uploads are listed in Table 8. It is important to follow the upload sequence as listed.

Table 8. ENABLE CLOCK MANAGEMENT UPLOAD

No.	Address	Data	Description
1	2	0x0000	NOIV1SN025KA
		0x0001	NOIV1SE025KA
2	32	0x2002	Configure Clock Management
3	34	0x0001	Enable Logic Blocks

Required Register Uploads

In this phase the 'reserved' register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads are listed in Table 9.

Table 9. REQUIRED REGISTER UPLOADS

No.	Address	Data	Description
1	65	0x008B	General Biasing
2	66	0x53C6	AFE Biasing
3	67	0x0844	Mux Biasing
4	68	0x0086	LVDS Biasing
5	128	0x4520	Set desired output level to code 32 for 10-bit mode, code 8 for 8-bit mode. Set number of samples for black calibration to 2^5.
6	204	0x09E5	Configure unity gain
7	224	0x3E04	Dummy rows upon integration start
8	225	0x6733	Configure internal latency
9	129[13]	0x0	10-bit Mode
		0x1	8-bit Mode
10	447	0x0BF1	Configure sequencer
11	448	0x0BC3	Configure sequencer

Soft Power Up

During the soft power-up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power-up uploads are listed in Table 10.

Table 10. SOFT POWER UP REGISTER UPLOADS

No.	Address	Data	Description
1	32	0x2003	Enable Analog Clock Distribution
2	64	0x0001	Enable Biasing Block
3	40	0x0003	Enable Column Multiplexer
4	48	0x0001	Enable Analog Front-End (AFE)
5	112	0x0007	Enable LVDS Transmitters

Enable Sequencer

During the 'Enable Sequencer'-action, the frame grabbing sequencer is enabled. The sensor will start grabbing images in the configured operation mode. Refer to Operating Modes on page 11 for an overview of the possible operation modes.

The 'Enable Sequencer' action consists of a set op register uploads. The required uploads are listed in Table 11.

Table 11. ENABLE SEQUENCER REGISTER UPLOADS

No.	Address	Data	Description
1	192[0]	0x1	Set 'reg_seq_enable' to '1'. All other configuration bits of register 192 should remain unchanged.

User Actions: Functional Mode to Power Down Sequences

Disable Sequencer

During the 'Disable Sequencer'-action, the frame grabbing sequencer is stopped. The sensor will stop grabbing images and returns to the idle mode.

The 'Disable Sequencer' action consists of a set op register uploads. The required uploads are listed in Table 12.

Table 12. DISABLE SEQUENCER REGISTER UPLOADS

No.	Address	Data	Description
1	192[0]	0x0	Disable of Sequencer. NOTE: This address contains other configuration bits to select the operation mode.

Soft Power Down

During the soft power-down action, the internal blocks are disabled and the sensor is put in standby state in order to reduce the current dissipation. This action exists of a set of register uploads. The soft power-down uploads are listed in Table 13.

Table 13. SOFT POWER DOWN REGISTER UPLOADS

No.	Address	Data	Description
1	112	0x0000	Disable LVDS Transmitters
2	48	0x0000	Disable Analog Front-End (AFE)
3	40	0x0000	Disable Column Multiplexer
4	64	0x0000	Disable Biasing Block
5	32	0x2002	Disable Analog Clock Distribution

Disable Clock Management

The 'Disable Clock Management'-action stops the internal clocking in order to further decrease the power dissipation. This action exists of a set of register uploads as listed in Table 14.

Table 14. DISABLE CLOCK MANAGEMENT UPLOADS

No.	Address	Data	Description
1	34	0x0000	Disable Logic Blocks

Power-down Sequence

The timing diagram of the advised power-down sequence is given in Figure 14. Any other sequence might cause high peak currents.

NOTE: vdd_casc should be powered down after vdd_respd, vdd_resfd, and vdd_trans.

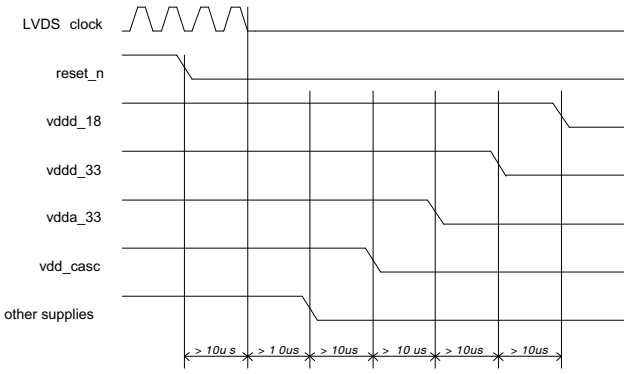

Figure 14. Power−down Sequence

Shutter and Operation Mode Reconfiguration

The VITA 25K sensor operates in two shutter modes: global shutter and rolling shutter. The global shutter mode can be combined with a set of operation modes, as described Operation Modes on page 11.

These modes can be combined with subsampling and binning modes.

The shutter and operation modes are controlled by register 192, when the sensor is in standby or idle mode. Table 15 gives an overview of the available register settings to control the shutter and operation modes. During this action, only the fields listed in Table 15 are affected. All other settings encapsulated in register 192 must remain unchanged.

Table 15. SHUTTER/OPERATION MODE CONFIGURATION REGISTERS

Address	Default Value	Description
192 [1]	0x0	Shutter type selection 0: Global shutter 1: Rolling shutter
192 [4]	0x0	Triggered mode selection (global shutter only) 0: Normal mode 1: Triggered mode
192 [5]	0x0	Master/Slave selection (global shutter only) 0: Master mode 1: Slave mode
192 [7]	0x0	Subsampling mode selection 0: Subsampling disabled 1: Subsampling enabled
192 [8]	0x0	Binning mode selection 0: Binning disabled 1: Binning enabled

Windowing Reconfiguration

The windowing settings can be configured during standby, idle, and running mode.

The required regions of interest (ROI) can be programmed in the roi_configuration registers (addresses 256 up to 351). Registers roi_active0 and roi_active1 are used to activate the desired ROIs.

Default window configuration (after sensor reset) is one window, full frame (window #0).

Exposure/Gain Reconfiguration

The exposure time and gain settings can be configured during standby, idle, and running mode. Refer to Signal Gain Path on page 29 for more information.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 16. Table 16 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 16. STATIC READOUT PARAMETERS

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64–71	Configure according to recommendation
LVDS	112	Configure according to recommendation
Sequencer mode selection	192	• Rolling shutter enable • triggered_mode • slave_mode • nzrot_xsm_delay_enable
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the recommendation

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 17 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the reconfiguration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 17. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

Group	Addresses	Description
Black level configuration	128–129 197[8]	Reconfiguration of these registers may have an impact on the black-level calibration algorithm. The effect is a transient number of images with incorrect black level compensation.
Sync codes	129[13] 130–135	Incorrect sync codes may be generated during the frame in which these registers are modified.
Datablock test configurations	144–150	Modification of these registers may generate incorrect test patterns during a transient frame.

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame-related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 18.

Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

Table 18. DYNAMIC READOUT PARAMETERS

Group	Addresses	Description
Subsampling/binning	192[7] 192[8]	Subsampling or binning is synchronized to a new frame start.
Black lines	197	Reconfiguration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. No blanking in global shutter mode
Dummy lines	198	Reconfiguration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. N/A for global shutter mode.
ROI configuration	195-196 256–351	Optionally, it is possible to blank out one frame after reconfiguration of the active ROIs in rolling shutter mode. Therefore, register 206[8] must be asserted (blank_roi_switch configuration). An ROI switch is only detected when a new window is selected as the active window (reconfiguration of registers 195, 196, or both). Reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image.
Exposure reconfiguration	199-201	Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to ‘1’ in triggered global mode (master).
Gain reconfiguration	204	Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] - gain_lat_comp).

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re-enable the synchronization. The sensor’s sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 15 shows a reconfiguration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

With sync_configuration = ‘1’. Configurations are synchronized to the frame boundaries (The registers exposure, fr_length, and mult_timer are not used in this mode)

Figure 16 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is deasserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

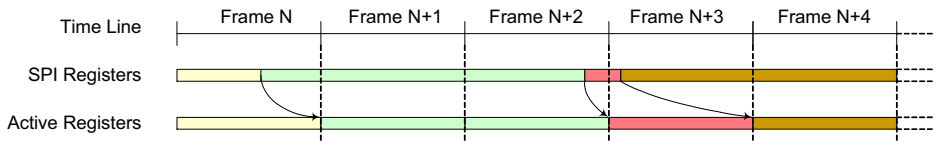

Figure 15. Frame Synchronization of Configurations (no freezing)

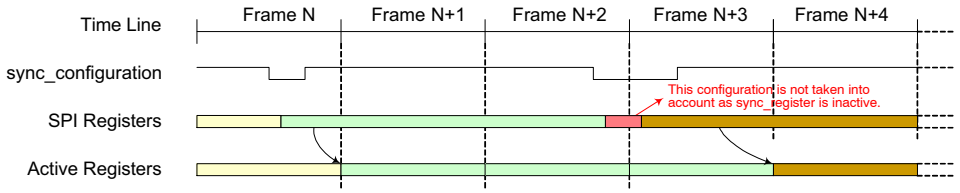

Figure 16. Reconfiguration Using Sync_configuration

NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 19 lists the several sync_configuration possibilities along with the respective registers being frozen.

Table 19. ALTERNATE SYNC CONFIGURATIONS

Group	Affected Registers	Description
sync_rs_x_length	rs_x_length	Update of x-length configuration (rolling shutter only) is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_black_lines	black_lines	Update of black line configuration is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_dummy_lines	dummy_lines	Update of dummy line configuration is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_exposure	mult_timer fr_length exposure	Update of exposure configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_gain	mux_gainsw afe_gain	Update of gain configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_roi	roi_active0[15:0] roi_active1[15:0] subsampling binning	Update of active ROI configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations. **Note:** The window configurations themselves are not frozen. Re-configuration of active windows is not gated by this setting.

Window Configuration

Global Shutter Mode

Up to 32 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 351. Each window can be activated or deactivated separately using registers 195 and 196. It is possible to reconfigure the inactive windows while acquiring images. Switching between prederfined windows is achieved by activation of the respective windows. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is tracked. Switching between the two modes only requires an upload of one (if the total number of windows is smaller than 17) or two (if more than 16 windows are defined) registers.

Rolling Shutter Mode

In rolling shutter mode it is not possible to read multiple windows. Do not activate more than one window (registers 205–206). However, it is possible to configure more than one window and dynamically switch between the different window configurations. Note that switching between two different windows might result in a corrupted frame. This is inherent in the rolling shutter mechanism, where each line must be reset sequentially before being read out. This corrupted window can be blanked out by setting register 206[8]. In this case, a dead time is noted on the LVDS interface when the window-switch occurs in the sensor. During this blank out, training patterns are sent out on the data and sync channels for the duration of one frame.

Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to ‘0’. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to ‘0’ when setting the black level target to ‘0’.

The black level is calibrated for the 64 columns contained in one kernel. This implies 64 black level offsets are generated and applied to the corresponding columns. Configurable parameters for the black-level algorithm are listed in Table 20.

Table 20. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

Group	Addresses	Description
Black Line Generation		
197[7:0]	black_lines	This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 255. **Note:** When the automatic black-level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black-level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations: Global Shutter - Each black line contains 80 kernels. Rolling Shutter - As the line length is fundamental for rolling shutter operation, the length of a black line is defined by the active window.
197[8]	gate_first_line	When asserting this configuration, the first black line of the frame is blanked out and is not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm.
Black Value Filtering		
129[0]	auto_blackcal_enable	Internal black-level calibration functionality is enabled when set to ‘1’. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to ‘0’, the automatic black-level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1]. **Note:** Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations.
129[9:1]	blackcal_offset	Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to ‘0’. The sign of the offset is determined by register 129[10] (blackcal_offset_dec). **Note:** All channels use the same offset compensation when automatic black calibration is disabled. The calculated black calibration factors are frozen when this register is set to 0x1FF (all−‘1’) in auto calibration mode. Any value different from 0x1FF re−enables the black calibration algorithm. This freezing option can be used to prevent eventual frame to frame jitter on the black level as the correction factors are recalculated every frame. It is recommended to enable the black calibration regularly to compensate for temperature changes.
129[10]	blackcal_offset_dec	Sign of blackcal_offset. If set to ‘0’, the black calibration offset is added to each pixel. If set to ‘1’, the black calibration offset is subtracted from each pixel. This register is not used when auto_blackcal_enable is set to ‘1’.
128[10:8]	black_samples	The black samples are low-pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate. The effective number of samples taken into account for filtering is $2^{black\_samples}$. **Note:** An error is reported by the device if more samples than available are requested (refer to registers 136 to 139).
Black Level Filtering Monitoring		
136 137 138 139	blackcal_error0 blackcal_error1 blackcal_error2 blackcal_error3	An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation: • Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197). • Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128). • Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift.

NOTE: The maximum number of samples taken into account for black level statistics is half the number of kernels.

Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor's system clock. When the master wants to write or read a sensor's register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 17 shows the communication protocol for read and write accesses of the SPI registers. The VITA 25K sensor uses 9-bit addresses and 16-bit data words

Data driven by the system is colored blue in Figure 17, while data driven by the sensor is colored yellow. The data in grey indicates high-Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

1. Select the sensor for read or write by pulling down the ss_n line.
2. One SPI clock cycle (100 ns) after selecting the sensor, the 9-bit address is transferred, most significant bit first. The sck clock is passed through to the sensor as indicated in Figure 17. The sensor samples this data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock)
3. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
4. Data transmission:
   - For write commands, the master continues sending the 16-bit data, most significant bit first.
   - For read commands, the sensor returns the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
5. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Maximum frequency for the SPI is $1/30^{th}$ (in 10-bit mode) and $1/24^{th}$ (in 8-bit mode) of the LVDS input clock frequency. For nominal input frequency (310 MHz / 248 MHz), this is 10 MHz.

Bursts of SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

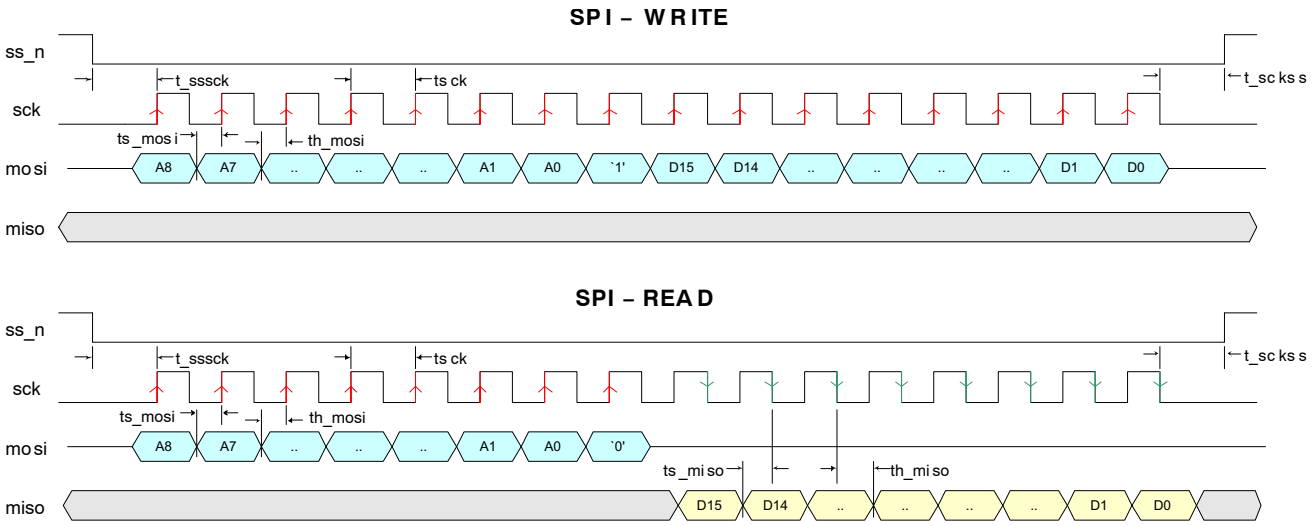

Figure 17. SPI Read and Write Timing Diagram

Table 21. SPI TIMING REQUIREMENTS

Group	Addresses	Description	Units
tsck	sck clock period	100 (*)	ns
tsssck	ss_n low to sck rising edge	tsck	ns
tsckss	sck falling edge to ss_n high	tsck	ns
ts_mosi	Required setup time for mosi	20	ns
th_mosi	Required hold time for mosi	20	ns
ts_miso	Setup time for miso	tsck/2-10	ns
th_miso	Hold time for miso	tsck/2-20	ns
tspi	Minimal time between two consecutive SPI accesses (not shown in figure)	2 x tsck	ns

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as $1/f_{SPI}$. See text for more information on SPI clock frequency restrictions.

IMAGE SENSOR TIMING AND READOUT

Global Shutter Mode

Pipelined Global Mode (Master)

The sensor timing in master global shutter mode is controlled by the user by means of configuration registers. One can distinguish three parameters for the frame timing in global shutter mode:

- Image Array Reset Length
- Integration Time
- Frame Length

The relation between these parameters is:

Frame Length = Reset Length + Integration Time

The FOT time needs to be added to the frame length parameter to determine the total frame Time

Total Frame Time = FOT Time + Frame Length

Frame and integration time configuration can be controlled in two ways:

1. fr_mode = 0x0
   The reset length and integration time is configured by the user. The sensor shall calculate the frame length as the sum of both parameters.
2. fr_mode = 0x1
   The frame length and integration time is configured by the user. The reset time during which the pixels are reset, is calculated by the sensor as being the difference between the frame length and the desired integration time.

The configuration registers are exposure[15:0] and fr_length[15:0]. The latter configuration registers is either used as Reset Length configuration (fr_mode = 0x0) or as Frame Length (fr_mode = 0x'1). The granularity of both registers is defined by the mult_timer[15:0] register and is expressed in number of 62 MHz cycles (16.129 ns nominal).

Reset Length and Integration Time as Parameters

The reset time for the pixel array is controlled by the registers fr_length[15:0] and exposure[15:0]. The mult_timer configuration defines the granularity of the registers fr_length and exposure and is to be read as the number of 62 MHz cycles (16.129 ns nominal).

The exposure control for pipelined global master mode is depicted in Figure 18.

The pixel values are transferred to the storage node during the FOT, after which all photo diodes are reset. The reset state remains active for a certain time, defined by the fr_length and mult_timer registers, as shown in the figure. Meanwhile, the image array is read out line by line. After this reset period, the global photodiode reset condition is abandoned. This indicates the start of the integration or exposure time. The length of the exposure time is defined by the registers exposure and mult_timer.

NOTES:

- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in a reset state is extended to the start of a new line.
- Make sure that the sum of the reset time and exposure time exceeds the time required to read out all lines. If this is not the case, the exposure time is extended until all (active) lines are read out.

Frame Length and Integration Time as Parameters

When fr_mode is configured to 0x1, one configures the frame time and exposure. The reset_length is determined by the sequencer. This configuration mode is depicted in Figure 2.

The frame length is configured in register fr_length, while the integration time is configured in register exposure. The mult_timer register defines granularity of both settings. Note that the FOT needs to be added to the configured fr_length to calculate the total frame time.

Triggered Global Shutter (Master)

In master triggered global mode, the start of integration time is controlled by a rising edge on the trigger pin. The exposure or integration time is defined by the registers exposure and mult_timer, similar to the master pipelined global mode. The fr_length configuration is not used. This operation is graphically shown in Figure 20.

NOTES:

- The falling edge on the trigger pin does not have any impact. However, the trigger must be asserted for at least 100 ns.
- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in reset state is extended to the start of a new line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 – a new trigger can be initiated after a rising edge on monitor0).

If the exposure timer expires before the end of readout, the exposure time is extended until the end of the last active line.

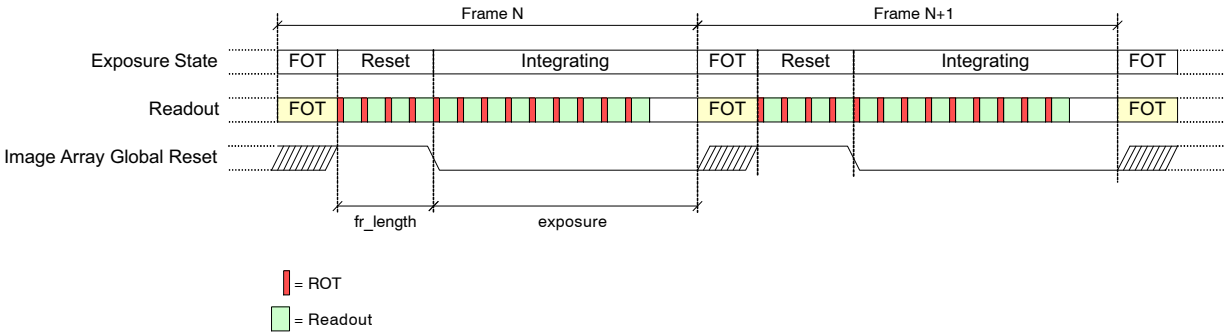

Figure 18. Integration Control for Pipelined Global Shutter Mode (Master, fr_mode = 0x0)

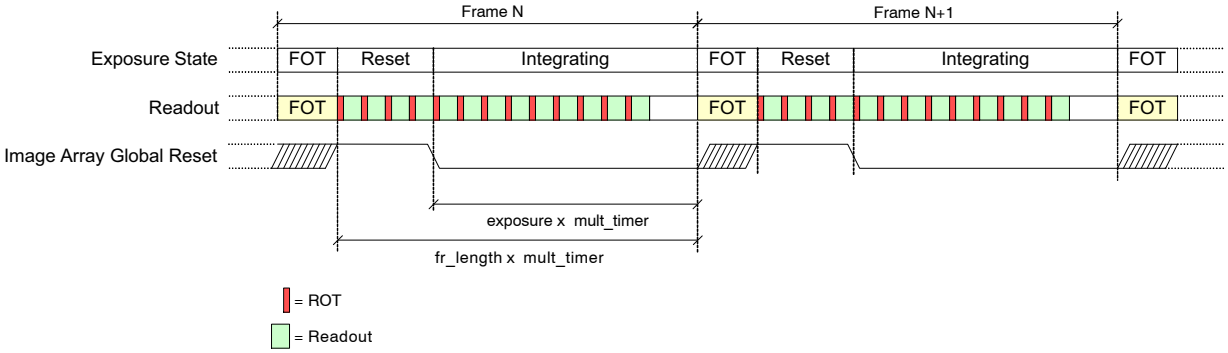

Figure 19. Integration Control for Pipelined Global Shutter Mode (Master, fr_mode = 0x1)

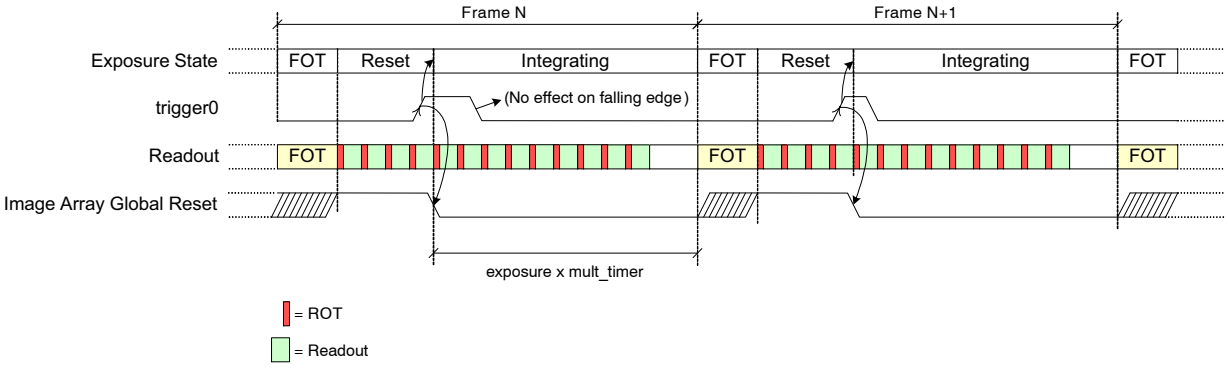

Figure 20. Exposure Time Control in Triggered Global Mode (Master)

Triggered Global Shutter (Slave)

Exposure or integration time is fully controlled by means of the trigger pin in slave mode. The register's fr_length, exposure, and mult_timer are ignored by the sensor.

A rising edge on the trigger pin indicates the start of the exposure time, while a falling edge initiates the transfer and readout of the image array. In other words, the high time of the trigger pin indicates the integration time, the period of the trigger pin indicates the frame time.

The use of the trigger during slave mode is shown in Figure 21.

NOTES:

- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in a reset state is extended to the start of a new line.
- If the trigger is deasserted before the end of readout, the exposure time is extended until the end of the last active line. Consequently the FOT and start of frame readout is postponed accordingly.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 – a new trigger can be initiated after a rising edge on monitor0).