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NOIV1SN1300A, NOIV2SN1300A

VITA 1300 1.3 Megapixel 150 FPS Global Shutter CMOS Image Sensor

ON Semiconductor®

www.onsemi.com

Features

- SXGA: 1280 x 1024 Active Pixels
- 4.8 μm x 4.8 μm Pixel Size
- 1/2 inch Optical Format
- Monochrome (SN) or Color (SE)
- 150 Frames per Second (fps) at Full Resolution (LVDS)
- 37 Frames per Second (fps) at Full Resolution (CMOS)
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 8-bit or 10-bit Output Mode
- Four LVDS Serial Outputs or Parallel CMOS Output
- Random Programmable Region of Interest (ROI) Readout
- Pipelined and Triggered Global Shutter, Rolling Shutter
- On-chip Fixed Pattern Noise (FPN) Correction
- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- High Dynamic Range (HDR)
- Dual Power Supply (3.3 V and 1.8 V)
- −40°C to +85°C Operational Temperature Range
- 48-pin LCC and Bare Die
- 475 mW Power Dissipation (LVDS)
- 290 mW Power Dissipation (CMOS)
- These Devices are Pb−Free and are RoHS Compliant

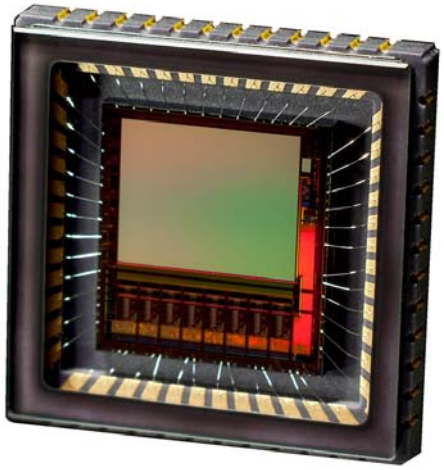


Figure 1. VITA 1300 Photograph

Applications

- Machine Vision
- Motion Monitoring
- Security
- Barcode Scanning (2D)

Description

The VITA 1300 is a 1/2 inch Super-eXtended Graphics Array (SXGA) CMOS image sensor with a pixel array of 1280 by 1024.

The high sensitivity 4.8 μm x 4.8 μm pixels support pipelined and triggered global shutter readout modes and can also be operated in a low noise rolling shutter mode. In rolling shutter mode, the sensor supports correlated double sampling readout, reducing noise and increasing the dynamic range.

The sensor has on-chip programmable gain amplifiers and 10-bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on-chip automatic exposure control loop (AEC) controls these parameters dynamically. The image's black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to 8 regions can be programmed, achieving even higher frame rates.

The image data interface of the V1-SN/SE part consists of four LVDS lanes, facilitating frame rates up to 150 frames per second. Each channel runs at 620 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receive end. The V2-SN/SE part provides a parallel CMOS output interface at reduced frame rate.

The VITA 1300 is packaged in a 48-pin LCC package and is available in a monochrome and color version.

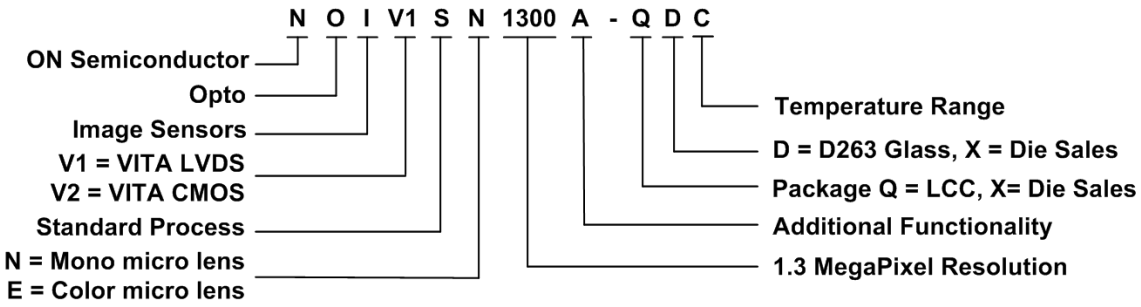
Contact your local ON Semiconductor office for more information.

ORDERING INFORMATION

Part Number	Mono/Color	Package
NOIV1SN1300A-QDC	LVDS Interface mono	48−pin LCC
NOIV1SE1300A-QDC	LVDS Interface color	
NOIV2SN1300A-QDC	CMOS Interface mono	
NOIV2SE1300A-QDC	CMOS Interface color	
NOIV1SN1300A-XXC	Die sales, mono	Die Sales

The V1-SN/SE base part is used to reference the mono and color versions of the LVDS interface; the V2-SN/SE base part is used to reference the mono and color versions of the CMOS interface.

ORDERING CODE DEFINITION



PACKAGE MARK

Following is the mark on the bottom side of the package with Pin 1 to the left center

Line 1: **NOI xxxx 1300A** where xxxx denotes LVDS (V1) / CMOS (V2), mono micro lens (SN) /color micro lens (SE) option

Line 2: **-QDC**

Line 3: **AWLYYWW**

CONTENTS

SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	Specification
Pixel type	Global shutter pixel architecture
Shutter type	Pipelined and triggered global shutter, rolling shutter
Frame rate at full resolution	V1-SN/SE: 150 fps V2-SN/SE: 37 fps
Master clock	V1-SN/SE: 62 MHz when PLL is used, 310 MHz (10-bit) / 248 MHz (8-bit) when PLL is not used V2-SN/SE: 62 MHz
Windowing	8 Randomly programmable windows. Normal, sub-sampled and binned read-out modes
ADC resolution (1)	10-bit, 8-bit
LVDS outputs	V1-SN/SE: 4 data + sync + clock
CMOS outputs	V2-SN/SE: 10-bit parallel output, frame_valid, line_valid, clock
Data rate	V1-SN/SE: 4 x 620 Mbps (10-bit) / 4 x 496 Mbps (8-bit) V2-SN/SE: 62 MHz
Power dissipation	475 mW for V1-SN/SE in 10-bit mode 290 mW for V2-SN/SE
Package type	48-pin LCC, bare die

Table 2. ELECTRO−OPTICAL SPECIFICATIONS

Parameter	Specification
Active pixels	1280 (H) x 1024 (V)
Pixel size	4.8 μm x 4.8 μm
Optical format	1/2 inch
Conversion gain	0.072 LSB10/e^- 90 μV/e^-
Dark noise	2.2 LSB10, 30e^- in global shutter 0.9 LSB10, 14e^-in rolling shutter
Responsivity at 550 nm	24 LSB10 /nJ/cm^2, 4.6 V/lux.s
Parasitic Light Sensitivity (PLS)	<1/450
Full well charge	13700 e^-
Quantum efficiency	53% at 550 nm
Pixel FPN	rolling shutter: 0.5 LSB10 global shutter: 1.0 LSB10
PRNU	< 2% of signal
MTF	60% @ 630 nm - X-dir & Y-dir
PSNL @ 25°C	100 LSB10/s, 1360 e^-/s
Dark signal @ 25°C	4.5 e^-/s, 0.33 LSB10/s
Dynamic range	60 dB in rolling shutter mode 53 dB in global shutter mode
Signal to Noise Ratio (SNR max)	41 dB

Table 3. RECOMMENDED OPERATING RATINGS (Note 2)

Symbol	Description	Min	Max	Units
T_J	Operating temperature range	−40	85	°C

Table 4. ABSOLUTE MAXIMUM RATINGS (Notes 3 and 4)

Symbol	Parameter	Min	Max	Units
ABS (1.8 V supply group)	ABS rating for 1.8 V supply group	−0.5	2.2	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	−0.5	4.3	V
T_S	ABS storage temperature range	−40	+150	°C
	ABS storage humidity range at 85°C		85	%RH
Electrostatic discharge (ESD)	Human Body Model (HBM): JS−001−2010	2000		V
	Charged Device Model (CDM): JESD22−C101	500		
LU	Latch-up: JESD−78	140		mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The ADC is 11−bit, down−scaled to 10−bit. The VITA 1300 uses a larger word−length internally to provide 10−bit on the output.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
4. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6 and 7)

Parameter	Description	Min	Typ	Max	Units
Power Supply Parameters - V1-SN/SE LVDS					
vdd_33	Supply voltage, 3.3 V	**3.0**	3.3	**3.6**	V
Idd_33	Current consumption 3.3 V supply	90	110	130	mA
vdd_18	Supply voltage, 1.8 V	**1.6**	1.8	**2.0**	V
Idd_18	Current consumption 1.8 V supply	45	60	75	mA
vdd_pix	Supply voltage, pixel	**3.0**	3.3	**3.6**	V
Idd_pix	Current consumption pixel supply	0.8	1.8	2.5	mA
Ptot	Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V	375	475	575	mW
Pstby_lp	Power consumption in low power standby mode. See Silicon Errata on page 66			50	mW
Popt	Power consumption at lower pixel rates	Configurable			
Power Supply Parameters - V2-SN/SE CMOS					
vdd_33	Supply voltage, 3.3 V	**3.0**	3.3	**3.6**	V
Idd_33	Current consumption 3.3 V supply	70	90	110	mA
vdd_18	Supply voltage, 1.8 V	**1.6**	1.8	**2.0**	V
Idd_18	Current consumption 1.8 V supply	4	7	10	mA
vdd_pix	Supply voltage, pixel	**3.0**	3.3	**3.6**	V
Idd_pix	Current consumption pixel supply		0.5	1	mA
Ptot	Total power consumption	220	290	360	mW
Pstby_lp	Power consumption in low power standby mode. See Silicon Errata on page 66			50	mW
Popt	Power consumption at lower pixel rates	Configurable			
I/O - V2-SN/SE CMOS (JEDEC- JESD8C-01): Conforming to standard/additional specifications and deviations listed					
fpardata	Data rate on parallel channels (10-bit)			62	Mbps
Cout	Output load (only capacitive load)			10	pF
tr	Rise time (10% to 90% of input signal)	2.5	4.5	6.5	ns
tf	Fall time (10% to 90% of input signal)	2	3.5	5	ns
I/O - V1-SN/SE LVDS (EIA/TIA-644): Conforming to standard/additional specifications and deviations listed					
fserdata	Data rate on data channels DDR signaling - 4 data channels, 1 synchronization channel;			620	Mbps
fserclock	Clock rate of output clock Clock output for mesochronous signaling			310	MHz
Vicm	LVDS input common mode level	0.3	1.25	2.2	V
Tccsk	Channel to channel skew (Training pattern allows per channel skew correction)			50	ps
V1-SN/SE LVDS Electrical/Interface					
fin	Input clock rate when PLL used			62	MHz
fin	Input clock when LVDS input used			310	MHz
tidc	Input clock duty cycle when PLL used	40	50	60	%
tj	Input clock jitter		20		ps
fspi	SPI clock rate when PLL used at fin = 62 MHz			10	MHz
V2-SN/SE CMOS Electrical/Interface					
fin	Input clock rate			62	MHz

Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6 and 7)

Parameter	Description	Min	Typ	Max	Units
tj	Input clock jitter		20		ps
fspi	SPI clock rate at fin = 62 MHz			2.5	MHz
Frame Specifications (V1-SN/SE-LVDS - Global Shutter)					
fps	Frame rate at full resolution			150	fps
fps_roi1	Xres x Yres = 1024 x 1024			180	fps
fps_roi2	Xres x Yres = 640 x 480			540	fps
fps_roi3	Xres x Yres = 512 x 512			590	fps
fps_roi4	Xres x Yres = 256 x 256			1650	fps
FOT	Frame Overhead Time		45		μs
ROT	Row Overhead Time		1.1		μs
fpix	Pixel rate (4 channels at 62 Mpix/s)			248	Mpix/s
Frame Specifications (V2-SN/SE CMOS - Global Shutter)					
fps	Frame rate at full resolution			37	fps

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.

For recommendations on power supply management guidelines, refer to application note AN65463: VITA 1300 HSMC Cyclone Reference Board Design Recommendations.

Color Filter Array

The V1SE and V2SE sensors are processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left.

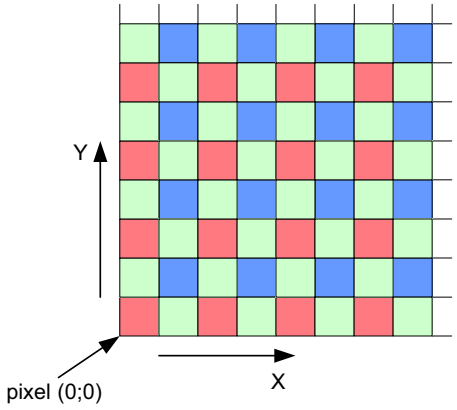


Figure 2. Color Filter Array for the Pixel Array

Spectral Response Curve

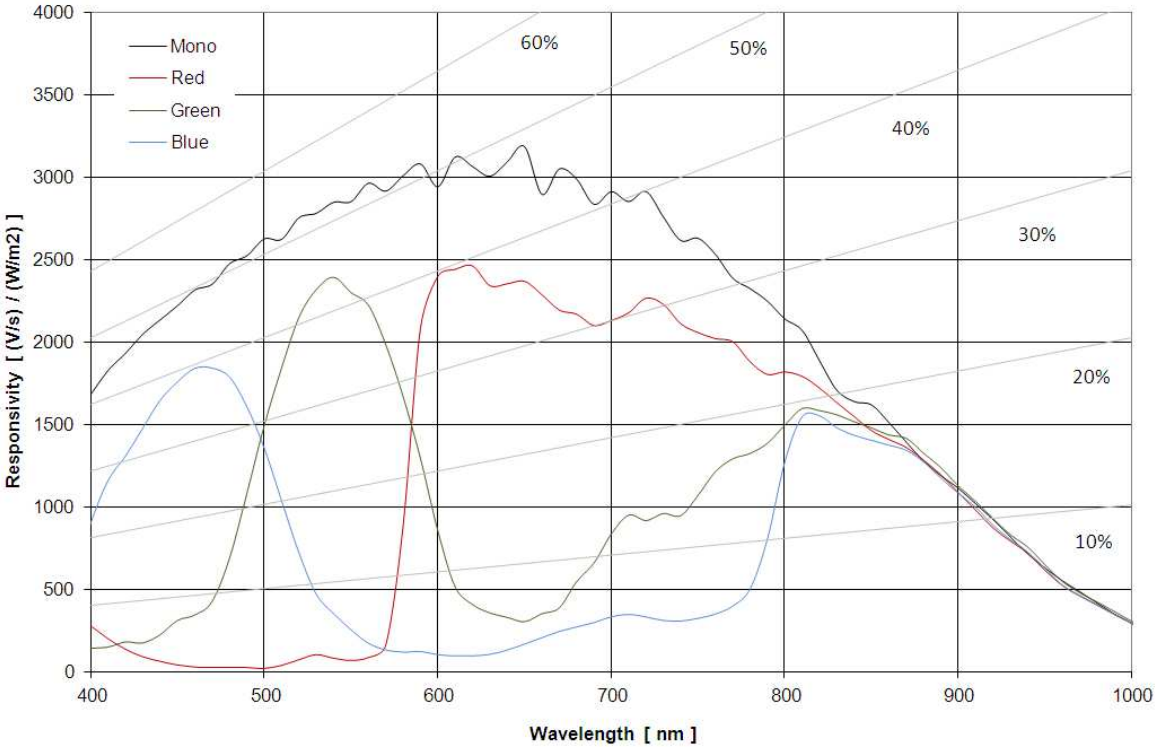


Figure 3. Spectral Response Curve for Mono and Color

Note that green pixels on a Green−Red (Green 1) and Green−Blue (Green 2) row have similar responsivity to wavelength trend as is depicted by the legend “Green”.

OVERVIEW

Figure 4 and Figure 5 give an overview of the major functional blocks of the V1-SN/SE and V2-SN/SE sensor respectively. The system clock is received by the CMOS clock input. A PLL generates the intenal, high speed, clocks, which are distributed to the other blocks. Optionally, the V1-SN/SE can also accept a high speed LVDS clock, in which case the PLL will be disabled.

The sequencer defines the sensor timing and controls the image core. The sequencer is started either autonomously (master mode) or on assertion of an external trigger (slave mode). The image core contains all pixels and readout circuits. The column structure selects pixels for readout and performs correlated double sampling (CDS) or double sampling (DS). The data comes out sequentially and is fed into the analog front end (AFE) block. The programmable gain amplifier (PGA) of the AFE adds the offset and gain. The output is a fully differential analog signal that goes to the ADC, where the analog signal is converted to a 10-bit data stream. Depending on the operating mode, eight or ten bits are fed into the data formatting block. This block adds synchronization information to the data stream based on the frame timing. For the V1-SN/SE version, the data then goes to the low voltage serial (LVDS) interface block which sends the data out through the I/O ring. The V2-SN/SE sensor does not have an LVDS interface but sends out the data through a 10-bit parallel interface.

On-chip programmability is achieved through the Serial Peripheral Interface (SPI). See the Register Map on page 50 for register details.

A bias block generates bias currents and voltages for all analog blocks on the chip. By controlling the bias current, the speed-versus-power of each block can be tuned. All biasing programmability is contained in the bias block.

The sensor can automatically control exposure and gain by enabling the automatic exposure control block (AEC). This block regulates the integration time along with the analog and digital gains to reach the desired intensity.

Block Diagram

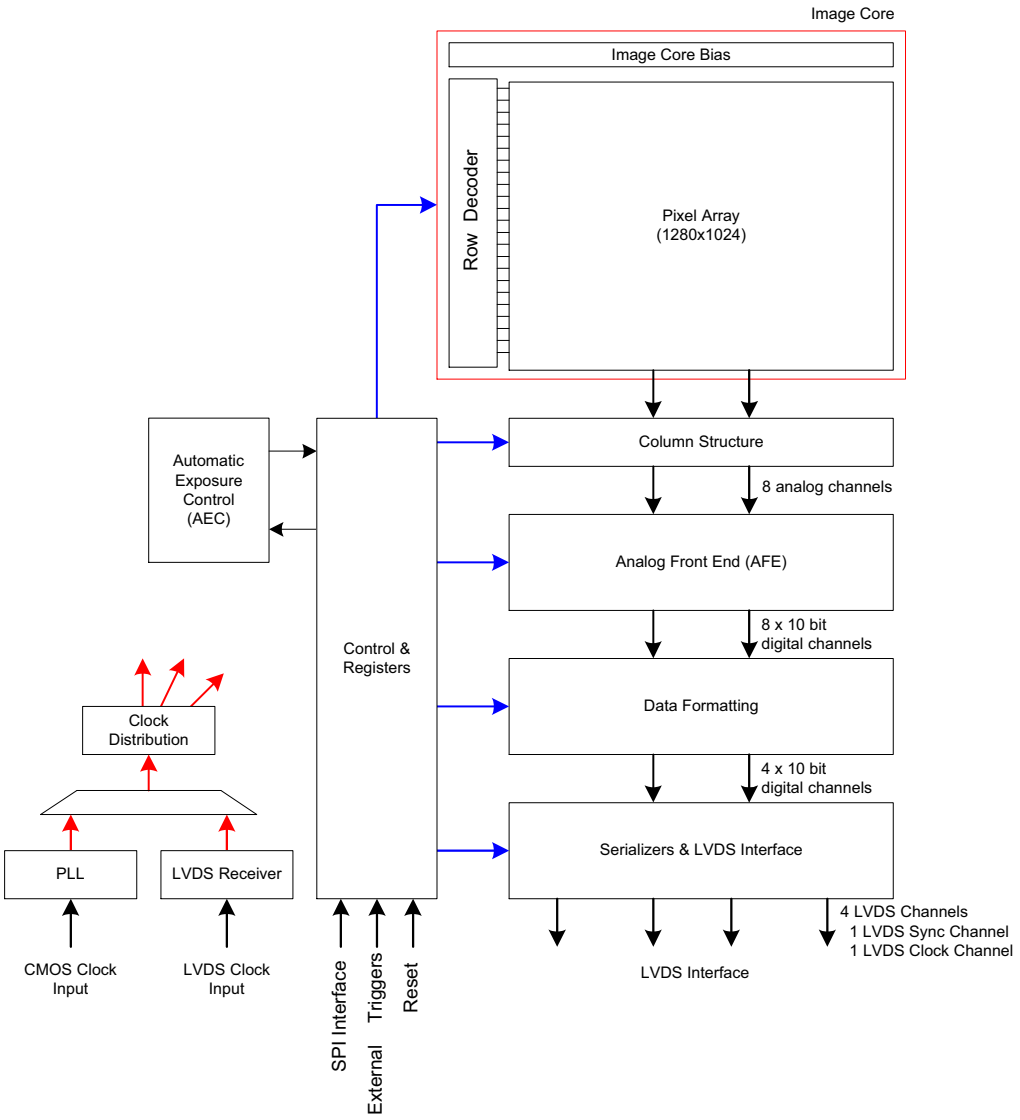


Figure 4. Block Diagram – V1−SN/SE

Block Diagram

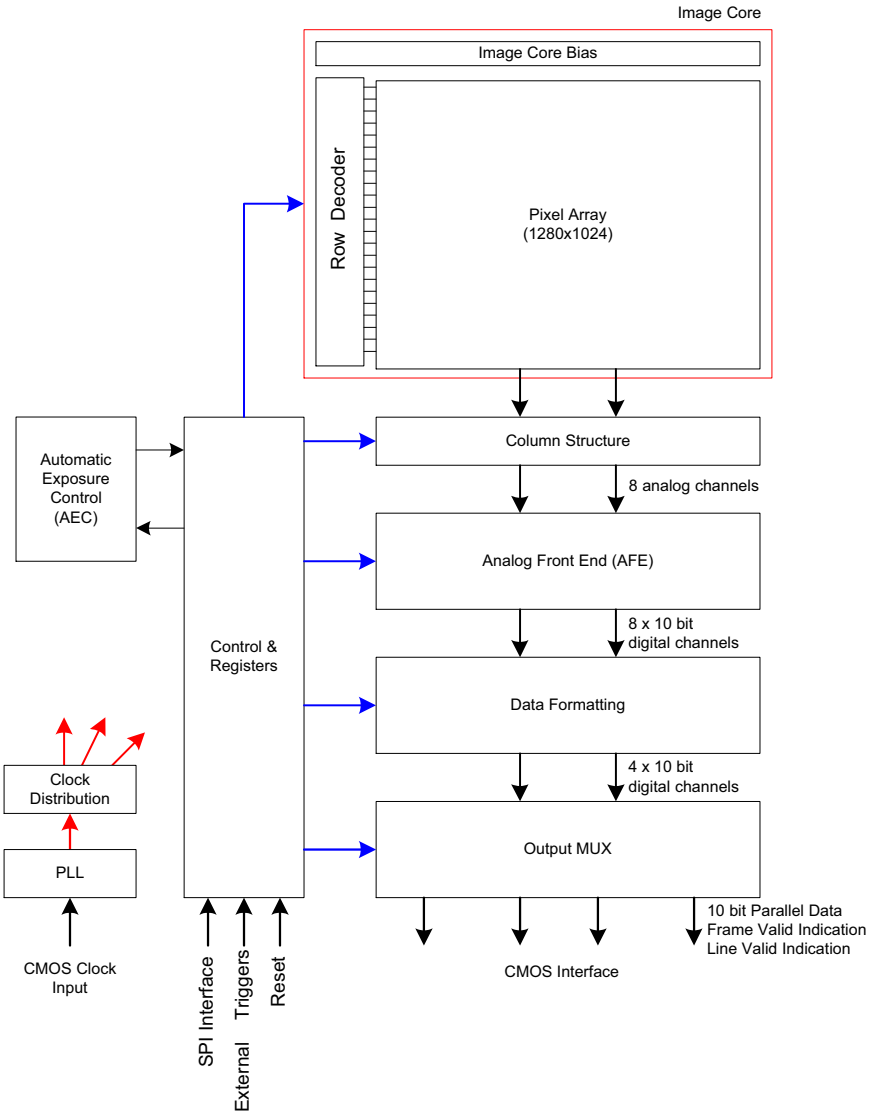


Figure 5. Block Diagram − V2−SN/SE

Image Core

The image core consists of:

- Pixel Array
- Address Decoders and Row Drivers
- Pixel Biasing

The pixel array contains 1280 (H) x 1024 (V) readable pixels with a pixel pitch of 4.8 μm. Four dummy pixel rows and columns are placed at every side of the pixel array to eliminate possible edge effects. The sensor uses a 5T pixel architecture, which makes it possible to read out the pixel array in global shutter mode with double sampling (DS), or in rolling shutter mode with correlated double sampling (CDS).

The function of the row drivers is to access the image array line by line, or all lines together, to reset or read the pixel data. The row drivers are controlled by the on-chip sequencer and can access the pixel array in global and rolling shutter modes.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

Phase Locked Loop

The PLL accepts a (low speed) clock and generates the required high speed clock. Optionally this PLL can be bypassed. Typical input clock frequency is 62 MHz.

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 310 MHz in 10-bit mode and 248 MHz in 8-bit mode. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

All pixels of one image row are stored in the column sample-and-hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 8 parallel differential outputs operating at a frequency of 31 MHz.

At this stage, the reset signal and integrated signal values are transferred into an FPN-corrected differential signal.

The column multiplexer also supports read-1-skip-1 and read-2-skip-2 mode. Enabling this mode can speed up the frame rate, with a decrease in resolution.

Bias Generator

The bias generator generates all required reference voltages and bias currents that the on-chip blocks use. An external resistor of 47 kΩ, connected between pin IBIAS_MASTER and gnd_33, is required for the bias generator to operate properly.

Analog Front End

The AFE contains 8 channels, each containing a PGA and a 10-bit ADC.

For each of the 8 channels, a pipelined 10-bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one data stream. A cyclic redundancy check (CRC) code is calculated on the passing data.

A frame synchronization data block is foreseen to transmit synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface (V1−SN/SE only)

The serializer and LVDS interface block receives the formatted (10-bit or 8-bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

In 10-bit mode, the maximum output data rate is 620 Mbps per channel. In 8-bit mode, the maximum output data rate is 496 Mbps per channel.

In addition to the LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system-level image reconstruction.

Output MUX (V2−SN/SE only)

The output MUX multiplexes the four data channels to one channel and transmits the data words using a 10-bit parallel CMOS interface.

Frame synchronization information is communicated by means of frame and line valid strobes.

Sequencer

The sequencer:

- Controls the image core. Starts and stops integration in rolling and global shutter modes and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

Automatic Exposure Control

The AEC block implements a control system to modulate the exposure of an image. Both integration time and gains are controlled by this block to target a predefined illumination level.

OPERATING MODES

The VITA 1300 sensor is able to operate in the following shutter modes:

- Global Shutter Mode
  - ♦ Pipelined Global Shutter
    - Master
    - Slave
  - ♦ Triggered Global Shutter
    - Master
    - Slave
- Rolling Shutter Mode

Global Shutter Mode

In the global shutter mode, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 6 shows the integration and readout sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially.

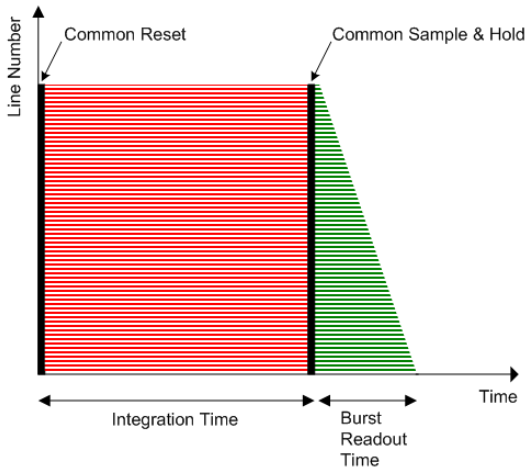


Figure 6. Global Shutter Operation

Pipelined Global Shutter

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N-1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line per line and the readout of each line is preceded by the Row Overhead Time (ROT). Figure 7 shows the exposure and readout time line in pipelined global shutter mode.

- Master

In this operation mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

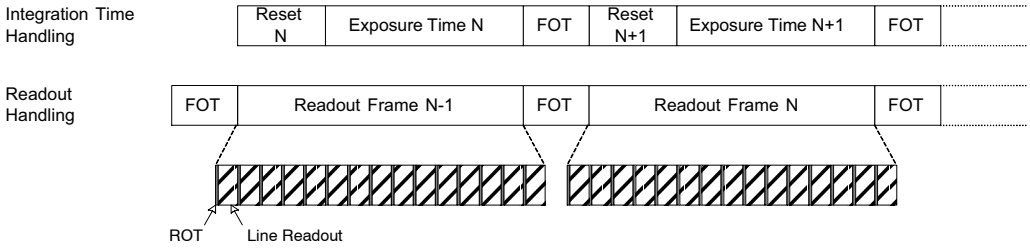


Figure 7. Integration and Readout for Pipelined Shutter

- Slave

The slave mode adds more manual control to the sensor. The exposure time registers are ignored in this mode and the integration time is controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the external pin is de-asserted by the system. Now, the image is sampled and the readout is started. Figure 8 shows the relation between the external trigger signal and the exposure/readout timing.

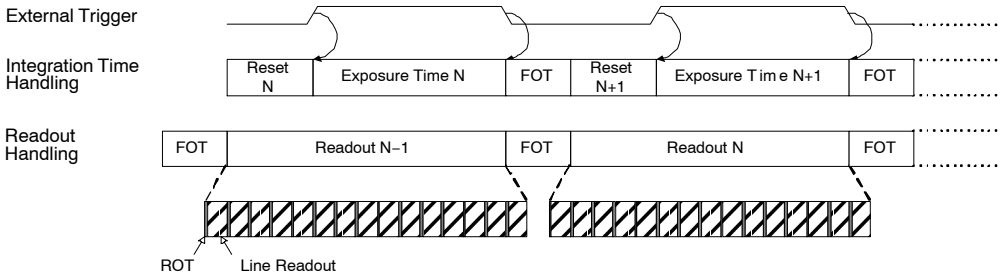


Figure 8. Pipelined Shutter Operated in Slave Mode

Triggered Global Shutter

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences with the pipelined global shutter mode are

- Upon user action, one single image is read.
- Integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is under user control through an external pin.

This mode requires manual intervention for every frame. The pixel array is kept in reset state until requested.

The triggered global mode is also controlled in a master or slave mode fashion.

- Master

In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is readout sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge. Figure 9 shows the relation between the external trigger signal and the exposure/readout timing.

If a rising edge is applied on the external trigger before the exposure time and FOT of the previous frame is complete, it is ignored by the sensor.

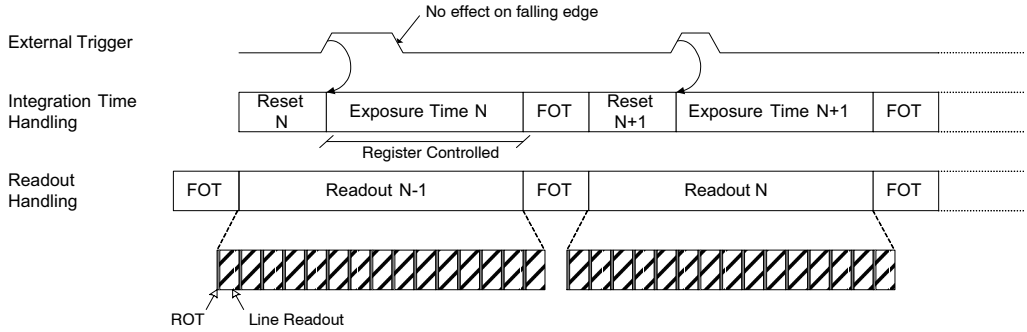


Figure 9. Triggered Shutter Operated in Master Mode

- Slave

Integration time control is identical to the pipelined shutter slave mode. An external synchronization pin controls the start of integration. When it is de-asserted, the FOT starts. The analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

Rolling Shutter Mode

Another shutter mode supported by the sensor is the rolling shutter mode. The shutter mechanism is an electronic rolling shutter and the sensor operates in a streaming mode similar to a video. This mechanism is controlled by the on-chip sequencer logic. There are two Y pointers. One points to the row that is to be reset for rolling shutter operation, the other points to the row to be read out. Functionally, a row is reset first and selected for read out sometime later. The time elapsed between these two operations is the exposure time.

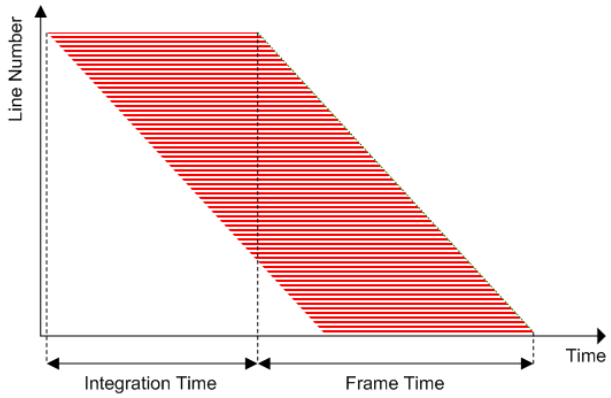


Figure 10. Rolling Shutter Operation

Figure 10 schematically indicates the relative shift of the integration times of different lines during the rolling shutter operation. Each row is read and reset in a sequential way. Each row in a particular frame is integrated for the same time, but all lines in a frame ‘see’ a different stare time. As a consequence, fast horizontal moving objects in the field of view give rise to motion artifacts in the image; this is an unavoidable property of a rolling shutter.

In rolling shutter mode, the pixel Fixed Pattern Noise (FPN) is corrected on-chip by using the CDS technique. After light integration on all pixels in a row is complete, the storage node in the pixel is reset. Afterwards the integrated signal is transferred to that pixel storage node. The difference between the reset level and integrated signal is the FPN corrected signal. The advantage of this technique, compared to the DS technique used in the global shutter modes, is that the reset noise of the pixel storage node is cancelled. This results in a lower temporal noise level.

SENSOR OPERATION

Flowchart

Figure 11 shows the sensor operation flowchart. The sensor can be in six different ‘states’. Every state is indicated with the oval circle. These states are:

- Power off
- Low power standby
- Standby (1)
- Standby (2)
- Idle
- Running

These states are ordered by power dissipation. In ‘power-off’ state, the power dissipation is minimal; in ‘running’ state the power dissipation is maximal.

On the other hand, the lower the power consumption, the more actions (and time) are required to put the sensor in ‘running’ state and grab images.

This flowchart allows the trade-off between power saving and enabling time of the sensor.

Next to the six ‘states’ a set of ‘user actions’, indicated by arrows, are included in the flowchart. These user actions make it possible to move from one state to another.

Sensor States

Power Off

In this state, the sensor is inactive. All power supplies are down and the power dissipation is zero.

Low Power Standby

In low power standby state, all power supplies are on, but internally every block is disabled. No internal clock is running (PLL / LVDS clock receiver is disabled).

All register settings are unchanged.

Only a subset of the SPI registers is active for read/write in order to be able to configure clock settings and leave the low power standby state. The only SPI registers that should be touched are the ones required for the ‘Enable Clock Management’ action described in Enable Clock Management – Part 1 on page 17

Standby (1)

In standby state, the PLL/LVDS clock receiver is running, but the derived logic clock signal is not enabled.

Standby (2)

In standby state, the derived logic clock signal is running. All SPI registers are active, meaning that all SPI registers can be accessed for read or write operations. All other blocks are disabled.

Idle

In the idle state, all internal blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in different rolling/global master/slave modes.

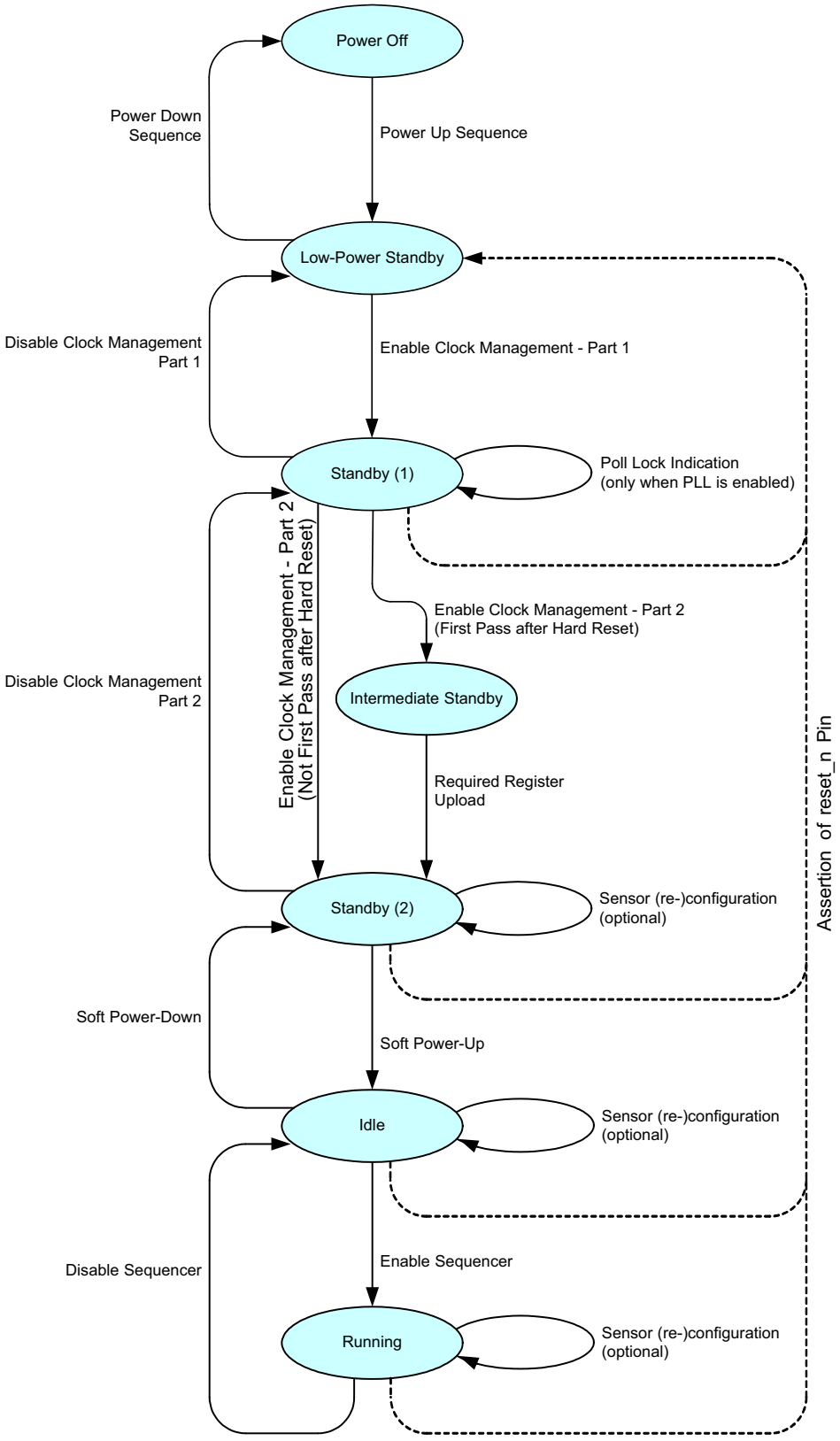


Figure 11. Sensor Operation Flowchart

User Actions: Power Up Functional Mode Sequences

Power Up Sequence

Figure 12 shows the power up sequence of the sensor. The figure indicates that the first supply to ramp-up is the vdd_18 supply, followed by vdd_33 and vdd_pix respectively. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. When the clock frequency is stable, the reset_n signal can be de-asserted. After a wait period of 10 μs, the power up sequence is finished and the first SPI upload can be initiated.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

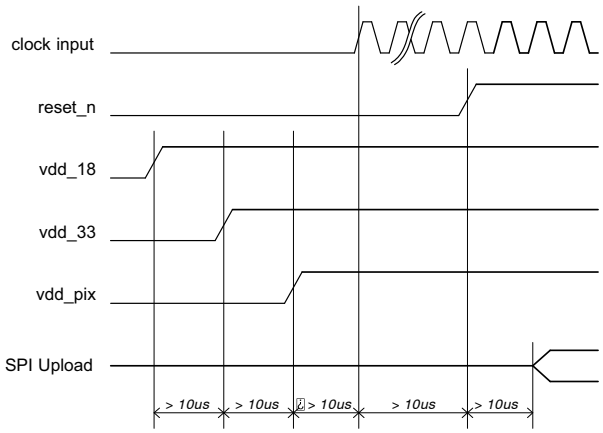


Figure 12. Power Up Sequence

Enable Clock Management – Part 1

The ‘Enable Clock Management’ action configures the clock management blocks and activates the clock generation and distribution circuits in a pre-defined way. First, a set of clock settings must be uploaded through the SPI register. These settings are dependent on the desired operation mode of the sensor.

Table 6 shows the SPI uploads to be executed to configure the sensor for V1-SN/SE 8-bit serial, V1-SN/SE 10-bit serial, or V2-SN/SE 10-bit parallel mode, with and without the PLL.

In the serial modes, if the PLL is not used, the LVDS clock input must be running.

In the V2-SN/SE10-bit parallel mode, the PLL is bypassed. The clk_pll clock is used as sensor clock.

It is important to follow the upload sequence listed in Table 6.

Use of Phase Locked Loop

If PLL is used, the PLL is started after the upload of the SPI registers. The PLL requires (dependent on the settings) some time to generate a stable output clock. A lock detect circuit detects if the clock is stable. When complete, this is flagged in a status register.

NOTE: The lock detect status must not be checked for the V2-SN/SE sensor.

Check this flag by reading the SPI register. When the flag is set, the ‘Enable Clock Management- Part 2’ action can be continued. When PLL is not used, this step can be bypassed as shown in Figure 11 on page 16.

Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 1

Upload #	Address	Data	Description
V1-SN/SE 8-bit mode with PLL			
1	2	0x0000	Monochrome sensor
		0x0001	Color sensor
2	32	0x200C	Configure clock management
3	20	0x0000	Configure clock management
4	17	0X210F	Configure PLL
5	26	0x1180	Configure PLL lock detector
6	27	0xCCBC	Configure PLL lock detector
7	8	0x0000	Release PLL soft reset
8	16	0x0003	Enable PLL
V1-SN/SE 8-bit mode without PLL			
1	2	0x0000	Monochrome sensor
		0x0001	Color sensor
2	32	0x2008	Configure clock management
3	20	0x0001	Enable LVDS clock input

Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 1

Upload #	Address	Data	Description
V1-SN/SE 10-bit mode with PLL			
1	2	0x0000	Monochrome sensor
		0x0001	Color sensor
2	32	0x2004	Configure clock management
3	20	0x0000	Configure clock management
4	17	0x2113	Configure PLL
5	26	0x2280	Configure PLL lock detector
6	27	0x3D2D	Configure PLL lock detector
7	8	0x0000	Release PLL soft reset
8	16	0x0003	Enable PLL
V1-SN/SE 10-bit mode without PLL			
1	2	0x0000	Monochrome sensor
		0x0001	Color sensor
2	32	0x2000	Configure clock management
3	20	0x0001	Enable LVDS clock input
V2-SN/SE 10-bit mode			
1	2	0x0002	Monochrome sensor parallel mode selection
		0x0003	Color sensor parallel mode selection
2	32	0x200C	Configure clock management
3	20	0x0000	Configure clock management
4	16	0x0007	Configure PLL bypass mode

Enable Clock Management - Part 2

The next step to configure the clock management consists of SPI uploads which enables all internal clock distribution. The required uploads are listed in Table 4. Note that it is important to follow the upload sequence listed in Table 7.

Table 7. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
V1-SN/SE 8-bit mode with PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x200E	Enable logic clock
3	34	0x0001	Enable logic blocks
V1-SN/SE 8-bit mode without PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x200A	Enable logic clock
3	34	0x0001	Enable logic blocks
V1-SN/SE 10-bit mode with PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x2006	Enable logic clock
3	34	0x0001	Enable logic blocks
V1-SN/SE 10-bit mode without PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x2002	Enable logic clock

Table 7. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
3	34	0x0001	Enable logic blocks
V2-SN/SE 10-bit mode			
1	9	0x0000	Release clock generator soft reset
2	32	0x200E	Enable logic clock
3	34	0x0001	Enable logic blocks

Required Register Upload

In this phase, the 'reserved' register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads are listed in Table 8.

Table 8. REQUIRED REGISTER UPLOAD

Upload #	Address	Data	Description
1	41	0x085A	Configure image core
2	129[13]	0x0	10-bit mode
		0x1	8-bit mode
3	65	0x288B	Configure CP biasing
4	66	0x53C5	Configure AFE biasing
5	67	0x0344	Configure MUX biasing
6	68	0x0085	Configure LVDS biasing
7	70	0x4800	Configure AFE biasing
8	128	0x4710	Configure black calibration
9	197	0x0103	Configure black calibration
10	176	0x00F5	Configure AEC
11	180	0x00FD	Configure AEC
12	181	0x0144	Configure AEC
13	387	0x549F	Configure sequencer
14	388	0x549F	Configure sequencer
15	389	0x5091	Configure sequencer
16	390	0x1011	Configure sequencer
17	391	0x111F	Configure sequencer
18	392	0x1110	Configure sequencer
19	431	0x0356	Configure sequencer
20	432	0x0141	Configure sequencer
21	433	0x214F	Configure sequencer
22	434	0x214A	Configure sequencer
23	435	0x2101	Configure sequencer
24	436	0x0101	Configure sequencer
25	437	0x0B85	Configure sequencer
26	438	0x0381	Configure sequencer
27	439	0x0181	Configure sequencer
28	440	0x218F	Configure sequencer
29	441	0x218A	Configure sequencer
30	442	0x2101	Configure sequencer

Table 8. REQUIRED REGISTER UPLOAD

Upload #	Address	Data	Description
31	443	0x0100	Configure sequencer
32	447	0x0B55	Configure sequencer
33	448	0x0351	Configure sequencer
34	449	0x0141	Configure sequencer
35	450	0x214F	Configure sequencer
36	451	0x214A	Configure sequencer
37	452	0x2101	Configure sequencer
38	453	0x0101	Configure sequencer
39	454	0x0B85	Configure sequencer
40	455	0x0381	Configure sequencer
41	456	0x0181	Configure sequencer
42	457	0x218F	Configure sequencer
43	458	0x218A	Configure sequencer
44	459	0x2101	Configure sequencer
45	460	0x0100	Configure sequencer
46	469	0x2184	Configure sequencer
47	472	0x1347	Configure sequencer
48	476	0x2144	Configure sequencer
49	480	0x8D04	Configure sequencer
50	481	0x8501	Configure sequencer
51	484	0xCD04	Configure sequencer
52	485	0xC501	Configure sequencer
53	489	0x0BE2	Configure sequencer
54	493	0x2184	Configure sequencer
55	496	0x1347	Configure sequencer
56	500	0x2144	Configure sequencer
57	504	0x8D04	Configure sequencer
58	505	0x8501	Configure sequencer
59	508	0xCD04	Configure sequencer
60	509	0xC501	Configure sequencer

Soft Power Up

During the soft power up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power up uploads are listed in Table 9.

Table 9. SOFT POWER UP REGISTER UPLOADS FOR MODE DEPENDENT REGISTERS

Upload #	Address	Data	Description
V1-SN/SE 8-bit mode with PLL			
1	32	0x200F	Enable analog clock distribution
2	10	0x0000	Release soft reset state
3	64	0x0001	Enable biasing block
4	72	0x0203	Enable charge pump
5	40	0x0003	Enable column multiplexer

Table 9. SOFT POWER UP REGISTER UPLOADS FOR MODE DEPENDENT REGISTERS

Upload #	Address	Data	Description
6	48	0x0001	Enable AFE
7	112	0x0007	Enable LVDS transmitters
V1-SN/SE 8-bit mode without PLL			
1	32	0x200B	Enable analog clock distribution
2	10	0x0000	Release soft reset state
3	64	0x0001	Enable biasing block
4	72	0x0203	Enable charge pump
5	40	0x0003	Enable column multiplexer
6	48	0x0001	Enable AFE
7	112	0x0007	Enable LVDS transmitters
V1-SN/SE 10-bit mode with PLL			
1	32	0x2007	Enable analog clock distribution
2	10	0x0000	Release soft reset state
3	64	0x0001	Enable biasing block
4	72	0x0203	Enable charge pump
5	40	0x0003	Enable column multiplexer
6	48	0x0001	Enable AFE
7	112	0x0007	Enable LVDS transmitters
V1-SN/SE 10-bit mode without PLL			
1	32	0x2003	Enable analog clock distribution
2	10	0x0000	Release soft reset state
3	64	0x0001	Enable biasing block
4	72	0x0203	Enable charge pump
5	40	0x0003	Enable column multiplexer
6	48	0x0001	Enable AFE
7	112	0x0007	Enable LVDS transmitters
V2-SN/SE 10-bit mode			
1	32	0x200F	Enable analog clock distribution
2	10	0x0000	Release soft reset state
3	64	0x0001	Enable biasing block
4	72	0x0203	Enable charge pump
5	40	0x0003	Enable column multiplexer
6	48	0x0001	Enable AFE
7	112	0x0000	Configure I/O

Enable Sequencer

During the ‘Enable Sequencer’ action, the frame grabbing sequencer is enabled. The sensor starts grabbing images in the configured operation mode. Refer to Sensor States on page 15.

The ‘Enable Sequencer’ action consists of a set of register uploads. The required uploads are listed in Table 10.

Table 10. ENABLE SEQUENCER REGISTER UPLOAD

Upload #	Address	Data	Description
1	192[0]	0x1	Enable sequencer. Note that this address contains other configuration bits to select the operation mode.

User Actions: Functional Modes to Power Down Sequences

Refer to Silicon Errata on page 73 for standby power considerations.

Disable Sequencer

During the ‘Disable Sequencer’ action, the frame grabbing sequencer is stopped. The sensor stops grabbing images and returns to the idle mode.

The ’Disable Sequencer’ action consists of a set of register uploads. as listed in Table 11.

Table 11. DISABLE SEQUENCER REGISTER UPLOAD

Upload #	Address	Data	Description
1	192[0]	0x0	Disable sequencer. Note that this address contains other configuration bits to select the operation mode.

Soft Power Down

During the soft power down action, the internal blocks are disabled and the sensor is put in standby state to reduce the current dissipation. This action exists of a set of SPI uploads. The soft power down uploads are listed in Table 12.

Table 12. SOFT POWER DOWN REGISTER UPLOAD

Upload #	Address	Data	Description
1	112	0x0000	Disable LVDS transmitters
2	48	0x0000	Disable AFE
3	40	0x0000	Disable column multiplexer
4	72	0x0200	Disable charge pump
5	64	0x0000	Disable biasing block
6	10	0x0999	Soft reset

Disable Clock Management - Part 2

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 13.

Table 13. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
V1-SN/SE 8-bit mode with PLL			
1	34	0x0000	Disable logic blocks
2	32	0x200C	Disable logic clock
3	9	0x0009	Soft reset clock generator
V1-SN/SE 8-bit mode without PLL			
1	34	0x0000	Disable logic blocks
2	32	0x2008	Disable logic clock
3	9	0x0009	Soft reset clock generator
V1-SN/SE 10-bit mode with PLL			
1	34	0x0000	Disable logic blocks

Table 13. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
2	32	0x2004	Disable logic clock
3	9	0x0009	Soft reset clock generator
V1-SN/SE 10-bit mode without PLL			
1	34	0x0000	Disable logic blocks
2	32	0x2000	Disable logic clock
3	9	0x0009	Soft reset clock generator
V2-SN/SE 10-bit mode			
1	34	0x0000	Disable logic blocks
2	32	0x200C	Disable logic clock
3	9	0x0009	Soft reset clock generator

Disable Clock Management - Part 1

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 14.

Table 14. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 1

Upload #	Address	Data	Description
1	16	0x0000	Disable PLL
2	8	0x0099	Soft reset PLL
3	20	0x0000	Configure clock management

Power Down Sequence

Figure 13 illustrates the timing diagram of the preferred power down sequence. It is important that the sensor is in reset before the clock input stops running. Otherwise, the internal PLL becomes unstable and the sensor gets into an unknown state. This can cause high peak currents.

The same applies for the ramp down of the power supplies. The preferred order to ramp down the supplies is first vdd_pix, second vdd_33, and finally vdd_18. Any other sequence can cause high peak currents.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

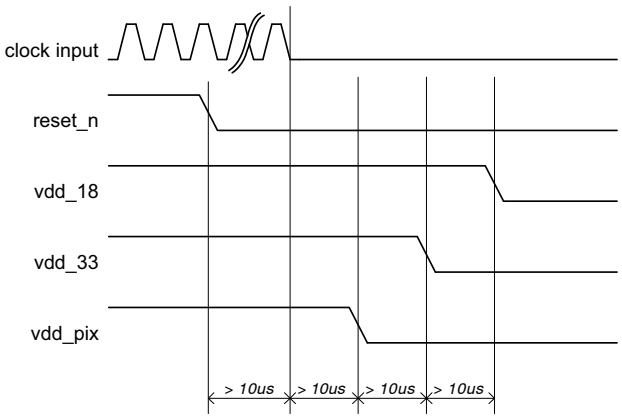


Figure 13. Power Down Sequence

Sensor Re−configuration

During the standby, idle, or running state several sensor parameters can be reconfigured.

- Frame Rate and Exposure Time: Frame rate and exposure time changes can occur during standby, idle, and running states.
- Signal Path Gain: Signal path gain changes can occur during standby, idle, and running states.
- Windowing: Changes with respect to windowing can occur during standby, idle, and running states. Refer to Multiple Window Readout on page 33 for more information.
- Subsampling: Changes of the subsampling mode can occur during standby, idle, and running states. Refer to Subsampling on page 34 for more information.
- Shutter Mode: The shutter mode can only be changed during standby or idle mode. Reconfiguring the shutter mode during running state is not supported.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Re-configuration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 15 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 15. STATIC READOUT PARAMETERS

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64–71	Configure according to recommendation
LVDS	112	Configure according to recommendation
Sequencer mode selection	192 [6:1]	Operation modes are: • Rolling shutter enable • triggered_mode • slave_mode
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the recommendation

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 16 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the re-configuration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed.

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 16. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

Group	Addresses	Description
Black level configuration	128–129 197[8]	Re-configuration of these registers may have an impact on the black-level calibration algorithm. The effect is a transient number of images with incorrect black level compensation.
Sync codes	129[13] 130–135	Incorrect sync codes may be generated during the frame in which these registers are modified.
Datablock test configurations	144–150	Modification of these registers may generate incorrect test patterns during a transient frame.

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame-related parameters are internally re-synchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 17. Some re-configuration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

Table 17. DYNAMIC READOUT PARAMETERS

Group	Addresses	Description
Subsampling/binning	192[7] 192[8]	Subsampling or binning is synchronized to a new frame start.
Black lines	197	Re-configuration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. No blanking in global shutter mode
Dummy lines	198	Re-configuration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. No blanking in global shutter mode.
ROI configuration	195 256–279	Optionally, it is possible to blank out one frame after re-configuration of the active ROI in rolling shutter mode. Therefore, register 206[8] must be asserted (blank_roi_switch configuration). A ROI switch is only detected when a new window is selected as the active window (re-configuration of register 195). Re-configuration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image.
Exposure re-configuration	199-203	Exposure re-configuration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to ‘1’ in triggered global mode (master).
Gain re-configuration	204	Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] - gain_lat_comp).

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the re-configuration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before re-configuration. When all registers are uploaded, re-enable the synchronization. The sensor’s sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 14 shows a re-configuration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

With sync_configuration = ‘1’. Configurations are synchronized to the frame boundaries.

Figure 15 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is de-asserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

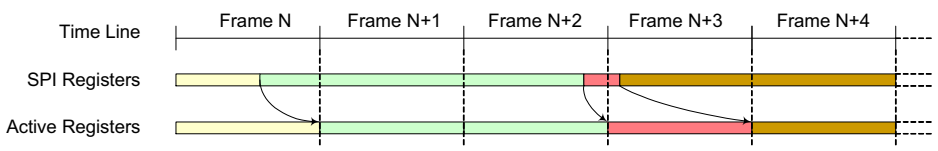


Figure 14. Frame Synchronization of Configurations (no freezing)