Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

nRF2460

2.4 GHz wireless mono audio streamer

Product Specification v1.0

Features

- World-wide 2.4 GHz ISM band operation
- 6x6 mm 36 pin QFN package
- 4 Mbps on-air data rate
- Mono 32 kHz audio rate
- 16 bit resolution
- I2S interface for audio support
- SPI or 2-wire interface to transfer bi-directional control data
- On-chip voltage regulators
- Few external components
- Programmable latency
- Quality of Service engine
- Option to synchronize two pairs of audio receivers

Applications

- Wireless microphone
- Subwoofer

2011-6-28

Liability disclaimer

Nordic Semiconductor ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic Semiconductor ASA does not assume any liability arising out of the application or use of any product or circuits described herein. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

Life support applications

Nordic Semiconductor's products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic Semiconductor ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic Semiconductor ASA for any damages resulting from such improper use or sale.

Datasheet status	
Objective Product Specification	This product specification contains target specifications for product development.
Preliminary Product Specification	This product specification contains preliminary data, supplementary data may be published from Nordic Semiconductor ASA later.
Product Specification	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice to improve design and supply the best possible product.

Contact details

For your nearest dealer, please see www.nordicsemi.com

Main office:

Otto Nielsens veg 12
7004 Trondheim
Phone: +47 72 89 89 00
Fax: +47 72 89 89 89

Revision History

Date	Version	Description
June 2011	v1.0	

RoHS statement

Nordic Semiconductor's products meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substances (RoHS). Complete hazardous substance reports as well as material composition reports for all active Nordic Semiconductor products can be found on our web site www.nordicsemi.com.

Contents

1 Introduction

The nRF2460 provides a solution for mono 16 bit 32 kHz LPCM audio streaming. The I2S interface is supported for audio- input or output. The device features seamless interfacing of low cost A/D and D/A for analog audio input and output. An external microcontroller controls the nRF2460 through a slave SPI or 2-wire (I2C compatible) control interface.

1.1 Prerequisites

In order to fully understand this product specification, a good knowledge of electronic- and software engineering is necessary.

1.2 Writing Conventions

This document follows a set of typographic rules to make the document consistent and easy to read. The following writing conventions are used:

- Pin names are written in **`Courier New bold.`**
- Commands, bit state conditions, and register names are written in `Courier New`.
- File names and User Interface components are written in regular **bold**.
- Cross references are underlined and highlighted in blue.

2 Product overview

The nRF2460 is a 4 Mbps single-chip RF transceiver that operates in the worldwide, 2.4 GHz license-free ISM band. The nRF2460 is based on the ShockBurst™ link layer from Nordic Semiconductor.

2.1 Features

The device offers a wireless channel for seamless streaming of mono LPCM in parallel with a low, data rate control channel. To enable this, the device has the following features:

- Standard digital audio interface (I2S)
- SPI or 2-wire slave control interfaces
- Fully embedded Quality of Service engine handling all RF protocol and RF link tasks

As all processing related to audio I/O, RF protocol, and RF link management are embedded, the device offers a transparent audio channel with a capacity of 512 kbits, with no true time processing needed. The nRF2460 is used in conjunction with a microcontroller that only needs to handle low speed tasks through the control interface (for example: volume up/down).

2.2 Block diagram

Figure 1. is a block schematic of a typical nRF2460 based system.

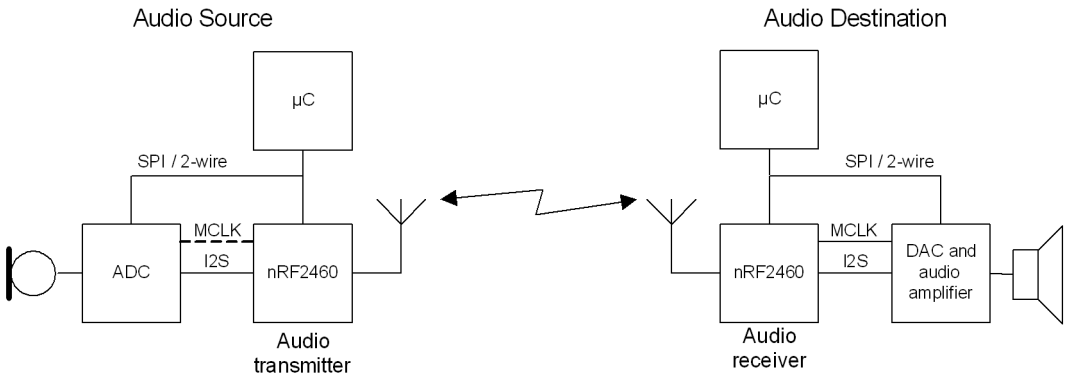

Figure 1. Typical audio application using nRF2460

In this system a microphone is connected to an nRF2460 by way of an ADC using standard audio format (I2S). An nRF2460 pair transfers audio data from the source and presents it to a DAC on the receiving side. Application-wise, the nRF2460 link will appear as a transparent channel (like a cable).

Initial configuration of nRF2460 is done by the microcontroller through an SPI or 2-wire control interface. The microcontrollers on both sides are also able to monitor link status and turn the link on and off. When a link is established, there is also a low data-rate reliable control link between the two microcontrollers.

2.2.1 Pin assignments

Table 1. on page 10 shows the nRF2460 pin functions. Note that pin functions depend on the operational mode of the device and the slave interface of choice.

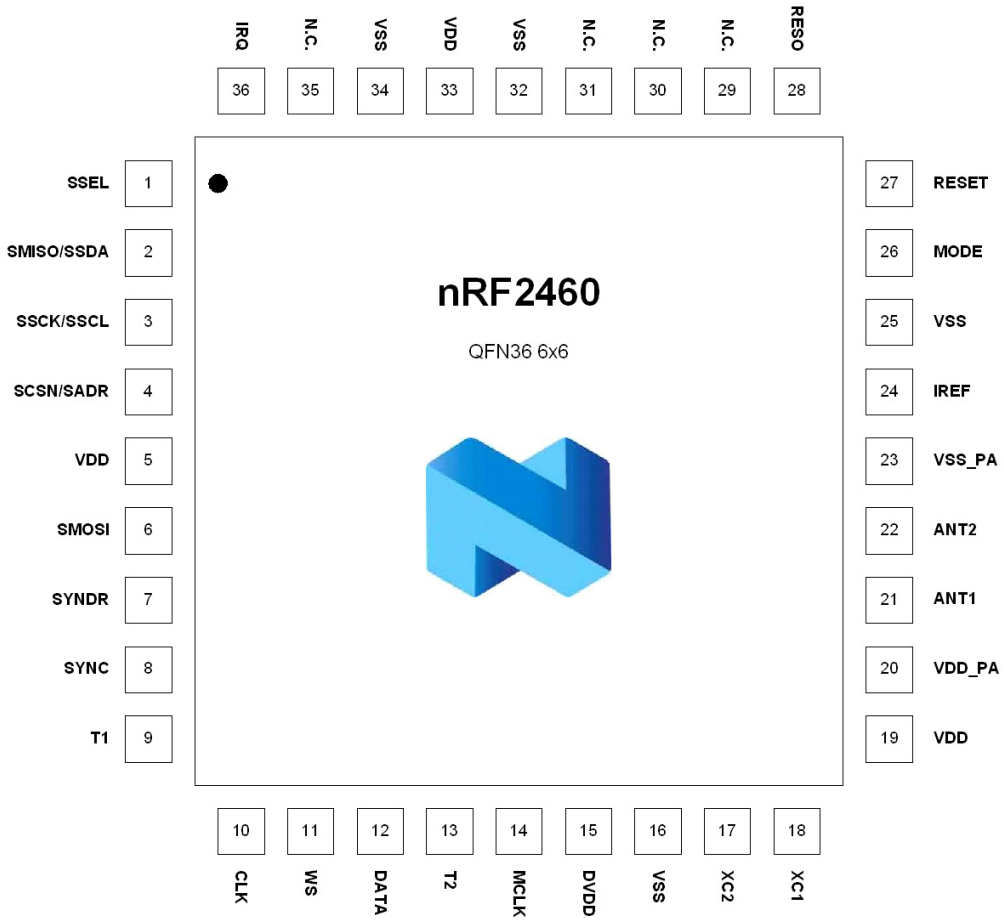

Figure 2. Pin assignment nRF2460

2.3 Pin functions

The nRF2460 can be set up as either an audio transmitter (ATX) or audio receiver (ARX), controlled by the logic level of the **MODE** pin.

Serial slave interface is controlled by the logic level of the **SSEL** pin. See Table 1. on page 10.

Pin no.	Pin name	Pin function	Description
1	SSEL	Digital input	Slave interface select 0: SPI, 1:2-wire
2	SMISO SSDA	Digital output Digital I/O	Slave SPI serial out (SSEL=0) Slave 2-wire data (SSEL=1)
3	SSCK SSCL	Digital input Digital I/O	Slave SPI clock (SSEL=0) Slave 2-wire clock (SSEL=1)
4	SCSN SADR	Digital input Digital input	Slave SPI slave select (SSEL=0) Address select 2-wire slave (SSEL=1)
5	VDD	Power	Power supply
6	SMOSI	Digital input	Slave serial in (SSEL=0) Connect to ground (0V) (SSEL=1)
7[1]	SYNDR	Digital input	Select SYNC direction 0: Output, 1: Input
8	SYNC	Digital output Digital input	No synchronization (default) SYNDR=0 Optional signal to synchronize 2 ARX (SYNDR=1)
9	T1	Digital input	Reserved, connect to ground (0V)
10	CLK	Digital I/O Digital output	I2S bit clock (MODE=1) I2S bit clock (MODE=0)
11	WS	Digital I/O Digital output	I2S word clock (MODE=1) I2S word clock (MODE=0)
12	DATA	Digital input Digital output	I2S data signal (MODE=1) I2S data signal (MODE=0)
13	T2	Digital Input	Reserved, connect to ground(0V)
14	MCLK	Digital Output	256X sample rate clock to ADC or DAC
15	DVDD	Regulator output	Internal voltage regulator output for decoupling
16	VSS	Power	Ground (0V)
17	XC2	Analog output	Crystal connection for 16 MHz crystal oscillator
18	XC1	Analog input	Crystal connection for 16 MHz crystal oscillator
19	VDD	Power	Power supply
20	VDD_PA	Regulator output	Power supply output (+1.8V) for on-chip RF Power amplifier
21	ANT1	RF	Differential antenna connection (TX and RX)

Pin no.	Pin name	Pin function	Description
22	ANT2	RF	Differential antenna connection (TX and RX)
23	VSS_PA	Power	Ground (0V)
24	IREF	Analog output	Device reference current output. To be connected to reference resistor on PCB
25	VSS	Power	Ground (0V)
26	MODE	Digital Input	Mode 1:audio transmitter (ATX), 0:audio receiver (ARX)
27	RESET	Digital Input	Active high reset, connect to ground(0V) if not used
28	RESO	Digital Output	Optional RESET pulse for ADC
29	NC	Digital Output	Reserved, leave unconnected
30	NC	Digital Input	Reserved, connect to ground(0V)
31	NC	Digital Output	Reserved, leave unconnected
32	VSS	Power	Ground (0V)
33	VDD	Power	Power Supply
34	VSS	Power	Ground (0V)
35	NC	Digital Output	Reserved, leave unconnected
36	IRQ	Digital Output	Interrupt request

1. Must be connected to ground (0V) if synchronization is not required.

Table 1. nRF2460 pin functions

2.3.1 Modes of operation

A wireless system streaming audio will have an asymmetrical load on the RF link as audio data is fed from an audio source (as in a microphone) to a destination (as in loud speakers). From the destination back to the audio source, only service- and control communication are needed.

The nRF2460 is used both on the audio source side (for example in a microphone) transmitting audio data, and on the destination side (for example in a loudspeaker) receiving audio data.

Due to the asymmetry, nRF2460 has two operational modes set by the external pin **MODE**, depending on whether it represents the transmitter or the receiver. The two modes show significant differences both in internal and I/O functionality. The operational mode is selected by the logic level on the **MODE** pin:

MODE	Description
0	Audio destination
1	Audio source

*Table 2. Operation modes set by **MODE** pin*

The **MODE** pin is read during power-up and reset only.

In this context, the abbreviations ATX (for audio transmitter) and ARX (for audio receiver) refer to the directional flow of the audio, while the nRF2460 radio transceiver always operates in half-duplex (bi-directional) mode.

2.3.2 Communication and data transfer principle

To differentiate between audio data and other control and status information, we have organized the information about the data traffic between the ATX/ARX in this document, into two data channels.

The audio channel is defined as the communication channel sourcing audio data from the ATX to the ARX. The audio data is divided into two categories; real time data from the audio source and retransmitted audio information.

If there is audio information lost, the ARX requests re-transmission of the lost packets. The real-time audio bit rate is constant, whereas the amount of retransmitted audio varies across time.

The control channel is a two-way, low data rate channel superimposed on the audio stream.

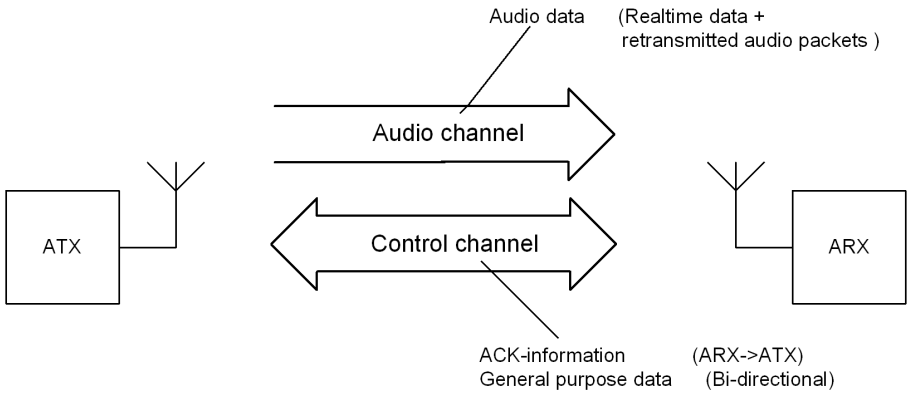

Figure 3. nRF2460 communication channel concept

2.3.3 Mode- and interface alternatives

A number of interfaces are available for the nRF2460 device. The available interfaces depend on the nRF2460 mode of operation and the type of data to be transferred. Data is divided into two categories; audio data (audio channel) and configuration/status data (control channel). Figure 4. illustrates the available data interfaces for the various modes of operation. Interface options are illustrated by grey circles, whilst functionality / operation modes are shown in white. Relevant configuration settings are shown in the lines drawn between the circles.

Note: A choice about interface is made by a combination of pin and register settings. Refer to Chapter 4 on page 21 for details.

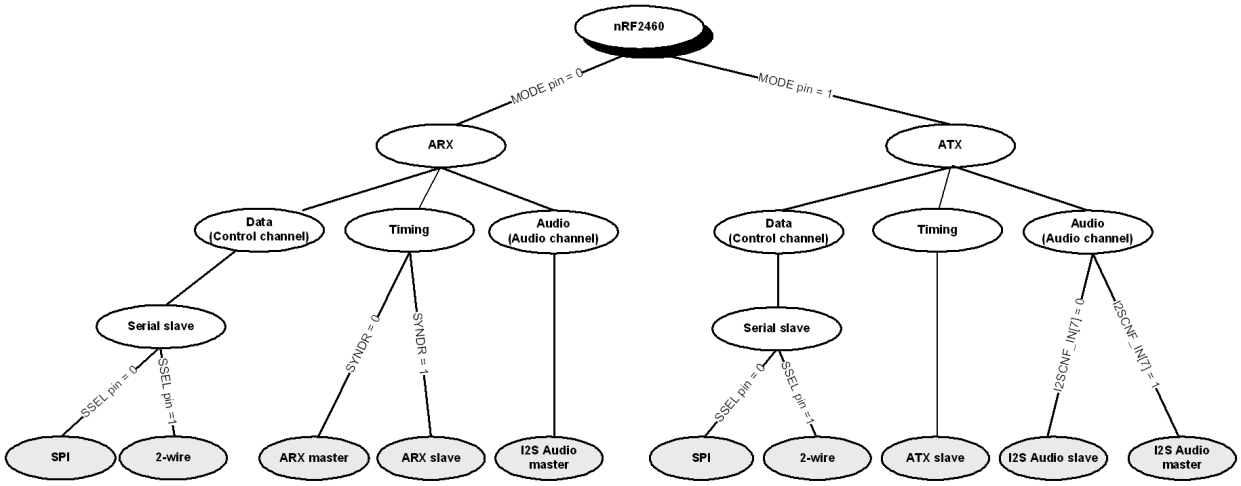

Figure 4. nRF2460 functional modes and interface alternatives

2.3.4 Audio transmitter (ATX)

When an nRF2460 is applied at the audio source side of the RF link, the **MODE** pin must be set high and nRF2460 will become an audio transmitter. The block schematic of nRF2460 in ATX mode can be seen in Figure 5.

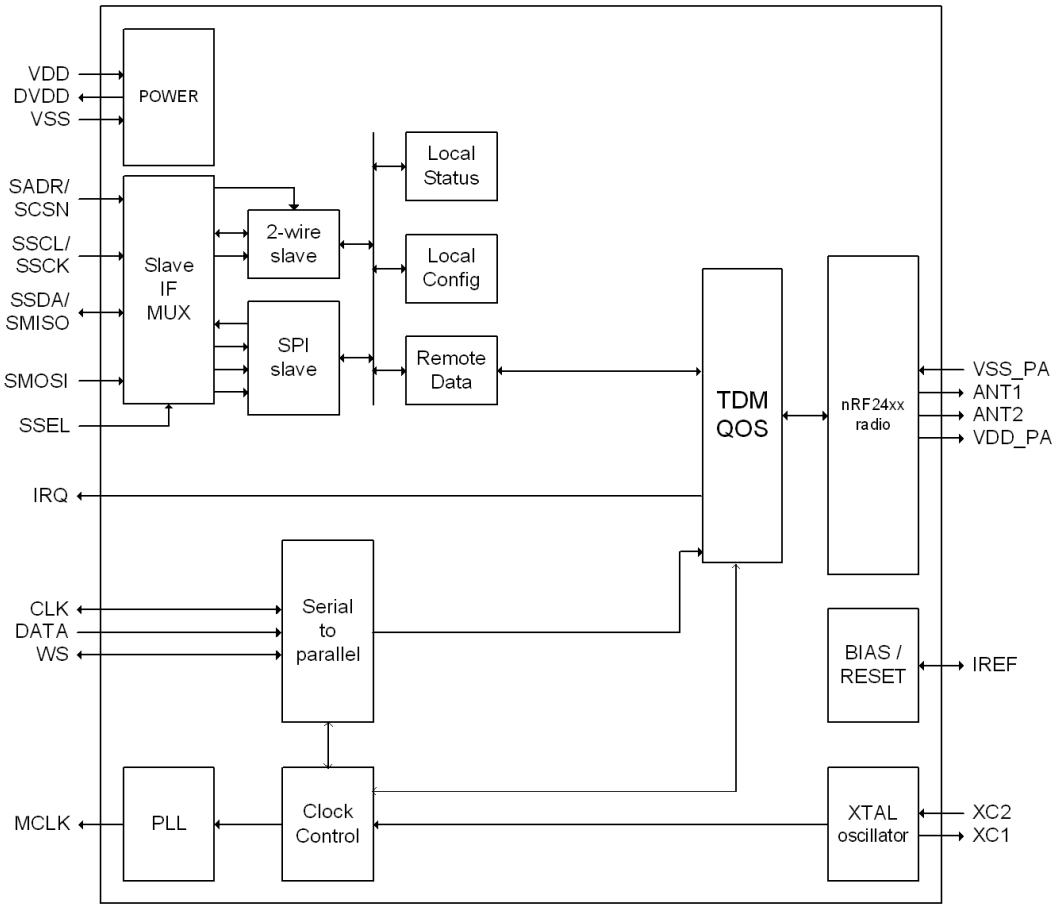

Figure 5. nRF2460 ATX mode block diagram

2.3.4.1 I2S audio input

I2S is the audio interface to the nRF2460. The I2S interface consists of pins **CLK**, **DATA** and **WS**. This interface supports a sampling rate of 32 kHz.

I2S may be used with an external stereo or mono ADC for analog audio sources. The nRF2460 offers a sampling rate clock (f_S) of 256 times the audio sampling rate. The sample rate clock is available on the **MCLK** pin and may be used as system clock for the ADC. Only mono 32 kHz audio is streamed from ATX to ARX. Data is in a 16-bit format.

2.3.5 Audio Receiver (ARX)

When nRF2460 is put at the destination side of the RF link, MODE must be low and nRF2460 becomes the audio receiver (ARX). A block schematic of nRF2460 in ARX mode can be seen in Figure 6. I2S is now used for audio real time data output.

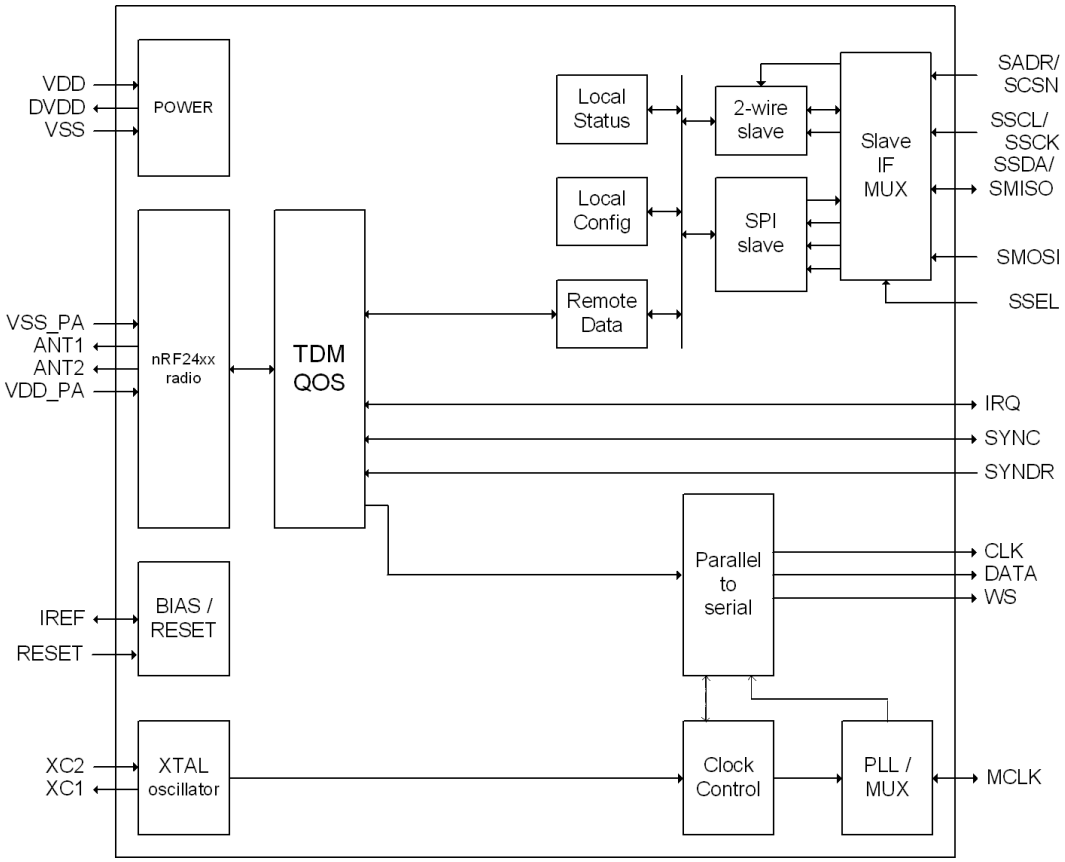

Figure 6. nRF2460 ARX mode block diagram

2.3.5.1 I2S audio output

The audio output (typically a DAC) is driven by the I2S output (pins **CLK**, **DATA** and **WS**). In audio receiver mode, the **MCLK** pin provides a sampling rate clock (f_S) of 256 times the audio sampling rate for an external DAC.

2.3.6 Blocks and functionality common to ATX and ARX

2.3.6.1 Serial control (slave) interfaces

Both ATX and ARX are controlled by an external MCU, and configuration and control data may be entered through a 2-wire or SPI slave serial interface. The same interface is used for reading back status information. The register map is identical to both interfaces, but only one of the interfaces (selected by the **SSEL** pin) may be used in a given application:

SSEL	Description
0	SPI (pin functions **SCSN**, **SSCK**, **SMISO**, **SMOSI**)
1	2-wire (pins **SADR**, **SSCL** and **SSDA**)

*Table 3. Serial interface set by **SSEL** pin*

The **SSEL** pin is read during power-up and reset only.

Pin **SADR** is not part of a standard 2-wire interface, but selects one of two possible bus addresses for the nRF2460.

2.3.6.2 Interrupt output

The nRF2460 can interrupt the external application through pin **IRQ** based on a number of sources. Once **IRQ** has triggered the external MCU, interrupt status can be read through the serial slave interface.

2.3.6.3 XTAL oscillator

The crystal oscillator will provide a stable, reference frequency with low phase noise for the radio and audio functions. See section 15.1 on page 51.

2.3.6.4 Radio transceiver

The RF transceiver part of the circuit is a member of the nRF family of low power highly integrated 2.4 GHz ShockBurst™ transceivers. The transceiver interface is optimized for high speed streaming of up to 4 Mbps. Output power and some radio protocol parameters can be controlled by the user through the Quality of Service (QoS) module.

2.3.6.5 Quality of Service (QoS) engine

The primary function of the QoS engine is to ensure robust communication between the ATX and the ARX in an audio streaming application.

Various data streams with different properties are handled. The available bandwidth is shared among audio data, service data and remote data.

Data integrity is ensured through a number of RF protocol features:

1. Packets of data are organized in frames with each packet consisting of an RF address, payload and CRC.
2. Packets that are lost or received with errors are handled by the error correction level of the QoS engine; a two way, acknowledge protocol: When a packet is received by ARX, it is registered and CRC is verified. After ARX has received a frame, it sends a packet back to ATX acknowledging the packets successfully transferred. Packets lost or received with errors, are re-transmitted from ATX in the next frame.
3. The information (audio data) is dispersed across the 2.4 GHz band by use of an adaptive frequency hopping algorithm. This enables the nRF2460 link to cope with RF propagation

challenges like reflections, multi-path fading and avoid heavily trafficked areas of the 2.4 GHz band. Handling co-existence scenarios with contemporary RF systems such as *Bluetooth*, WLAN as well as other nRF applications, is increasingly important.

The main function of the QoS is to constantly monitor the quality of the RF link.

The secondary function of the QoS module is to run a link initialization algorithm which manages initial connect and re-connect if link is lost (ex: out of range) between paired nRF2460s.

2.3.6.6 Power-supply regulators

The nRF2460 has an internal, linear-regulated, power supply to all internal parts of the device. This makes it very robust with respect to external voltage supply noise and isolates (audio) devices (in an application) from any noise generated by the nRF2460.

2.3.6.7 Bias reference

The **IREF** pin sets up the bias reference for the nRF2460 by use of an external resistor. See section 15.2 on page 51.

3 Operation overview

3.1 Power on / RESET sequence

When a power supply voltage is connected, nRF2460 performs a power-on reset. Reset is held until the supply voltage has been above the minimum supply voltage for a few milliseconds. Pulling **RESET** pin high also puts the device into reset.

After reset (power on or RESET high) is released, the device needs to be configured. An external microcontroller must configure the nRF2460 ATX and ARX through the slave SPI or 2-wire serial interface. The nRF2460 will then start a link initialization procedure based on the link configuration data. The value of the **MODE** pin determines whether it will be in ATX or ARX mode.

It is important that all configuration data are set before the RF transceiver is enabled, by writing to the TXMOD (for the ATX) or RXMOD (for the ARX) registers.

3.2 RF link initialization

The process of establishing a communication link between the ATX and the ARX is referred to as RF link initialization. This involves the ATX systematically probing the frequency band in search for an active ARX with the identical address. Once found, the ATX and ARX are synchronized before audio transmission starts.

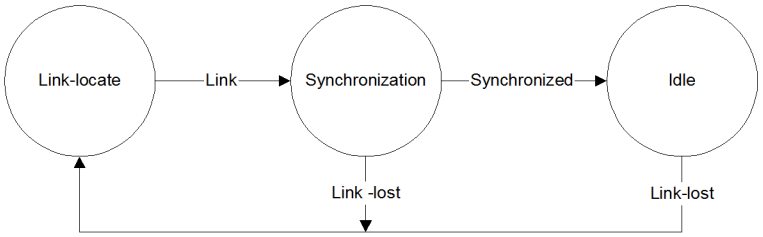

Figure 7. Link initialization algorithm

3.2.1 Idle state

The nRF2460 link initialization algorithm will be in idle state when a link is established. Once established, the frequency hopping engine is initiated and synchronized.

3.2.2 Link-locate state

A special link-locate routine is initiated on both sides in order to (re-)establish a link, see Figure 7. During initialization, nRF2460 uses the NLCH first positions of the frequency hopping table.

3.2.2.1 Link-locate state on ATX

The ATX tries to establish a link with ARX by iteratively sending short search packets on all available channels until an acknowledge signal is received from the ARX. The ATX will send one packet on each channel and wait for acknowledge long enough to secure that the ARX has time to respond. The accumulated time used by the ATX while looping through all available channels, is defined as the ATX-loop-time. After receiving an acknowledge packet from the ARX, the ATX will enter the synchronization state as illlustrated in Figure 7. on page 17 . The dwell time for linking is approximately 600 µs. The dwell time is defined as the time duration for which the ATX is active at a given frequency before changing frequency position.

3.2.2.2 Link-locate state on ARX

The ARX tries to establish a link with the ATX by listening for incoming search packets on all available channels. When a search packet is received, the ARX will proceed by sending one acknowledge packet to confirm a feasible link. The ARX will listen for incoming search packets on each channel for a fixed time longer than the ATX-loop-time. This guarantees at least one search packet to get through on each available channel used by the ARX, as long as this channel is not being occupied by another radio device. After sending the acknowledge packet, the ARX will enter the synchronization state. The dwell time for ARX is approx. (NLCH+1)× 600 µs.

3.2.3 Synchronization state

This state synchronizes the frequency hopping engine on ATX and ARX, ensuring that both units follow the same hopping sequence. The initial start frequency is found in link-locate mode.

3.3 Audio channel

The input audio data can be one of the following common digital audio formats:

- Left justified
- I2S

In the ATX, the input audio stream format is converted to the nRF2460 RF protocol and transferred over the air.

Upon reception in the ARX, the received data is validated and converted to the specified audio output format and fed to the audio output interface.

3.3.1 Audio receiver clock rate generation

The ARX will lock MCLK to its XC1 clock input and derive CLK and WS by dividing the MCLK by the appropriate divisor for the audio rate.

3.3.2 Audio transmitter clock rate generation

Maintaining equal data rates on both sides of the RF link is crucial in any RF system streaming true-time data. This implies keeping the master clock frequency (MCLK) for the ADC on the transmitting side equal to the clock frequency used to output audio samples from the RF device on the receiver side.

If these two clocks are not identical, the receiving end will either run out of samples for the DAC (ARX clock frequency > ATX clock frequency) or overflow (ARX clock frequency < ATX clock frequency), skipping samples.

This problem is solved in the nRF2460 device without the need for a tight tolerance crystal or extensive digital filtering.

As long as the nRF2460 QoS engine is able to maintain the RF link, the ATX locks its master clock output (MCLK) to the rate of the incoming audio stream. The MCLK signal on the ATX side is locked to the reference (crystal) of the ARX side.

3.4 Control channel

A two-way, low bit rate, control and signaling channel runs in parallel with the audio stream. This control channel is a part of the QoS overhead, meaning the difference between on- the- air data rate (4 Mbits) and

the nominal audio data rate 0.5 Mbps. Hence the data channel rate cannot be traded for higher audio data rate. The functionality of the control channel is illustrated in Figure 8.

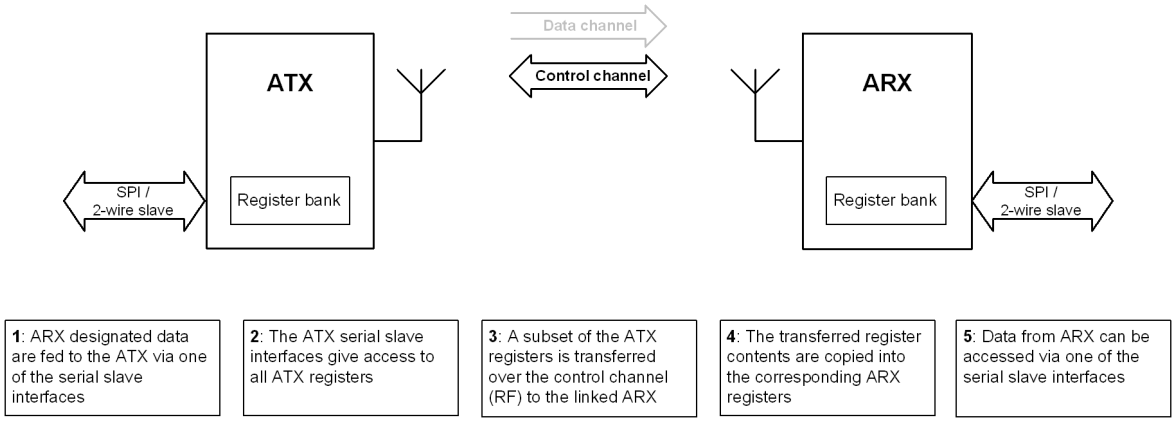

Figure 8. nRF2460 control channel transfer principle

3.5 Register map

The nRF2460 control and status registers are listed in Table 4. on page 20. The registers may be accessed by an external MCU through the slave interface (SPI or 2-wire). The registers are organized functionally into six groups. All registers are present both in audio transmitter and audio receiver. Registers are functional on both sides and the values should match on both sides of the link. DATA channel registers are also functional on both sides, thus creating a bi-directional data channel between the two microcontrollers.

Address HEX	Register	R/W	Initial value	Description
ATX				
0x01	TXSTA	R/W	0x50	Table 8. on page 23
0x02	INTSTA	R/W	0x00	Table 22. on page 39
0x5A	TXMOD	R/W	0x03	Table 8. on page 23
0x52	TXLAT	R/W	0x06	Table 19. on page 37
0x53	INTCF	R/W	0x00	Table 22. on page 39
0x54	I2SCNF_IN	R/W	0x80	Table 8. on page 23
0x56	TXPWR	R/W	0x03	Table 20. on page 37
0x50	TXRESO	R/W	0x08	Table 23. on page 40
LINK status				
0x03	LNKSTA	R/W	0x00	Table 17. on page 36
LINK control				
0x0C-0x31	CH[0:37]	R/W		Table 15. on page 34
0x32	BCHD	R/W	0x0A	Table 16. on page 35
0x33	NBCH	R/W	0x12	Table 16. on page 35
0x34	NACH	R/W	0x26	Table 16. on page 35
0x35	NLCH	R/W	0x26	Table 16. on page 35
0x36	LNKMOD	R/W	0x00	Table 17. on page 36
0x0B	MDUR	R/W	0x00	Table 18. on page 36
0x39-0x3D	ADDR[0:4]	R/W	0x98-38-A2-34-85	Table 14. on page 33
0x3E	LNKCSTATE	R/W	0x00	Table 25. on page 42
DATA channel				
0x4E	DTXSTA	R	0x00	Table 25. on page 42
0x5B	RXCOUNT	R	0x00	Table 13. on page 31
0x5C	TXCOUNT	R/W	0x00	Table 13. on page 31
0x5D-0x5f	RXBUF[0:2]	R	0x00	Table 13. on page 31
0x65-0x67	TXBUF[0:2]	R/W	0x00	Table 13. on page 31
ARX				
0x4A	RXMOD	R/W	0x00	Table 9. on page 24
0x44	I2SCNF_OUT	R/W	0x00	Table 9. on page 24
0x49	RXPWR	R/W	0x03	Table 20. on page 37
0x37	SYNCDL	R/W	0x77	Table 21. on page 38
Test				
0x7E	TESTREG	R/W	0x00	Table 27. on page 44
0x7F	TESTCH	R/W	0x00	Table 27. on page 44
0x7D	REVBYT	R	0x05	Revision byte

Table 4. nRF2460 register listing

4 Digital I/O

This chapter describes the digital I/O pins, control registers and important interface timing of the nRF2460.

The digital I/O pins are divided into two groups:

- Audio interface
- Serial slave interfaces

4.1 Digital I/O behavior during RESET

During RESET, all digital pins are set as inputs to avoid driving conflicts with external devices. All pins will maintain their respective directions until any of the configuration read routines described in section 3.1 on page 17 are completed. The I/O pins are then set according to the new configuration data.

4.2 Audio interface

The audio interfaces consist of the I2S interface plus the **MCLK** pin.

Pin name	Function
CLK	bit clock
WS	word sync clock
DATA	audio data
MCLK	256 x CLK

Table 5. Serial audio port pins

4.2.1 I2S audio interface

The nRF2460 has a three-wire serial audio interface which can be configured to be compatible with various serial audio formats. In ATX mode, the audio interface is in slave or master input mode. In ARX mode, the audio interface is in master output mode. The audio interface consists of 4 pins in total, see Table 5.

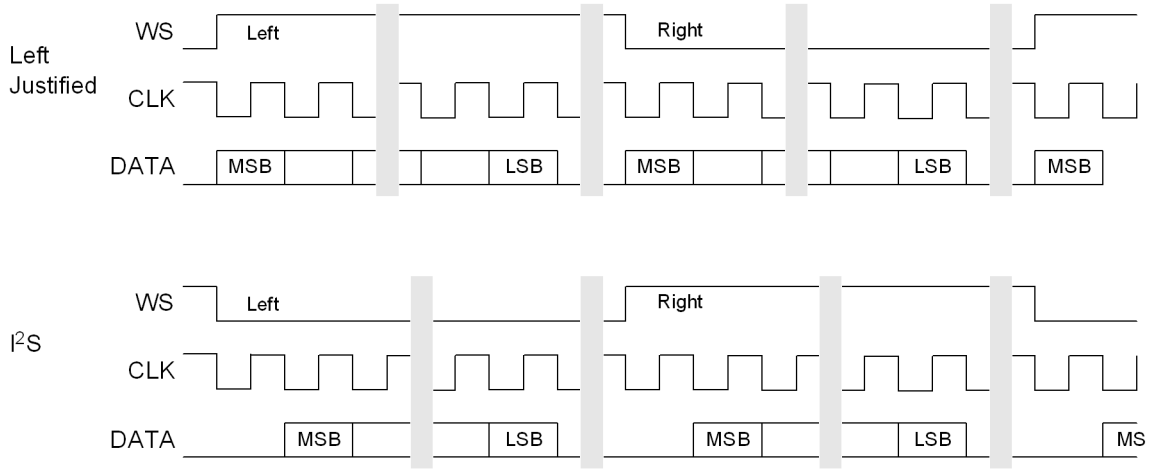

Figure 9. Serial audio formats I2S and left-justified

Audio format	I2SCNF[3:0] value
Left justified	0xA
I2S	0x0

Table 6. Settings for two common serial audio formats

4.2.2 Audio interface functionality

The functionality and direction of the pins in the audio interfaces are listed in Table 7.

Pin number	Pin name	ARX direction	ATX direction (I2SCNF_IN[7]=1)	ATX direction (I2SCNF_IN[7]=0)
10	CLK	OUT	OUT	IN
11	WS	OUT	OUT	IN
12	DATA	OUT	IN	IN
14	MCLK	OUT	OUT	OUT

Table 7. nRF2460 operational modes and audio interface pin functions

4.2.3 ATX audio interface control

The audio interfaces in ATX mode are controlled by the registers listed in Table 8. on page 23.

Address HEX	Register	R/W	Description		
0x01	TXSTA	R/W	ATX audio input rate register		
			Bit	**Interpretation**	
			7:5	Reserved. Must be “010”	
			4:3	Value	Description
				00	Reserved
				01	Reserved
				10	32 kHz
				11	Reserved
			2:0	Reserved, MBZ	
0x5A	TXMOD	R/W	ATX modes of operation		
			7	RF transceiver enable	
			6	Audio transmitter power down	
			5:2	Reserved, MBZ	
			1:0	MCLK output control	
				00	MCLK off (logic 0)
				01	Reserved
				10	Reserved
				11	Output 256 × 32 kHz
0x54	I2SCNF_IN	R/W	ATX I2S interface configuration. See Table 6. on page 22		
			7	I2S audio in clock mode	
				0	Slave mode, WS, CLK, DATA are input (needs to be coherent with MCLK)
				1	Master mode, WS, CLK are output, DATA is input
			6:5	Reserved, MBZ	
			4	Mono sample location	
				0	Use left channel samples
				1	Use right channel samples
			3	WS polarity	
				0	WS=0 for left sample
				1	WS=1 for left sample
			2	Reserved, MBZ	
			1	WS to MSB delay	
				0	1 clock cycle
				1	0 clock cycle
			0	Reserved, MBZ	

Table 8. ATX audio interface control registers

The nRF2460 offers a 256 x clock output on pin **MCLK**. Clock frequency is set in register TXMOD [1:0]. This clock shall be used as master clock to the device that drives the I2S data input on the ATX side.

4.2.4 ARX audio interface control

In ARX mode the audio interfaces are controlled by registers `RXMOD` and `I2SCNF_OUT` listed below.

Address HEX	Register	R/W	Description	
0x4A	`RXMOD`	R/W	ARX modes of operation	
			Bit	**Interpretation**
			7	Audio receiver power down
			6	Reserved, MBZ
			5	RF transceiver enable
			4:0	Reserved, MBZ
0x44	`I2SCNF_OUT`	R/W	ARX I2S interface configuration for audio output. See Table 6. on page 22	
			Bit	**Interpretation**
			7	Reserved, MBZ
			6	Mute sound output
			5:4	Reserved, MBZ
			3	WS polarity
				0 WS=0 for left sample
				1 WS=1 for left sample
			2	Data to Bit Clock relation (data valid at clock edge)
				0 Rising edge
				1 Falling edge
			1	WS to MSB delay
				0 1 clock cycle
				1 0 clock cycle
			0	Reserved, MBZ

Table 9. ARX audio interface control registers

The Mute bit holds the last audio sample and holds it until the Mute bit is cleared again. Then a simple three-sample interpolation scheme is applied between the last sample value and the first unmuted sample value. The same mute behavior is also applied to audio packet loss. Mute on and off is synchronized to the next audio packet boundary.

4.2.5 I2S audio interface timing

4.2.5.1 I2S input (ATX) timing

The I2S input protocol may be configured in register `I2SCNF_IN` to handle various I2S formats. This section describes the detailed bit-, clock- and word timing requirements for audio slave and audio master mode (as set by `I2SCNF_IN` [7]).

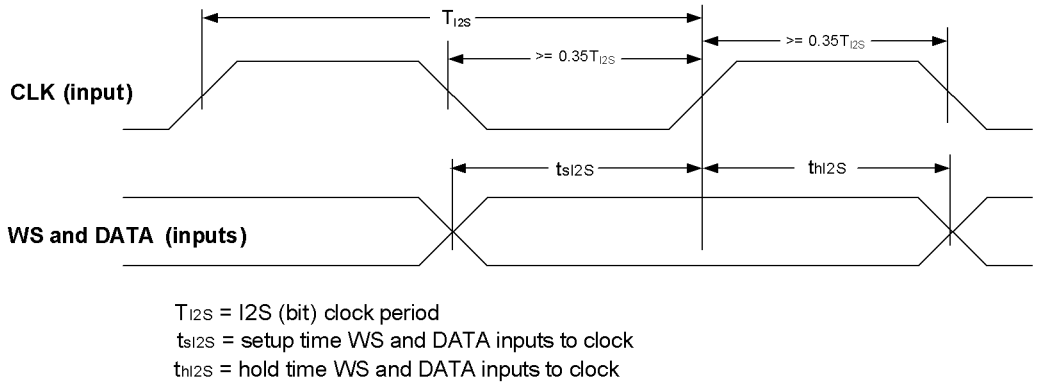

Figure 10. I2S input timing in audio slave mode (I2SCNF_IN[7]=0)

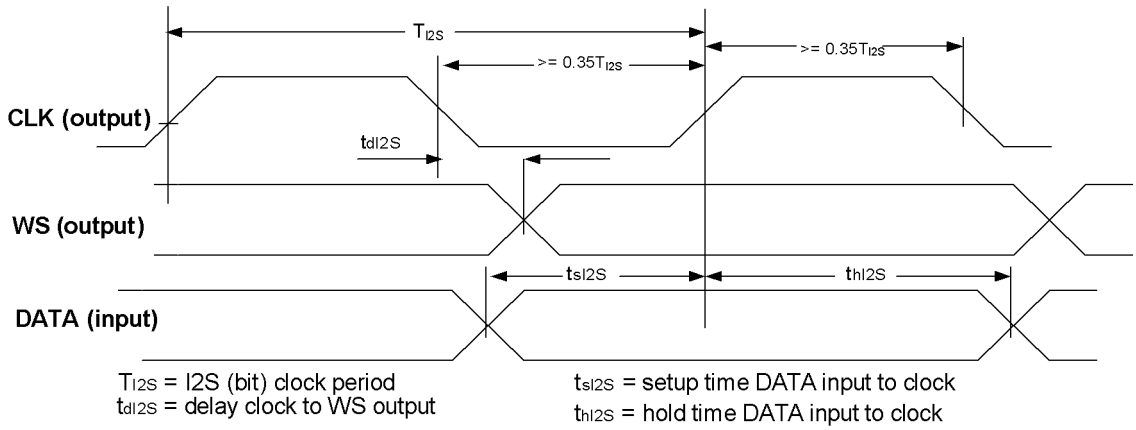

Figure 11. I2S input timing in audio master mode (I2SCNF_IN[7]=1)